EXAR ...the analog plus company DATABOOK

TELECOMMUNICATION ICs

DATA COMMUNICATION ICs

MICROPERIPHERAL ICs

USER SPECIFIC ICs

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Commitment to Customer Satisfaction

One of the founding principles of EXAR has been to focus on customers satisfaction through unsurpassed service and quality. Every individual at EXAR takes this principle as a personal commitment, assuring that quality and reliability are built into all our products from inception through production.

It is this very commitment which has given EXAR worldwide recognition as a dependable supplier of mixed signal application-specific and custom integrated circuits to the communication and computer peripheral markets. This commitment along with our "analog plus" design expertise using in-house bipolar, CMOS, EEPROM and BiCMOS technologies, has increasingly made us the vendor of choice by customers seeking total system solutions.

I view this corporate dedication to quality, advanced technologies and service as the foundation to a mutually beneficial long term relationship with you, our valued customer.

Nob Hatta
President

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Telecommunication ICs

Data Communication ICs

Communication / Microperipheral Support ICs

CROSS REFERENCE GUIDE

The following guide is provided to assist you in determining the EXAR part number equivalent to industry standard products from various manufacturers. The level of interchangeability is indicated in the accompanying note as described below:

No reference note: "Direct replacement"
Note (1): "Pin compatible" - pin-for-pin compatible device but specifications may differ. Consult datasheet for suitability.
Note (2): "Functional equivalent" - functional equivalent, but not be pin-for-pin compatible. Consult datasheet for suitability.

Competitor	Competitor Part Number	EXAR Part Number	Note
Dallas Semiconductor	DS2009	XR-T7201	
	DS2010	XR-T7202	
	DS2011	XR-T7203	
	DS2176	XR-T5691	
	DS2180	XR-T5690	
Gould/AMI	S3528	XR-1015	(2)
	S3528	XR-1016	(2)
	S3541	XR-1020A	(2)
Harris	ICM7555	XR-L555	(1)
	ICM7556	XR-L556	(1)
	ICM7240	XR-2240	(1)
	ICM8240	XR-2240	(1)
	ICM8038	XR-8038	(1)
	CP82C50A	XR-16C450	(1)
	HF10	XR-1010	(1)
	HA5002	XR-117	
IDT	IDT7201	XR-T7201	
	IDT7202	XR-T7202	
	IDT7203	XR-T7203	
Silicon General	SG1524/ 3524	XR-1524/ 3524	
Linear Technology	LTC1060	XR-1010	(1)
	LTC1062	XR-1015	(2)
Maxim	MF10	XR-1010	(1)
	ICM7240	XR-2240	
	ICM7242	XR-2242	(1)

Competitor	Competitor Part Number	EXAR Part Number	Note
Motorola	MC14412	XR-14412	(1)
	MC34072	XR-34072	
	MC34074	XR-34074	
	MC2681	XR-88C681	(1)
	MC3590	XR-6118	
National	LM146/346	XR-146/346	
	LM567	XR-567	
	MF4C-100	XR-1001	(1)
	MF4C-50	XR-1002	(1)
	MF4C-100	XR-1003	(1)
	MF4C-50	XR-1004	(1)
	MF4C-100	XR-1005	(1)
	MF4C-50	XR-1006	(1)
	MF4C-1007	XR-1007	(1)
	MF4C-1007	XR-1007	(2)
	MF10	XR-1010	(1)
	LM1524/3524	XR-1524/3524	
	LM13600	XR-13600	
	NS16C450	XR-16C450	
	µA2240	XR-2240	
	DM8887	XR-6118	
Raytheon	XR2207	XR-2207	
	XR2211	XR-2211	
	RC4136	XR-4136	
	RC4151	XR-4151	
	RC5532/5532A	XR-5532/5532A	
	RC5534/5534A	XR-5534/5534A	
Reticon	RU5621/22	XR-1010	(2)
	RF5609	XR-1015	(2)
	RF56009	XR-1016	(2)
	RF5651	XR-1020A	(2)
Signetics	NE567	XR-567	
	SG3524	XR-3524	
	NE5532	XR-5532	
	NE5534	XR-5534	
	NE594	XR-6118	
	NE5517	XR-13600	
	SCN2681	XR-88C681	(1)

Competitor	Competitor Part Number	EXAR Part Number	Note
Silicon Systems	SSI32R117 SSI32R501 SSI32R511 SSI32P541 SSID5321	XR-117 XR-501 XR-511 XR-541 XR-532	
Texas Instruments	TL062 µA2240 SG3524 RC4136 NE5532 NE5534	XR-062 XR-2240 XR-3524 XR-4136 XR-5532 XR-5534	

SO Availability List

Part No.	Description	SO Package (Suffix)
XR-062	Low Power J-FET Input Op-Amp	JEDEC SO (D)
XR-117	Hard Disk Read/Write Amplifier	JEDEC SO (D), PLCC (CJ)
XR-215	Monolithic Phase-Locked Loop	Japanese SO (MD)
XR-C277	Low Voltage Receiver	JEDEC SO (D)
XR-346	Programmable Quad Op-Amp	JEDEC SO (D)
XR-501	Hard Disk Read/Write Interface	JEDEC SO (D), PLCC (CJ)
XR-501R	Hard Disk Read/Write Interface	JEDEC SO (D), PLCC (CJ)
XR-505	Low Power Single Supply Disk Drive Read/Write Amplifier	JEDEC SO (D), PLCC (CJ)
XR-510A	Hard Disk Read/Write Interface	JEDEC SO (D), PLCC (CJ)
XR-510AR	Hard Disk Read/Write Interface	JEDEC SO (D), PLCC (CJ)
XR-532	Low Power Single Supply Pulse Detector	JEDEC SO (D), PLCC (CJ)
XR-541	Disk Drive Pulse Detector	JEDEC SO (D), PLCC (CJ)
XR-L555	Micropower Timing Circuit	Japanese SO (MD)
XR-567	Monolithic Tone Decoder	Japanese SO (MD)
XR-L567	Micropower Tone Decoder	Japanese SO (MD)
XR-1001/1008	General Purpose Low Pass Filters	JEDEC SO (D)
XR-1010	Second Order Switched Capacitor Filter	JEDEC SO (D)
XR-1016	Seventh Order Switched Capacitor Filter	JEDEC SOL (D)
XR-2100	V.21 Modem	PLCC (CJ)
XR-2135A	Bell/CCITT Type Data Buffer	JEDEC SOL (D)
XR-2206	Monolithic Function Generator	JEDEC SO (MD)
XR-2207	Voltage Controlled Oscillator	JEDEC SO (D)
XR-2211	FSK Demodulator/Tone Decoder	JEDEC SO (D), Japanese SO (MD)
XR-2321	V.23/V.21 Modem	PLCC (CJ)
XR-2400	V.22bis Modem	PLCC (CJ)
XR-2403B	Enhanced MNP 5 Modem Microcontroller	PLCC (CJ)
XR-2900	FAX Data Modem	PLCC (CJ)
XR-T3052	Sinlge Chip Codec / Filter Circuit	PLCC (CJ)
XR-T3053	Single Chip Codec / Filter Circuit	PLCC (CJ)
XR-3524	Pulse-Width Modulating Regulator	Japanese SO (MD)
XR-4136	Quad Operational Amplifier	Japanese SO (MD)
XR-4151	Voltage-to-Frequency Converter	Japanese SO (MD)
XR-T56L22	Low Power PCM Receiver/Repeater	JEDEC SO (D)
XR-T5650	PCM Line Receiver & Clock Recovery Circuit	JEDEC SO (D)
XR-T5675	PCM Line Driver	JEDEC SO (D)

Part No.	Description	SO Package (Suffix)
XR-T5690	T1/ISDN Primary Rate Framer	PLCC (CJ)
XR-T5691	T1/ISDN Primary Rate Framer	PLCC (CJ)
XR-6118	Fluorescent Display Driver	Japanese SO (MD)
XR-T6420-2	Speakerphone Audio Control Circuit	PLCC (CJ)
XR-8038	Precision Waveform Generator	Japanese SO (MD)
XR-9600	V.32 High Speed Modem	PLCC (CJ)
XR-13600	Dual Transconductance Op-Amp	JEDEC SOL (D), Japanese SO (MD)
XR-16C450	CMOS UART	PLCC (CJ)
XR-34072	Dual High Performance Op-Amp	JEDEC SO (D)
XR-34074	Quad High Performance Op-Amp	JEDEC SO (D)
XR-T34118	Voice Switched Speakerphone IC	SOIC
XR-T34119	Low Power Audio Amplifier	SOIC
XR-T61574	PCM Line Interface	PLCC (CJ)
XR-68C681	CMOS Dual Channel UART (DUART)	PLCC (CJ, J) CLCC (ML)
XR-82C684	CMOS Quad Channel UART (QUART)	PLCC (CJ, J)
XR-88C681	CMOS Dual Channel UART (DUART)	PLCC (CJ, J) CLCC (ML)

Ordering Information
(for products introduced prior to 1989)

Part Identification

XR
Manufacturer's Prefix

XXXXX
Basic Type

Grade

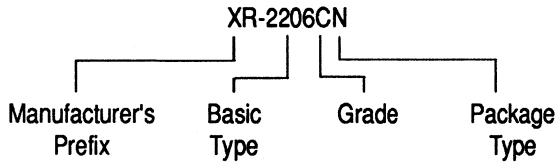
M = Military
N = Prime Electrical
P = Prime Electrical
C = Commercial

F = 4.75 V to 15 V Operating
V = 4.75 V to 6 V Voltage Ranges
K = Kit

Package Type

N = Ceramic Dual-in-Line
P = Plastic Dual-in-Line
MD = Plastic SOIC (Surface Mount)
Q = Quad Package

Example



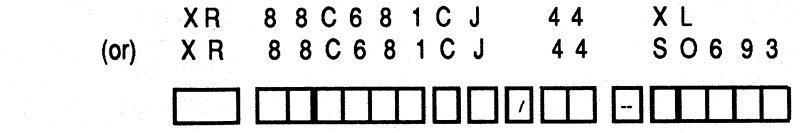
Definition of Symbols:

M = Military Grade Part, Ceramic Package Only are guaranteed to operate over military temperature range. Consult factory for level of high rel screening
N = Prime Grade Part, Ceramic Package
P = Prime Grade Part, Plastic Package

N, P, CN, and CP parts are electricaly identical and operate over 0°C to +70°C unless otherwise stated. In addition, N and P parts generally have operating parameters more tightly controlled than the CN or CP parts.

For details, consult EXAR Sales Headquarters or your Sales/Technical Representatives.

Ordering Information (Continued)
(for products introduced after 1989)
Example



XR Logo
(Mandatory)

Generic Part #
(Mandatory)
1. Max. Alphanumeric
2. Hyphens are permitted.

Temperature Range
(Mandatory)
(see Table 1)

This field is optional, it can be used for:
1. Bin. Eg. XR6118P-1
2. Speed
3. Screen Level. See Table 3
4. Cust. Spec.
Esc. XR88C681CJ/44-SO693

Pin Count
Mandatory for parts with multiple pin count option in same package type.
Eg. XR88C681CP/40
XR88C681CP/28

Package Description
(Mandatory) (see Table 2)

Ordering Information (Continued)

Table 1. Temperature Range

Suffix	Description
C	(O°C to +70°C)
W	As spceified on data sheet
I	(-40°C to +85°C)
M	(-55°C to +125°C)

Table 2. Package Description

P	Plastic DIP
N	Ceramic DIP
J	PLCC Plastic Leaded Chip Carrier
L	LCC Ceramic Leadless Chip Carrier
D	JEDEC SOIC
Q	Quad Flat Pack
K	Japanese SOIC
H	Hybrid

Table 3. Screen Level

	Plastic (P)			Ceramic (N)		
Screening	STD	XL2	XL3	STD	XL5	XL6
Pre cap. internal visual	X	per. XR Std.	per. XR Std.	X	per. XR Std.	per. XR Std.
Sta. Bake		6 hrs @ 175°C	6 hrs @ 175°C	X		
Temp. Cycling		-65°C to +150°C	-65°C to +150°C	X	-65°C to +150°C	-65° to +150°C
Const. Accel.				X	30,000 GY1 ax.	30,000 GY1 ax.
Fine Leak				1%AQL	1%AQL	1%AQL
Gross Leak				1%AQL	1%AQL	1%AQL
Pre Burn In Electrical		100%	100%		100%	100%
Burn In		48 hours	160 hours		48 hours	160 hours
Final Electrical	X	100%	100%	X	100%	100%
AQL Sample	0.1%	0.1%	.0.1%	X	0.1%	0.1%
External Visual	X	per XR Std.	per XR Std	X	per XR Std	per XR Std
QA Plant Clearance	X	100%	100%	X	100%	100%

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Part Number	Description	Product Features	Technology	Supply Voltages	Package
PCM Repeaters					
XR-C240	Monolithic PCM Repeater	Recovers and Regenerates AMI Encoded Data 1 Port ALBO 13.5mA Supply Current 2.048 MBPS (6300 ft) Operation Pulsed Clock Recovery	Bipolar	+8.2V ±5% +4.3V ±5%	16 Pin Ceramic
XR-C262 XR-C262Z (Improved ALBO)	Monolithic PCM Repeater	Recovers and Regenerates AMI Encoded Data 15mA Supply Current 2.048 MBPS (6300 ft) Operation Pulsed Clock Recovery Automatic Zero Input Shutdown	Bipolar	+6.8V ±5%	16 Pin Ceramic
XR-C277	High Performance Low Power Repeater	Recovers and Regenerates AMI Encoded Data 1ALBO Port 13mA Supply Current 2.048 MBPS (6300 ft) Operation Pulsed/Locked Clock Recovery	Bipolar	+6.3V ±5% +4.3V ±5%	16 Pin Ceramic
XR-TM044H		Line Equalization Optimized to 1.544MBPS Complete ALBO Circuitry Smoothing ALBO Filter Network Fixed Gain and Compensation Network Improved Crosstalk and Noise Through Simplified Layout	Hybrid	+5V ±10%	16 Pin Ceramic
XR-T5600/ T5620	High Performance PCM Repeater	Recovers and Regenerates AMI Encoded Data Triple Matched ALBO Ports 22mA Supply Current 2.37 MBPS (6300 ft) Operation Pulsed Clock Extraction	Bipolar	+5.1V ±5%	18 Pin Ceramic Plastic
XR-T5720	High Performance Crystal Clock Repeater	Recovers and Regenerates AMI Encoded Data Triple Matched ALBO Ports 22mA Supply Current 2.37 MBPS (6300 ft) Operation Crystal Clock Extraction	Bipolar	+5.1V ±5%	18 Pin Ceramic Plastic
XR-T56L22	High Performance, Long Haul PCM Repeater	Extracts +Data, -Data & Clock Dynamic Range: 5 to 42dB Very Low Power (8.75mA Max) Applications: T1, CEPT Double Matched ALBO Ports Operating Range: -40°C to +85°C Internal Shunt Regulator Internal Adjustable Phase Shift Circuit	Bipolar	+5V ±5%	18 Pin Ceramic Plastic S.O.P.
PCM Line Interface					
XR-T5681	Short Distance, Low Power PCM Line Interface	Receiver and Transmitter in One Package Dynamic Range: 0 to 10dB Balanced or Unbalanced Receiver Inputs All TTL Compatible Interface LC Clock Extraction Applications: Up to 3MBPS Supply Current: 35mA	Bipolar	+5V ±5%	18 Pin Ceramic

Part Number	Description	Product Features	Technology	Supply Voltages	Package
XR-T5683	Short Distance, High Freq. PCM Line Interface	Receiver and Transmitter in One Package Dynamic Range: 0 to 10dB Balanced or Unbalanced Receiver Inputs All TTL Compatible Interface LC Clock Extraction Applications: Up to 8.448MBPS Supply Current: 40mA	Bipolar	+5V ±5%	18 Pin Ceramic
XR-T5684	Short Distance DSX-1 PCM Line Interface	Receiver and Transmitter in One Package Dynamic Range: 0 to 10dB (DSx-1 Interface) Accepts Balanced or Unbalanced Inputs TTL Compatible Interfaces No LC Tuning Required Meets Bell Pub 62411, Pub 43802 and G.703 Transmitter Equalizer From 0 to 655 feet	CMOS	+5V ±5%	28 Pin Ceramic Plastic S.O.P.
XR-T61574	PCM Line Interface	PCM Line Interface for T1 or CEPT Applications Pulse Shaping Line Driver and Clock/Data Recovery Functions Jitter Attenuator Microprocessor Controllable Compatible with CSU's DAC's Diagnostic Features Pin and Functionally Compatible to CS61574	CMOS	+5V ±10%	Plastic PLCC
XR-T56L85	Short Distance, Single Ended PCM Line Interface	Receiver and Transmitter in One Package Dynamic Range: 0 to 10dB Receiver Accepts: Transformer Input Capacitive Coupled Single Coaxial Input TTL Compatible Inputs LC Clock Extraction Applications: T1, CEPT Very Low Power (14mA Typ) Pin Compatible with XR-T5683	Bipolar	+5V ±5%	18 Pin Ceramic Plastic S.O.P.
XR-T6164	Codirectional G.703 CCITT Line Interface	Analog IC (Short Line Transceiver Function Adaptive Detection Threshold Dual High Current Line Drivers Loss of Signal Alarm	Bipolar	+5V ±5%	16 Pin Ceramic
XR-T6165 XR-T6166	Codirectional G.703 CCITT Line Interface	Digital IC (Digital Data Processor) Converters 64kbit/s Data to 2.048MBPS Data and Vice Versa Recovers Both Clock and Octet Timing Performs Byte Insertion and Deletion Programmable Loss of Lock Alarm AMI Coding and Bipolar Violation Insertion	CMOS	+5V ±5%	22 Pin Ceramic
XR-T3400	3rd Ordering Line Interface	34Mbps CCITT G.703 Compatible Transmitter and Receiver in One IC 1 ALBO Port (20db Dynamic Range) Diagnostic Loopback Capability BiCMOS Technology Signal Loss Monitor Driver Activity Monitor CMOS Level Inputs and Outputs	Bipolar	±5V ±10%	28 Pin Plastic 44 Pin PLCC

Part Number	Description	Product Features	Technology	Supply Voltages	Package
XR-T4500	T3 Line Interface	T3 or STS-1 Line Receive and Transmit Functions Automatic Line Build out (ALBO) for up to 900 ft. Built in Transmit Pulse Shaping Circuit Requiring no Relays or Plug in Modules Diagnostic Loopback Capability Advanced BiCMOS Technology Signal Loss Monitor PLL Clock Recovery Requires no Tuning CMOS Level Inputs and Outputs Minimal External Components	Bipolar	±5V ±10%	44 Pin PLCC
Framers					
XR-T5690	Serial T1 Framer	Supports 12 Frame and 24 frame / Superframe Pin Compatible to: DS2180 B8ZS, B7 Stuffing and Zero Suppression Modes Operates in Hardware or Serial Processor Mode 0, 2, 4 and 16 State Robed Bit Signaling Modes Clear and Non-Clear DS0 Channels on DS1 Link Alarm Generation and Detection Receive Error Detection and Counting	CMOS	+5V ±5%	40 Pin Plastic 44 Pin PLCC
XR-T5691	Receive Buffer	Synchronize T1 Data Streams to System Clocks Two Frame Buffer Depth Frame Slip Output at Frame Boundaries Buffer Recentering Capability Recommended Operating Frequency: 1.544 and 2.048 MBPS Interfaces to Parallel and Serial Backplanes Robbed-bit Signaling Extraction and Buffering Inhibits Signaling Updates During Alarm or Slip Conditions Integration Feature "Debounces" Signaling Pin Compatible to: DS2176	CMOS	+5V ±5%	24 Pin Plastic PLCC
Coder/Decoder					
XR-T3052 XR-T3053 XR-T3054 XR-T3057	Codec Filter Interface IC	Transmit High Pass, Low Pass Filtering Pin Compatible to NS 3052/53/54/57 Receive Sinx /x Correction Filtering U and A Law Coding and Decoding Internal Auto Zero Circuitry Serial I/O Interface Typical Power 60mW, Power Down 3mW	CMOS	±5V ±5%	18 Pin Ceramic 20 Pin PLCC 20 Pin Ceramic 16 Pin Ceramic 16 Pin Ceramic 20 Pin PLCC
XR-T5670	B8ZS/AMI Line Transcoder	B8ZS/AMI Coding and Decoding Max Frequency: 6MHz Complies to Tech Advisory 69 Code Error Detector Looptest Capability All Ones Alarm Indicator	CMOS	+5V ±5%	16 Pin Ceramic Plastic
Loopback Circuits					
XR-T2713	Loopback Detector	Loopback Detector According to Bell Pub 4300 Detection Band: 2713 or 2813 ± 15Hz Detection Level: -32dB Complementary Output Signal Low Power (2mA @ 12V) 4 or 20 minutes Time Out	CMOS	+5V ±5%	16 Pin Plastic

Part Number	Description	Product Features	Technology	Supply Voltages	Package
Drivers/Receivers					
XR-T3588 XR-T3589	V.35 Line Driver/Receiver	CCITT V.35 & Bell 306 Compatible Interface Driver Inputs and Receiver Output are TTL High Common Mode Voltage Range 10MBPS Operation Capability Individual Power Down Capability	Bipolar	+ 5V ±5%	18 Pin Ceramic 14 Pin Ceramic
XR-T5650	Long Distance PCM Line Receiver	Extracts +Data, -Data & Clock Dynamic Range 10 to 36dB Applications: T1, CEPT Double Matched ALBO Ports	Bipolar	+5V ±5%	18 Pin Ceramic
XR-T5675	PCM Line Driver	High Speed Switching Dual Matched Driver Outputs TTL or DTL Compatible Inputs 50mA Output Current Capability Current Consumption: 18mA	Bipolar	+5V ±5%	8 Pin Ceramic Plastic
XR-T5676	Low Power PCM Line Receiver	Low Power T1/CEPT Receiver Up to 2.048 MBPS Operation TTL Compatible Interface Inputs: Balanced Transformer Capacitively Coupled Single Coaxial	Bipolar	+5V ±10%	Ceramic Plastic SOIC
Speakerphones					
XR-T6420-1	Speakerphone Audio Front Circuits	Two Matched Variable Cells Internal Microphone Amplifier Independent Transmitting & Receiving Control Gains and Frequency Response Control	Bipolar	±5V ±5%	20 Pin Ceramic Plastic
XR-T6420-2	Speakerphone Audio Front Circuits	Two Matched Variable Cells Internal Microphone Amplifier Independent Transmitting & Receiving Control Gains and Frequency Response Control Enable and Mute Logic Pins	Bipolar	±5V ±5%	24 Pin PLCC Plastic
XR-T6421	Speakerphone Audio Control IC	External Control of Attack and Decay Time Independent Gain & Frequency Response Control Background Noise Detection and Suppression Low Power Consumption	Bipolar	+5V ±5%	24 Pin Plastic PLCC
XR-T34118	Voice Switched Speakerphone Circuit	Attenuator Gain Range: 52dB Improved Sensitivity: 4 Point Signal Sensing Background Noise Monitor on Transmit and Receive Sides Mute Feature with Externally Adjustable Microphone Amplifier Gain Chip Disable for Active/Standby Operation On Board Filter Pinned Out for User Defined Function Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence Compatible with the XR-T34119 Speaker Amplifier	Bipolar	+5V ±10%	Plastic SOIC
XR-T34119	Low Power Audio	Low Quiescent Supply Current (2.7mA Typical-Battery Powered Applications) Chip Disable Input for Power Down Applications Low Power Down Quiescent Current (65µA typical) Wide Range Drive Capability (8-100 ohms) Low Harmonic Distortion (0.5% typical) Adjustable Gain (0 to 46dB for Voice Band)	Bipolar	+5V ±10%	Plastic SOIC

Monolithic PCM Repeater

GENERAL DESCRIPTION

The XR-C240 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (Mbps) data rate on T1-type PCM lines.

The XR-C240 monolithic IC is packaged in a hermetic 16-Pin DIP package, and is designed to operate over a temperature range of -40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Build-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

Compared to conventional repeater designs using discrete components, the XR-C240 monolithic repeater IC offers greatly improved reliability and performance, along with significant savings in power consumption and system cost.

FEATURES

Contains all Active Components of PCM Repeater
On-Chip ALBO Port
High-Current Output Drivers
Low-Power Consumption
Increased Reliability over Discrete Designs
2 Megabit Operation Capability

APPLICATIONS

PCM Repeater for T1 Systems
PCM Repeater for 2 M Bit/s Systems

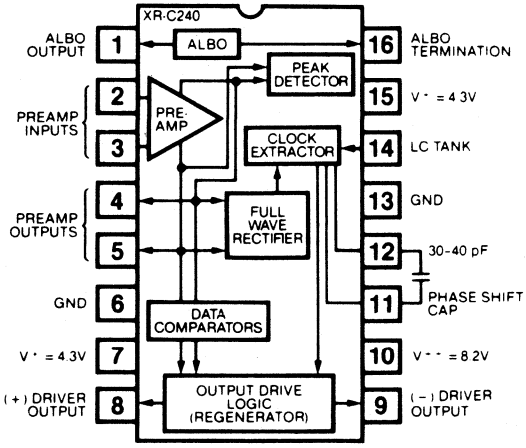
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Supply Voltage	-0.5 to 10 V
Input Voltage (Except Pin 1,16)	-0.5 to +7 V
Input Voltage (Pin 7,16)	-0.5 to +0.5 V
Data Output Voltage (Pin 8,9)	+20 V
Voltage Surge (Pin 2,3,8,9) (10 msec only)	50 V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-C240	Ceramic	-40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-C240 contains all the active circuits required to build one side of a T1 or 2 M bit/s PCM repeater. T1 is the most widely used PCM transmission system, operating at 1.544 M bit/s. It can operate on either pulp or plastic insulated twisted pair cables. Although the cable gauge may vary, the total cable loss should not exceed 36 dB at 772 kHz. For a 22 gauge pulp insulated cable and a bit error rate (BER) of less than 10^{-6}, the max allowable repeater to repeater spacing is about 6300 feet.

Bipolar PCM signal is attenuated and dispersed in time as it travels along a transmission cable. This signal, when received, is amplified and reconstructed by the preamplifier automatic line build out (ABLO), clock and data threshold detector circuits contained within the XR-C240. Amplitude equalization and frequency spectrum shaping is achieved through the variable impedance of the ALBO ports and its associated ALBO network.

Incoming pulse stream is full wave rectified and timing information is extracted by the clock threshold detector. Clock recovery is then achieved by driving an injection locked oscillator tuned to 1.544 MHz. The oscillator's sinusoidal waveform is amplified and phase shifted by 90 degrees with the help of a capacitor between Pins 11 and 12.

Data is sampled and stored in the output data latches by an internally generated sampling pulse. Buffer drivers are then enabled to produce precisely timed output pulses whose width and time of occurence are controlled by the regenerated clock signal.

ELECTRICAL CHARACTERISTICS

(Measured at 25°C with V++ = 8.2V, V+ = 4.3V, unless specified otherwise.)

PARAMETERS	LIMITS MIN.	LIMITS MAX.	UNIT	CONDITIONS
Supply Voltage:				
V++	7.79	8.61	V	Measured at Pin 10
V+	4.085	4.515	V	Measured at Pins 7 and 15
Supply Current:				
I_A	1.1	2.5	mA	
I_B	6	11	mA	Supply = 8.2V
Total Current	7.9	13.5	mA	
Preamplifier				
Input Offset Voltage, V_{OS}		15	mV	
Open Loop Differential Gain, A_O	50	54	dB	
Input Bias Current, I_B		4	µA	
Input Offset Current, I_{OS}		2	µA	
Input Impedance, R_{in}	50		kΩ	
Comparator Thresholds				
Peak Detector (ALBO) Threshold	±1.3	±1.6	V	Measured Differentially Across Pins 4 and 5
Full-Wave Rectifier Threshold	±0.9	±1.15	V	
Data Threshold	±0.28	±0.48	V	
Clock Extractor Section				
Tank Drive Impedance	50		kΩ	At Pin 14
Tank Drive Current				
"Zero" Signal Current	12	24	µA	
"One" Signal Current	80	220	µA	
Recommended Tank Q	100			
Phase Shifter Offset Voltage	-18	+18	mV	Voltage applied to Pins 7 and 14 to reduce differential voltage across Pins 11 and 12 to zero.
Output Drive Section				
				Voltage levels referenced to Pin 7
Output Voltage Swing	3.0		V	R_L = 100 Ω
Low Output Voltage	0.65	0.95	V	Referenced to Pin 7, I_L = 30 mA
Output Leakage Current		50	µA	
Output Pulse				
Maximum Pulse Width Error		±30	ns	
Rise and Fall Times		80	ns	

High-Performance PCM Repeater

GENERAL DESCRIPTION

The XR-C262 is a high-performance monolithic repeater IC for pulse-code modulated (PCM) telephone lines. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (Mbps) data rates on T1-type PCM lines.

The XR-C262 operates with a single 6.8 volt power supply, and with a typical supply current of 13 mA. It provides bipolar output drive with high-current handling capability. The clock-extractor section of XR-C262 uses the resonant-tank circuit principle, rather than the injection-locked oscillator technique used in earlier monolithic repeater designs. The bipolar output drivers are designed to go to their "off" state automatically, when there is no input signal present.

FEATURES

Contains all Necessary Active Components of a PCM Repeater
Uses L-C Tank for Clock Recovery
Low-Voltage Operation (6.8 volts)
Low-Current Drain (13 mA, typical)
High-Current Bipolar Output Drivers
On-Chip ALBO Equalizer
Automatic Zero-Input Shutdown
Increased Reliability Over Discrete Designs
2 Megabit Operation Capability

APPLICATIONS

PCM Repeater for T1 Systems
Repeater for 2 Megabit PCM Systems

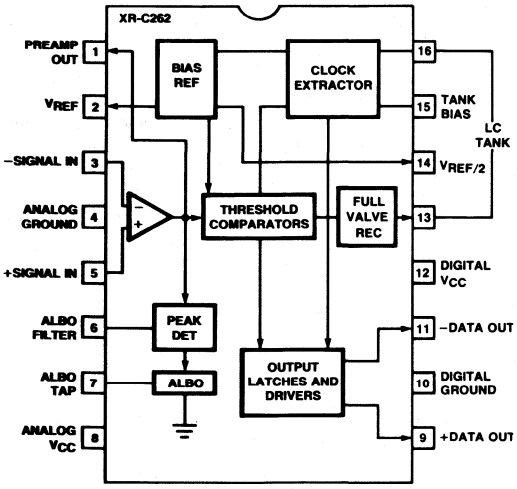
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Operating Temperature	−40°C to +85°C
Supply Voltage	−0.5 to +10 V
Input Voltage (Except Pin 6,7)	−0.5 to +7 V
Input Voltage (Pin 6,7)	−0.5 to +0.5 V
Data Output Voltage (Pin 9,11)	+20 V
Voltage Surge (Pin 3,5,9,11) (10 msec only)	50 V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-C262	Ceramic	−40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-C262 contains all the active functions required to build one side of a T1 or 2 M bit/s PCM repeater. T1 is the most widely used PCM transmission system, operating at 1.544 M bit/s. It can operate on either pulp or plastic insulated twisted pair cables. Although the cable gauge may vary, the total cable loss should not exceed 36 dB at 772 kHz. For a 22 gauge pulp insulated cable and a bit error rate (BER) of less than 10^{-6}, the max allowable repeater to repeater spacing is about 6300 feet.

Bipolar PCM signal is attenuated and dispersed in time as it travels along a transmission cable. This signal, when received, is amplified and reconstructed by the peamplifier automatic line build out (ALBO), clock and data threshold detector circuits contained within the XR-C262. Amplitude equalization and frequency spectrum shaping is achieved through the variable impedance of the ALBO port and its associated ALBO network.

Incoming pulse stream is full wave rectified and timing information is extracted by the clock threshold detector. Clock recovery is then achieved by pulsing a tank circuit tuned to 1.544 MHz.

Data is sampled and stored in the output data latches. Buffer drivers are then enabled to produce precisely timed output pulses whose width and time of occurrence are controlled by the regenerated clock signal.

ELECTRICAL CHARACTERISTICS

Test Conditions: $+V_{CC}$ = 6.8 V, T_A = −40°C to +85°C.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
Supply Current					
Digital Current	7	10	13	mA	Measured at Pin 12
Analog Current	2	3.5	5	mA	Measured at Pin 8
Total Current		13	17	mA	
Preamplifier					
Input Offset Voltage	−15		+15	mV	Measured between Pins 3 and 5
DC Gain	60	69	74	dB	
Output High Level	4.3			V	Measured at Pin 1
Output Low Level			0.5	V	Measured at Pin 1
Clock Recovery Section					
Clock Drive Swing (High)	5.1			V	Measured at Pin 13
Clock Drive Swing (Low)			3.8	V	Measured at Pin 13
Clock Bias	3.8	4	4.2	V	Measured at Pin 15
Clock Source Input Current		0.5	4	μA	Measured at Pin 16
Comparator Thresholds					Measured at Pin 1 relative to Pin 14
ALBO Threshold	0.75	0.9	1.1	V	
Clock Threshold	0.323	0.4	0.517	V	
Data Threshold	0.323	0.4	0.517	V	
Internal Reference Voltages					
Reference Voltage	5.2	5.45	5.55	V	Measured at Pin 2
Divider Center Tap	2.6	2.78	2.85	V	Measured at Pin 14
ALBO Section					
Off Voltage		10	75	mV	Measured at Pin 7
On Voltage	1.2		1.7	V	Measured at Pin 7
On Impedance			15	Ω	Measured at Pin 7
Filter Drive Current	0.7	1	1.5	mA	Drive current available at Pin 6
Output Driver Section					Measured at Pins 9 and 11
Output High Swing	5.9	6.8		V	R_L = 400 Ω
Output Low Swing	0.6	0.7	0.9	V	I_L = 15 mA
Leakage Current			100	μA	Measured with output in off state
Output Pulse Width	294	324	354	nsec	
Output Rise Time			100	nsec	
Output Fall Time			100	nsec	
Pulse Width Unbalance			15	nsec	

High-Performance PCM Repeater

GENERAL DESCRIPTION

The XR-C262Z is a high-performance monolithic repeater IC for pulse-code modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (Mbps) data rate on T1-type PCM lines.

The XR-C262Z operates with a single 6.8 volt power supply, and with a typical supply current of 13 mA. It provides bipolar output drive with high-current handling capability. The clock-extractor section of XR-C262Z uses the resonant-tank circuit principle, rather than the injection-locked oscillator technique used in earlier monolithic repeater designs. The bipolar output drivers are designed to go to their "off" state automatically, when there is no input signal present.

FEATURES

Contains all Necessary Active Components of a PCM Repeater
Uses L-C Tank for Clock Recovery
Low-Voltage Operation (6.8 volts)
Low-Current Drain (13 mA, typical)
High-Current Bipolar Output Drivers
On-Chip ALBO Port
Automatic Zero-Input Shutdown
Increased Reliability Over Discrete Designs
2 Megabit Operation Capability
Pin-to-Pin Compatible with XR-C262 with Improved Switching Characteristics

APPLICATIONS

PCM Repeater for T1 Systems
PCM Repeater for 2 M Bit/s Systems

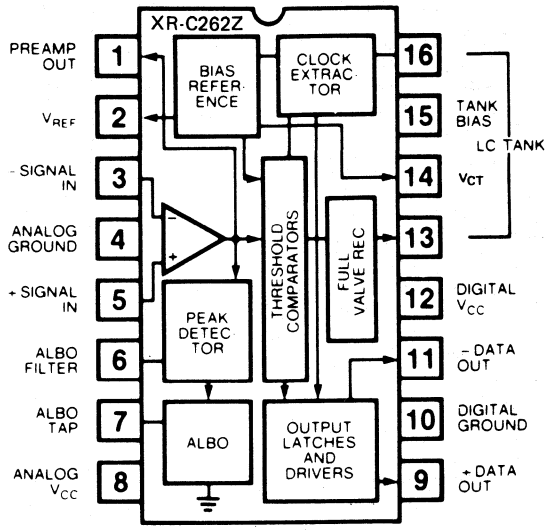
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Supply Voltage	-0.5 to +10 V
Input Voltage (Except Pin 6,7)	-0.5 to +7 V
Input Voltage (Pin 6,7)	-0.5 to +0.5 V
Data Output Voltage (Pin 9,11)	+20 V
Voltage Surge (Pin 3,5,9,11) (10 msec only)	50 V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-C262Z	Ceramic	-40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-C262Z contains all the active functions required to build one side of a T1 or 2 M bit/s PCM repeater. T1 is the most widely used PCM transmission system, operating at 1.544 M bit/s. It can operate on either pulp or plastic insulated twisted pair cables. Although the cable gauge may vary, the total cable loss should not exceed 36 dB at 772 kHz. For a 22 gauge pulp insulated cable and a bit error rate (BER) of less than 10^{-6}, the max allowable repeater to repeater spacing is about 6300 feet.

Bipolar PCM signal is attenuated and dispersed in time as it travels along a transmission cable. This signal, when received, is amplified and reconstructed by the preamplifier automatic line build out (ALBO), clock and data threshold detector circuits contained within the XR-C262Z. Amplitude equalization and frequency spectrum shaping is achieved through the variable impedance of the ALBO ports and its associated ALBO network.

Incoming pulse stream is full wave rectified and timing information is extracted by the clock threshold detector. Clock recovery is then achieved by pulsing a tank circuit tuned to 1.544 MHz.

Data is sampled and stored in the output data latches. Buffer drivers are then enabled to produce precisely timed output pulses whose width and time of occurence are controlled by the regenerated clock signal.

ELECTRICAL CHARACTERISTICS

Test Conditions: $+V_{CC}$ = 6.8 V, T_A = −40°C to +85°C, unless specified otherwise.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
SUPPLY CURRENT					
Digital Current	6	10	13	mA	Measured at Pin 12
Analog Current	1.5	3.5	5	mA	Measured at Pin 8
Total Current		13	15	mA	
PREAMPLIFIER					
Input Offset Voltage	−15		+15	mV	Measured between Pins 3 & 5
Open Loop Gain	58	69	76	dB	
Output High Level	4.3			V	Measured at Pin 1
Output Low Level			0.8	V	Measured at Pin 1
CLOCK RECOVERY SECTION					
Clock Drive Swing (High)	5.1			V	Measured at Pin 13
Clock Drive Swing (Low)			4.0	V	Measured at Pin 13
Clock Bias	3.8	4		V	Measured at Pin 15
Clock Source Input Current		0.5	4	μA	Measured at Pin 16
COMPARATOR THRESHOLDS					
ALBO Threshold	0.75	0.9	1.1	V	Measured at Pin 1 relative to Pin 14
Clock Threshold	0.323	0.4	0.517	V	
Data Threshold	0.323	0.4	0.517	V	
INTERNAL REFERENCE VOLTAGES					
Reference Voltage	5.0	5.45	5.65	V	Measured at Pin 2
Divider Center Tap	2.5	2.78	2.85	V	Measured at Pin 14
ALBO SECTION					
Off Voltage		10	75	mV	Measured at Pin 7
On Voltage	1.2		1.7	V	Measured at Pin 7
On Impedance			15	Ω	Measured at Pin 7
Filter Drive Current	0.7	1	3	mA	Drive Current available at Pin 6
OUTPUT DRIVER SECTION					Measured at Pins 9 & 11
Output High Swing	5.9	6.8		V	R_L = 400Ω
Output Low Swing	0.5	0.7	1.0	V	I_L = 15 mA
Leakage Current			100	μA	Measured with output in off state
Output Pulse Width	298	324	350	nsec	
Output Rise Time			80	nsec	
Output Fall Time			80	nsec	
Pulse Width Unbalance			15	nsec	

Low-Voltage PCM Repeater

GENERAL DESCRIPTION

The XR-C277 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (Mbps) data rate on T1-type PCM lines. It is packaged in a hermetic 16-Pin CERDIP package and is designed to operate over a temperature range of -40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system, including Automatic Line Build-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

The key feature of the XR-C277 is its ability to operate with low supply voltage (6.3 volts and 4.3 volts) with a supply current of less than 13 mA. Compared to conventional repeater designs using discrete components, the XR-C277 monolithic repeater IC offers greatly improved reliability and performance, along with significant savings in power consumption and system cost.

The XR-C277-5F is an improved version of XR-C277 with an internal feedback that improved the phase gain margin which enables the system to be more stable and less sensitive to PC board layouts.

Other versions of the XR-C277-5F are XR-C277-F and XR-C277-FL. XR-C277-F is an AC tested device of XR-C277-5F at 2 Mbit while XR-C277-FL is the equivalent at 1.544 Mbit.

FEATURES

Contains all the Active Components of a PCM Repeater
Low-Voltage Operation (6.3 volts)
Low-Power Dissipation (13 mA)
On-Chip ALBO Port
High-Current Output Drivers
Increased Reliability over Discrete Designs
2 Megabit Operation Capability
Pin-Compatible with XR-C240

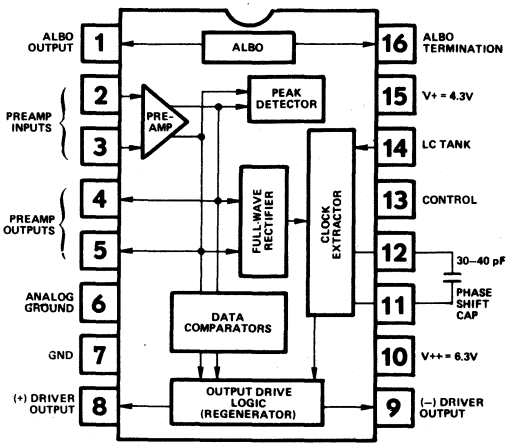
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Supply Voltage	-0.5 to +10 V
Input Voltage (Except Pin 1,16)	-0.5 to +7 V
Input Voltage (Pin 1,16)	-0.5 to +0.5 V
Data Output Voltage (Pin 8,9)	20 V
Voltage Surge (Pin 2,3,8,9) (10 msec only)	50 V

APPLICATIONS

PCM Repeater for T1 Systems
PCM Repeater for 2 M Bit/s Systems

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-C277	Ceramic	-40°C to +85°C
XR-C277-5F	Ceramic	-40°C to +85°C
XR-C277-F	Ceramic	-40°C to +85°C
XR-C277-FL	Ceramic	-40°C to +85°C

SYSTEM DESCRIPTION

The XR-C277 contains all the active circuits required to build one side of a T1 or 2 M bit/s PCM repeater. T1 is the most widely used PCM transmission system, operating at 1.544 M bit/s. It can operate on either pulp or plastic insulated twisted pair cables. Although the cable gauge may vary the total cable loss should not exceed 36 dB at 772 kHz. For a 22 gauge pulp insulated cable and a bit error rate (BER) of less than 10-6 the max allowable repeater to repeater spacing is about 6300 feet.

Bipolar PCM signal is attenuated and dispersed in time as it travels along a transmission cable. This signal, when received, is amplified and reconstructed by the preamplifier automatic line build out (ALBO), clock and data threshold detector circuits contained within the XR-C277. Amplitude equalization and frequency spectrum shaping is achieved through the variable impedance of the ALBO port and its associated ALBO network.

Incoming pulse stream is full wave rectified and timing information is extracted by the clock threshold detector. Clock recovery is then achieved by pulsing a tank circuit tuned to 1.544 MHz. Either injection locking or pulsed tank type clock extraction are possible with the XR-C277. By grounding Pin 13, the circuit works in the injection

ELECTRICAL CHARACTERISTICS

Test Conditions: +25°C, V++ = 6.3V ±5%, V+ = 4.4V ±5%, unless specified otherwise.

PARAMETERS	LIMITS			UNITS	CONDITIONS
	MIN.	TYP.	MAX.		
Supply Current					
I_A		3.5		mA	Measured at Pin 10
I_B		7.5		mA	Measured at Pin 15
Total Current	8	11	13	mA	(I_C + I_B)
Preamplifier					
Input Offset Voltage		1.5	15	mV	Measured at Pins 2 and 3
Input Bias Current		0.3	4	µA	Measured at Pins 2 and 3
Voltage Gain	44	48	51	dB	Single-ended Gain
Preamp Output Swing					Measured at Pins 4 and 5
High Swing	3.45	3.6	3.75	V	Maximum Voltage Swing
Low Swing	1.25	1.4	1.55	V	Minimum Voltage Swing
Output DC Level	2.47	2.55	2.72	V	
ALBO Section					
ALBO "Off" Voltage		10	75	mV	Measured from Pin 1 and 16 to Ground
ALBO "On" Voltage	0.6	0.87	1.1	V	Measured at Pin 1
ALBO "On Voltage	1.2	1.5	2.1	V	Measured at Pin 16
ALBO Threshold	1.35	1.50	1.65	V	Measured Differentially Across Pins 4 and 5
Differential Threshold	-75		+75	mV	Threshold Difference for Polarity Reversal at Pins 4 and 5
ALBO "On" Impedance		5	10	Ω	Measured at Pin 1
ALBO "Off" Impedance	20	50		kΩ	Measured at Pin 1
Comparator Thresholds					
Clock Threshold	68	73	78	%	% of ALBO Threshold
Data Threshold	47	50	53	%	% of ALBO Threshold
Clock Extractor					
Oscillator Current	10	14	20	µA	
Tank Drive Impedance		50		kΩ	
Recommended OSC. Q	100				
$I_{injection}/I_{OSC.}$	6.0	7	7.5		Ratio of Current Q_{1B} to Current in Q_{1A}
Output Driver					
Low Output Voltage	0.65	0.75	0.95	V	Measured at Pins 8 and 9 I_L = 15 mA
Output "Off" Current		5	100	µA	V_{out} = 20V
Output Pulse					
Max. Pulse Width Error			±30	n sec	
Rise Time			80	n sec	
Full Time			80	n sec	

lock mode. Floating (open) Pin 13 switches the XR-C277 to a pulse tank mode. The oscillator's sinusoidal waveform is amplified and phase shifted by 90 degrees with the help of a capacitor between Pins 11 and 12.

Data is sampled and stored in the output data latches by an internally generated sampling pulse. Buffer drivers are then enabled to produce precisely timed output pulses whose width and time of occurence are controlled by the regenerated clock signal.

T1 Repeater Equalization Hybrid Module

GENERAL DESCRIPTION

The TM-044H is a passive equalizer module designed for use in conjunction with the XR-C277 repeater/receiver family. The TM-044H provides a complete solution for T1 PCM line repeater or line termination units. Using hybrid technology, the TM-044H replaces 17 precision external components normally required for T1 line equalization (up to 36 dB of cable loss), with automatic line build out (ALBO) and filter network. This simple front stage network provides space saving, enhanced performance, increased reliability and reduction in manufacturing costs.

FEATURES

Line Equalization Optimized to 2.048 MBPS
Complete ALBO Circuitry
Smoothing ALBO Filter Network
Fixed Gain and Compensation Network
Improved Crosstalk and Noise Through Simplified Layout

APPLICATIONS

T1 PCM Line Repeaters and Receivers
CPI
DMI
T1 Test and Maintenance Equipment

ABSOLUTE MAXIMUM RATINGS

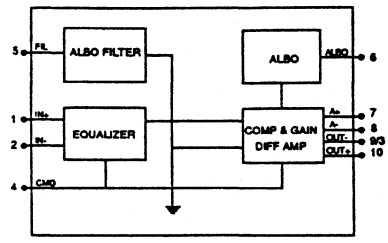
Storage Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

ORDERING INFORMATION

Part Number	Package	Operating Temp.
TM-044H	Ceramic Hybrid	-40°C to +85°C

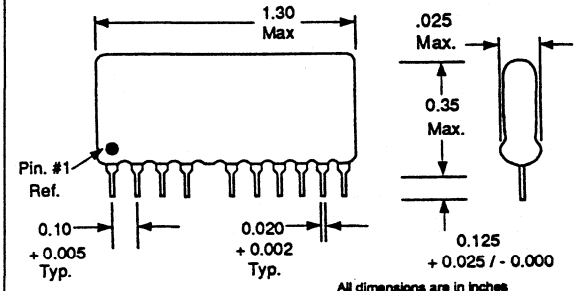
PIN ASSIGNMENT

BLOCK DIAGRAM



SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM OF TM-044H

DIMENSIONS



All dimensions are in inches

SYSTEM DESCRIPTION

The equalizer module includes all the front end circuitry necessary to equalize the incoming bipolar signals, which are attenuated and distorted due to the transmission medium. It is the function of the equalizer when working with the preamplifier of the repeater to provide the necessary amount of gain and phase equalization, so that the attenuated incoming data can be faithfully extracted and regenerated. In addition, the network band limits the input signal in order to optimize the performance of the repeater for near-end crosstalk produced by other systems operating within the same cable bundle.

The ALBO Network is providing an Automatic-Gain-Control for the preamplifier in the feedback loop, such that all input signals applied to the preamplifier will appear to be transmitted from the same cable length, which is usually set at 6,000 ft. The TM-044H also includes our ALBO filter that determines the ALBO time constant for optimum performance.

Other circuits included in the module is a preamplifier gain adjustment network and a simple high pass filter that further reduces any noise on the signals before they are applied to the input of the repeater. The preamplifier gain is set at around 40 dB and this enables the preamplifier to recover signals which have been attenuated more than 36 dB.

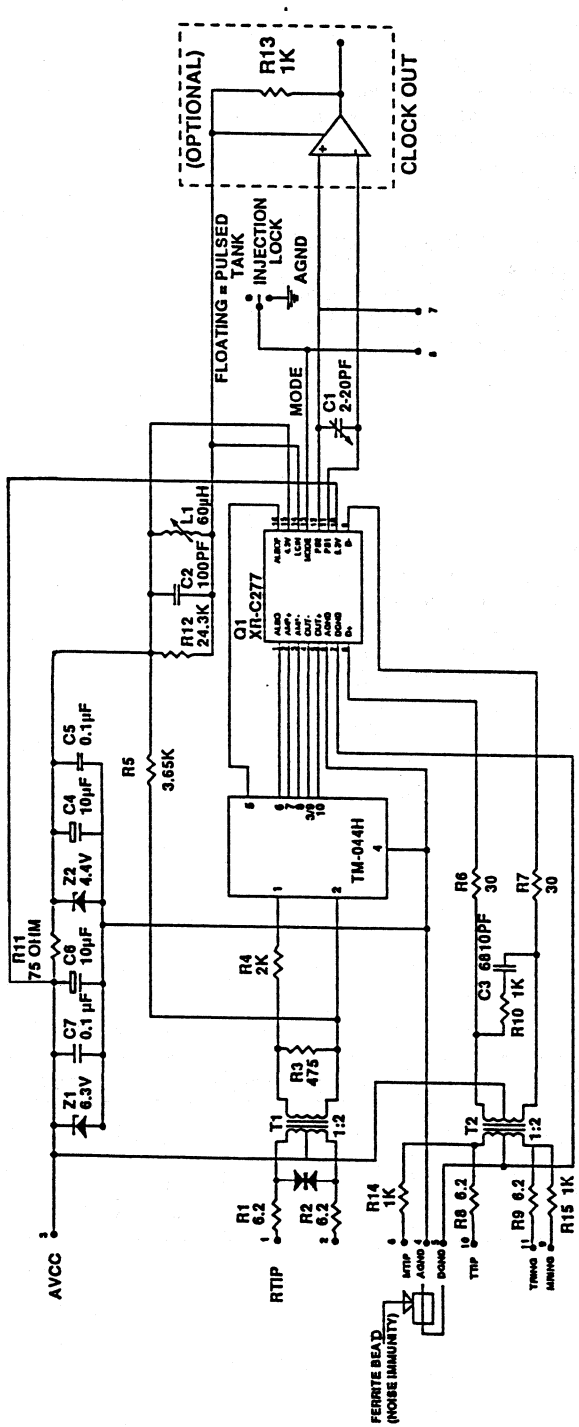
PIN DESCRIPTION

Pins	Description
1-2	Network Input Pins. These two pins connect directly to the secondary side of the isolation transformer. A line termination resistor to minimize reflections and possibly a trimming resistor may be required to maximize performance.
3	This Output pin is connected directly to the negative pre-amplifier output. (XR-C277 pin 4.
4	Ground. (XR-C277 pin 6)
5	Automatic Line Build Out (ALBO) smoothing filter input pin. (XR-C277 pin 16)
6	This input is part of the ALBO feedback network and connect directly to the ALBO output port. (XR-C277 pin 1)
7	Preamplifier negative input pin. (XR-C277 pin 2)
8	Preamplifier positive input pin. (XR-C277 pin3)
9	Same as pin 3. (XR-C277 pin 4)
10	This pin connects to the pre-amplifier negative output pin and determines the preamplifier gain. (XR-C277 pin 5)

DC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V +10% T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	UNIT	MIN	TYP	MAX	CONDITIONS
f-in	Input Frequency	MHz		2.048		1.544 (Adjusted)
Zin	Input Impedance	kohm	3			
t-ALBO	ALBO Time Constant	ns		20		
f-ALBO	ALBO Pole	kHz		60		


(OPTIONAL)
R13
1K
CLOCK OUT
FLOATING = PULSED TANK
INJECTION LOCK
AGND
MODE
C1
2-20PF
L1
60µH
C2
100PF
R12
24.3K
Q1
XR-C277
R5
3.65K
C5
0.1µF
C4
10µF
Z2
4.4V
R11
75 OHM
C6
10µF
C7
0.1 µF
Z1
6.3V
R4
2K
R3
475
TM-044H
R6
30
R7
30
C3
6810PF
R10
1K
T1
1:2
T2
1:2
R1
6.2
R2
6.2
R14
1K
R8
6.2
R9
6.2
R15
1K
AVCC
RTIP
RTIP
AGND
TRIP
TRING
RRING
FERRITE BEAD
(NOISE IMMUNITY)

Triple ALBO PCM Repeater

GENERAL DESCRIPTION

The XR-T5600/T5620 is a bipolar monolithic repeater IC designed for PCM carrier systems operating at 1.544 M bit/s (T1), 2 M bit/s, or 2.37 M bit/s (T148C). It provides all of the active circuits required for one side of a PCM repeater.

FEATURES

Single 5.1 V Power Supply
Less than 10 ns Sampling Pulse over the Operating Range
Triple Matched ALBO Ports
2 M Bit/s Capability

APPLICATIONS

T1 PCM Repeater
T148C PCM Repeater
European 2 M Bit/s PCM Repeater
T1C PCM Repeater (requires external preamplifier)

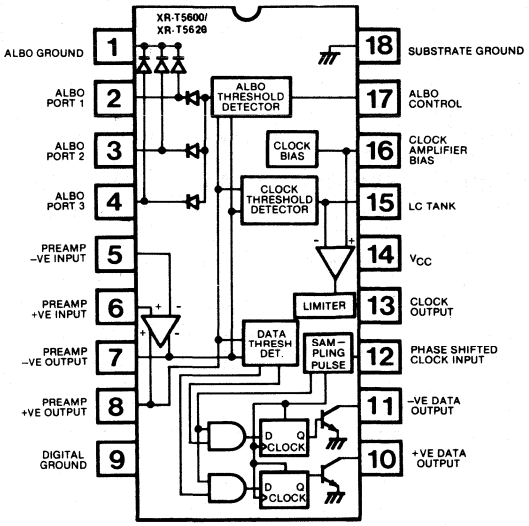
ORDERING INFORMATION

Part Number	Package	Operation Temperature
XR-T5600	Plastic	−40°C to 85°C
XR-T5620	Plastic or Ceramic	−40°C to 85°C

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Supply Voltage	-0.5 to +10 V
Supply Voltage Surge (10 ms)	+25 V
Input Voltage (except Pin 2,3,4,17)	-0.5 to 7 V
Input Voltage (Pin 2,3,4,17)	-0.5 to +0.5 V
Data Output Voltage (Pin 10, 11)	20 V
Voltage Surge (Pin 5,6,10,11) (10 msec only)	50 V

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-T5600/T5620 performs most of the functions required for one side of a PCM repeater operating at 2 M bit/s or similar baud rate. The integrated circuit amplifies the received positive and negative pulses and feeds them into Automatic Line Build-out (ALBO), clock and data threshold detectors, see Figure 1. The ALBO threshold detector ensures that the received pulses at Pins 7 and 8 have the correct amplitude and shape. This is carried out by controlling the gain and frequency shaping of the ALBO network with three variable impedance ALBO ports.

The clock threshold detector extracts timing information from the pulses received at Pins 7 and 8 and passes it into the external tank coil at Pin 15. The sinusoidal-type waveform is amplified into a square wave at Pin 13, and forwarded through an external phase shift network into Pin 12. This waveform provides the data sampling pulse which opens latches into which the data from the data threshold detectors is passed. The resulting pulses are stored for half a bit period (normally 488 ns) in the latches. They appear as half-width output pulses at Pins 10 and 11.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{CC} = 5.1\ V \pm 5\%$, unless specified otherwise (see Figure 1).

PARAMETERS	PINS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Current	14		22	30	mA	
Data Output Leakage Current	10,11		0	100	μA	$V_{pull\text{-}up} = 15\ V$, $V_{CC} = 5.35\ V$
ALBO Port Off Voltage	2,3,4		0	0.1	V	
Amplifier Pin Voltage	5,6,7,8	2.4	2.9	3.4	V	
DYNAMIC CHARACTERISTICS AMPLIFIER						
Output Offset Voltage		-50	0	50	mV	$R_S = 8.2\ k\Omega$
AC Gain @ 1 MHz		47	50	53	dB	
Input Impedance		20			kΩ	
Output Impedance				200	Ω	
ALBO						
ALBO Off Impedance		20		25	kΩ	
ALBO On Impedance				25	Ω	
THRESHOLDS						
ALBO Threshold		1.4	1.5	1.6	V	
Clock Threshold as % of ALBO Threshold		68		80	%	
DATA Threshold as % of ALBO Threshold		42		49	%	
Clock Drive Current		0.7		1.4	mA	At $V_O = V_{ALBO}$ Threshold
OUTPUT STAGES						$R_L = 130\Omega$, $V_{pull\text{-}up} = 5.1 \pm 5\%$
Output Pulse Rise Time				40	ns	
Output Pulse Fall Time				40	ns	
Output Pulse Width		224	244	264	ns	
Output Pulse Width Differential		-10		+10	ns	
Buffer Gate Voltage (Low)		0.65		0.95	V	
Buffer Gate Voltage Differential		-0.15		0.15	V	

ELECTRICAL CHARACTERISTICS

Test Conditions: Unless otherwise stated, all characteristics shall apply over the operating temperature range of -40°C to +85°C with V_{CC} = 5.1 V ± 5%, all voltages referred to ground = 0 V.

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL (Ref. Figure 2)							
I_S	Supply Current	14		22	30	mA	
I_{LD}	Data Output Leakage Current	10,11		6	100	µA	From V_S (See Note 1)
	Amplifier Pin Voltages	5,6,7,8	2.4	2.9	3.4	V	
	ALBO Ports Off Voltage	2,3,4		0	0.1	V	

Note: 1. V_S = 15 V, V_{CC} = 5.35 V

AMPLIFIER (Ref. Figure 2, Only Pins 1, 9, 10...18 connected)							
	Input Offset Voltage	5 & 6	-10		+10	mV	R_S = 8.2 kΩ (See Note 1)
	Input Bias Current	5 & 6	0		5	µA	R_S = 8.2 kΩ (See Note 1)
	Input Offset Current	5 & 6	-1		1	µA	R_S = 8.2 kΩ (See Note 1)
	Output Offset Voltage	7 & 8	-50	0	50	mV	R_S - 8.2 kΩ (See Note 1)
	Common Mode Rejection Ratio	7 & 8	30			dB	V_{CC} ±10%
	Output Voltage Swing	7 & 8	2.2			V	

Note: 1. R_S = Source Resistance

CLOCK AMPLIFIER (Ref. Figure 2, Disconnect Pin 15 from Pin 16)							
	Input Offset Voltage	15 & 16	0.5		6	mV	R_S = 10 kΩ (See Note 1)
	Input Bias Current	15 & 16			10	µA	T = 25°C
	Max. Output Voltage	13	0.7			V	
	Min. Output Voltage	13	0.7			V	
	Max./Min. Output Voltage Difference	–	0.7		50	mV	

Notes:
1. R_S = Source resistance, Pin 15 positive with respect to Pin 16
2. Pin 15 = Pin 16 = 3.6 V
3. Pin 15 = 2.6 V, Pin 16 = 3.6 V
4. Pin 15 = 4.6 V, Pin 16 = 3.6 V
5. Calculation only

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
ALBO (Ref. Figure 2)							
	On Current	1	3			mA	V_8-V_7 = ± 1.75 V
	Drive Current	17	0.4		1.4	mA	V_8-V_7 = ± 1.75 V
	Resistance Pin 17 to Ground		35	50	70	kΩ	Not Powered

DYNAMIC CHARACTERISTICS

AMPLIFIER (Ref. Figure 3)							
Ao	AC Gain @ 1 MHz	5 to 8	47	50	53	dB	
Z_{in}	Input Impedance	5	20			kΩ	(See Note 1)
Z_{out}	Output Impedance	7,8			200	Ω	(See Note 2)

Notes: 1. At 1 MHz, AC ground Pins 7 and 8, disconnect 51 Ω resistor, allow for in-circuit R,C
2. At 1 MHz, use Figure 2

CLOCK AMPLIFIER (Ref. Figure 3)							
Ao	AC Gain	15, 16 to 13	32			dB	(See Note 1)
BW	-3 dB Bandwidth	15, 16 to 13	10		MHz		(See Note 2)
t_d	Delay	15 to 13	8		12	ns	(See Note 3)
Z_{out}	Output Impedance	13			200	Ω	(See Note 4)

Notes: 1. Remove dc offset, at 2.048 MHz, Pin 13 = 1 V pk-pk sine wave
2. Remove dc offset, Pin 13 = 1 V pk-pk sine wave
3. Remove dc offset, Pin 15 = 2 V pk-pk sine wave; delay from Pin 15 negative-going zero crossover to Pin 13 positive edge
4. Remove dc offset, at 2.048 MHz

ALBO (Ref. Figure 2)							
	Off Impedance	2,3,4	20			kΩ	(See Note 1)
	Intermediate Impedance Difference	2,3,4			5	%	(See Note 2)
	On Impedance	2,3,4			25	Ω	(See Note 3)
	Transconductance	7/8 to 1			0.03	dB	(See Note 4)

Notes: 1. At 1 MHz, allow for in-circuit R,C
2. At 1 MHz, V_8-V_7 adjusted for current at Pin 1 = 100 μA
3. At 1 MHz, V_8-V_7 adjusted for ± 1.75 V
4. At 1 MHz, change in V_8-V_7 for current at Pin 1 = 10 μA to 100 μA

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
THRESHOLD VOLTAGES (Ref. Figure 3)							
	ALBO Threshold +ve	8-7	1.4	1.5	1.6	V	(See Notes 1 & 2)
	ALBO Threshold -ve	7-8	1.4	1.5	1.6	V	(See Notes 1 & 2)
	ALBO Threshold Difference	–	-5	0	5	%	(See Note 3)
	Clock Drive on Current (peak) +ve	18		1.0	1.4	mA	(See Note 4)
	Clock Drive on Current (peak) -ve	18		1.0	1.3	mA	(See Note 5)
	Clock Drive on Current Difference	–	-5	0	5	%	(See Note 3)
	Clock Threshold +ve	87	68		80	%	(See Notes 1, 6, 8)
	Clock Threshold -ve	7-8	68		80	%	(See Notes 1, 7, 8)
	Clock Threshold Difference	–	-5	0	5	%	(See Note 3)
	Data Threshold +ve	8-7	44	46	48	%	(See Notes 1,8,9,11)
	Data Threshold -ve	7-8	44	46	48	%	(See Notes 1,8,10,11)
	Data Threshold Difference	–	-3	0	3	%	(See Note 3)

Notes: 1. Pk/pk voltage at Pins 7 and 8 of a 1 MHz sine wave derived through amplifier and measured differentially
2. Pk/pk voltage at Pins 7 and 8 adjusted for current at Pin 1 = 3 mA
3. Calculation only
percentage difference calculated from $\left(\frac{\text{higher value}}{\text{lower value}} - 1\right) \times 100$ %
4. V_8-V_7 adjusted to ALBO threshold +ve voltage, ref. Pin 16 = 3.6 V
5. V_7-V_8 adjusted to ALBO threshold -ve voltage, ref. Pin 16 = 3.6 V
6. V_8-V_7 adjusted to peak current at Pin 18 = ½ (clock drive on current peak +ve)
7. V_7-V_8 adjusted to peak current at Pin 18 = ½ (clock drive on current peak -ve)
8. Figure taken as a percentage of lower ALBO threshold
9. V_8-V_7 increased until 1 MHz PRF on counter at Pin 10
10. V_7-V_8 increased until 1 MHz PRF on counter at Pin 11
11. With 2,048 MHz 2 V pk-pk sine wave to Pin 15 with 180 µH in parallel with 36 Ω to Pin 16 = 3.6 V

OUTPUT STAGES (Ref. Figure 3. Use 180 µH inductor between Pins 15 and 16. Apply 2.048 MHz 2V pk/pk to Pin 15.)							
t_r	Output Pulse Rise Time +ve	10			40	ns	10% - 90%
t_r	Output Pulse Rise Time -ve	11			40	ns	10% - 90%
t_f	Output Pulse Fall Time +ve	10			40	ns	10% - 90%
t_f	Output Pulse Fall Time -ve	11			40	ns	10% - 90%
t_w	Output Pulse Width +ve	10	224	244	264	ns	at 50%
	Output Pulse Width -ve	11	224	244	264	ns	at 50%
Δt_w	Output Pulse Width Difference	–	-10		10	ns	
V_{OL}	Buffer Gate Voltage (low) +ve	10	0.65		0.95	V	
V_{OL}	Buffer Gate Voltage (low) -ve	11	0.65		0.95	V	
ΔV_{OL}	Buffer Gate Voltage Difference	–	-0.15		0.15	V	

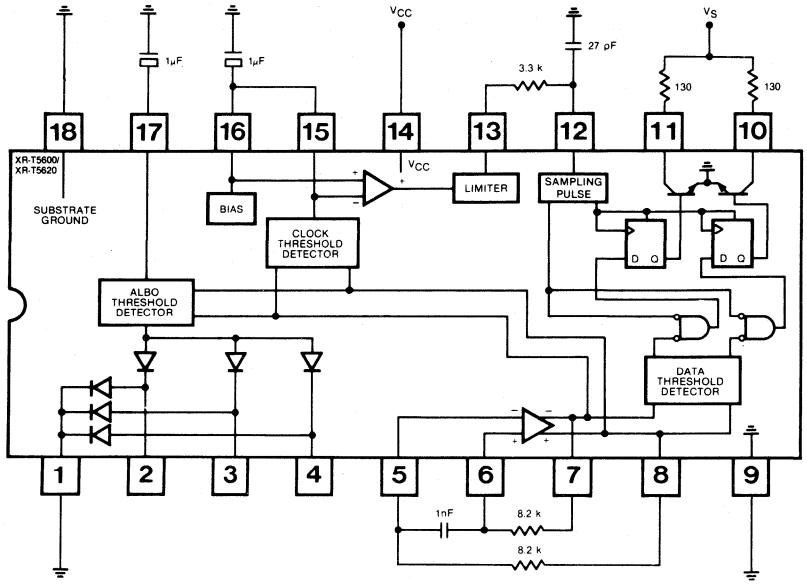


Figure 2. D.C. Parameter Test Circuit

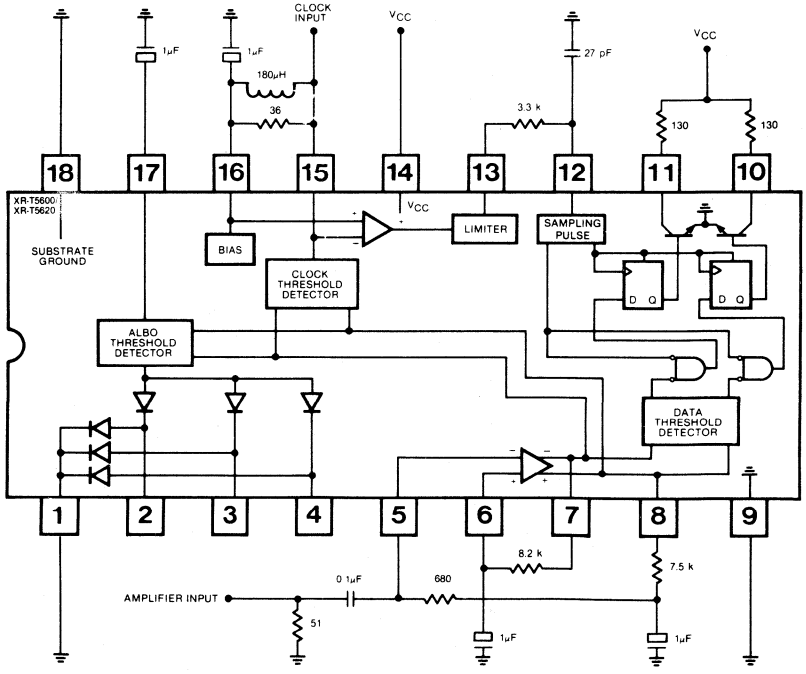


Figure 3. A.C. Parameter Test Circuit

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
SAMPLE PULSE WIDTH (Ref. Figure 4, Cy = 27 pF)							
	Sample Pulse Width			10		ns	(See Notes 1...5)

Notes:
1. The sample pulse width is the period during which the output latches are opened to accept a signal above the data hold at Pin 7 or 8 and cause a half-width output pulse at Pin 11 or 10 respectively.
2. Sample pulse width is specified with a 2.048 MHz TTL waveform at clock input (Pin 15) and a 2,400 MHz Schottky TTL waveform at amplifier input in the circuit of Figure 4. Figure 7 shows the relevant IC waveforms.
3. Monitor the frequency of coincident output pulses at Pins 10 and 11 either directly or through ouput circuit to frequency counter.
4. Sample pulse width = X ns + (0,1 x measured frequency in kHz) ns where X is the mean rise/fall times of the waveform at Pin 8 between 25% and 75%.
5. X to be within the range of 10 nx < X < 12 ns. THis requires HF layout techniques with the amplifier operated closed loop.

SAMPLE PULSE GENERATOR INPUT WAVEFORM (pin 12 - Ref. Figure 4, Cy = 40 pF)							
	Output Pulse Frequency	10,11	1,024 -100 ppm	1,024	1,024 +100 ppm	MHz	(See Note 1)

Note: 1. With 2,048 MHz ±100 ppm TTLwaveform at clock input. With half of above waveform frequency at amplifier input.

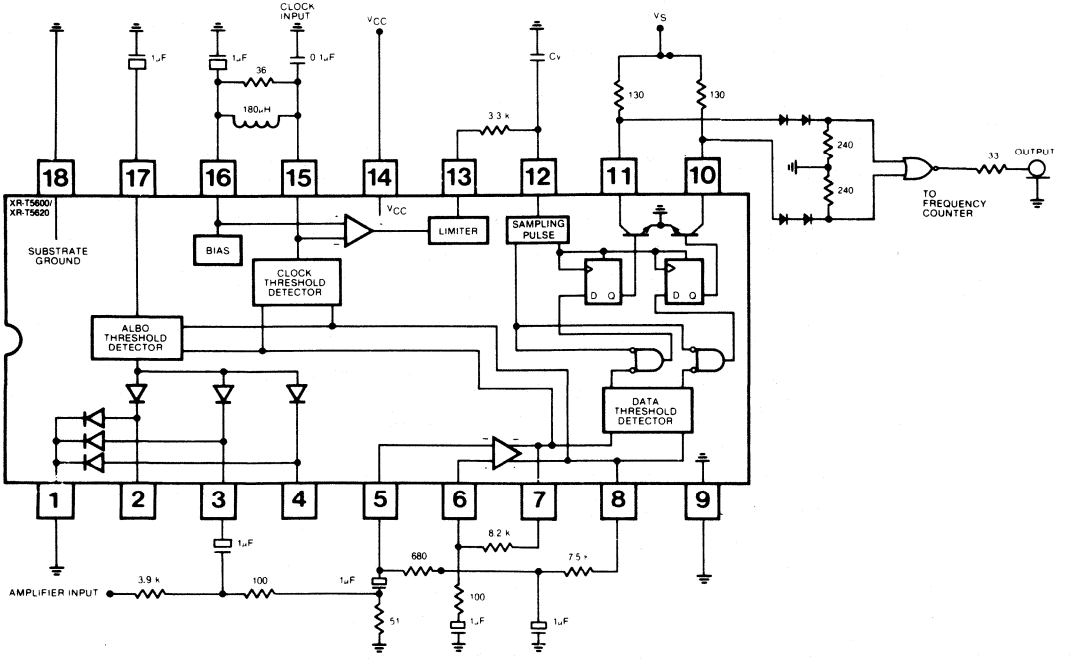


Figure 4. Sampling Pulse Test Circuit

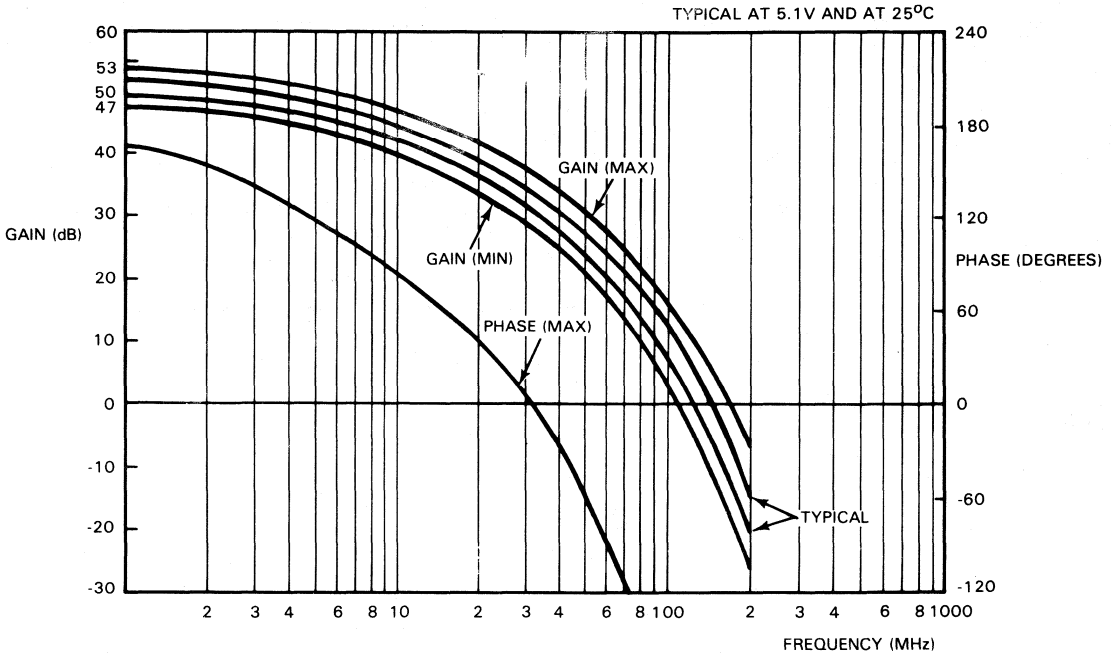


Figure 5. Typical and Limiting Values of Gain and Phase

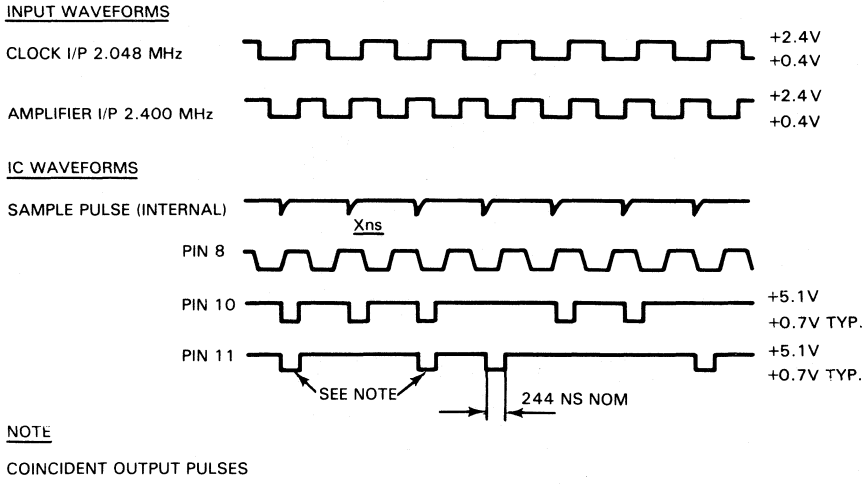
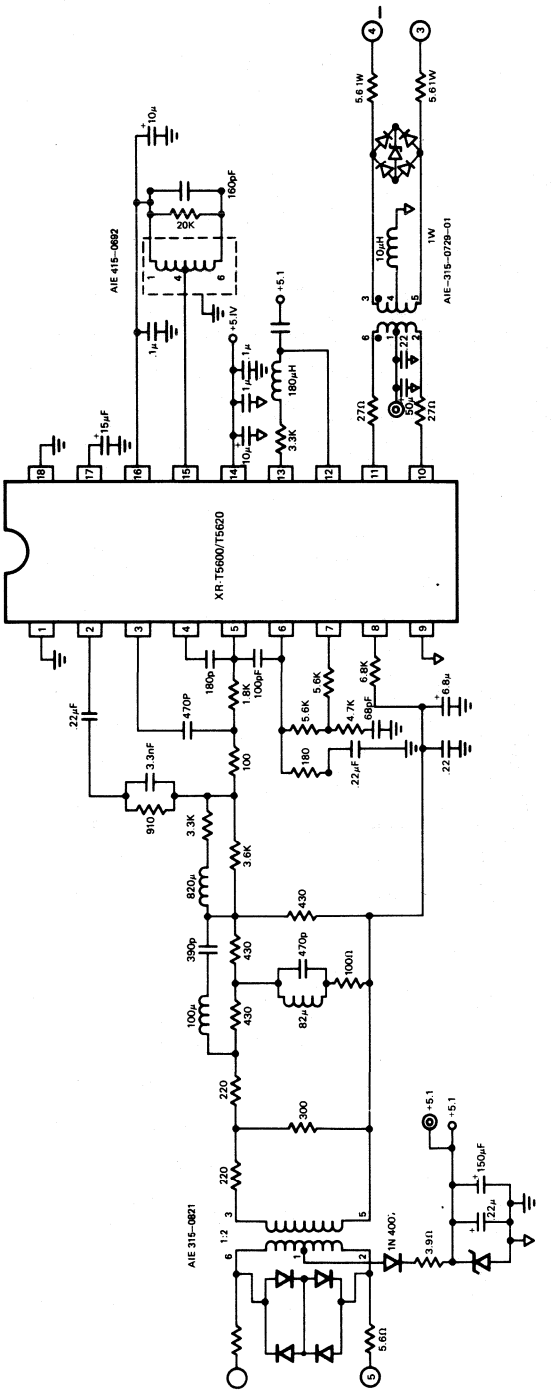
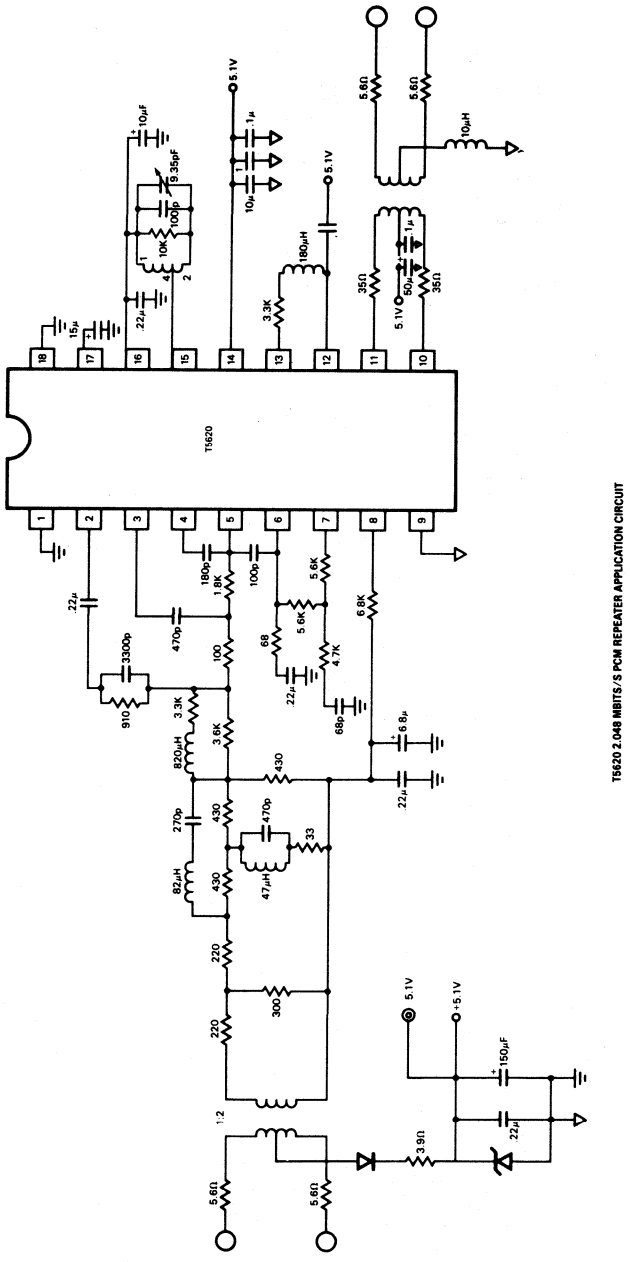


Figure 6. IC Waveforms for Measuring Sampling Pulse Width



T5600/T5620 1.544 M BITS/SEC REPEATER APPLICATION CIRCUIT



T5620 2.048 MBITS/S PCM REPEATER APPLICATION CIRCUIT

PCM Line Repeater

GENERAL DESCRIPTION

The XR-T5720 is a bipolar monolithic repeater IC that provides all the active circuits required for one side of a PCM repeater. The IC is designed for clock extraction by using a crystal filter.

The primary applications of the XR-T5720 are T1 (1.544 M bit/s), T148C (2.37 M bit/s), and European 2 M bit/s PCM repeater.

A tank circuit clock extraction version of XR-T5720 is available as XR-T5600/T5620.

FEATURES

Crystal Clock Extraction
Single 5.1 V Power Supply
Less than 10 ns Sampling Pulse over the Operating Range
Triple Matched ALBO Ports

APPLICATIONS

T1 PCM Repeater
T148C PCM Repeater
T1C PCM Repeater (requires external preamplifier)
European 2 M Bit/s PCM Repeater

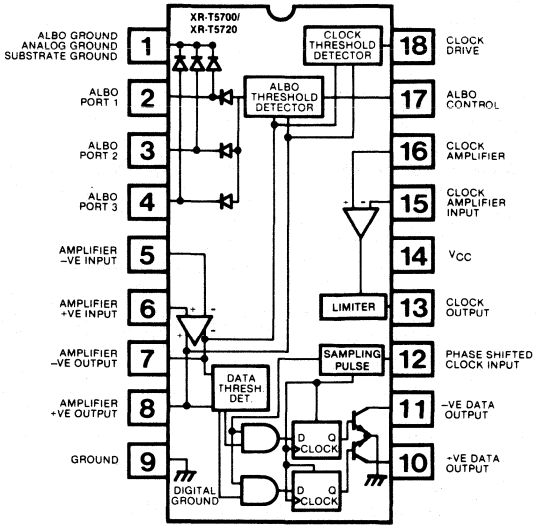
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Supply Voltage	-0.5 to +10 V
Supply Voltage Surge (10 ms)	+25 V
Input Voltage(except Pins 2,3,4,17)	-0.5 to 7 V
Input Voltage (Pins 2,3,4,17)	-0.5 to +0.5 V
Data Output Voltage (Pins 10, 11)	20 V
Voltage Surge (Pins 5,6,10,11) (10 msec only)	50 V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5720	Ceramic	-40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-T5720 performs most of the functions required for one side of a PCM repeater operating at 2 M bit/s or similar baud rate. The integrated circuit amplifies the received positive and negative pulses and feeds them into Automatic Line Build-out (ALBO), clock and data threshold detectors, see Figure 1. The ALBO threshold detector ensures that the received pulses at Pins 7 and 8 have the correct amplitude and shape. This is carried out by controlling the gain and frequency shaping of the ALBO network with three variable impedance ALBO ports.

The clock threshold detector extracts timing information from the pulses received at Pins 7 and 8 and passes it into open collector Pin 18. A crystal filter is connected from Pin 18 to clock amplifier input Pins 16 and 15. the sinusoidal-type waveform is amplified into a square wave at Pin 13, and forwarded through an external phase shift network into Pin 12. This waveform provides the data sampling pulse which opens latches into which the data from the data threshold detectors is passed. The resulting pulses are stored for half a bit period (normally 488 ns for 2 M bit/s) in the latches. They appear as half-width output pulses at Pins 10 and 11.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25^{\circ}C$, $V_{CC} = 5.1\ V \pm 5\%$, unless specified otherwise (see Figure 1).

PARAMETERS	PINS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Current	14		22	30	mA	
Data Output Leakage Current	10,11		0	100	μA	$V_{pull\text{-}up} = 15\ V$, $V_{cc} = 5.35\ V$
ALBO Port Off Voltage	2,3,4		0	0.1	V	
Amplifier Pin Voltage	5,6,7,8	2.4	2.9	3.4	V	
DYNAMIC CHARACTERISTICS AMPLIFIER						
Output Offset Voltage		-50	0	50	mV	$R_S = 8.2\ k\Omega$
AC Gin @ 1 MHz		47	50	53	dB	
Input Impedance		20			kΩ	
Output Impedance				200	Ω	
ALBO						
ALBO Off Impedance		20		25	kΩ	
ALBO On Imepdance				25	Ω	
THRESHOLDS						
ALBO Threshold		1.4	1.5	1.6	V	
Clock Threshold as % of ALBO Threshold		68		80	%	
DATA Threshold as % of ALBO Threshold		42		49	%	
Clock Drive Current		0.7		1.4	mA	At $V_O = V_{ALBO}$ Threshold
OUTPUT STAGES						$R_L = 130\Omega$, $V_{pull\text{-}up} = 5.1 \pm 5\%$
Output Pulse Rise Time				40	ns	
Output Pulse Fall Time				40	ns	
Output Pulse Width		224	244	264	ns	
Output Pulse Width Differential		-10		+10	ns	
Buffer Gate Voltage (Low)		0.65		0.95	V	
Buffer Gate Voltage Differential		-0.15		0.15	V	

ELECTRICAL CHARACTERISTICS

Test Conditions: Unless otherwise stated, all characteristics shall apply over the operating temperature range of -40°C to +85°C with V_{CC} = 5.1 V ± 5%, all voltages referred to ground = 0 V.

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL CHARACTERISTICS (Ref. Figure 2)							
I_S	Supply Current	14		22	30	mA	
I_{LD}	Data Output Leakage Current	10,11			100	µA	from V_S (See Note 1)
	Amplifier Pin Voltages	5,6,7,8	2.4	2.9	3.4	V	
	ALBO Ports Off Voltage	2,3,4		0	0.1	V	

Note 1: V_S = 15V, V_{CC} = 5.35 V

AMPLIFIER (Ref. Figure 2, Only Pins 1, 9, 10...18 Connected)							
	Input Offset Voltage	5 & 6	-10		+10	mV	R_S = 8, 2 kΩ (See Note 1)
	Input Bias Current	5 & 6	0		5	µA	R_S = 8, 2 kΩ (See Note 1)
	Input Offset Current	5 & 6	-1		1		R_S = 8, 2 kΩ (See Note 1)
	Output Offset Voltage	7 & 8	-50	0	-50	mV	R_S = 8, 2 kΩ (See Note 1)
	Common Mode Rejection Ratio	7 & 8	30			dB	Vcm ± 0, 3 V
	Power Supply Rejection Ratio	7 & 8	30			dB	Vcc ± 10
	Output Voltage Swing	7 & 8	2.2			V	

Note 1: R_S = Source Resistance

CLOCK AMPLIFIER (Ref. Figure 2 Disconnect Pin 15 from Pin 16)							
	Input Offset Voltage	15 & 16	0.5		6	mV	R_S = kΩ (See Note 1)
	Input Bias Current	15 & 16			10	µA	T = 25°C
	Max. Output Voltage	13	0.7			V	
	Min. Output Voltage	13	0.7			V	
	Max./Min. Output Voltage Difference	–			50	mV	

Notes:
1. R_S = Source resistance, Pin 15 positive with respect to Pin 16.
2. Pin 15 = Pin 16 = 3.6 V
3. Pin 15 = 2.6 V, Pin 16 = 3.6 V
4. Pin 15 = 4.6 V, Pin 16 = 3.6 V
5. Calculation only

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
ALBO (Ref. Figure 2)							
	On Current	1	3			mA	V_8-V_7 = ±1.75 V
	Drive Current	17	0.4		1.4	mA	V_8-V_7 = ±1.75 V
	Resistance Pin 17 to GN		35	50	70	kΩ	Not Powered

DYNAMIC CHARACTERISTICS

AMPLIFIER (Ref. Figure 3)							
Ao	AC Gain @ 1 mHz	5 to 8	47	50	53		
Z_{in}	Input Impedance	5	20			kΩ	(See Note 1)
Z_{out}	Output Impedance	7, 8			200	Ω	(See Note 2)

Notes: 1. At 2 MHz, AC ground Pins 7 and 8, disconnect 51 Ω resistor. Allow for in-circuit R, C.
2. At 1 MHz, use Figure 2.

CLOCK AMPLIFIER (Ref. Figure 3)							
Ao	AC Gain	15,16 to 13	32			dB	(See Note 1)
BW	-3 dB Bandwidth	15, 16 to 13	10			MHz	(See Note 2)
	Delay	15, 16 to 13	8		12	ns	(See Note 3)
	Output Impedance	13			200	Ω	(See Note 4)

Notes: 1. Remove dc offset, at 2.048 MHz, Pin 13 = 1 V pk-pk sine wave
2. Remove dc offset, Pin 13 = 1 V pk-pk sine wave
3. Remove dc offset, Pin 15 = 2 V pk-pk sine wave. Delay from Pin 15 negative-going zero crossover to Pin 13 positive edge.
4. Remove dc offset, at 2.048 MHz

ALBO (Ref. Figure 2)							
	Off Impedance	2,3,4	20			kΩ	(See Note 1)
	Intermediate Impedance Difference	2,3,4,			5		(See Note 2)
	On Impedance	2,3,4			25	M	(See Note 3)
	Transconductance	7,8 to 1			0.03	dB	(See Note 4)

Notes: 1. At 1 MHz, allow for in-curcuit R,C
2. At 1 MHz, V_8-V_7 adjusted for current at Pin 1 = 100 μA
3. At 1 MHz, V_8-V_7 adjusted for ± 1.75 V
4. At 1 MHz, change in V_8-V_7 for current at Pin 1 = 10 μA to 100 μA

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
THRESHOLD VOLTAGES (Ref. Figure 3)							
	ALBO Threshold +ve	8-7	1.4	1.5	1.6	V	(See Notes 1 & 2)
	ALBO Threshold -ve	7-8	1.4	1.5	1.6	V	(See Notes 1 & 2)
	ALBO Threshold Difference	–	-5	0	5		(See Note 3)
	Clock Drive on Current (Peak) +ve	18	0.65	1.0	1.4	mA	(See Note 4)
	Clock Drive on Current (Peak) -ve	18	0.65	1.0	1.3	mA	(See Note 5)
	Clock Drive on Current Difference	–	-5	0	5		(See Note 3)
	Clock Threshold +ve	8-7	68		80		(See Notes 1, 6, 8)
	Clock Threshold -ve	7-8	68		80	%	(See Notes 1, 7, 8)
	Clock Threshold Difference	–	-5	0	5	%	(See Note 3)
	Data Threshold +ve	8-7	44	46	48	%	(See Notes 1, 8, 9, 11)
	Data Threshold -ve	7-8	44	46	48	%	(See Notes 1, 8, 10, 11)
	Data Threshold Difference	–	-3	0	3	%	(See Note 3)

Notes:
1. Pk/pk voltage at Pins 7 and 8 of a 1 MHz sine wave derived through amplifier and measured differentially
2. Pk/pk voltage at Pins 7 and 8 adjusted for current at Pin 1 = 3 mA
3. Calculation only

$$\text{percentage difference calculated from} \left(\frac{\text{higher value}}{\text{lower value}} - 1 \right) \times 100 \quad \%$$

4. V_8-V_7 adjusted to ALBO threshold +ve voltage (ref. Pin 16 = 3.6 V)
5. V_7-V_8 adjusted to ALBO threshold -ve voltage (ref. Pin 16 = 3.6 V)
6. V_8-V_7 adjusted to peak current at Pin 18 = ½ (clock drive on current peak +ve)
7. V_7-V_8 adjusted to peak current at Pin 18 = ½ (clock drive on current peak -ve)
8. Figure taken as a percentage of lower ALBO threshold
9. V_8-V_7 increased until 1 MHz PRF on counter at Pin 10
10. V_7-V_8 increased until 1 MHz PRF on counter at Pin 11
11. With 2,048 MHz 2 V pk-pk sine wave to Pin 15 with 180 μH in parallel with 36 Ω to Pin 16 = 3.6 V

OUTPUT STAGES (Ref. Figure 3. Use 180 μH inductor between Pins 15 and 16. Apply 2.048 MHz 2V pk/pk to Pin 15.)							
t_r	Output Pulse Rise Time +ve	10			40	ns	10% - 90%
t_r	Output Pulse Rise Time -ve	11			40	ns	10% - 90%
t_f	Output Pulse Fall Time +ve	10			40	ns	10% - 90%
t_f	Output Pulse Fall Time -ve	11			40	ns	10% - 90%
t_w	Output Pulse Width +ve	10	244	244	264	ns	at 50%
t_w	Output Pulse Width -ve	11	244	244	264	ns	at 50%
Yt_w	Output Pulse Width Difference	–	-10		10	ns	
V_{OL}	Buffer Gate Voltage (low) +ve	10	0.65		0.95	V	
V_{OL}	Buffer Gate Voltage (low) -ve	11	0.65		0.95	V	
bV_{OL}	Buffer Gate Voltage Difference	–	-0.15		0.15	V	

Note: 1. Calculation only

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
SAMPLE PULSE WIDTH (Ref. Figure 4. Cy = 27 pF)							
	Sample Pulse Width	–		10	20	ns	(See Notes 1...5)

Notes:
1. The sample pulse width is the period during which the output latches are opened to accept a signal above the data threshold at Pin 7 or 8 and cause a hlaf-width output pulse at Pin 11 or 10 respectively.
2. Sample pulse width is specified with a 2,048 MHz TTL waveform at clock input (Pin 15) and a 2,400 MHz Schottky TL waveform at amplifier input in the circuit of Figure 5. Figure 7 shows the relevant IC waveforms.
3. Monitor the frequency of coincident output pulses at Pins 10 and 11 either directly or through output circuit to frequency counter.
4. Sample pulse width = Xns + (0,1 x measured frequency in kHz ns where x is the mean rise/fall times of the waveform at Pin 8 between 25% and 75%.
5. X to be within the range 10 ns < X < 12 ns. This requires HF layout techniques with the amplifier operated closed loop.

SAMPLE PULSE GENERATOR INPUT WAVEFORM (Pin 12 Ref. Figure 4, Cy = 40 pF)							
	Output Pulse Frequency	10,11	1,024 -100 ppm	1,024	1,024 +100 ppm	MHz	(See Note 1)

Note: 1. Width 2.048 MHz ± 100 ppm TTL waveform at clock input with half of above waveform frequency at amplifier input.

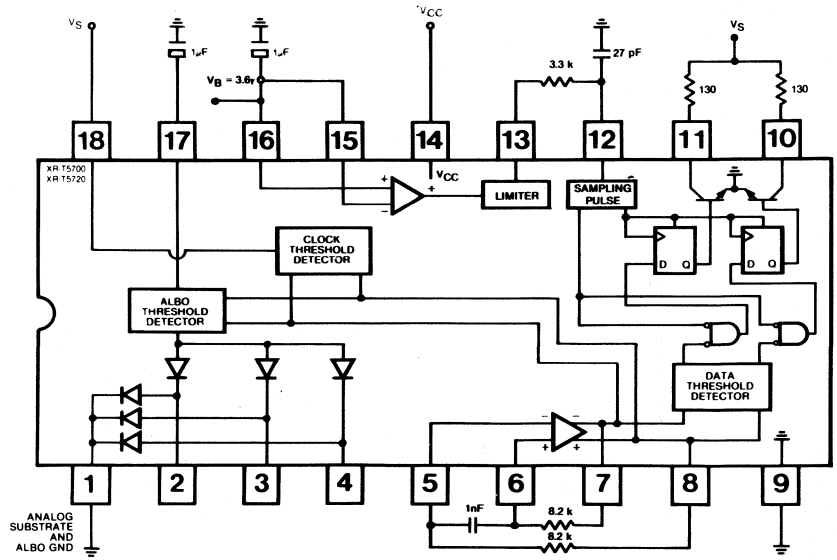


Figure 2. DC Parameter Test Circuit

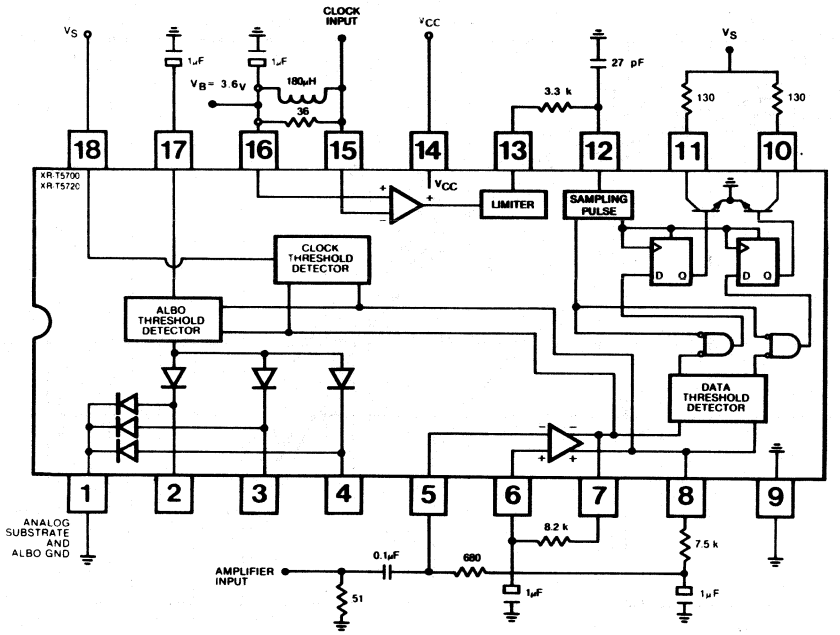


Figure 3. AC Parameter Test Circuit

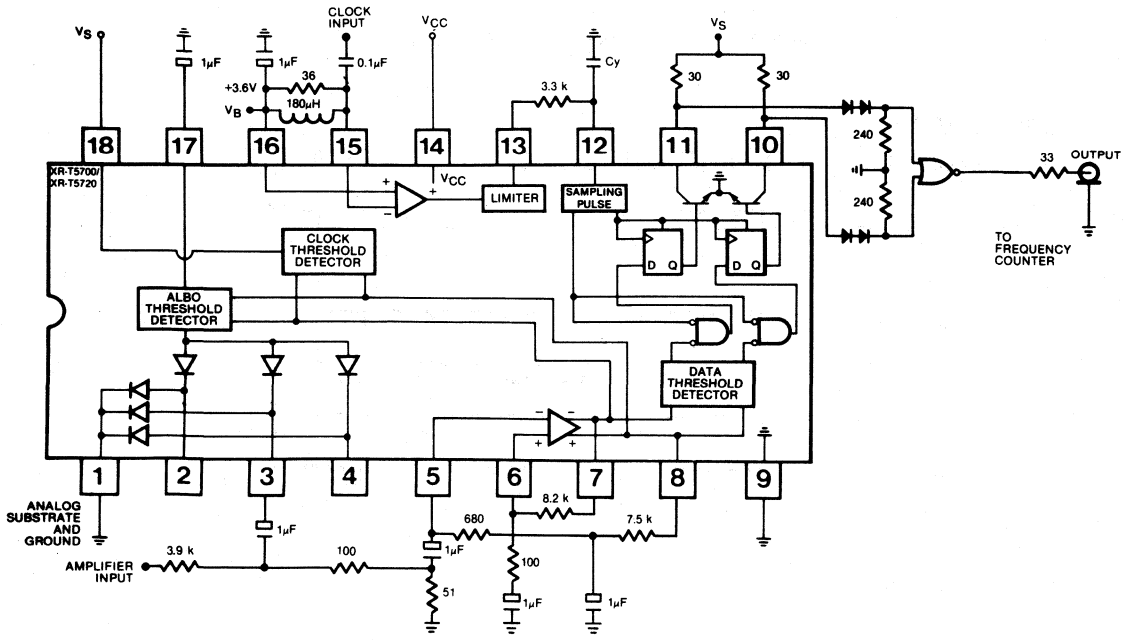


Figure 4. Sampling Pulse Test Circuit

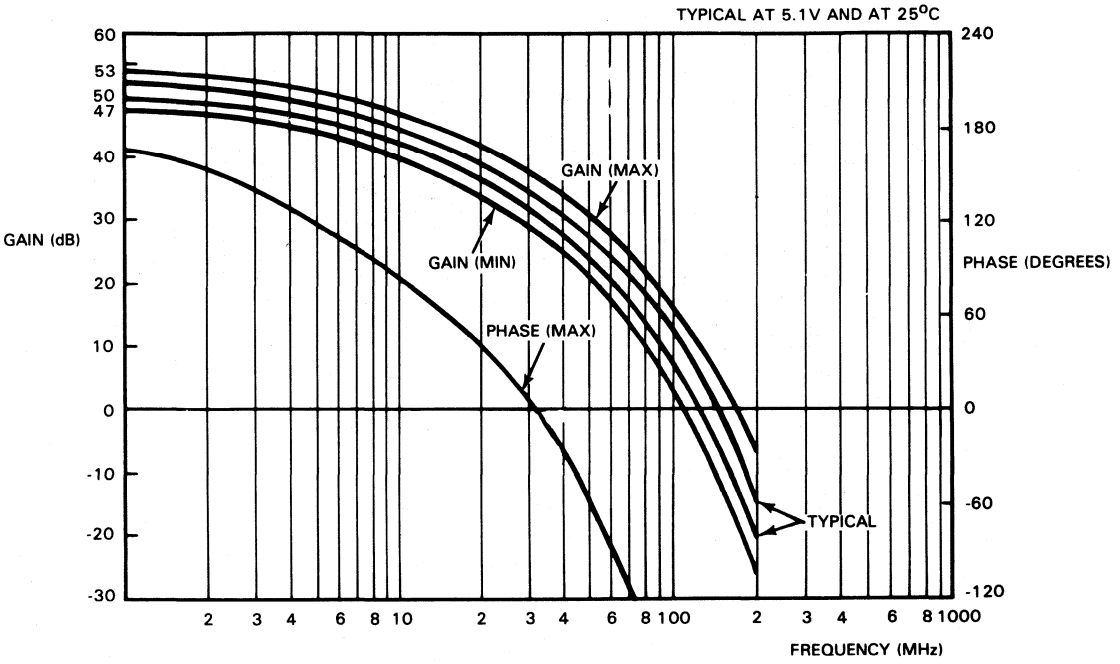


Figure 5. Typical and Limiting Values of Gain and Phase

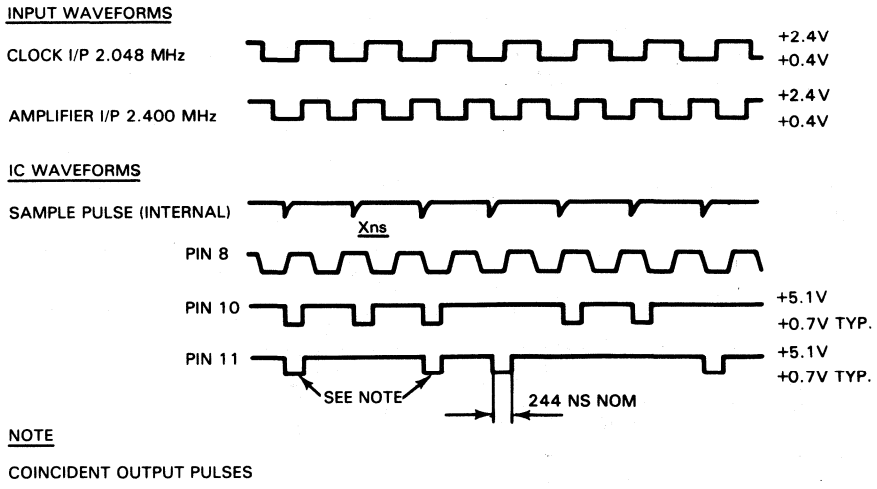
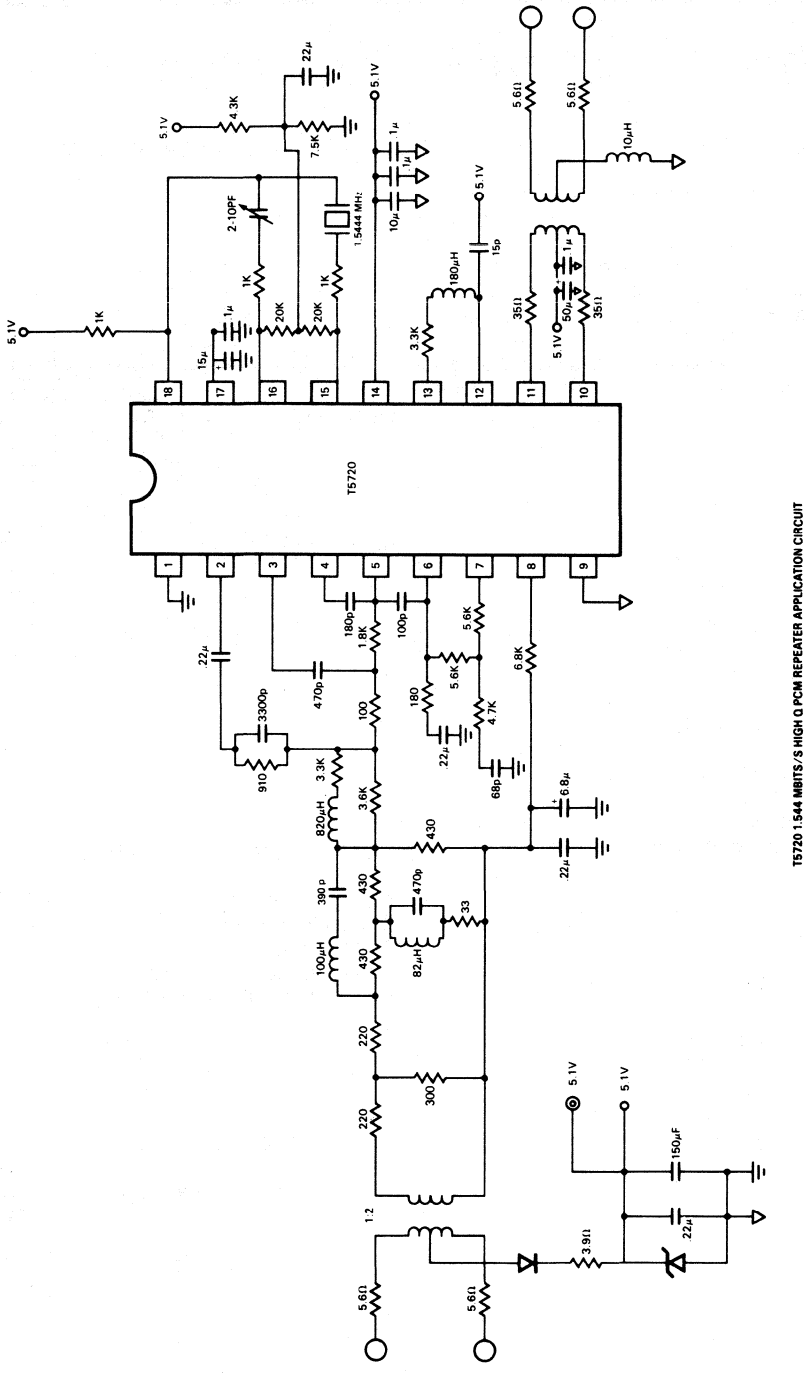


Figure 6. IC Waveforms for Measuring Sampling Pulse Width



T5720 1.544 MBITS/S HIGH Ω PCM REPEATER APPLICATION CIRCUIT

Low Power Repeater/Receiver

GENERAL DESCRIPTION

The XR-T56L22 is a very low power monolithic repeater/receiver IC designed for PCM carrier systems operating between 1.544 Mbps and 2.37 Mbps. The IC provides all the active circuitry required to implement one side of a PCM repeater. The XR-T56L22 features on chip adjustable phase shifting, an extracted clock output and an on-board shunt regulator. The very low power consumption of the device makes it ideal for long haul "tandem" repeater applications.

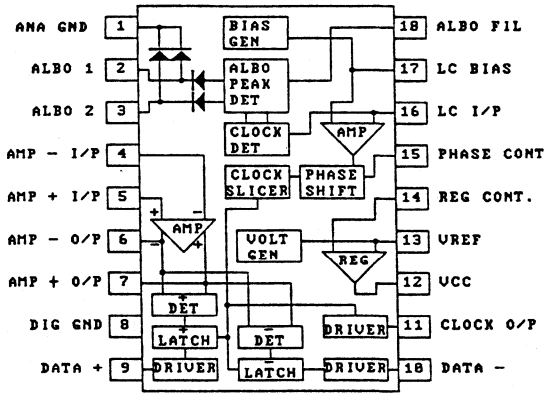
FEATURES

Contains All The Active Components For A Long Haul PCM Repeater Or Receiver
Low Voltage Operation (5.1V)
Low Power Consumption (8.75 mA Max)
2 Mbps Operation Capability
Dual Matched ALBO Ports
Internal Adjustable Phase Shift Circuitry
Extracted Clock Output
Internal Shunt Regulator
Temperature Independent Current Biasing

APPLICATIONS

T1 PCM Repeater/Receiver
T148C PCM Repeater/Receiver
European 2.048 Mbps PCM Repeater/Receiver
Digital Multiplexers, CSU'S, Switching Equipment
ISDN Compatible Equipment: Fax Machines, Computers etc.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65° C to +150° C
Operating Temperature	-40° C to +85° C
Supply Voltage	-0.5 to 7V
Supply Voltage Surge (10 ms)	+25V
Data Output Voltage (Pin 9, 10)	+12V

ORDERING INFORMATION

Part Number	Package	Operation Temperature
XR-T56L22IP	Plastic	-40° C to +85° C
XR-T56L22IN	Ceramic	-40° C to +85° C
XR-T56L22ID	SOIC	-40° C to +85° C

PIN DESCRIPTION

Pin #	Name	Description
1	ANA GND	Ground for analog sections of IC and substrate.
2	ALBO 1	ALBO PORT 1 output. Port impedance varies between 25 ohm and 20 kohm proportional to input signal level.
3	ALBO 2	ALBO PORT 2 output. Similar to pin 2.
4	AMP - I/P	Inverting input of signal preamp Rin > 20kohm.
5	AMP + I/P	Non-inverting input of signal preamp. Rin > 20kohm.
6	AMP - O/P	Inverting output of signal preamp. Rout < 200ohm. DC level typically 3.2V.
7	AMP + O/P	Non-inverting output of signal preamp. Similar to pin 6.
8	DIG GND	Ground for digital portion of IC.
9	DATA +	Positive data driver output (open collector). Vol <0.95V @ Iout = 32mA.
10	DATA -	Negative data driver output (open collector). Vol <0.95V @ Iout = 32mA.
11	CLOCK O/P	Phase shifted clock output (open collector). Decouple to GND with 0.1 µF if not required. With Rpull -up = 1K Vol < 1.1V @ Iout = 4mA.
12	VCC	Input pin of shunt regulator and supply pin for IC. For voltage feed applications the regulator must be disabled and a 5V ±5% supply connected. For line feed a current of 48-120mA is required. Icc <8.75mA @ Ron ALBO = 25ohm typical.
13	VREF	Output voltage of internal reference of shunt regulator. For parallel operation of regulators should be tied to pin 13 of 2nd T56L22 device. Vref approximately VCC/2. Decouple to gnd with 0.1µF.
14	REG CONT	Input voltage of shunt regulator amp. To inhibit regulator, pin should be tied to ground. For line feed operation decouple to gnd with 0.1µF. For parallel operation of regulators tie pin 14 of 2nd T56L22 device. Vreg approximately Vref.
15	PHASE CONT	Phase shift adjust input. A resistor to gnd from the pin allows adjustment of phase shift from 90° to approximately 0°. Rp typical 1.8K to 1K. Vphase typical 340mV.
16	LC I/P	Clock amplifier input. Pulsed with current from clock comparator. Connect LC tank between 16, 17 for clock recovery. Ickon = -110µA typical.
17	LC BIAS	Clock amplifier reference voltage. VLC = 3.6V typical.
18	ALBO FIL	Control pin for ALBO ports. Voltage developed across a capacitor on this pin defines ALBO on impedance VALBO = 1.5V typical.

SYSTEM DESCRIPTION

With reference to the functional block diagram, the basic operation of the XR-T56L22 may be described as follows:
The received bipolar signal, is applied to a linear amplifier and automatic equalizer. These circuits provide the necessary amount of gain and phase equalization to recover the transmitted data, and band limit the signal, to optimize repeater performance for near-end crosstalk produced by other systems operating within the same cable bundle.

The preamplifier output signals which are balanced and of opposite phase, are applied to the clock extraction and pulse regenerator circuits. Here they are rectified and then applied to a high Q resonant circuit which extracts the 1.544/2.048 Mbps frequency component from the received signal. This signal is then sliced and fed to an adjustable phase shift circuit. A second slicer is used to control the time at which the output signals from the preamplifier are sampled by the pulse regenerator circuits. The phase shifted clock signal is made available as an output from the circuit for interface applications. The clock phase adjustment is performed with a single pin using an external resistor. Adjustment of the position of the clock sampling edge by the phase shift circuit allows performance of the pulse regenerator to be optimized. The pulse regenerator performs the sampling and data slicing to regenerate the appropriate output pulse. These pulses are applied to an external output transformer to create the bipolar signal that drives the next section of twisted pair.

ELECTRICAL CHARACTERISTICS

Test Conditions: -40°C to + 85°C, V_{CC} = 5.1V±5%, unless otherwise specified – refer to test circuit (Fig 6).

PARAMETERS	PIN	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL						
Supply Voltage	12	4.85		5.35	V	Pin 12, 13 to V_{CC}, Note 1
Supply Current	12		7	8.75	mA	
Data Output Leakage Current	9,10			100	µA	Vpull-up = 8V V_{CC} = 5.35V, Note 1
ALBO Port Off Voltage	2,3			0.1	V	
Amplifier Pin Voltage	4,5 6,7	2.7	3.2	3.7	V	
Note: 1. Internal Regulator disabled.						
AMPLIFIER						
Input Impedance	4,5	40			KΩ	
Input Offset Voltage	4,5	-10		+10	mV	R_S = 8.2K, Note 1
Input Bias Current	4,5			5	µA	"
Input Offset Current	4,5	-1		+1	µA	"
Output Offset Voltage	6,7	-50		+50	mV	"
Common Mode Rejection Ratio	4,5,6,7	40			dB	
Output Voltage Swing	6,7	1.9			V	
Note: 1. Source Resistance						
CLOCK AMPLIFIER						
Input Offset Voltage	17,16	0.5		6	mV	R_S = 10K, Note 1
Input Bias Current	17,16			5	µA	Note 2
AC Gain		40			dB	
-3 dB Bandwidth		10			MHz	
Delay			35		nS	
Note: 1. Rs = Source resistance Pin 16 positive with respect to Pin 17 2. Pin 16 = Pin 17 = 3.6V						
ALBO						
ALBO Filter Resistance	18-1	31		57	KΩ	
ALBO Impedance Match	2,3			10	%	
On Current	1	1.3		2.4	mA	
Drive Current	18	0.4		1.4	mA	
Maximum On Impedance	2, 3-1			25	Ω	Note 1
Minimum Off Impedance	2, 3-1	20			KΩ	"
Note: 1. ftest = 1MHz						

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A =-40°C to +85°C, V_{CC} = 5.1V±5% unless otherwise specified – refer to test circuit (Fig 6).

PARAMETERS	PIN	MIN	TYP	MAX	UNIT	CONDITIONS
THRESHOLD VOLTAGES						
ALBO Threshold +Ve	7,6	1.4		1.6	V	Note 1 & 2
ALBO Threshold -Ve	7,6	1.4		1.6	V	Note 1 & 2
ALBO Threshold Difference		-3		+3	%	Note 3
Clock Drive on Current +Ve		80		140	µA	Note 4
Clock Drive on Current -Ve		80		140	µA	Note 4
Clock Drive Difference		-3		+3	%	Note 3
Clock Threshold +Ve	7,6	69		79	%	Note 5
Clock Threshold -Ve	7,6	69		79	%	Note 5
Clock Threshold Difference		-3		+3	%	Note 3
Data Threshold +Ve	7,6	41		50	%	Note 5
Data Threshold -Ve	7,6	41		50	%	Note 5
Data Threshold Difference		-3		+3	%	Note 3
Notes: 1. Pk/pk voltage at Pins 6 and 7 of a 1MHz sine wave derived through amplifier and measured differentially. 2. Pk/pk voltage at Pins 6 and 7 adjusted for a current increase of 2mA at pin 1. 3. Calculation only: percentage difference = $\left[\frac{\text{higher value}}{\text{lower value}} - 1\right] \times 100\ \%$ 4. $V_6 - V_7$ adjusted to ALBO threshold voltage (Pin 16 = 3.6V) 5. Figure taken as a percentage of ALBO threshold						
DATA OUTPUT STAGES						
Output Pulse Rise Time +Ve (Tr)	9			40	nS	10%-90% Note 1
Output Pulse Rise Time -Ve (Tr)	10			40	nS	"
Output Pulse Fall Time +Ve (Tf)	9			40	nS	"
Output Pulse Fall Time -Ve (Tf)	10			40	nS	"
Output Pulse Width +Ve (Tw)	9	224		264	nS	at 50%
Output Pulse Width -Ve (Tw)	10	224		264	nS	"
Output Pulse Width Difference (dTw)		-12		+12	nS	"
Output Voltage (low) (Vol)	9,10	0.6		0.95	V	Note 1
Output Voltage Diff (Vol)	9,10	-0.15		+0.15	V	"
Note 1. Using a 130Ω pull up resistor between 9, 10 and Vcc and 15pF capacitance to GND.						
CLOCK OUTPUT STAGE						
Output Pulse Rise Time (Tr)	11			40	nS	Note 1
Output Pulse Fall Time (Tf)	11			40	nS	"
Output Pulse Width (Tw)	11	224		264	nS	
Output Voltage Low (Vol)	11			1.1	V	
Note 1. Using a 2K pull up resistor between 11 and Vcc and 15 pF capacitance to GND.						
SHUNT REGULATOR						
Output Voltage	12	4.85	5.1	5.35	V	Pin 13, 14 floating
Voltage Regulation Over Temp.	12		-0.02		%/°C	"
Load Regulation	12			0.027	%/mA	1 mA to 100 mA load

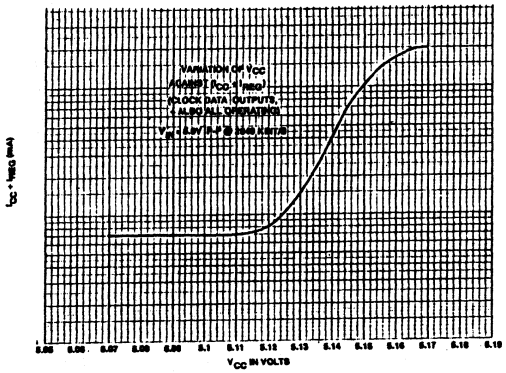


Figure 1. Regulator Output Voltage Versus Current (I_{CC} + I_{REG})

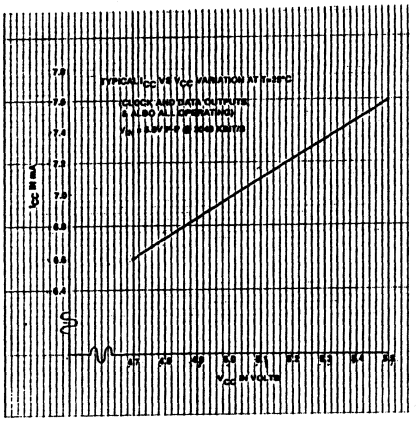


Figure 2. Supply Current Variation with V_{CC}(Regulator Inhibited)

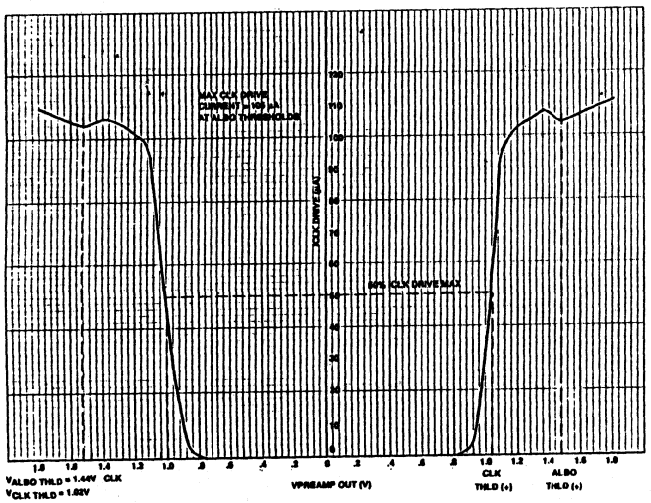


Figure 3. Clock Drive Current Against Preamp Output Voltage

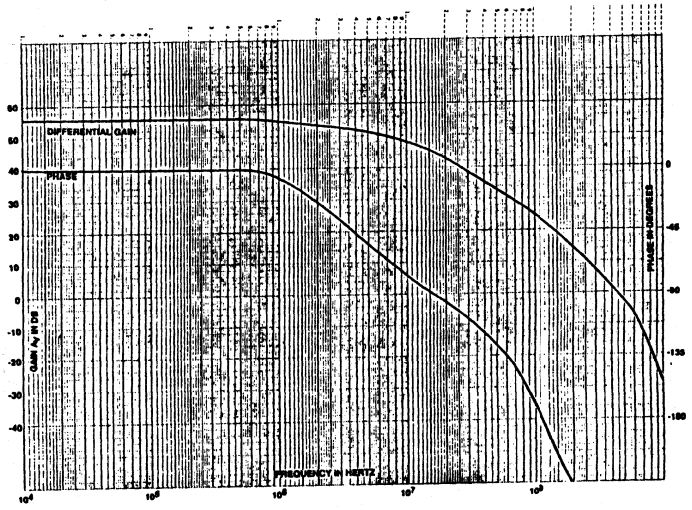


Figure 4. Preamp Gain/Phase Characterisitcs

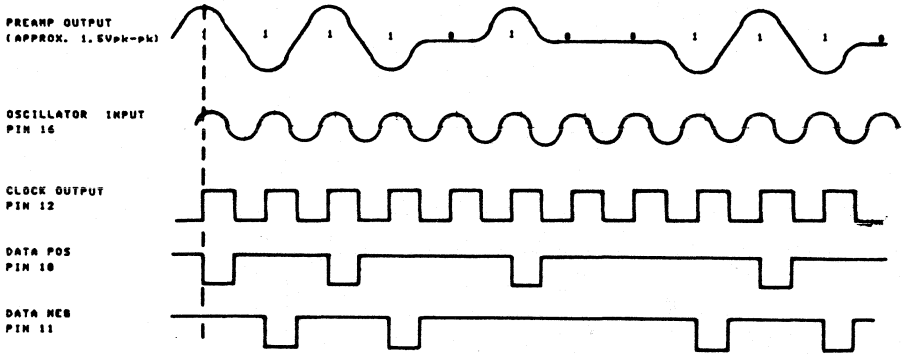


Figure 5. Typical T56L22 Waveforms

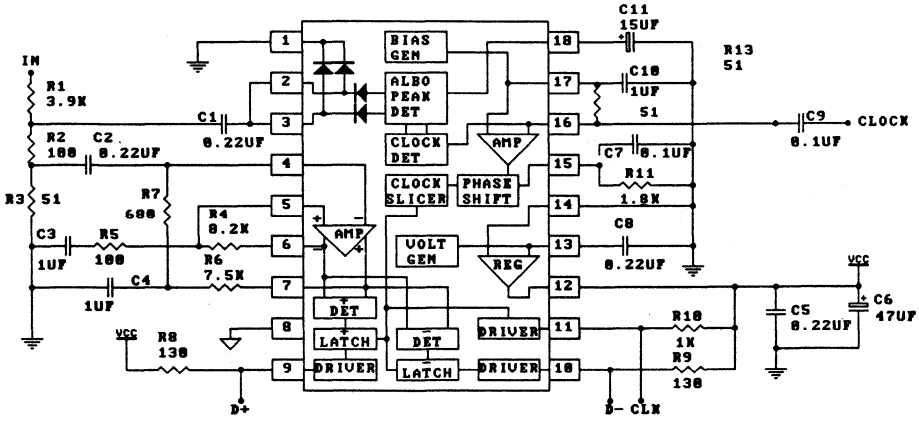
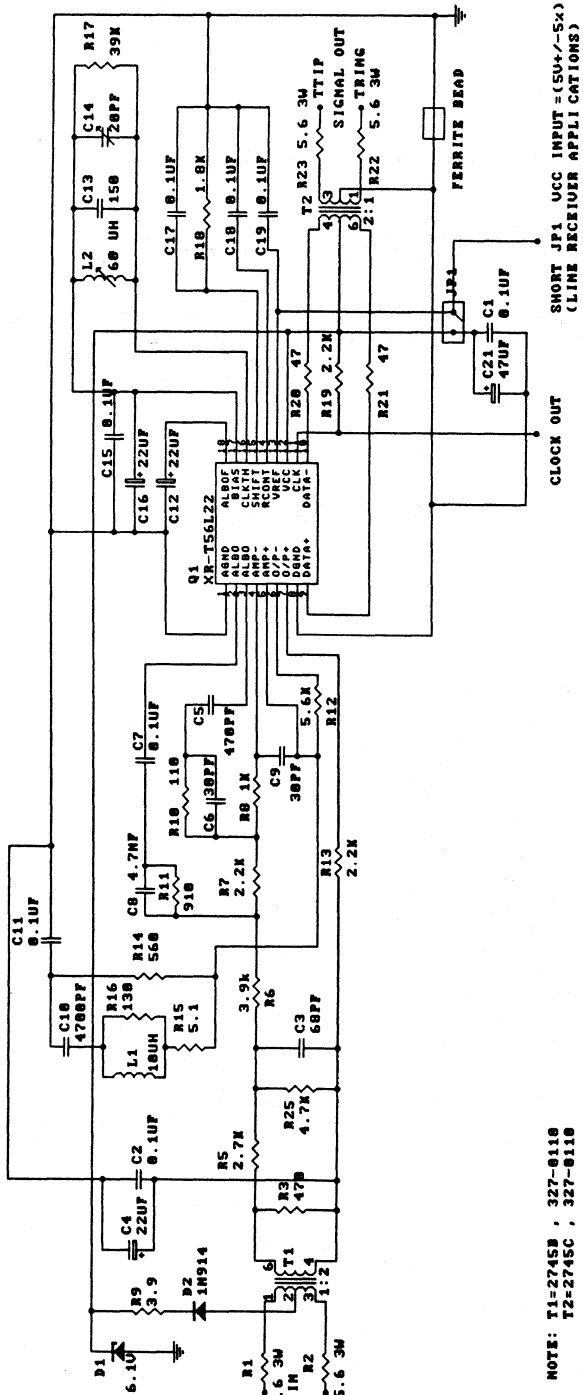
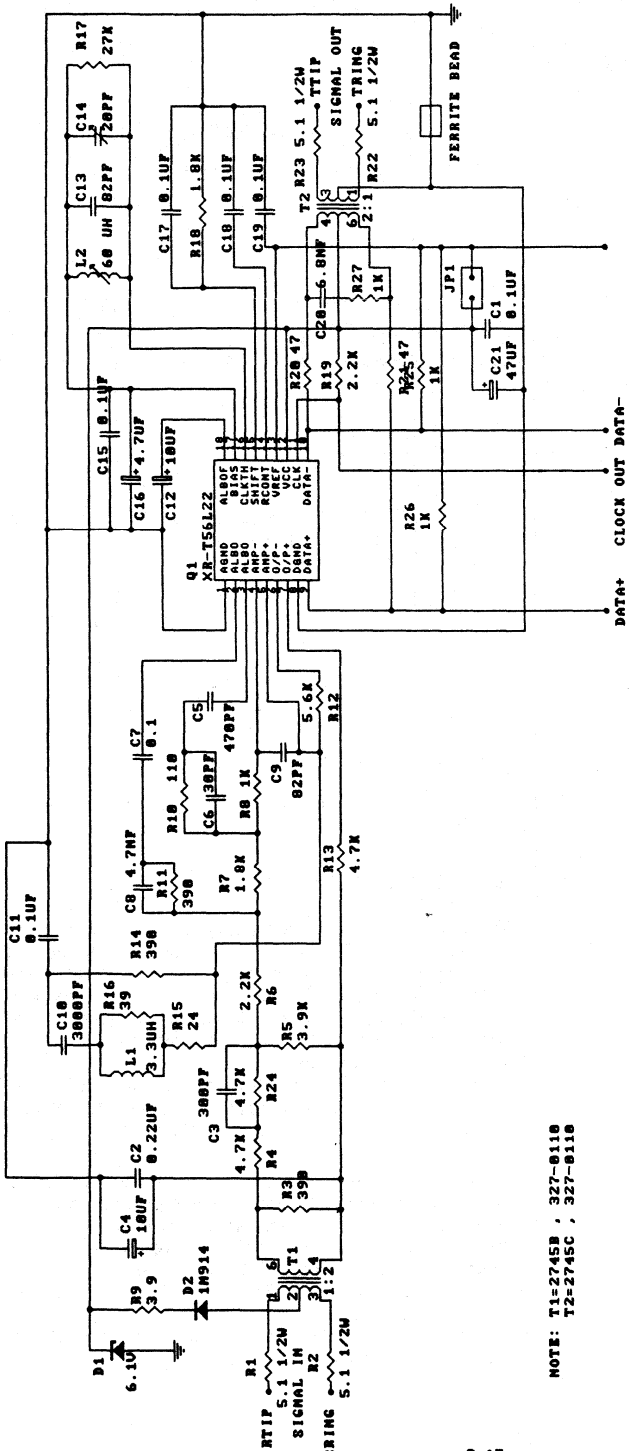


Figure 6. AC Parameter Test Circuit



Typical Application for the XR-T56L22 at 1.544 MBPs.



NOTE: T1=2745B , 327-0110
T2=2745C , 327-0110

Typical Application for the XR-T56L22 at 2.048 MBps

PCM Transceiver Chip

GENERAL DESCRIPTION

The XR-T5681 is a PCM transceiver chip. It consists of both transmit and receive circuitry in a CERDIP 18 pin package. The transceiver is designed for short line application (<–10 dB) such as in digital multiplexed interfacing and digital PBX environments. The maximum frequency of operation is 3 MBits/s so it covers T1, T148C, and Europe's 2.048 MBit/s PCM system.

FEATURES

Single +5.0 V Supply
Receiver Can Accept Either Balanced or Unbalanced Inputs
TTL Compatible Interface
Transmitter and Receiver in One Package

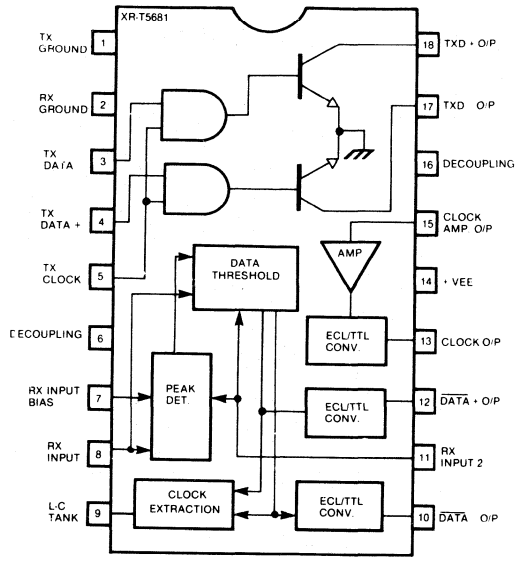
APPLICATIONS

T1, T148C, and 2.048 MBits/s PCM Line Interface
CPI
DMI

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+20 V
Storage Temperature	-65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5681	Ceramic	0°C to 70°C

SYSTEM DESCRIPTION

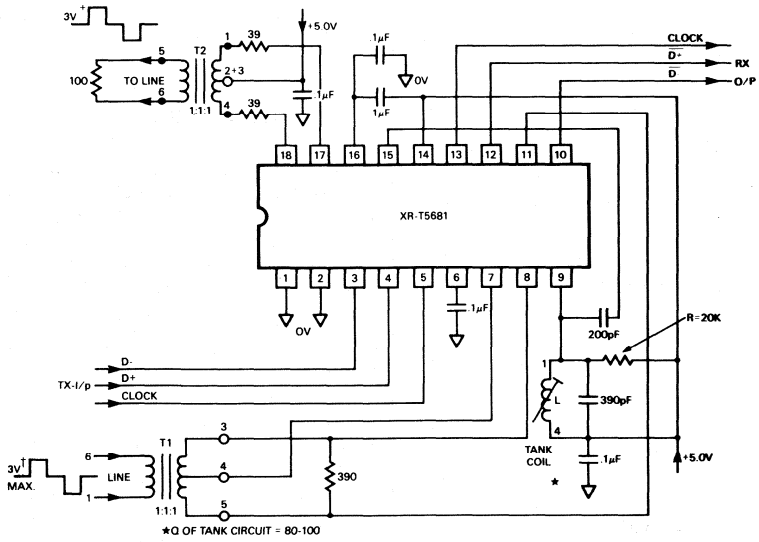
The functions of the circuit terminals are defined in the Functional Block Diagram. At the receive direction, the incoming bipolar signal which has been attentuated and distorted by the cable is applied to the input of the peak detector. The variable threshold voltage produced by the peak detector controls the data comparator for positive and negative rails signal extractions. Timing information is obtained by means of a full wave rectifier and an L-C resonant circuit tuned at the appropriate frequency. All data and clock outputs are LSTTL compatible.

At the transmitter, the outputs have two identical nonsaturating open collector stages which can drive the output line transformer directly with a maximum current of 40 mA. Full width, TTL compatible, positive and negative rail signals at the inputs and a 50% duty cycle TTL clock are needed to form the bipolar line signal at the secondary of the transformer. The output signal conforms to CCITT G.703 recommendation. A circuit diagram connected for 2048 K bits/s line interface application is shown in Figure 1.

ELECTRICAL CHARACTERISTICS

Test Conditions: $+V_{CC}$ = 5.0 V, T_A = 0°C - +70°C, unless specified otherwise.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
DC Supply	+4.75	+5.0	+5.25	V	
Supply Current		35.0	46.0	mA	T_X Drivers Open
Tank Drive Current	1.5	2.0	2.5	mA	Measured at Pin 9,
Clock O/P/Low Level		0.3	0.8	V	Measured at Pin 13, I_{OL} = 1.0 mA
Clock O/P/High Level	3.0	4.3		V	Measured at Pin 13, I_{OH} = 400μA
Data O/P/Low Level		0.4	0.8	V	Measured at Pins 10,12, I_{OL} = 1.0 mA
Data O/P/High Level	3.0	4.5		V	Measured at Pin 10,12, I_{OH} = 400μA
Transmitter O/P/Low Level	0.6		0.95	V	Measured at Pin 13,15, I_{OL} = 40 mA
Transmitter O/P/Current Sink			40	mA	Measured at Pin 13,15, V_{OL} = 0.95V
Transmitter O/P/Rise Time		20	30	ns	Measured at Pin 13,15 with 150Ω Pull-up to +5.0 V, CL = 15 pF
Transmitter O/P/Fall Time		20	30	ns	Measured at Pin 13,15 with 150Ω Pull-up to +5.0 V, CL = 15 pF



T1 = AIE input transformer part o. 315–0765
Tank Coil = AIE part no. 415–0804 (only terminal 1 & 4 being used).
MAX input voltage to T1 primary = 3 Vp or 6 Vp-p at 5.0 V supply.
ADJUST L until min. clock jitter is obtained at pin 13.
T2 = AIE part no. 318–0696

Figure 2. Circuit Connection Diagram for 2048Kbits/s operating

PCM Line Interface Chip

GENERAL DESCRIPTION

The XR-T5683 is a PCM line interface chip. It consists of both transmit and receive circuitry in a DIL 18 pin package. The maximum bit rate the chip can handle is 8.448 M Bits/s and the signal level to the receiver can be attenuated by −10 dB cable loss at half the bit rate. At nominal supply voltage operation the typical current consumption is 40 mA.

FEATURES

Single +5.0 V Supply
Receiver Input Can Be Either Balanced or Unbalanced
Up to 8.448 MBits/s Operation in Both
T_X and R_X Directions
TTL Compatible Interface

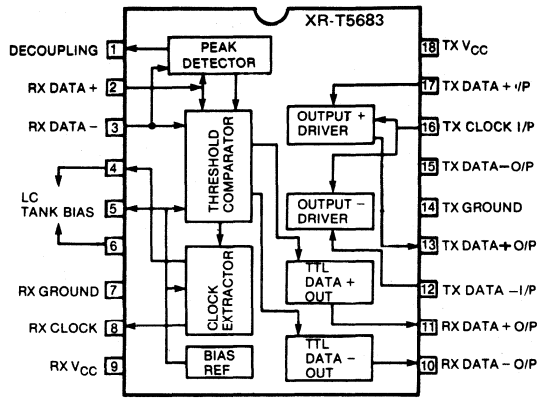
APPLICATIONS

T1, T148C, T2, 2048 & 8448 KBits/s
PCM Line Interface
CPI
DMI

ABSOULTE MAXIMUM RATINGS

Supply Voltage	+20 V
Storage Temperature	-65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5683	Ceramic	-40°C to +85°C

SYSTEM DESCRIPTION

The incoming bipolar PCM signal which is attenuated and distorted by the cable is applied to the threshold comparator and the peak detector. The peak detector generates a DC reference for the threshold comparator for data and clock extraction. A tank circuit tuned to the appropriate frequency is added to the later operation. The clock signal, data (+) data (−) all go through a similar level shifter to be converted into TTL level to be compatible for digital processing.

In the transmit direction, the output drivers consist of two identical TTL inputs with open collector output stages. The maximum low level current these output stages can sink is 40 mA. With full width data applied to the inputs together with a synchronized clock. The output will generate a bipolar signal when driving a centre-tapped transformer. A typical circuit diagram to XR-T5683 is shown in Figure 1.

DC ELECTRICAL CHARACTERISTICS

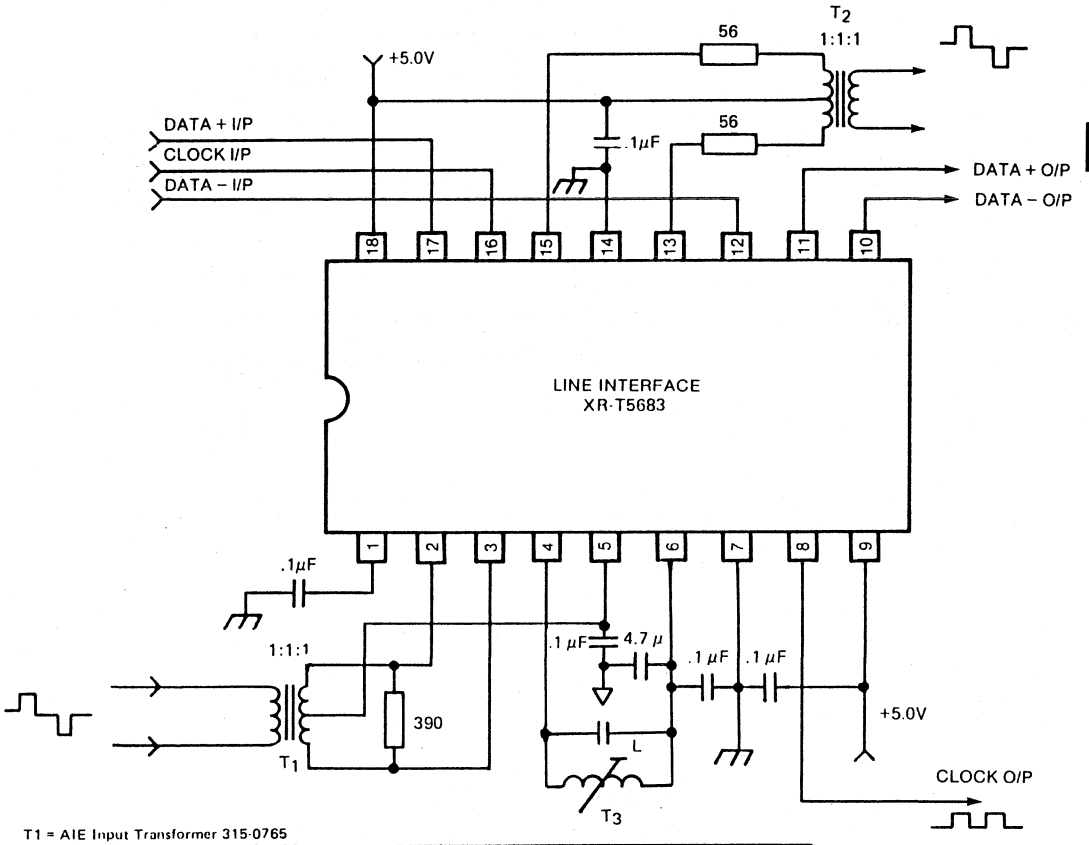
Test Conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° - 70°C, unless otherwise specified.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	4.75	5	5.25	V	
Supply Current		40	55	mA	Total Current to Pin 9 & Pin 18 Transmitter Outputs Open
RECEIVER SECTION					
Tank Drive Current	300	500	700	µA	Measured at Pin 4, V_{CC} = 5 V
Clock Output Low		0.3	0.6	V	Measured at Pin 8 I_{OL} = 1.6 mA
Clock Output High	3.0	3.6		V	Measured at Pin 8 I_{OH} = 400 µA
Data Output Low		0.3	0.6	V	Measured at Pin 10 & 11 I_{OL} = 1.6 mA
Data Output High	3.0	3.6		V	Measured at Pin 10 & 11 I_{OH} = 400 µA
TRANSMITTER SECTION					
Driver Ouput Low	0.6	0.8	1.0	V	Measured at Pin 13 & 15 I_{OL} = 40 mA
Output Leakage Current		0	100	µA	Measured in Off State Output Pull-up to + 20 V
Input High Voltage	2.2			V	Measured at Pin 12, 16 & 17 I_{OL} = 40 mA, V_{OL} = 1.0 V
Input Low Voltage			0.8	V	Measured at Pin 12, 16 & 17 Output Off
Input Low Current			−1.6	mA	Measured at Pin 12, 16 & 17 Input Low Voltage = 0.4 V
Input High Current			40	µA	Measured at Pin 12, 16 & 17 Input High Voltage = 2.7 V
Output Low Current			40	mA	Measured at Pin 13 & 15 V_{OL} = 1.0 V

AC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.0 V, T_A = 25°C, unless otherwise specified.

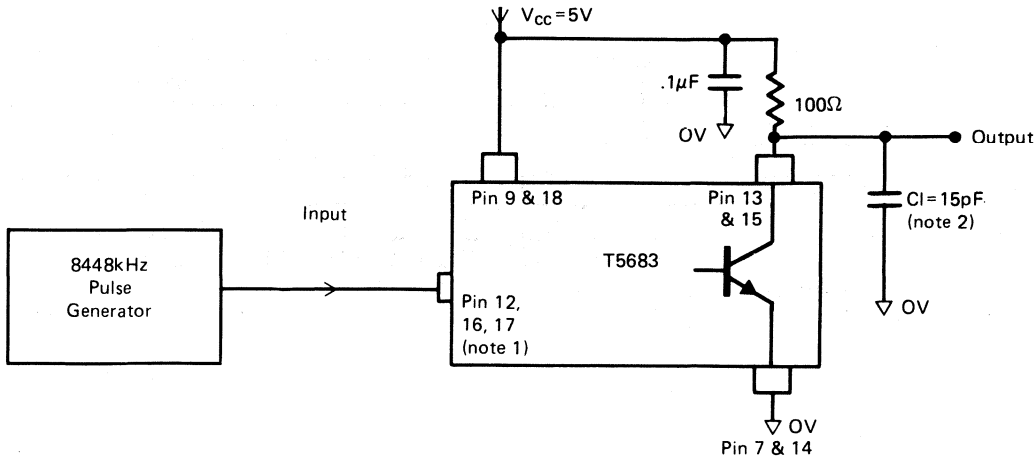
PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
RECEIVER SECTION					
Input Level		6	6.6	Vpp	Measured Between Pin 2 & 3
Loss Input Signal Alarm Level		0.8		Vpp	Measured Between Pin 2 & 3 Alarm On Pull Data Output High
Input Impedance at 2048 KHz		2.5		kΩ	Measured Between Pin 2 & 3 With Sinewave Input
Clock Duty Cycle	35	50	65	%	Measured at Pin 8 at 2.0 V DC Level
Clock Rise & Fall Time		20		ns	Measured at Pin 8, C_L – 15pF
Data Pulse Width	35	50	75	% of clock period	Measured at Pin 10 & 11 At 1 V DC Level, Cable Loss = 0
TRANSMITTER SECTION					
Pulse Width at **8448 KHz**	53		65	ns	Measured at Pin 13 & 15 See Test Circuit 1
Output Rise Time		12	25	ns	See Test Circuit 1
Output Fall Time		12	25	ns	See Test Circuit 1
Output Pulse Imbalance		2.5		ns	At 50% Output Level



T1 = AIE Input Transformer 315-0765
T2 = AIE Output Transformer 318-0696
T3 = AIE Tank Coil 415-0804

Device	1.544 MBPS	2.048 MBPS
L	~60μH	~60μH
C	175 pF	100 pF

Figure 1. A Recommended Circuit for 1.544 MBits/s Operation



Note 1. Inputs that are not connected to pulse generator will be tied to $+V_{CC}$ via 1k resistor.

Note 2. Cl included probe and jig capacitance.

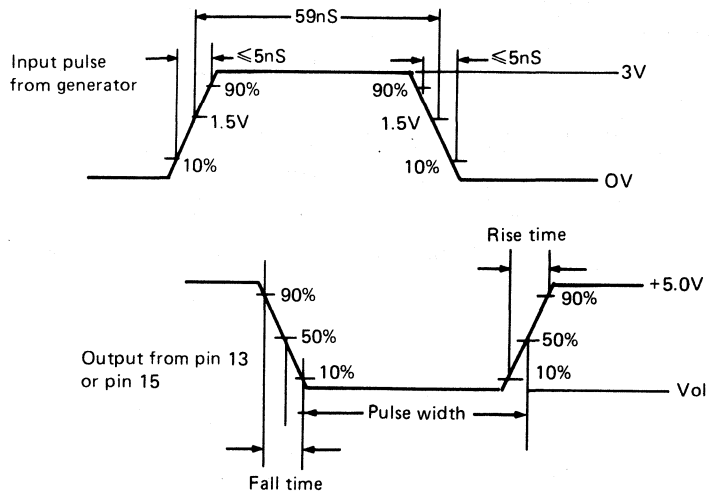


Figure 2. T5683 Transmitter test circuit and switching waveforms (measured @ 8.448 MBPS).

CMOS Digital T1 Line Interface

GENERAL DESCRIPTION

The XR-T5684 is a PCM line transceiver integrated circuit which is intended to interface the DSX-1 digital cross-connect. It combines both transmit and receive circuitry in a 28 pin package and performs the necessary physical layer interface requirements. This device is primarily designed for short loop applications (<-6 dB) such as digital office environments. Internal pulse shaping circuit at the transmitter generates appropriate pulse shape at the DSX-1 cross connect for line lengths ranging from 0 to 655 feet.

FEATURES

Single +5V Supply
Receiver accepts Balanced or Unbalanced Inputs
TTL Compatible Interface
Transmitter/Receiver in One Package
No LC Tuning Required
CMOS Digital Technology
High Jitter Tolerance
Meets Bell PUB 62411 and PUB 43802 requirements
Build-In Equalization For Line Lengths between 0 and 655 Feet
Functional Replacement for CS6152

APPLICATIONS

T1, PCM line interface used in network equipment such as multiplexers, channel banks and other DSX-1 switching systems.
Also used in Customer Premises Equipment like PABXs, Custom LANs and gateways to CSUs, T1 modems, test and measurement equipment and others.

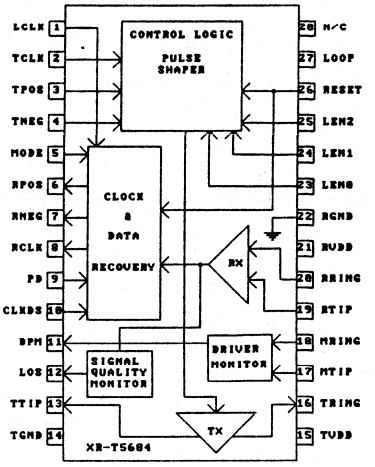
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (continuous)	-0.5 to +7V
Supply Current (continuous)	20mA to -20mA
Storage Temperature	-65° C to +150° C

ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-T5684CJ	PLCC	0°C to 70°C
XR-T5684IJ	PLCC	-40°C to 85°C
XR-T5684CP	Plastic DIP	0° C to 70° C
XR-T5684IP	Plastic DIP	-40°C to 85°C

PIN ASSIGNMENT



SYSTEM DESCRIPTION

The functions of the T1 line interface IC can simply be divided into the transmitter and receiver section. The two sections are electrically isolated by separate power supplies in order to minimize noise and crosstalk.

The receiver extracts the data and clock from the coded Alternate Mark Inverted (AMI) data stream and outputs TTL compatible and synchronized clock and data to the rest of circuitry. Optimized receiver sensitivity allows clock and data extraction over the specified cable attenuation without having to equalize or use any automatic line build out circuitry. The incoming AMI signals presented to RTIP and RRING have opposite polarity through a center-grounded, center-tapped transformer. These pulses, which have been attenuated and distorted by the cable are applied to the input of the peak detector. The variable threshold voltage produced by the peak detector controls the data comparator threshold for positive and negative data extraction.

In applications where the clock recovery scheme is not needed, the extracted data pulses appear directly at RPOS and RNEG after being stretched 80ns. If clock recovery is selected by setting MODE to high, an 8X or 16X clock must be input to LCLK for the clock recovery counter/divider to extract timing information from the incoming data pulses. When there is no data pulse at

DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A=25° C, V_{DD}=5V+/-5%, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
RECOMMENDED OPERATING CONDITIONS						
V_{DD}	Operating Supply Voltage	4.75	5	5.25	V	
PD	Total Power Dissipation			400	mW	
	100% ones Density and Max. Line Length					
INPUTS						
V_{IH}	Input High Level	2.0			V	
V_{IL}	Input Low Level			0.8	V	
I_{IL}	Input Leakage Current			10	µA	
OUTPUTS						
V_{OH}	Output High Level	2.4			V	
V_{OL}	Output Low Level			.35	V	
I_{OUT}	Output Drive Current		4		mA	
THRESHOLD						
D_{TH}	Data Threshold Vmin< Vin <Vmax		70		%	
L_{OS}	Loss of signal threshold	0.4	0.5	0.6	V	

AC CHARACTERISTICS

Test Conditions: T_A=25° C, V_{DD}=5V+/-5%, unless otherwise specified.

CLOCK						
T_{CLK}	Clock Frequency	1.544 MHz + 500 Hz				
L_{CLK}	Oversampling Clock 8x	12.352 +/- 0.5% MHz				
	16x	24.704 +/- 0.5% MHz				
P_W	Clock Pulse Width	294	324	354	ns	
D_{CLK}	Clock Duty Cycle		50		%	
DATA						
T_r	Output Rise Time 10%-90% L=50pF	25	ns			
T_f	Output Fall Time 10%-90% L=50pF	25	ns			

the input, the divider will operate in its free running mode, generating an even mark and space ratio square wave. This free running mode will however be interrupted if a received pulse is detected; the resultant mark and space ratio of the generated clock is then determined by the position of the arrival of the input pulse relative to its-free running position. The data at RPOS and RNEG in this case is always valid at the rising edge of the RCLK. The jitter tolerance of this circuit meets the requirements as specified in 662411 and 43802 publications.

Included as part of the receiver section is a signal quality monitor block which reports a loss of signal on the LOS pin whenever the signal level falls below 0.5V. This pin will go high within 200bit periods if the signal falls below the specified threshold level. Also, in the event of no signal at all, LOS will be set after 175 ±2 zeros is detected. The receiver will continue to recover data and will return to its normal operational state if it detects a signal on RTIP and RRING inputs.

The transmitter section is designed to take unipolar or NRZ data encoded as TPOS and TNEG and produce alternate bipolar pulses with the appropriate pulse shape conforming to the DSX-1 cross-connect specification. Pulse Shaping is selectable for line lengths between 0 and 655 feet through pins LEN1, LEN2 and LEN3 as illustrated in table 1. These inputs can be hardwired with a switch set at the time of installation or they can be used with an intelligent controller for variable line length select. The transmit data is driven to the line in a true differential manner by the output stage which has a maximum current capability of 60mA. The outputs (TTIP and TRING) are current limited and require a 1:1.36 step-up transformer in order to achieve the necessary preequalized voltage, which exceed the +5V supply.

As part of the transmitter section, the Driver Monitor section is able to monitor the transmitted signal and give an early warning signal to isolate nonfunctioning T1 links. If no signal is present at MTIP and MRING for 63 clock cycles DPMO will go high.

PIN DESCRIPTIONS

Pin#	Name	I/O	Description
1	LCLK	I	**Oversampling Clock Input.** Can be either 8X or 16X with respect to the incoming data rate. Selection is done through PD pin 9 PD = HIGH = 16X Clock; PD = Low = 8X Clock.
2	TCLK	I	**Transmit Clock Input.** (1.544MHz)
3	TPOS	I	**Transmit Positive Data Input.** (Full width NRZ Data) A positive pulse on this input causes a positive pulse to be transmitted on TTIP. TPOS is sampled on the falling edge of TCLK.
4	TNEG	I	**Transmit Negative Data Input.** (Full width NRZ Data) A positive pulse on this input causes a negative pulse to be transmitted on TRING. TNEG is sampled on the falling edge of TCLK.
5	MODE	I	**Receive Data Select.** When high, the extracted data is synchronized to the recovered clock and full width. When low, the extracted data have no relation to the clock and are typically stretched 80ns before being output on RPOS and RNEG. This pin is internally pulled down
6	RPOS	O	**Receive Positive Data Output.** A positive pulse on RTIP causes a positive pulse to appear on RPOS. (Also see MODE select).
7	RNEG	O	**Receive Negative Data Output.** A negative pulse on RRING causes a positive pulse to appear on RNEG. (Also see MODE select).
8	RCLK	O	**Receive Clock Output.** Synchronized recovered clock output at 1.544MHz. When MODE is set high.

9	PD	I	This pin can be selected high or low depending on LCLK clock frequency at pin 1. When LCLK clock = 16X, PD should be set high, when LCLK = 8X, PD should be set low. This pin is internally pulled down.
10	CLKDS	I	When high, recovered clock at pin 8 is disabled. This function is provided for some applications where upon input data loss, the clock can be inhibited by connecting LOS pin to CLKDS externally. This pin is internally pulled down.
11	DPM	O	**Driver Performance Monitor.** Used as early warning signal on non-func tioning T1 links. If no sig-nal is present on MTIP and MRING for 63 clock cycles DPM goes high until the first detected signal.
12	LOS		**Loss of Signal.** This out-put is used as a receive signal quality monitor which goes high either when the input level drops to below 0.5V peak or after 175 con secutive zeros have been detected . The 175 zeros detection is active only when the LCLK clock is applied.
13	TTIP	O	**Transmitter Positive Data Output.** Connected to the output transformer for AMI signal generation to the line
14	TGND	I	**Transmitter Ground.** (0V)
15	TVDD	I	**Transmit Positive Supply.** (5V ±5%).
16	TRING	O	**Transmit Negative Data Output.** Connected to the output transformer for AMI signal generation to the line.
17	MTIP	I	**Driver Monitor Input.** This pin is normally connect-ed to TTIP for monitoring the output of the line driver It can be left floating as it is internally pulled high.
18	MRING	I	**Driver Monitor Input.** This pin is normally connected to TRING for monitoring the output of the line driver. It can be left floating as it is internally pulled high.
19	RTIP	I	**Receiver Line Signal Input.** The AMI receive signal is in-put to this pin (TIP) A, a cen-tre-tapped, centre-grounded, 1:2 step-up transformer is required.
20	RRING	I	**Receiver Line Signal.** The AMI receive signal is input to this pin (RING). A centre-tapped, centre-grounded, 1:1.36 step-up transformer is required.
21	RVDD	I	**Receiver Positive Supply.** (5V)
22	RGND	I	**Receiver Ground.** (0V)
23	LEN0	I	**Pulse Shape Select.** Least significant bit. (See Table 1)
24	LEN1	I	**Pulse Shape Select.** Second significant bit. (See Table 1)
25	LEN2	I	**Pulse Shape Select.** Most significant bit. (See Table 1 for cable length selection).
26	TEST	I	**Factory Test Pin.** Internally pull down for normal opera tion.
27	NC		No Connection
28	TAOS	I	**Transmit All Ones.** Setting TAOS to a logic 1 causes continuous ones to be trans-mitted at the frequency de-termined by TCLK.

LEN2	LEN1	LEN0	LINE LEGNTH SELECTED (FT.)
0	1	1	0-133
1	0	0	133-266
1	0	1	266-399
1	1	0	399-533
1	1	1	533-655

TABLE 1

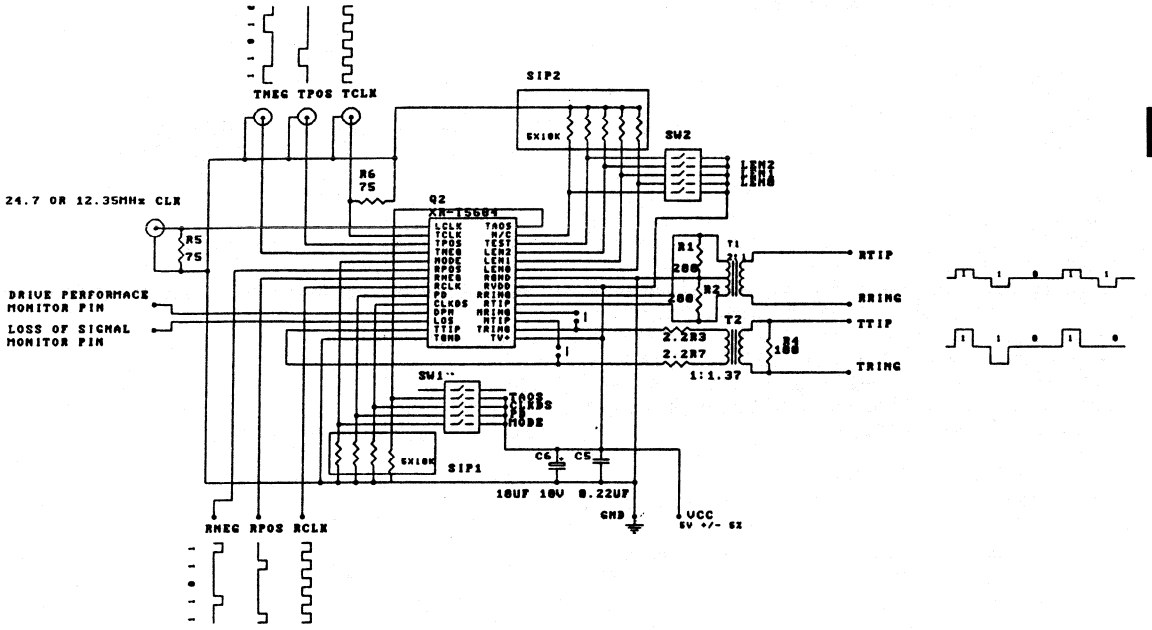


Figure 1. Typical Application Diagram for XR-T5684

PCM Line Interface

GENERAL DESCRIPTION

The XR-T61574 PCM Line Interface provides the transmit and receive line interface functions for a T1/CEPT interface in a 29 pin package. This device operates form a single 5V power source and is completely transparent to the framing format. On the transmit side, the transmit pulses are shaped to the appropriate pulse shape depending on the line length (0 to 655 feet: 1500 max). This is generally required by CSU's or other Cross-connect equipment. The receiver extracts data and clock from an AMI encoded signal and outputs clock and synchronized data. Included is an elastic store, intended to remove jitter from either the transmit or the receive path depending on the application in which it is used.

ORDERING INFORMATION

Part Number	Device	Operating Temperature
XR-T61574IP	Plastic	-40°C to +85°C
XR-T61574IJ	PLCC	-40°C to +85°C
XR-T61574CP	Plastic	0°C to +70°C
XR-T61574CJ	PLCC	0°C to +70°C

FEATURES

PCM Line Interface for T1 or CEPT Applications
Pulse Shaping Line Driver and Clock/Data Recovery Functions
Jitter Attenuator (300UI @ 6Hz)
Microprocessor Controllable
Compatible with CSU's and DACS's
Diagnostic Features
Pin-to-pin and Functionally Compatible to CS61574

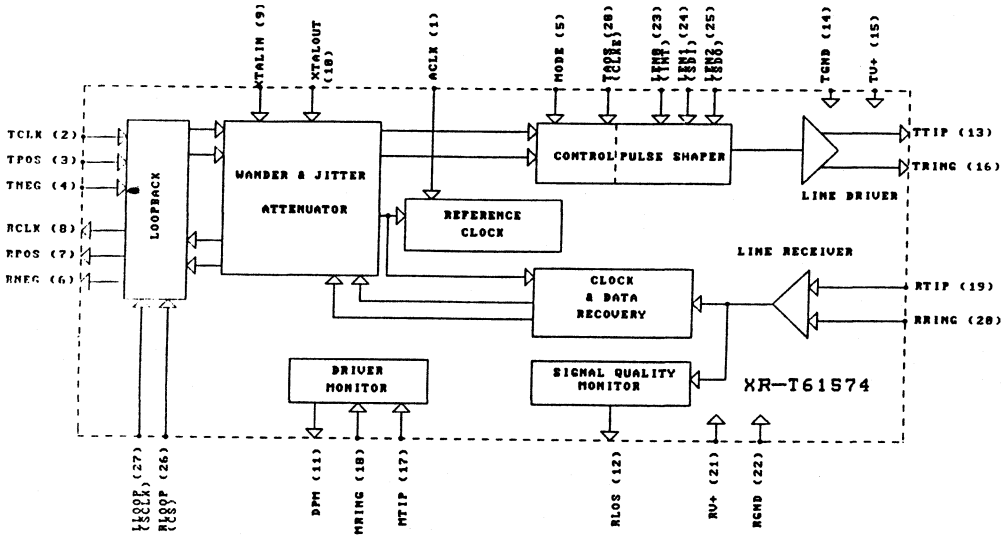
APPLICATIONS

DACS
Channel Banks
DSX-1 Cross-connect Equipment
CSU's
Building Channel Service Units

FUNCTIONAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6.0V
Input Voltage (any pin)	-0.3V to 6.3V
Input Current (any pin)	10mA
Storage Temperature	-65°C to 150°C



Low Power PCM Line Interface

GENERAL DESCRIPTION

The XR-T56L85 is a PCM line interface chip. It consists of both transmit and receive circuitry in a DIL 18 pin package. The maximum bit rate the chip can handle is 2.048 Mbps and the signal level to the receiver can be attenuated by -10dB of cable loss at half the bit rate. Total current consumption is between 12 - 16 mA at +5V.

FEATURES

Low Power (Typ 14 mA)
Single +5.0 V Supply
Up to 2.048 Mbps Operation in Both TX and RX Directions
TTL Compatible Interface
Receiver Input can be:
- Balanced Transformer Coupled
- Capacitively Coupled (Twisted Pair)
- Single Coaxial Capacitive Coupling

APPLICATIONS

T1 and CEPT Interfaces
CPI
DMI

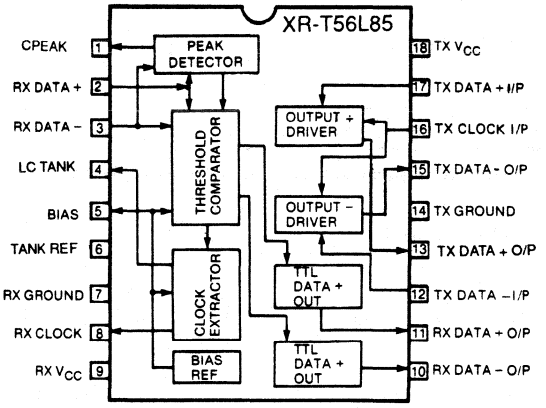
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+20 V
Storage Temperature	-65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-T56L85N	Ceramic DIP	-40°C to +85°C
XR-T56L85D	S.O.I.C.	-40°C to +85°C

PIN ASSIGNMENT



SYSTEM DESCRIPTION

The incoming bipolar PCM signal which is attenuated and distorted by the cable is applied to the receiver input either through a balanced transformer or a single ended capacitive coupled terminal. A peak detector following the input generates a DC reference for the positive threshold comparator. This voltage in turn is mirrored around a reference voltage to establish the threshold voltage for the negative pulses. This way it is possible to extract the positive and negative data pulses as well as the recovered clock. A tank circuit tuned to the appropriate frequency is added externally to maintain the clock output. The clock signal, data + and data -, all go through a similar level shifter to be converted into TTL level to be compatible for digital processing.

In the transmit direction, the output drivers consist of two identical TTL inputs with open collector output stages. The maximum low level current these output stages can sink is 80 mA. With full width data applied to the inputs together with a synchronized clock the output will generate a bipolar signal when driving a centre-tapped transformer. A typical application diagram for the XR-T56L85 is shown in Figure 5.

DC ELECTRICAL CHARACTERISTICS

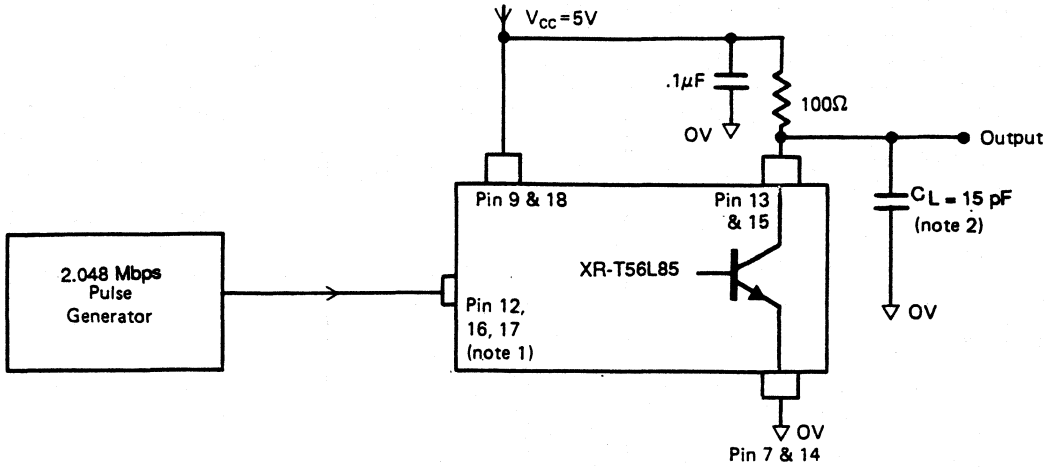
Test Conditions: VCC = 5.0 V ± 5%, TA = -40°C to +85°C, unless otherwise specified.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	4.75	5	5.25	V	
Supply Current		14	16	mA	Total Current to Pin 9 & Pin 18 (Transmitter Outputs Open and All Ones Pattern)
RECEIVER SECTION					
Tank Drive Current	300	500	700	µA	Measured at Pin 4, V_{CC} = 5 V
Clock Output Low		0.3	0.6	V	Measured at Pin 8 I_{OL} = -1.6 mA
Clock Output High	3.0	3.6		V	Measured at Pin 8 I_{OH} = 400 µA
Data Output Low		0.3	0.6	V	Measured at Pin 10 & 11 I_{OL} = -1.6 mA
Data Output High	3.0	3.6		V	Measured at Pin 10 & 11 I_{OH} = 400 µA
TRANSMITTER SECTION					
Driver Output Low	0.6	0.9	1.2	V	Measured at Pin 13 & 15 I_{OL} = -40 mA
Output Leakage Current			100	µA	Measured in Off State Output Pull-up to +20 V
Input High Voltage	2.2			V	Measured at Pin 12, 16 & 17 I_{OL} = -40 mA, V_{OL} = 1.0 V
Input Low Voltage			0.8	V	Measured at Pin 12, 16 & 17 Output Off
Input Low Current			-1.6	mA	Measured at Pin 12, 16 &17 Input Low Voltage = 0.4 V
Input High Current			40	µA	Measured at Pin 12, 16 &17 Input High Voltage = 2.7 V
Output Low Current			-80	mA	Measured at Pin 13 & 15 V_{OL} = 1.0 V

AC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC = 5.0 V ± 5%, TA = -40°C to +85°C, unless otherwise specified.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
RECEIVER SECTION					
Input Level		6	6.6	Vpp	Measured Between Pin 2 & 3
Loss Input Signal Alarm Level		0.6		Vpp	Measured Between pin 2 & 3 Alarm On Pull Data/Clock Output High
Input Impedance at 2048 KHz		2.5		kΩ	Measured Between Pin 2 & 3 With Sinewave Input
Clock Duty Cycle	35	50	65	%	Measured at Pin 8 at 2.0 V DC Level
Clock Rise & Fall Time		20	40	ns	Measured at Pin 8, CL = 15pF
Data Pulse Width	35	50	75	% of clock period	Measured at Pin 10 & 11 At 1 V DC Level, Cable Loss = 0dB
TRANSMITTER SECTION					
Pulse Width at 2048 KHz	234	244	264	ns	Measured at Pin 13 & 15 Figure 1
Output Rise Time		12	25	ns	Figure 1
Output Fall Time		12	25	ns	Figure 1
Output Pulse Imbalance		2.5		ns	At 50% Output Level



Note 1. Inputs that are not connected to pulse generator will be tied to $+V_{CC}$ via 1k resistor.

Note 2. C_L includes probe and jig capacitance.

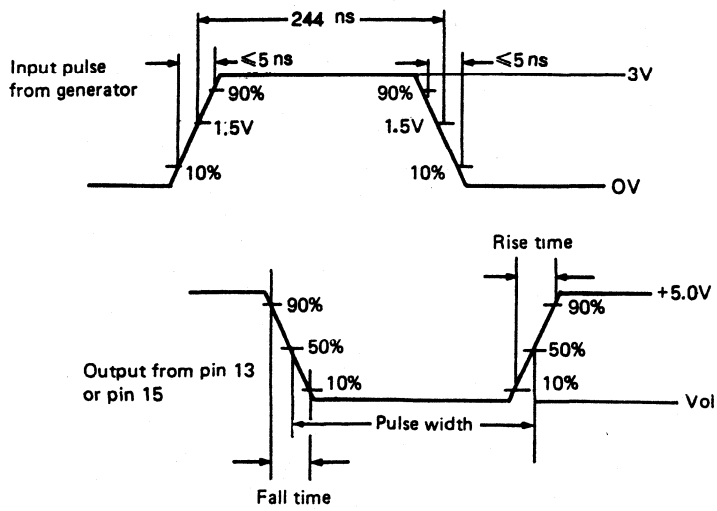


Figure 1. Transmitter Test Circuit and Switching Waveforms

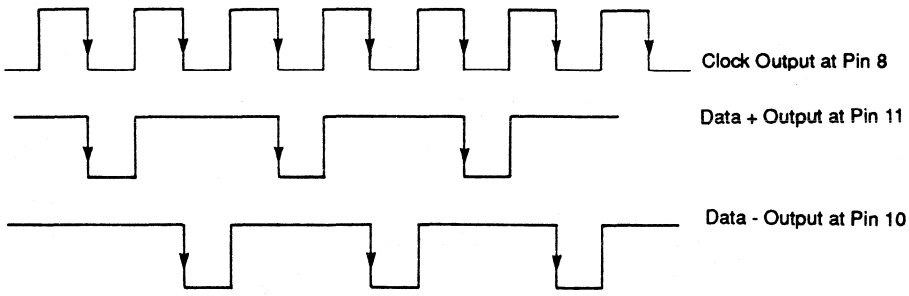


Figure 2. Receiver Output Timing Diagram With 1-1-1-1 Pattern

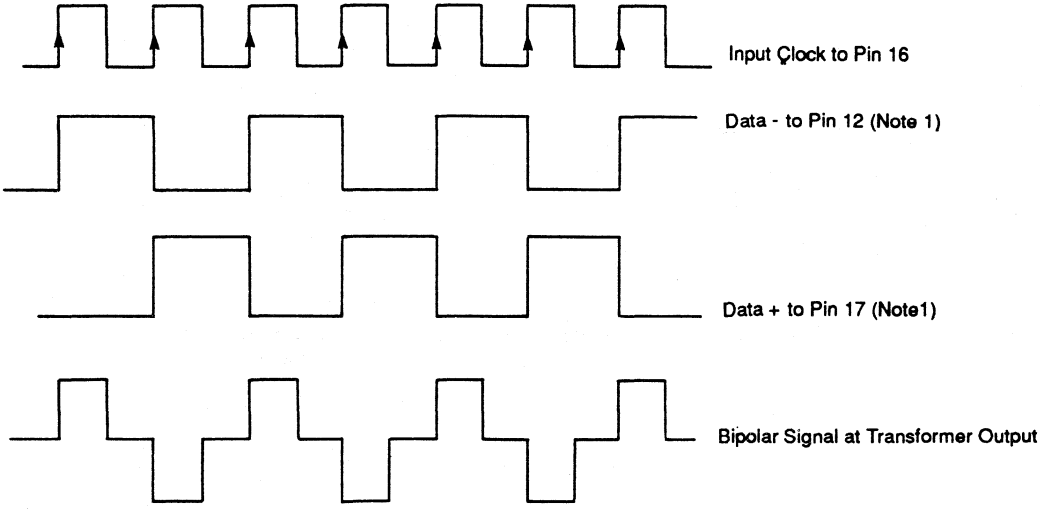


Figure 3. Transmitter Input Timing Diagram

Note 1: In the case where Data + and Data - are half-width data Pin 16 should be returned to $+V_{CC}$ via a 1k resistor.

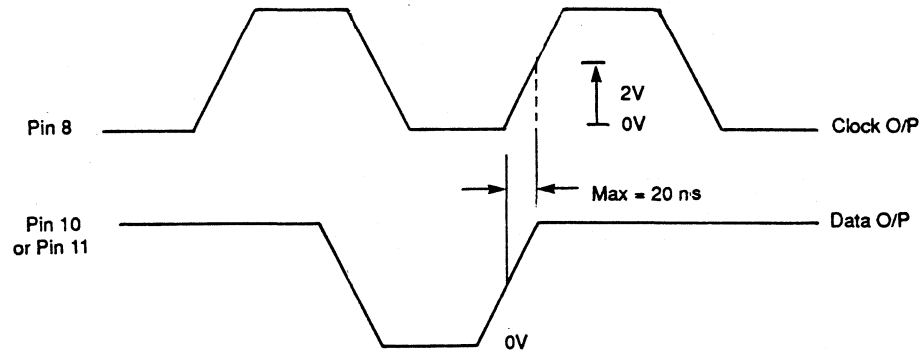
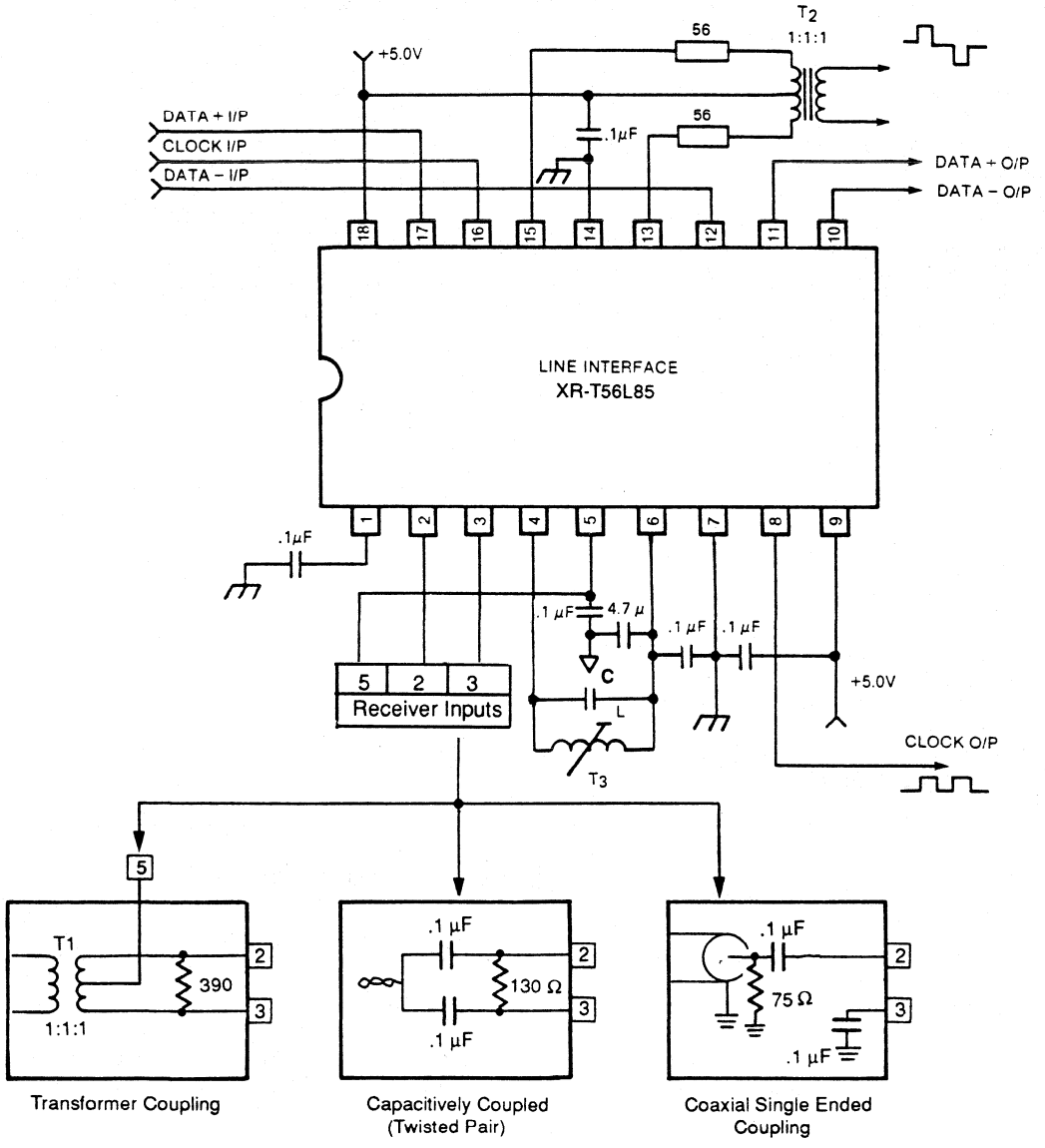


Figure 4. XR-T56L85 Data & Clock Timing Diagram With 1-1-1-1 Input Pattern and - 3db Cable Loss



T1 = AIE Input Transformer 315-0765
T2 = AIE Output Transformer 318-0696
T3 = AIE Tank Coil 415-0804

Device	1.544MBPS	2.048MBPS
L	60μH	60μH
C	175PF	100PF

Figure 5. Recommended Circuit for 1.544 & 2.048MBPS

64 Kbit/s Codirectional Interface

GENERAL DESCRIPTION

The XR-T6164 is a bipolar analog IC intended for general purpose line transceiver applications. The receiver is designed for short line applications (<10dB) at bit rates up to 1.544 Mbit/s (T1). When used in conjunction with either XR-T6165 or XR-T6166 the device conforms to CCITT G.703 specification requirements for a 64kbit/s codirectional interface. Typical current consumption is 25mA.

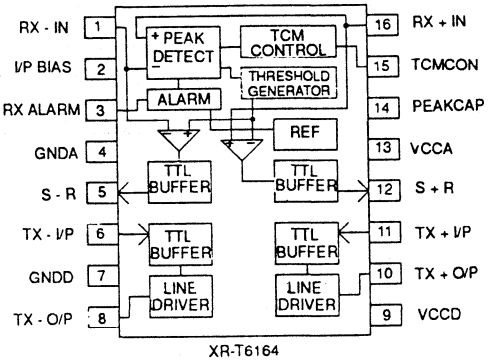
FEATURES

CCITT G.703 compatible when used with either XR-T6165 or XR-T6166
Low Power
TTL Compatible
Links Remote Equipment at Distances Up to 500M Without Equalization
Receive Input Gating Provides Ping Pong Operation Capability
Loss of Signal Alarm
Dual Matched Driver Outputs

APPLICATIONS

Data Adaption Unit (DAU).
General Purpose TTL Compatible Line Interface

PIN ASSIGNMENT



XR-T6164

APPLICATIONS

Data Adaption Unit (DAU).
General Purpose TTL Compatible Line Interface

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to 150°C
Supply Voltage	20V

ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-T6164 CN	Ceramic DIP	0°C to 70°C
XR-T6164 CP	Plastic DIP	0°C to 70°C

PIN DESCRIPTIONS

Name	I/O	Pin	Description
RX - I/P	I	1	Receiver negative bipolar input.
I/P BIAS	I	2	Internally generated bias voltage for receive inputs.
RX ALARM	O	3	Loss of signal alarm (<-15 dB) (active low).
GNDA	I	4	Analog Ground
S - R	O	5	Receive negative output data (active low).
TX - I/P	I	6	Transmit negative input signal (active high).
GNDD	I	7	Digital Ground.
TX -O/P	O	8	Transmit negative output data, open collector.
VCCD	I	9	+5V ±5% digital supply.
TX +O/P	O	10	Transmit positive output data, open collector.
TX +I/P	I	11	Transmit positive input signal - active high.
S + R	O	12	Receive positive output data (active low).
VCCA	I	13	+5V ±5% analog supply.
PEAK CAP	O	14	Receiver peak detector storage capacitor.
TCM CON	I	15	Time compression multiplex control pin (active low). When active disables Rx inputs and stores previous peak voltage.
RX +I/P	I	16	Receiver positive bipolar input.

SYSTEM DESCRIPTION

The XR-T6164 is a general purpose line interface chip. It contains both receive and transmit circuitry necessary to interface TTL signals either to or from a twisted pair cable.

Receiver

In the receive direction XR-T6164 takes balanced bipolar input signals, having been attenuated and distorted by twisted pair cable, and outputs TTL compatible active low signals corresponding to received positive and negative input data (S+R, S-R). Received signals are fed to a peak detector and threshold generator circuit providing a slicing threshold proportional to the peak received input level. Dual stage data comparators slice the input signals at this threshold and pass signals to TTL compatible output buffers. An alarm comparator, with hysteresis to prevent output jitter, monitors input signal levels (threshold set at -15dB).

Transmitter

The XR-T6164 transmitter contains two matched open collector output drivers capable of driving line transformers directly with currents up to 40mA. The transmitter output circuits include diode clamps to ensure non-saturating operation. Transmitter inputs are TTL compatible.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC = 5V ±5%. TA=25C, unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	4.75		5.25	V	
Analog Supply Current	4		6.5	mA	
Digital Supply Current	13		20	mA	
RECEIVER					
Peak Input Signal		2	2.2	Vp	Pins 1, 16 with respect to pin 2 (See Note 1)
Dynamic Range			10	dB	Without Equalization
Input Impedance		20		kohm	Pins 1, 16
Input Slicing Threshold		50		%	
Input Bias Voltage		1.45		V	Pin 2
Loss of Signal Alarm		-15		dB	
Alarm Level Hysteresis		1.5		dB	
Peak Detector Leakage		-80		uA	Pin 14; Vin = 1V
Data Output Low			0.4	V	Pins 5, 12; Iout = -1.6mA
Data Output High	3.6			V	Pins 5, 12; Iout = +40uA
Alarm Output Low			0.4	V	Pin 3; Iout = -1.6mA
Alarm Output High	4.9			V	Pin 3; Iout = +40uA
TCM Input Low Voltage			0.8	V	Pin 15; Iin min = -500uA
TCM Input High Voltage	2.2			V	Pin 15; Iin max = +5uA
TRANSMITTER					
Input Low Voltage			0.8	V	Pins 6, 11; Iin = -700uA
Input High Voltage	2.2			V	Pins 6, 11; Iin = +5uA
Output Low Voltage		1		V	Pins 8, 10; Iout = -40mA
Output Low Current	-40		-40	mA	Pins 8, 10; Vout = 1V
Output Leakage	-100			uA	Pins 8, 10; Vout = 10V Outputs in off state.

AC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC = 5V ±5% TA = 25°C, unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
RECEIVER					
Input Level	1		2.2	Vp	Pin 1, 16 with Respect to Pin 2 (See Note 1)
Output Rise Time			50	ns	Pins 5, 12; CL = 15 pF 10% to 90%
Output Fall Time			50	ns	Pins 5, 12; CL = 15pF 90% to 10%
TRANSMITTER					
Output Rise Time			50	ns	Pins 8, 10; RL=130, CL=15pF 10% to 90%
Output Fall Time			50	ns	Pins 8, 10; RL=130, CL=15pF 90% to 10%
Rising Edge Delay			60	ns	Pins 8, 10; RL=130, CL=15pF 50% to 50% (i/p to o/p)
Falling Edge Delay			60	ns	Pins 8, 10; RL=130, CL=15pF 50% to 50% (i/p to o/p)

Note 1. Higher input voltages are possible if a resistive input attenuator is used.

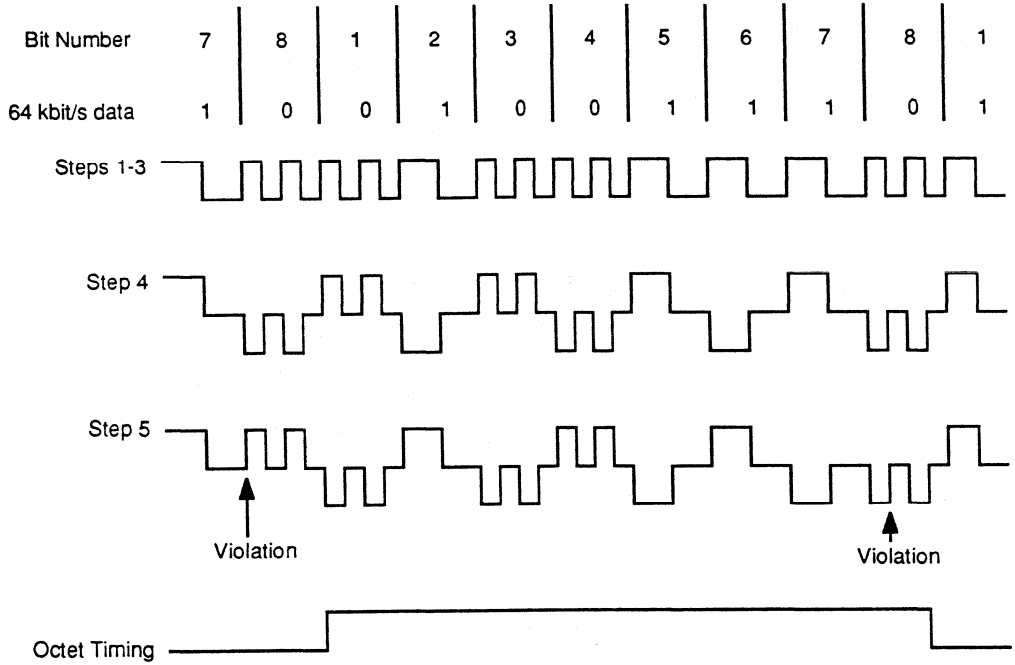


Figure 1. Transmitter Code Conversion for 64 Kbit/s Bipolar Line Signal

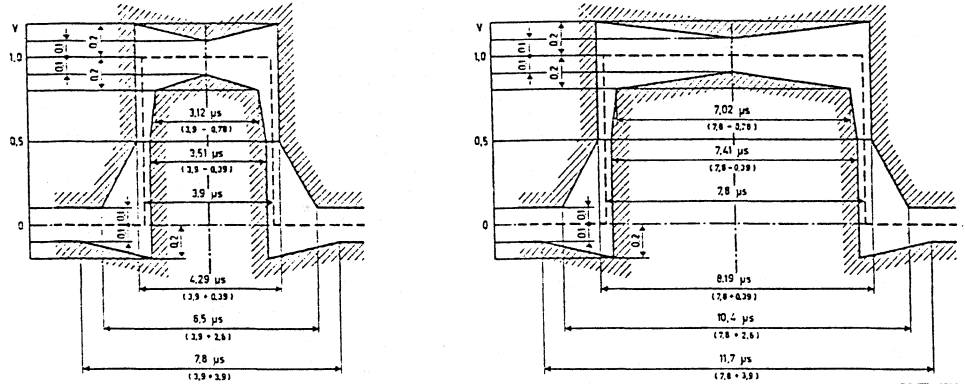


Figure 2. Pulse Masks of the 64 Kbit/s Codirectional Interface

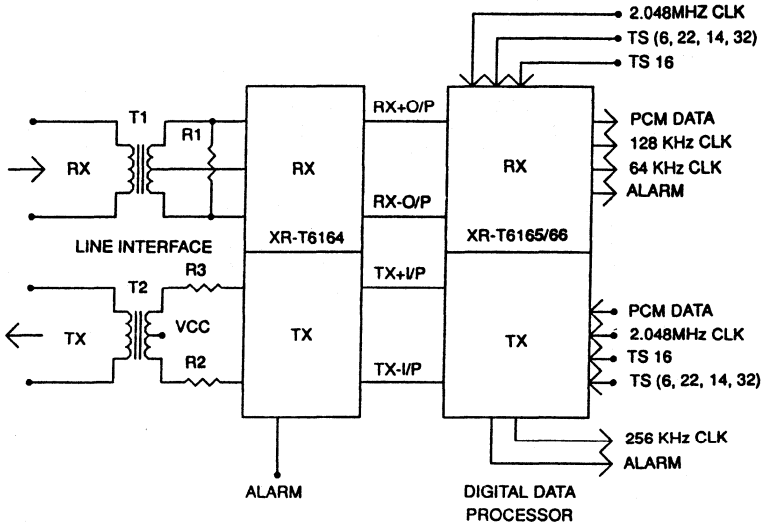


Figure 3. Digital Data Processor Application

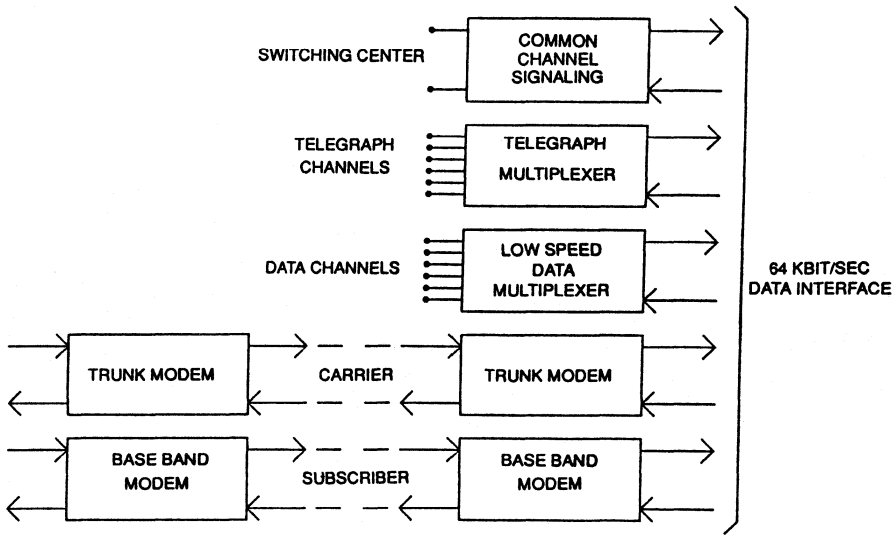


Figure 4. Typical 64 kbit/s Data Interface

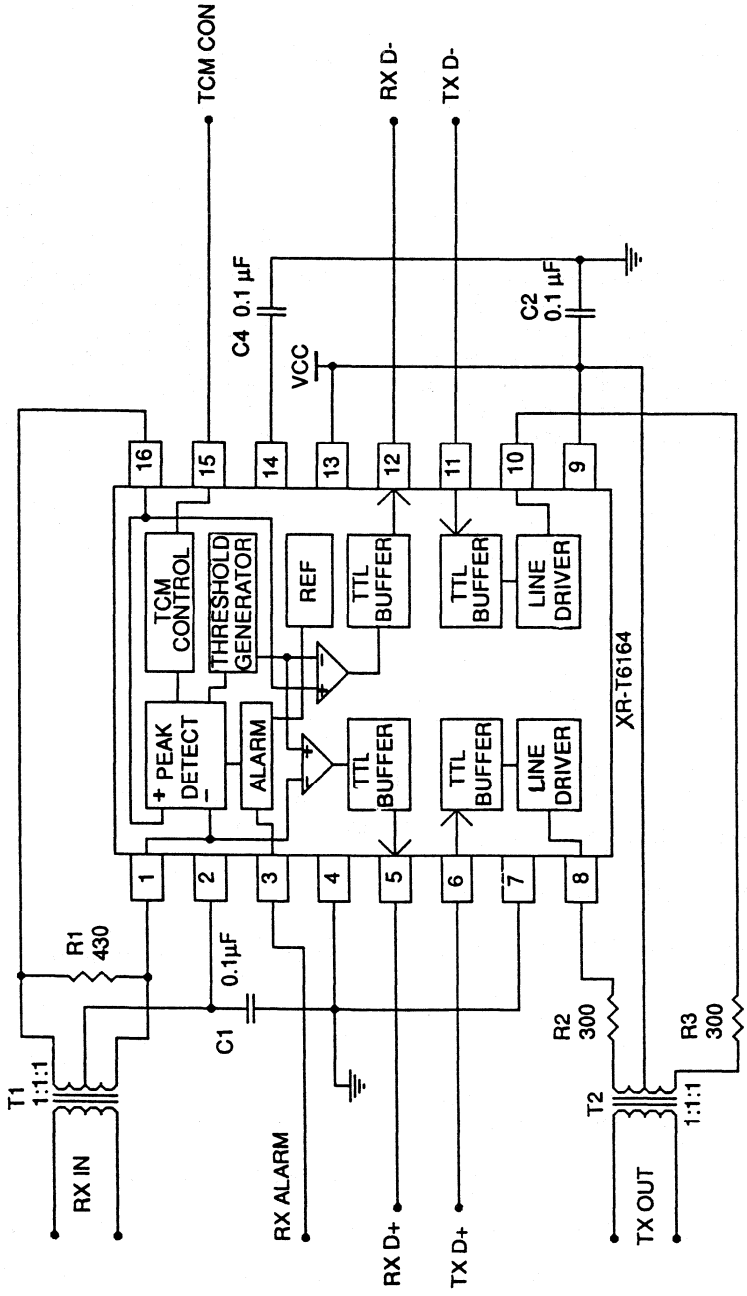


Figure 5. Typical Applications Schematic For XR-T6164

Codirectional Digital Data Processor

GENERAL DESCRIPTION

The XR-T6165 is a digital CMOS circuit which performs the interface function between a 64kbit/s data stream and a 2048kbit/s PCM timeslot data channel. When used in conjunction with the XR-T6164, the XR-T6165 conforms to CCITT G.703 specification requirements for a 64kbit/s codirectional interface.

The XR-T6165 is composed of a transmitter which transforms 8 bit 2048kbit/s timeslot data packets into a coded 64kbit/s data stream, and a receiver which performs the reverse operation. Repetition or deletion of received or transmitted data when clock skews or transients occur is automatic, allowing continuous synchronized data transmission or reception.

FEATURES

Low Power CMOS Technology
All Receiver and Transmitter Inputs and Outputs are TTL Compatible

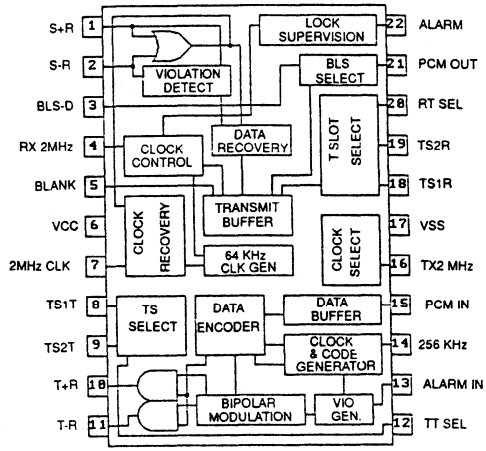
Receiver

Converts Received Encoded 64kbit/s Data to 2048kbit/s Binary Data For Insertion Into a Timeslot of a PCM Frame
Recovers Both Clock and Octet Timing
Performs Byte Insertion or Deletion in Response to Local Clock Slips
Programmable Loss of Lock Alarm (Output Inhibit/non-Inhibit)
Glitch Free Output Data Completely Available Within Supplied Timeslot Envelope
Up to 125usec Variance of Data Transfer Timing in Both Transmit and Receive Paths, Allowing Operation in Plesiochronous Networks

Transmitter

Extract 2048kbit/s Data From a PCM Frame Timeslot and Encodes it as 64kbit/s Data According to CCITT G.703 Requirements
Performs AMI Coding and Bipolar Violation Insertion for Octet Timing
Allows Inhibit of Bipolar Violation Insertion for Transmission of Alarm Conditions
Performs Byte Insertion or Deletion in Response to Local Clock Slips and Timeslot Changes

PIN ASSIGNMENT



APPLICATIONS

Data Adaptation Unit (DAU)
General 64 kbit/sec Interfaces

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to 150°C
Supply Voltage	4.5V to 5.5V

ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-T6165 CN	Ceramic DIP	0°C to 70°C
XR-T6165 CP	Plastic DIP	0°C to 70°C

Name	I/O	Pin	Description
S+R	I	1	Positive AMI data to receiver (Active Low).
S-R	I	2	Negative AMI data to receiver (Active Low).
BLS	I	3	Byte Locking Supervision (Active Low). When active causes blanking of PCMOUT under received alarm conditions.
RX2MHZ	I	4	Receiver 2048kHz clock.
BLANK	I	5	PCMOUT data blanking (Active High). When active, forces PCMOUT data to all ones(AIS)
VCC	I	6	+5V +/-10% power supply.
RXCK2 MHZ	I	7	2048kHz clock recovery signal.
TS1T	I	8	Timeslot input 1 for transmitter.
TS2T	I	9	Timeslot input 2 for transmitter.
T+R	O	10	Transmit positive output AMI data (Active Low).
T-R	O	11	Transmit negative output AMI data (Active Low).
TTSEL	I	12	Transmit timeslot select. When high pin 8 selected, when low pin 9 selected.
ALARMIN	I	13	Alarm input (Active High). When active inhibits insertion of violation in transmitted data.
TX256KHZ	I	14	Transmitter 256kHz clock.
PCMIN	I	15	Transmitter PCM input.
TX2MHZ	I	16	Transmitter 2048kHz clock.
VSS	I	17	0V power supply.
TS1R	I	18	Timeslot input 1 for receiver.
TS2R	I	19	Timeslot input 2 for receiver.
RTSEL	I	20	Receive timeslot select. When high pin 18 selected; when low pin 19 selected.
PCMOUT	O	21	Received PCM output data.
ALARM	O	22	Alarm (Active High). When active, indicates loss of received bipolar violations.

SYSTEM DESCRIPTION

When used in conjunction with the XR-T6164, the XR-T6165 will form a CCITT G.703 compatible 64kbit/s data adaption unit (DAU), interfacing between a 2048kbit/s PCM highway and a variable length twisted pair cable.

Transmitter

Operation of the transmit circuit is to convert eight bit 2048kbit/s PCM timeslot data packets into coded continuous 64kbit/s data. PCM data is read into the transmitter using a 2048kHz local clock and timeslot signal. Transmission is controlled by a 256kHz local clock. Four periods are dedicated to each bit in order to code "0" (0101) and "1" (0011). Timeslot is an envelope derived externally from the 2048kHz clock. and covers eight clock pulses. A two input selector at the timeslot input allows the transmitter to be hard wired to two timeslot positions, selectable using TTSEL. Data is loaded to a storage buffer and transferred to an output shift register, controlled by the external 256kHz signal, only after complete transmission of previously received data. Circuitry is included to delete or repeat complete words of data should skew between the clock signals occur, or during an adjustment of the timing of the timeslot signal, for example when changing from one timeslot position to another. A byte repetition just occurs once; if no new PCM data is received, the transmitter outputs stay high. Octet timing is maintained during these operations. Coded data is alternately fed to two output pins to realize AMI coding, using an external transformer and two line drivers. Transmission of octet timing is performed by feeding the seventh and eighth data bits in each word to the same output. This function may be inhibited by setting ALARMIN active.

Receiver

Operation is to receive coded continuous 64kbit/s input and extract data in the form required for insertion into a 2048kbit/s PCM timeslot. A 128kHz clock is derived from the received data and used to perform decoding of the input signal. If lock is lost with received data the clock circuit enters a seek mode, increasing the speed of the internal clock and reducing the time required to regain lock. Bipolar violations, used to identify bit 1 in the input signal are used to synchronize circuit operation for octet timing. In the absence of violations, for example when receiving a transmitted alarm condition, the circuit will continue to operate in synchronization with respect to the last received violation. Under this condition the received signal PCMOUT (Received PCM output data) is held high indicating AIS. This function may be inhibited using BLS, and the output set to all ones if required using the BLANK input. ALARM goes high after eight consecutive violations are missed. To accommodate differences between the remote (transmitting) and local clock rate, slip control logic is included in the receiver design. Under slow local clock conditions data will be deleted periodically, while under fast conditions the last output PCM data will be repeated. Octet timing is maintained during these operations. Data appearing at PCMOUT is arranged to be completely framed by the read timeslot signal and is glitch free. A two input selector at the timeslot input allows the receiver to be hard wired to two time slot positions, selectable using RTSEL.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
VIH	Logic 1	2.4			V	
VIL	Logic 0			0.4	V	
VDD	Supply	4.5		5.5	V	

DC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC = 5V +/- 10%, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
IDD	Supply Current		500		µA	
IIL	Input Leakage			1	µA	
IOL	O/P Low Current		2		mA	VOL< 0.4V
IOH	O/P High Current		2		mA	VOH> 2.4V

AC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC = 5V +/- 10%, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL						
tr, tf	Output rise/fall time		20		nS	
RECEIVER						
tRS	TS Rising Edge to RX2MHZ Set up	0		TRXL -100	nS	Figure 1
tRH	TS Falling Edge to RX2MHZ Hold	0		TRXL -100	nS	Figure 1
tDRS	PCMOUT Edge to RX2MHz Set up		10		nS	Figure 1
tDRH	PCMOUT Edge to RX2MHz Hold		10		nS	Figure 1
tPW	PCMOUT Pulse Width		488		nS	Figure 1
tRXH	RX2MHz High Time		244		nS	+/- 100ppm
tRXL	RX2MHz Low Time		244		nS	+/- 100ppm
TRANSMITTER						
tTS	TS Rising Edge to TX2MHZ Set Up	20		TTXL -100	nS	Figure 2
tTH	TS Falling Edge to TX2MHz Hold	0		TTXL -100	nS	Figure 2
tDS	PCMIN Edge to TX2MHz Set Up	100			nS	Figure 2
tDH	PCMIN Edge to TX2MHz Hold	100			nS	Figure 2
tTXH	TX2MHz High Time		244		nS	+/- 100ppm Figure 2
tTXL	TX2MHz Low Time		244		nS	+/- 100ppm Figure 2
tKXH	TX256kHz High Time		1.95		µS	+/- 100 ppm
tKXL	TX256kHz Low Time		1.95		µS	+/- 100ppm

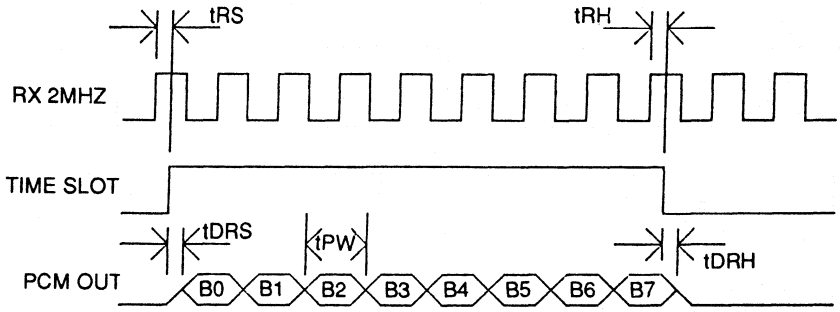


Figure 1. Receiver Time Slot Detail

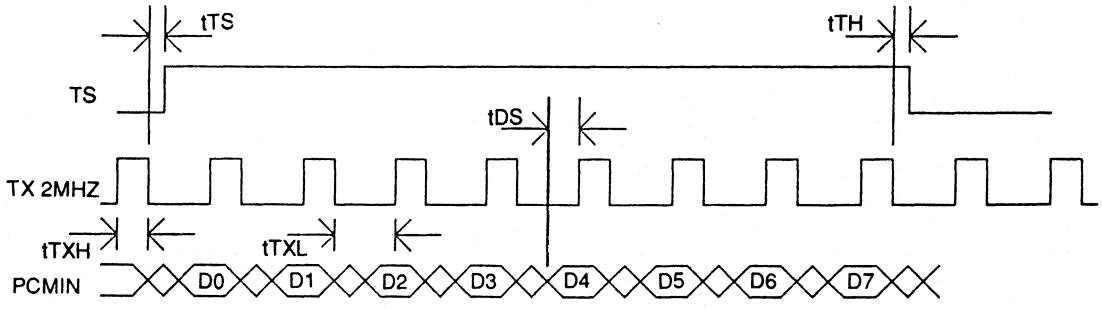


Figure 2. Transmit Time Slot

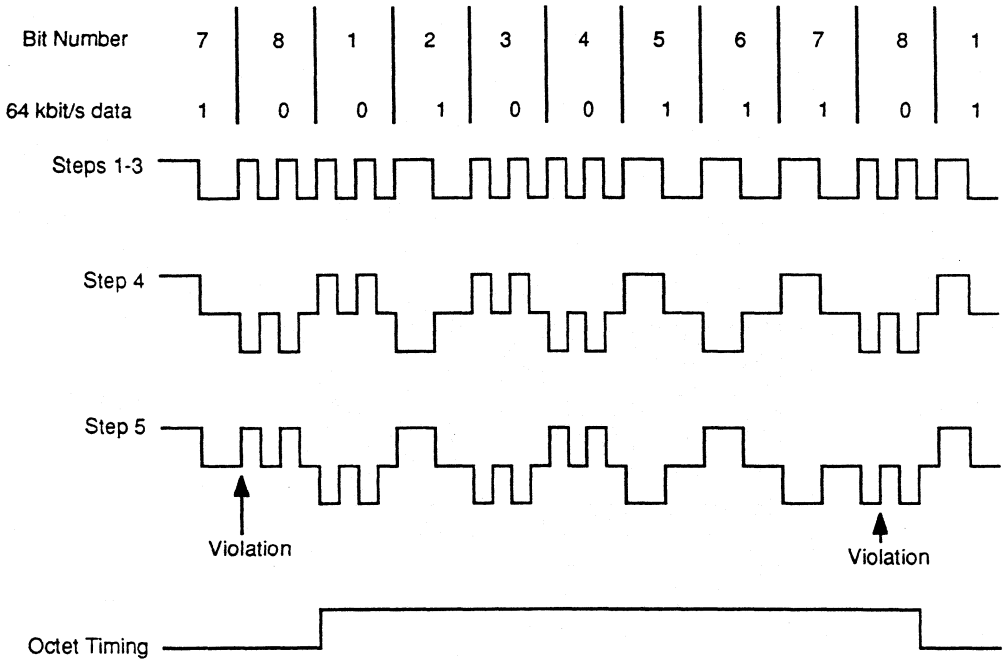


Figure 3. Transmitter Code Conversion for 64 Kbit/s Bipolar Line Signal

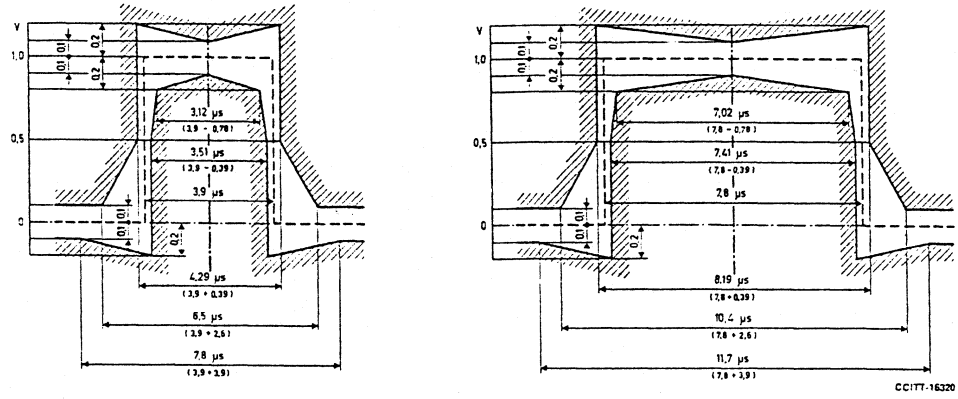


Figure 4. Pulse Masks of the 64 Kbit/s Codirectional Interface

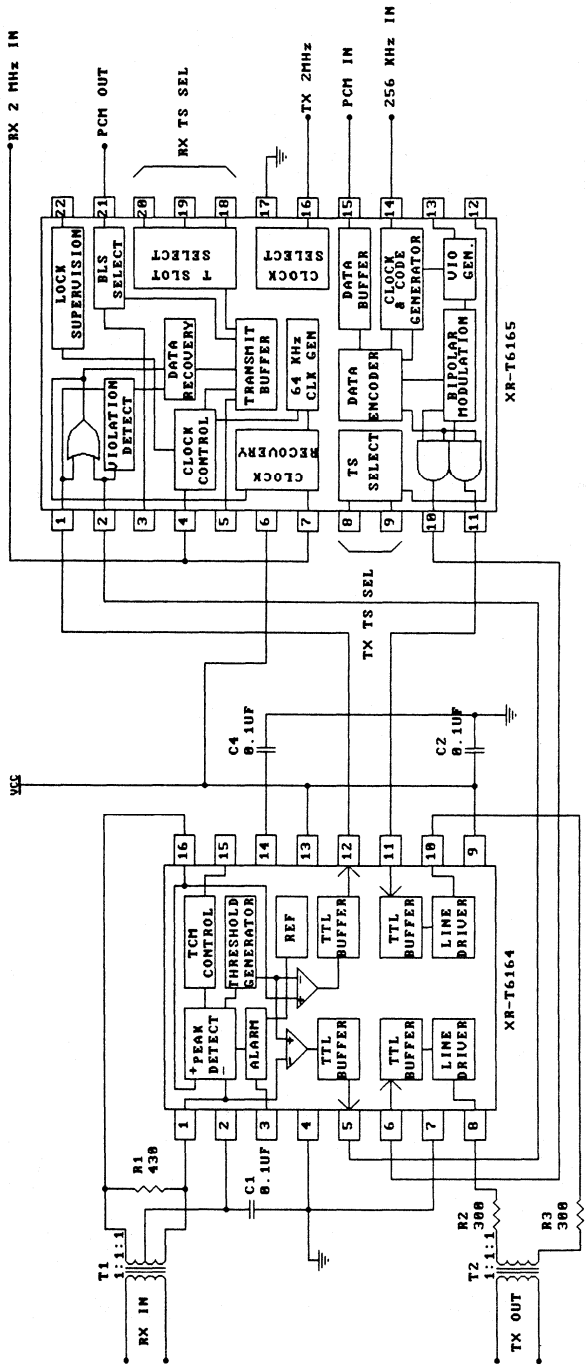


Figure 5. Typical Application Diagram For XR-T6164/65

Codirectional Digital Data Processor

GENERAL DESCRIPTION

The XR-T6166 is a digital CMOS circuit which performs the interface function betweeh a 64kbit/s data stream and a 2048kbit/s PCM timeslot data channel. When used in conjunction with the XR-T6164, the XR-T6166 conforms to CCITT G.703 specification requirements for a 64kbit/s co-directional interface.

The XR-T6166 is composed of a transmitter which transforms 8 bit 2048kbit/s timeslot data packets into a 64kbit/s data stream and a receiver which performs the reverse operation. The XR-T6166 provides additional features which allow the repetitions and deletions of both received and transmitted data as clock skews and transients occur. An extracted receive clock output is also provided together with a receive clock loss of lock flag.

FEATURES

Low Power CMOS Technology
All Receiver and Transmitter Inputs and Outputs are TTL Compatible
Up to 125µs Variance of Data Transfer Timing in Both Transmit and Receive Paths, Allowing Operation in Plesiochronous Networks

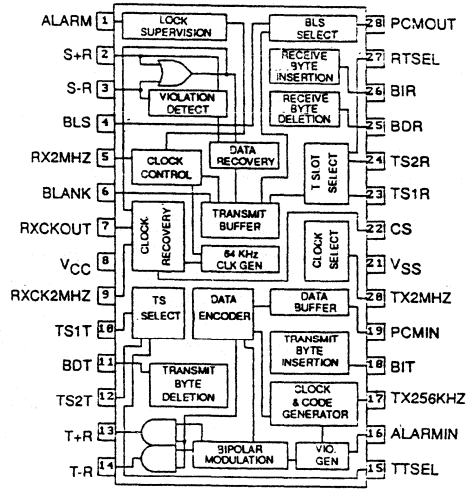
Receiver:

Converts Received Encoded 64kbit/s Data to2048kbit/s Binary Data For Insertion Into a Timeslot of a PCM Frame
Recovers Both Clock and Octet Timing. Outputs a Received Clock and Loss of Lock Signal
Performs Byte Insertion or Deletion in Response to Local Clock Slips. Provides Outputs Indicating Activity of Slip Logic
Programmable Loss of Lock Alarm (Output Inhibit/ Non-inhibit)
Glitch Free Output Data Completely Available Within Supplied Timeslot Pulse

Transmitter:

Extracts 2048kbit/s Data From a PCM Frame Time-Slot and Encodes It as 64kbit/s Data According to CCITT G.703 Requirements
Performs AMI Coding and Bipolar Violation Insertion For Octet Timing

FUNCTIONAL BLOCK DIAGRAM



Inhibits Bipolar Violation Insertion for Transmission of Alarm Conditions
Performs Byte Insertion or Deletion in Response to Local Clock Slips and Timeslot Changes. Provides Outputs Indicating Activity of Slip Logic

APPLICATIONS

When Used in Conjunction With the XR-T6164, it Forms a CCITT G.703 Compatible 64kbit/s Data Adaption Unit (DAU)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to 150°C
Operating Temperature	0°C to 70°C
Supply Voltage	4.5V to 5.5V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T6166 CN	Ceramic DIP	0°C to 70°C
XR-T6166 CP	Plastic DIP	0°C to 70°C

PIN DESCRIPTION

Name	I/O	Pin	Description
ALARM	O	1	Alarm (active high) When active, indicates loss of received bipolar violations.
S + R	I	2	Positive AMI data to receiver (active low).
S - R	I	3	Negative AMI data to receiver (active low).
BLS	I	4	Byte Locking Supervision (active low). Causes blanking of PCMOUT under received alarm conditions.
RX2MHZ	I	5	Receiver 2048kHz clock.
BLANK	I	6	PCMOUT data blanking (active high) When active, forces PCMOUT data to all ones. (AIS)
RXCKOUT	O	7	128kHz extracted clock.
VCC	I	8	+5V power supply.
RXCK2/ MHZ	I	9	2048kHz clock recovery signal.
TS1T	I	10	Timeslot input 1 for transmitter.
BDT	O	11	Transmitter data byte deletion flag (active high).
TS2T	I	12	Timeslot input 2 for transmitter.
T + R	O	13	Transmit positive output AMI data (active low).
T - R	O	14	Transmit negative output AMI data (active low).
TTSEL	I	15	Transmit timeslot select. When high, pin 8; when low, pin 9.
ALARMIN	I	16	Alarm input (active high). When active inhibits insertion flag (active high).
TX256/ KHZ	I	17	Transmitter 256kHz clock.
BIT	O	18	Transmitter data byte insertion flag (active high).
PCMIN	I	19	Transmitter PCM input.
TX2MHZ	I	20	Transmitter 2048kHz clock.
VSS	I	21	0V power supply.
CS	O	22	Clock seek (active high). Indicates loss of lock with received data.
TS1R	I	23	Timeslot input 1 for receiver.
TS2R	I	24	Timeslot input 2 for receiver.
BDR	O	25	Receive data byte deletion flag (active high).
BIR	O	26	Receive data byte insertion flag (active high).
RTSEL	I	27	Receive timeslot select. When high, pin 19; when low pin 18.
PCMOUT	O	28	Received PCM output data.

SYSTEM DESCRIPTION

Transmitter

Operation of the transmit circuit is to convert eight bit 2048kbit/s PCM timeslot data packets into coded continuous 64kbit/s data. PCM data is read into the transmitter using a 2048kHz local clock and timeslot signal. Transmission is controlled by 256kHz local clock. Four periods are dedicated to each bit in order to code "0" (0101) and "1" (0011). Timeslot is an envelope derived externally from the 2048kHz clock and covers eight clock pulses. A two input selector at the timeslot input allows the transmitter to be hard wired to two timeslot positions, selectable using TTSEL. Data is loaded to a storage buffer and transferred to an output shift register, controlled by the external 256kHz signal, only after complete transmission of previously received data. Circuitry is included to delete or repeat complete words of data should skew between the clock signals occur, or during an adjustment of the timing of the timeslot signal, for example when changing from one timeslot position to another. Octet timing is maintained during these operations. Outputs are provided to indicate when a data byte is inserted or deleted. A byte repetition just occurs once; if no new PCM data is

received, the transmitter outputs stay high. The BIT flag is active during the transmission of inserted data. The BDT flag is active when the transmitter receives extra data before transfer of the stored data byte to the output shift register. Under this condition, the stored data is overwritten. Coded data is alternately fed to two output pins to realize AMI coding, using an external transformer and two line drivers. Transmission of octet timing is performed by feeding the seventh and eighth data bits in each word to the same output. This function may be inhibited by setting ALARMIN active to transmit and alarm condition.

Receiver

Receiver operation is to take coded continuous 64kbit/s input and extract data in the form required for insertion into a 2048kbit/s PCM timeslot, under control of an external timeslot signal. A 128kHz clock is derived from the received data and used to perform decoding of the input signal. This signal is made available as the output RXCKOUT. If lock is lost with received data the clock recovery circuit enters a seek mode, increasing the speed of the internal clock to reduce the time required to regain lock. Hence, in clock seek mode the output CS is active. Bipolar violations, used to identify bit 1 in the input signal are used to synchronize circuit operation for octet timing. In the absence of violations, for example when receiving a transmitted alarm condition, the circuit will continue to operate in synchronization with respect to the last received violation. Under this condition the received signal PCMOUT (Received PCM output data) is held high indicating AIS. This function may be inhibited using BLS, and the output set to all ones if required using the BLANK input. ALARM goes high after eight consecutive violations are missed. To accommodate differences between the remote (transmitting) and local clock rate, slip control logic is included in the receiver design. Under slow local clock conditions data will be deleted periodically, while under fast conditions the last output PCM data will be repeated. Octet timing is maintained during these operations. Outputs are provided to indicate when a data byte is inserted or deleted. The BIR flag is active when PCMOUT data is a repetition of the previous data. The BDR flag is active when the receiver deletes a complete received data octet. Data appearing at PCMOUT is arranged to be completely framed by the read timeslot signal and is guaranteed glitch free. A two input multiplexer at the timeslot input allows the receiver to be hard wired at two timeslot positions, selectable using RTSEL.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYM	MIN	TYP	MAX	UNIT
Logic 1	VIH	2.4			V
Logic 0	VIL			0.4	V
Supply	VDD	4.5		5.5	V

DC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC = 5V ±5% Ta = 25°C unless otherwise specified.

PARAMETER	SYM	MIN	TYP	MAX	UNIT	CONDITION
Supply Current	IDD		100	1	µA	
Input Leakage	IIL				µA	
O/P Low Current	IOL		2		mA	VOL<0.4V\
O/P High Current	IOH		2		mA	VOH>2.4V

AC ELECTRICAL CHARACTERISTICS
PRELIMINARY Test Conditions: VCC = 5V ±10% Ta = 25°C unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL						
tr, tf	Output rise/fall time		20		nS	
RECEIVER						
tRS	TS rising edge to RX2MHz set up	0		TRXL -100	nS	Figure 5
tRH	TS falling edge to RX2MHz hold	0		TRXL -100	nS	Figure 5
tDRS	PCMOUT edge to RX2MHz set up		10		nS	Figure 5
tDRH	PCMOUT edge to RX2MHz		10		nS	Figure 5
tPW	PCMOUT pulse width		488		nS	Figure 5
tRXH	RX2MHz high time		244		nS	+/- 100 ppm
tRXL	RX2MHz low time		244		nS	+/- 100 ppm
tBDRH	BDR high time	488			nS	+/- 100 ppm
tBIRH	BIR high time		3.9		µS	
tRCKP	RXCKOUT period		7.8		µS	Figure 4
tRCKS	RXCKOUT active edge to received data edge		1.95		µS	Figure 4
TRANSMITTER						
tTS	TS rising edge to TX2MHz set up	20		TTXL -100	nS	Figure 6
tTH	TS falling edge to TX2MHz hold	0		TTXL -100	nS	Figure 6
tDS	PCMIN edge to TX2MHz set up	100			nS	Figure 6
tDH	PCMIN edge to TX2MHz hold	100			nS	Figure 6

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
tTXH	TX2MHz high time		244		nS	+/- 100 ppm Figure 6
tTXL	TX2MHz low time		244		nS	Figure 6
tKXH	TX256kHz high time		1.95		µS	+/- 100 ppm
tKXL	TX256kHz low time		1.95		µS	+/- 100 ppm
tBDTH	BDT high time	488			nS	Figure 3
tBITH	BIT high time		3.9		µS	Figure 3
tALH	ALARMIN high time	15.6			µS	Figure 3

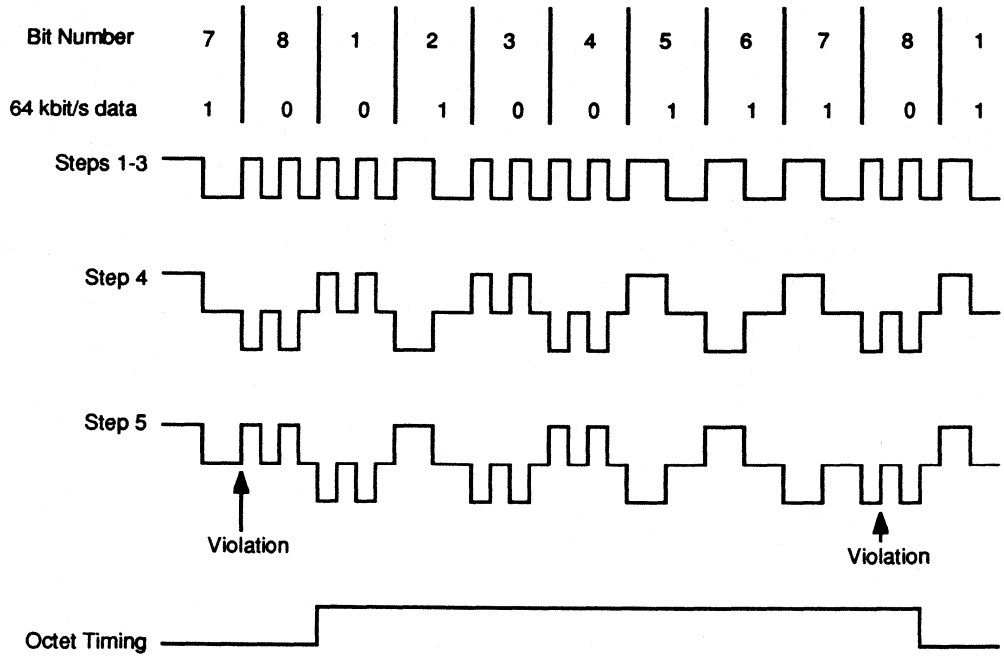


Figure 1. Transmitter Code Conversion for 64 Kbit/s Bipolar Line Signal

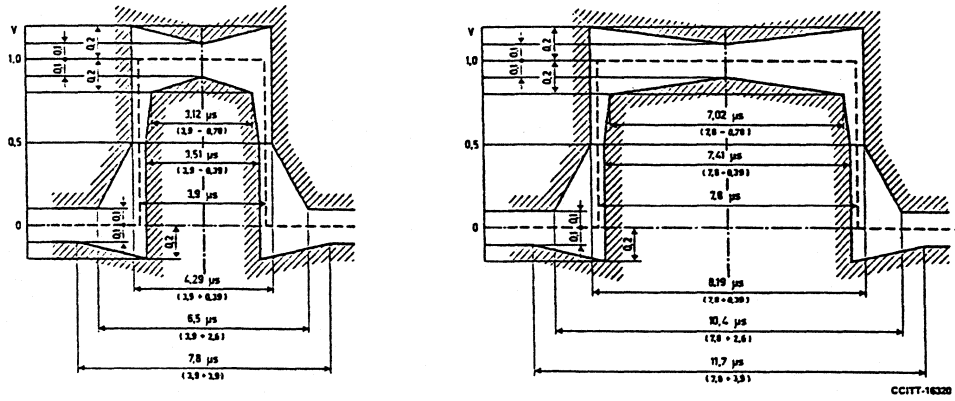


Figure 2. Pulse Masks of the 64 Kbit/s Codirectional Interface

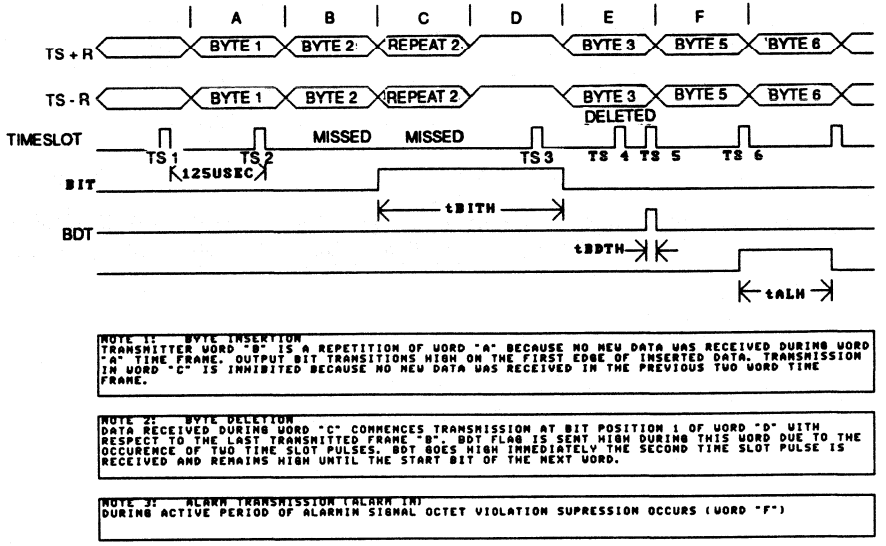


Figure 3. Transmitter Byte Insertion and Deletion

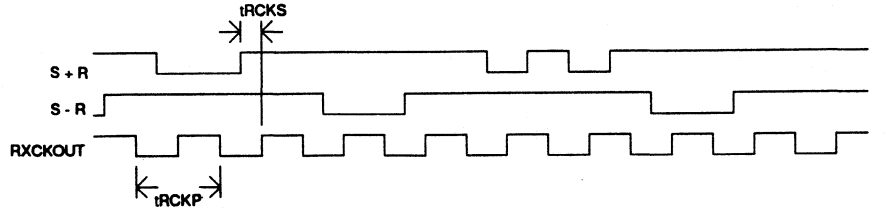


Figure 4. Extracted Clock Timing

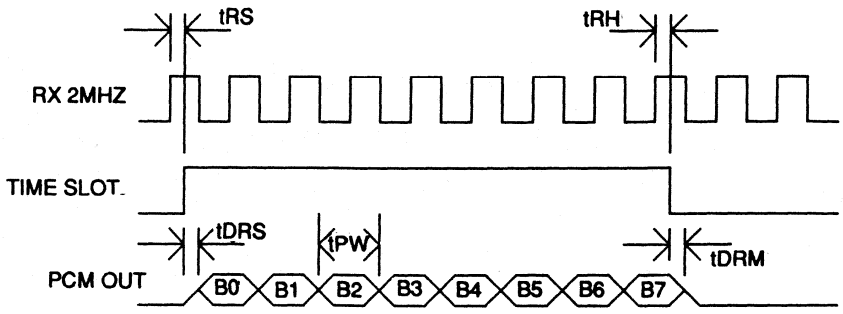


Figure 5. Receiver Time Slot Detail

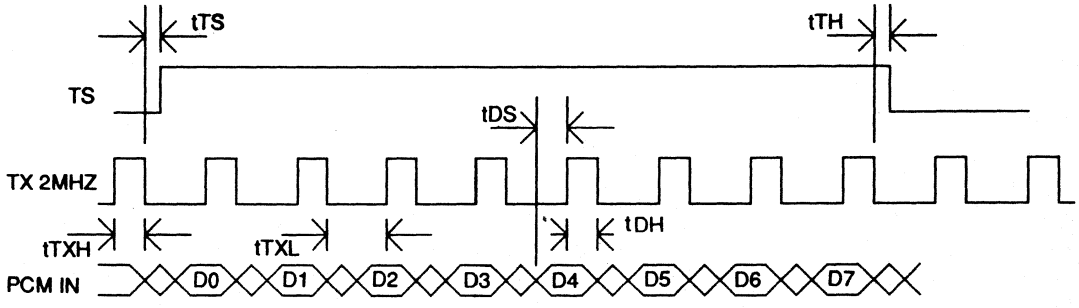


Figure 6. Transmit Time Slot

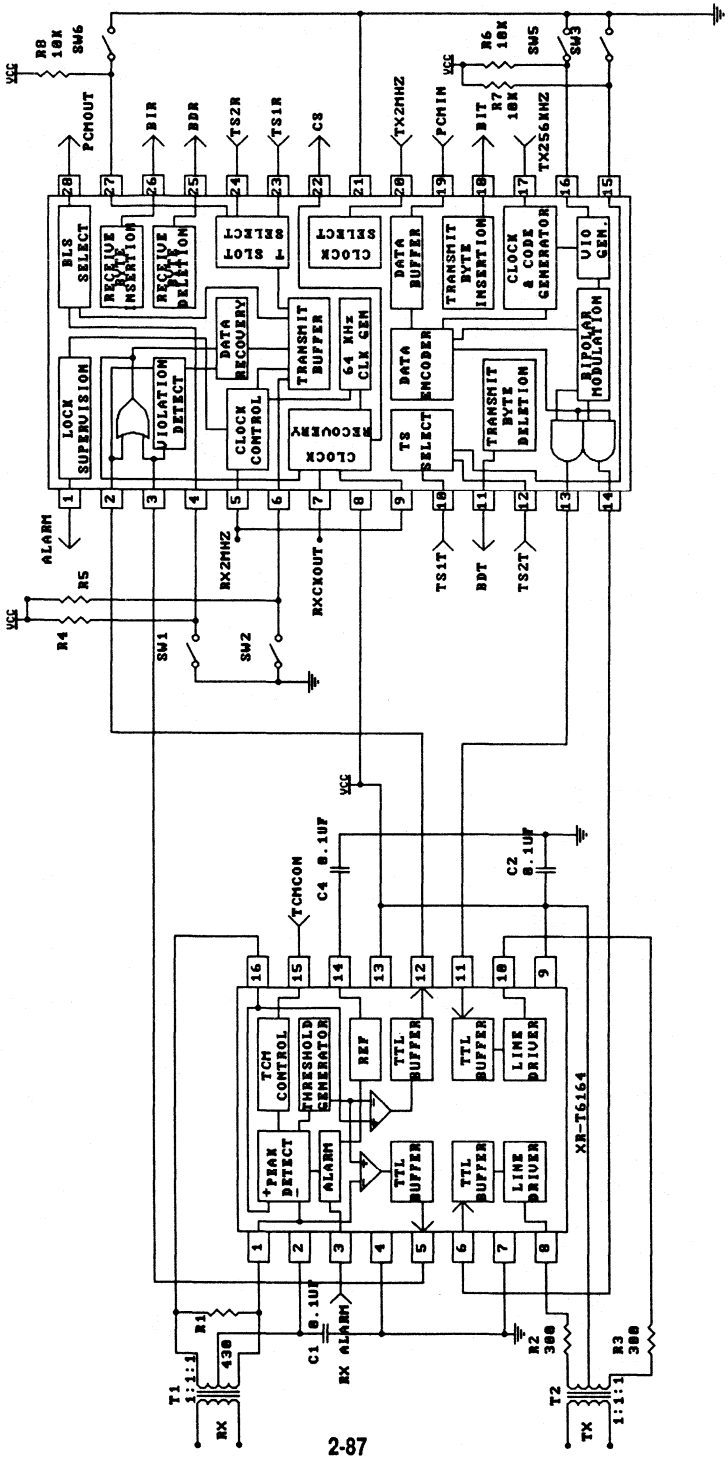
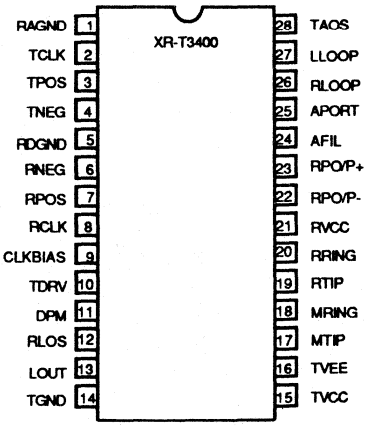


Figure 7. Block Diagram

3rd Order PCM Line Interface

GENERAL DESCRIPTION

The XR-T3400 is a third order PCM transceiver interface IC capable of operating up to 35MBPS and according to CCITT G.703 requirements. Included in this 28 pin DIP package are all the necessary transmit and receive functions plus driver and signal quality monitors. This device was primarily designed to perform the necessary physical layer interface requirements and be able to extract data signals which have been attenuated a maximum of 20db. It is powered with a dual +/-5V supply, and dissipates a maximum of 1W of power.



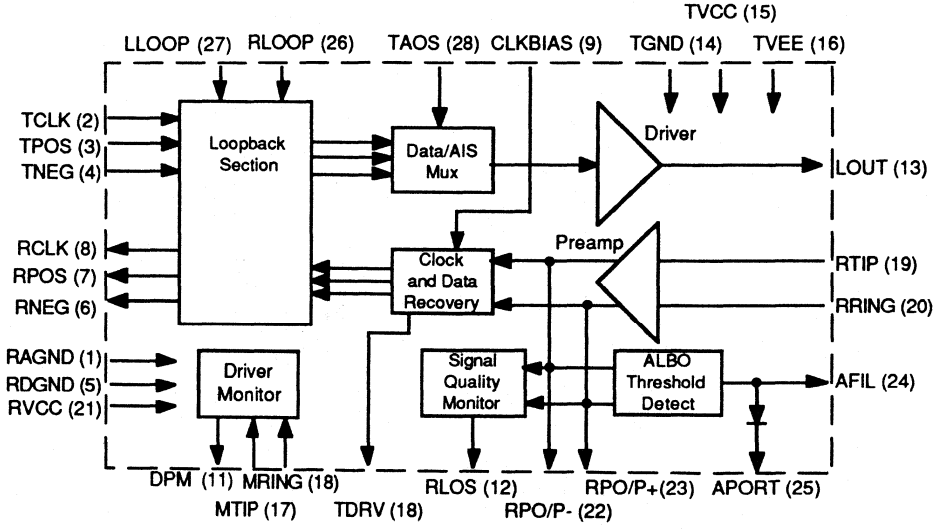
FEATURES

34MBPS CCITT G.703 Compatible Transmitter and Receiver in one IC
1 ALBO Port (20db Dynamic Range)
Diagnostic Loopback Capability
BICMOS Technology
Signal Loss Monitor
Driver Activity Monitor
CMOS Level Inputs and Outputs

APPLICATIONS

Optical Networks
Multiplexers
Cross Connects (DACS)
Digital Microwave Equipment
3rd Order Test and Measurement Equipment

FUNCTIONAL BLOCK DIAGRAM



PIN	NAME	DESCRIPTION
1	RAGND	**Receiver Analog Ground.** (0V)
2	TCLK	**Transmit Clock.** Typically 34.368 MHz with a 50% +/-1%
3	TPOS	**Transmit Positive Data.** High level indicates a positive pulse is to be transmitted over the line.
4	TNEG	**Transmit Negative Data.** High level indicates a negative pulse is to be transmitted over the line.
5	RDGND	**Receiver Digital Ground.** (0V)
6	RNEG	**Receiver Negative Data.** A positive signal on this pin corresponds to a negative signal received on RRING. Data transition occurs at rising edge of recovered clock.
7	RPOS	**Receiver Positive Data.** A positive signal on this pin corresponds to a positive signal received on RTIP. Data transition occurs at rising edge of recovered clock.
8	RCLK	**Receive Clock.** Derived from the incoming data.
9	CLKBIAS	**Clock Bias Voltage.** Supplies bias voltage to clock amplifier.
10	TDRV	**Tank Drive.** Tank pulse current.
11	DPM	**Driver Performance Monitor.** (active high) Output dedicated to indicate transmitter failure in case no signals are present on pins MTIP and MRING.
12	RLOS	**Receiver Loss of Signal.** (active high) Goes high when the receive input level falls below 100mV (peak). RPOS, RNEG and RCLK are all set low.
13	LOUT	**Line Output.** Transmitter line driver output pin.
14	TGND	**Transmitter Ground.** (0V)

PIN	NAME	DESCRIPTION
15	TVCC	**Transmitter Positive Supply Voltage.** (+5V +/-5%)
16	TVEE	**Transmitter Negative Supply Voltage.** (-5V +/-5%)
17	MTIP	**Driver Monitor Input.** (TIP) This input connects to the transmitter output for monitoring purpose.
18	MRING	**Driver Monitor Input.** (RING) This input connects to the transmitter output for monitoring purpose.
19	RTIP	**Receiver Line Signal Input.** Connects to the receive transformer input. (TIP)
20	RRING	**Receiver Line Signal Input.** Connects to the receiver transformer input. (RING).
21	RVCC	**Receiver Positive Supply.** (5V +/-5%)
22	RPO/P-	**Receiver Preamplifier Negative Output.**
23	RPO/P+	**Receiver Preamplifier Positive Output.**
24	ALIF	**ALCO Filter.** Control pin for ALBO ports. Voltage developed across a capacitor on this pin defines ALBO on impedance.
25	APORT	**ALBO Port.** Impedance at this pin varies as input signal changes.
26	RLOOP	**Remote Loopback.** (active high) When set, the recovered clock and data are routed back to the line through LOUT> Local TCLK, TPOS and TNEG are ignored.
27	LLOOP	**Local Loopback.** (active high) When set, the TPOS, TNEG and TCLK are connected to RPOS, RNEG and RCLK. Receive information is ignored and transmit information is sent out on the line.

PIN	NAME	DESCRIPTION
28	TAOS	**Transmit ALL Ones.** (active high) When selected, a bipolar all ones is transmitted on the line using TCLK.

SYSTEM DESCRIPTION

The two main functions of the circuit interface IC are the receive and transmit sections. The transmit and receive sections have separate power supplies to minimize crosstalk problems.

Receiver Section

On the receive path, the XR-T3400 amplifies and reconstructs the incoming bipolar signals and outputs synchronized CMOS compatible data and clock. Included in this path is a preamplifier and ALBO (Automatic Line Build Out) circuitry, which acts as a variable cable or fiber simulator (AGC circuit). The amplitude and frequency equalization is achieved through the variable impedance of the ALBO parts and associated network. The minimum input signal amplitude is 120 mV. When the amplitude of the input signal falls below 100mV, a loss of signal shall be set high at RLOS. This will also result in a low state of the data and clock outputs.

Following the preamplifier and ALBO section are a set of data and clock threshold detectors. The receiver clock is generated by a tank circuit tuned to 34.368 MHz. A PLL clock recovery system is under development.

Transmit Section

The transmitter section is designed to take unipolar NRZ (TTL/CMOS compatible) data encoded as TPOS and TNEG and produce alternate bipolar pulses with the appropriate pulse shape. This data pulses need to be asynchronous with a 34.368MHz clock whose negative going edge transitions occur at the center of the data. The bipolar output can be either capacitor or transformer coupled to the line for transmission. To prevent reflections on the line, a 75 ohm external resistor is used for line impedance matching.

As part of the transmitter, the driver monitor section is able to monitor the transmitted signal and give an early warning signal in case of malfunctioning of a line driver. This section consists of a counter that checks the transmitted signal on the input pins MTIP and MRING. If no signals are present on these input pins for 32 cycles of TCLK, DPM (Drive Performance Monitor) goes high.

Loopback Control

There are two loopback options included in the XR-T3400:

The local loopback when enabled bypasses the receive circuit and routes the digital transmit clock and data to the receive clock and data pins. The transmit data (TPOS and TNEG) are sent out on the line through LOUT unless transmit all ones, TAOS, is selected, in which case a bipolar all ones are transmitted on the line using TCLK.

In remote loopback, the recovered clock and data are routed back to the line through LOUT, any signal on TCLK, TPOS and TNEG shall be ignored. Setting remote loopback overrides TAOS requests. Simultaneous selection of local and remote loopback is not allowed.

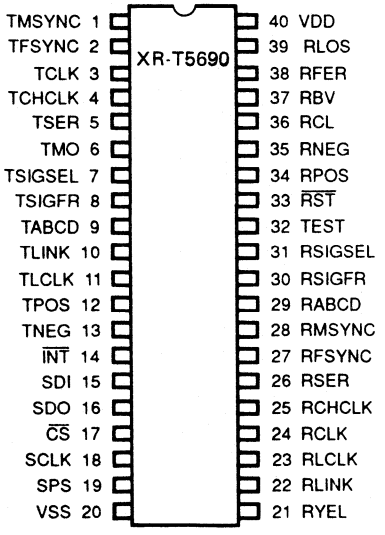
T1/ISDN Primary Rate Framer

GENERAL DESCRIPTION

The XR-T5690 is a monolithic CMOS IC designed to implement primary rate PCM (1.544 MHz) T-Carrier transmitter and receiver functions. It supports 193S framing (12 frame per superframe) and also 193E framing which is the extended superframe format (24 frames per superframe). Clear channel capability is provided by selection of appropriate zero suppression and signaling modes.

FEATURES

Single +5 V Supply
Low Power CMOS Digital Technology
Single Chip DS1 Rate Transceiver
Supports 12 Frames per Superframe and 24 Frames per Superframe
B8ZS, B7 Stuffing and Transparent Zero Suppression Modes
No Host Processor for Hardware Mode
Supports Host Processor for Serial Data Transmission
Selectable 0, 2, 4, 16 State Robbed Bit Signaling Mode
Allows Mix of "CLEAR" and "NON CLEAR" DS0 Channels on the same DS1 Link
Alarm Generation and Detection
Receive Error Detection and Counting for Transmission Performance Monitoring
Pin to Pin and Functionally Compatible with DS2180A



APPLICATIONS

Digital Multiplexers
Channel Banks

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7 Volts
Storage Temperature	-65° C to 150° C

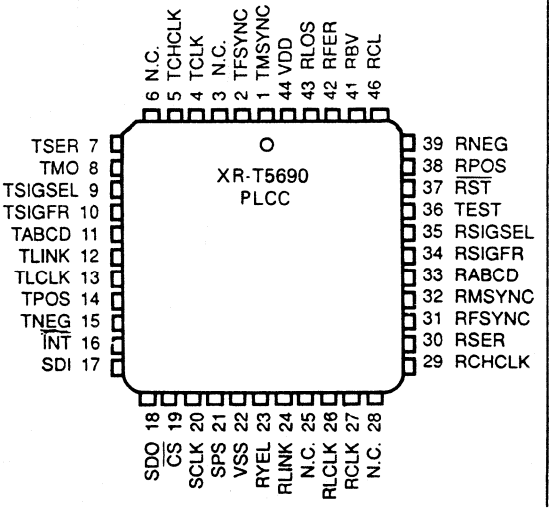
ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-T5690CP	Plastic DIP	0° C to 70° C
XR-T5690CJ	PLCC	0° C to 70° C
XR-T5690IP	Plastic DIP	-40°C to 85°C
XR-T5690IJ	PLCC	-40°C to 85°C

SYSTEM DESCRIPTION

Transmitter Section

The XR-T5690 is compatible with the existing BELL system D4 (193S) framing standard described in ATT

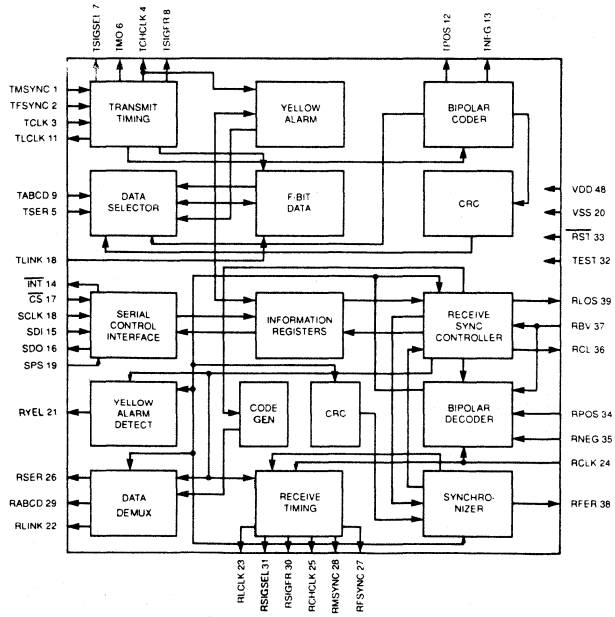


PUB 43801 and new extended superframe format (193E) as described in ATT C.B. #142. Programmable features of the XR-T5690 allows support of other framing standards which are derivatives of 193S and 193E. The salient differences between the 193S and 193E formats are the number of frames per superframe and use of the F-bit position. In 193S, 12 frames make up a superframe as opposed to 24 frames in 193E mode. Each frame consists of 24 channels of 8 bit data transmitted and received MSB first and preceded by an F-bit.

The transmit side of the XR-T5690 is made up of 6 major functional blocks: timing and clock generation, data selector, bipolar coder, yellow alarm, F-bit data and CRC block. The timing and clock generation circuit develops all on board and output system clocks from its inputs TCLK (Transmit Clock), TFSYNC (Transmit Frame Sync) and TMSYNC (Transmit Multiframe Sync). The yellow alarm circuitry generates mode dependent yellow alarms which is a repeating pattern of FF(hex) and 00(hex) on the 4KHz Facility Data Link (FDL). The CRC block generates checksum results utilized in 193E framing and the F-bit data provides mode dependent framing patterns which allow insertion of link or S-bit data externally. All of these blocks feed into the data selector, where it is possible to modify the outgoing data stream by bit selection and insertion of the transmit registers (CCR, TCR, TIR and TTR). The bipolar coder formats the output of the data selector, supports on board loopback features and inserts zero suppression codes to make it compatible with bipolar transmission techniques.

RECEIVER SECTION

The heart of the receiver is the synchronizer and sync monitor. This circuit serves two purposes: (A) that of monitoring the incoming data stream for loss of frame or multiframe alignment, and (B) searching for new frame alignment pattern when sync loss is detected. When sync loss is detected, the synchronizer begins an off line search for the new alignment. Whenever this occurs, all output timing signals remain at the old alignment with the exception of RSIGFR (Receive Signaling Frame), which is forced low during resync. At the instant a valid sequence is detected, the output timing will move to the new alignment at the beginning of the next multiframe. One frame later, RLOS (Receive Loss of Sync) will transition low, indicating valid sync and the resumption to the normal sync monitoring mode. Several bits in the RCR (Receive Control Register) allow tailoring of the resync algorithm by the user.



FUNCTIONAL BLOCK DIAGRAM

DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{DD} = 5V+/-5%, unless otherwise specified.

MODEL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{DD}	Supply Current		3		mA	Note1,2
I_L	Input Leakage			1	µA	
I_{LO}	Output Leakage			1	µA	Note 3
I_{OH}	Output Current @2.4V			+1	mA	Note 4
I_{OL}	Output Current @0.4V	-4			mA	Note 5
C_{IN}	Input Capacitance		5		pF	
C_{OUT}	Output Capacitance		7		pF	
V_{IH}	Logic 1	2		VDD +0.3	V	
V_{IL}	Logic 0	-0.3		+0.8	V	

Notes: 1. TCLK = RCLK = 1.544 MHz
2. Outputs Open
3. Applies to SDO when tristated
4. All outputs except $\overline{INT}$, which is open collector
5. All outputs

AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{DD} = 5V+/-5%, unless otherwise specified.

Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.

MODEL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
t_{DC}	SDI to SCLK Set-up	50			ns	
t_{CDH}	SCLK to SDI Hold	50			ns	
t_{CD}	SDI to SCLK	50			ns	
t_{CL}	SCLK Low Time	250			ns	
t_{CH}	SCLK High Time	250			ns	
t_R, t_F	SCLK Rise & Fall			500	ns	
t_{CC}	$\overline{CS}$ to SCLK Set Up	50			ns	
t_{CCH}	SCLK to $\overline{CS}$ Hold	50			ns	
t_{CWH}	$\overline{CS}$ Inactive Time	250			ns	
t_{CDV}	SCLK to SDO Valid			200	ns	Note 1
t_{CDZ}	$\overline{CS}$ to SDO High Z			75	ns	

Notes: 1. Output load capacitance = 100pF

AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{DD} = 5V ± 5%, unless otherwise specified.

TRANSMITTER

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
t_P	TLCK		648		ns	
t_{WL},t_{WH}	TCLK Pulse Width		324		ns	
t_F,t_R	TCLK,RCLK Rise/Fall		20		ns	
t_{STD}	TSER,TABCD Set Up to TCLK Falling	50			ns	
t_{HTD}	TSER,TABCD Hold to TCLK Rising	50			ns	
t_{STL}	TLINK Set Up to TCLK Rising	50			ns	
t_{HTL}	TLINK Hold to TCLK Rising	50			ns	
t_{STS}	TFSYNC,TMSYNC Set Up to TCLK Rising	125			ns	
t_{FTS}	Propagation Delay TFSYNC to TMO, TSIGSEL,TSIGFR,TLCLK			75	ns	
t_{PTCH}	Propagation Delay TCLK to TCHCLK			75	ns	
t_{SP}	TFSYNC,TMSYNC Pulse Width	100			ns	

RECEIVER

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
t_{PRS}	Propagation Delay RCLK to RMSYNC, RFSYNC, RLCLK RSIGSEL, RSIGFR, RCHCLK			75	ns	
t_{PRD}	Propagation Delay RCLK to RSER, RABCD, RLINK			75	ns	
t_{TTR}	Transition Time All Outputs			20	ns	
t_P	RCLK Period		648		ns	
t_{WL},t_{WH}	RCLK Pulse Width		324		ns	
t_F,t_R	RCLK Rise and Fall		20		ns	
t_{PRA}	Propagation Delay RCLK to RYEL, RCL, RFER, RLOS RBV			75	ns	
t_{RST}	RESET Pulse Width	1			µs	

PIN DESCRIPTION

Pin	Symbol	Description
1	TMSYNC	**Transmit Multiframe Sync:** May be pulsed high at multiframe boundaries to reinforce multiframe alignment, or tied low, which allows internal multiframe counter to free run.
2	TFSYNC	**Transmit Frame Sync:** Rising edge indentifies frame boundary, may be pulsed every frame to reinforce internal frame counter, or tied low (allowing TMSYNC to establish frame and multiframe alignment).
3	TCLK	**Transmit Clock:** 1.544 MHz primary clock
4	TCHCLK	**Transmit Channel Clock:** 192 KHz clock which identifies time slot boundaries. For parallel to serial conversion of channel data.
5	TSR	**Transmit Serial Data:** NRZ data input, sampled on falling edge of TCLK.
6	TMO	**Transmit Multiframe Out:** Output of internal multiframe counter, indicated multiframe boundaries. 50% duty cycle.
7	TSIGSEL	**Transmit Signaling Select:** 667 Hz clock which identified signaling frames A and C in 193E framing. 1.33 KHz clock in 193S.
8	TSIGFR	**Transmit Signaling Frame:** High during signaling frames, low otherwise.
9	TABCD	**Transmit ABCD Signaling:** When enabled via TCR(bit-4), sampled during channel LSB time in signaling frames on falling edge of TCLK.
10	TLINK	**Transmit Link Data:** Sampled during the F-bit time (falling edge of TCLK) of odd frames for insertion into the outgoing data stream (193E-FDL insertion). Sampled during the F-bit time of even frames for insertion into the outgoing data (193S-External S-bit insertion).
11	TLCLK	**Transmit Link Clock:** 4 KHz demand clock for TLINK input.
12	TPOS	**Transmit Bipolar +D Data Output.**
13	TNEG	**Transmit Bipolar -D Data Output.**
14	$\overline{INT}$	**Receive Alarm Interrupt:** Flags host controller during alarm conditions. Active low, open drain output.
15	SDI	**Serial Data In:** Data for on-board registers. Sampled on the rising edge of SCLK.
16	SDO	**Serial Data Out:** Control and status information from on-board registers. Updated on falling edge of SCLK, and tristated during serial port write or when $\overline{CS}$ is high.
17	$\overline{CS}$	**Chip Enable:** Active low during read or write operation from or to serial port.
18	SCLK	**Serial Data Clock:** Used to read or write the serial port registers.
19	SPS	**Serial Port Select:** When tied to VDD, serial port is selected. On-board mode is selected, when it is tied to VSS.

Pin	Symbol	Description
20	VSS	**Ground**
21	RYEL	**Receive Yellow Alarm:** Transitions high when yellow alarm is detected; goes low when alarm clears.
22	RLINK	**Receiver Link Data:** Updated with extracted FDL data one RCLK before start of odd frames (193E) and held until next update. Updated with extracted S-bit data one RCLK before start of even frames (193S) and held until next update.
23	RLCLK	**Receive Link Clock:** 4 KHz demand clock for RLINK.
24	RCLK	**Receive Clock:** 1.544 MHz primary clock.
25	RCHCLK	**Receive Channel Clock:** 192 KHz clock, identifies time slot (channel) boundaries.
26	RSER	**Receive Serial Data:** Received NRZ serial data, updated on rising edges of RCLK.
27	RFSYNC	**Receive Frame Sync:** Extracted 8 KHz clock, one RCLK wide, indicates F-bit position in each frame.
28	RMSYNC	**Receive Multiframe Sync:** Extracted multiframe sync; edge indicates start of multiframe, 50% duty cycle.
29	RABCD	**Receive ABCD Signaling:** Extracted signaling data output valid for each channel time in signaling frames. In non signaling frames, RABCD outputs the LSB of each channel word.
30	SIGFR	**Receive Signaling Frames:** High during signaling frames, low during resync and non signaling frames.
31	RSIGSEL	**Receive Signaling Select:** In 193E framing a 667 Hz clock which identifies signaling frames A and C. A 1.33 KHz clock in 193S.
32	TEST	**Test Mode:** Tie to VSS for normal operation.
33	$\overline{\text{RST}}$	**Reset:** A high to low transition clears all internal registers and resets receive side counters. A high to low to high transition will initiate a receive resync.
34	RPOS	**Receive Bipolar +D Data Input:** Sampled on falling edge of RCLK.
35	RNEG	**Receive Bipolar -D Data Input:** Sampled on falling edge of RCLK. Tie RPOS and RNEG together to receive NRZ data and disable bipolar violation monitoring circuitry.
36	RCL	**Receive Carrier Loss:** High if 32 consecutive "0's" appear at RPOS and RNEG, goes low after next "1".
37	RBV	**Receive Bipolar Violation:** High during accused bit time at RSER if bipolar violation detected, low otherwise.
38	RFER	**Receive Frame Error:** High during F bit time when F_T, or Fs error (193S), or when FPS or CRC errors occur (193E). low during resync.
39	RLOS	**Receive Loss Sync:** Indicates sync status; high when internal resync is in progress, low otherwise.
40	VDD	**Positive Supply Voltage.**

REGISTER ADDRESS SUMMARY

Register	Address	T/R[1]	Function
RSR	0000	R*	Receive Status Register
RIMR	0001	R	Receive Interrupt Mask Register
BVCR	0010	R	Receive Bipolar Violation Count Register
ECR	0011	R	Error Count Register
CCR	0100	T/R	Common Control Register
RCR	0101	R	Receive Control Register
TCR	0110	T	Transmit Control Register
TIR1	0111	T	Transmit Idle Register 1
TIR2	1000	T	Transmit Idle Register 2
TIR3	1001	T	Transmit Idle Register 3
TTR1	1010	T	Transmit Transparent Register 1
TTR2	1011	T	Transmit Transparent Register 2
TTR3	1100	T	Transmit Transparent Register 3
RMR1	1101	R	Receive Mark Register 1
RMR2	1110	R	Receive Mark Register 2
RMR3	1111	R	Receive Mark Register 3

[1]Transmit or receive side register
* Read only register

REGISTER DESCRIPTION

RECEIVE STATUS REGISTER (RSR)

Reports all receive alarm conditions

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

Symbol	Bit #	Description
BVCS	RSR.7	**Bipolar Violation Count Saturation:** Set when the 8 bit counter at BVCR saturates.
ECS	RSR.6	**Error Count Saturation:** Set when either of the 4 bit counters at ECR saturates.
RYEL	RSR.5	**Receive Yellow Alarm:** Set when yellow alarm detected. (Detected yellow alarm format determined by CCR bit-4 and CCR bit-3).
RCL	RSR.4	**Receive Carrier Loss:** Set when 32 consecutive "0's" appears at RPOS and RNEG.
FERR	RSR.3	**Frame Bit Error:** Set when Ft (193S) or FPs (193E) bit error occurs.
B8ZSD	RSR.2	**Change of Frame Alignment Set via CCR.6:** When CCR.6=0; detected B8ZS code word is reported at RSR.2. When CCR.6=1; COFA (Change of frame alignment) is reported when last resync resulted in change of frame or multi-frame alignment.
RBL	RSR.1	**Receive Blue Alarm:** Set when 2 consecutive frames have less than 3 zeros in the data stream.
RLOS	RSR.0	**Receive Loss Sync:** Set when resync is in process; if RCR bit-1=0, RLOS transitions high on an OOF event or carrier loss, indicating auto resync.

RECEIVE INTERRUPT MASK REGISTER (RIMR)

Allows masking of individual alarm generated interupts

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

BVCS	RIMR.7	**Bipolar Violation Count Saturation Mask:** 1=interrupt enabled 0=interrupt disabled (masked)
ECS	RIMR.6	**Error Count Saturation Mask:** 1=interrupt enabled 0=interrupt disabled (masked)
RYEL	RIMR.5	**Receive Yellow Alarm Mask:** 1=interrupt enabled 0=interrupt disabled (masked)
RCL	RIMR.4	**Receive Carrier Loss Mask:** 1=interrupt enabled 0=interrupt disabled (masked)
FERR	RIMR.3	**Frame Bit Error Mask:** 1=interrupt enabled 0=interrupt disabled (masked)
B8ZSD	RIMR.2	**B8ZS Detect Mask:** 1=interrupt enabled 0=interrupt disabled (masked)
RBL	RIMR.1	**Receive Blue Alarm Mask:** 1=interrupt enabled 0=interrupt disabled (masked)
RLOS	RIMR.0	**Receive Loss Of Sync Mask:** 1=interrupt enabled 0=interrupt disabled (masked)

BIPOLAR VIOLATION COUNT REGISTER (BVCR)
This is an 8 bit presetable counter which records individual bipolar violations.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BVD7	BVD6	BVD5	BVD4	BVD3	BVD2	BVD1	BVD0

BVD BVCR.7 **MSB of Bipolar Violation Count**

BVD0 BVCR.0 **LSB of Bipolar Violation**

ERROR COUNT REGISTER (ECR)
There are 2 independent 4 bit counters which record out-of-frame occurences and CRC (Cyclic Redundancy Check) errors.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00F3	00F2	00F1	00F0	ESF3	ESF2	ESF1	ESF0

OOFD3 ECR.7 **MSB of OOF Event Count**

OOFD0 ECR.4 **LSB of OOF Event Count**

ESFD3 ECR.3 **MSB of Extended Superframe Error Count**

ESFD0 ECR.0 **LSB of Extended Superframe Error Count**

COMMON CONTROL REGISTER (CCR)
Selects device operating characteristics common to receive and transmit sides.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	B8ZSC	EFYA	FM	YELMD	B8ZS	B7	LPBK

0 CCR.7 This bit must be zero for proper operation.

B8ZSC CCR.6 **B8ZS/Change of Frame Report:**
0= detected B8ZS code word is reported at RSR.2
1= detected change of frame or multiframe alignment after last resync is reported at RSR.2

EFYA CCR.5 **193E Yellow Alarm Mode Select:**
0= Yellow alarm is a repeating pattern set of 00 hex and FF hex.
1= Yellow alarm is a "0" in the bit 2 position of all channels.

FM CCR.4 **Frame Mode Select:**
0=193S, 12 frame/superframe
1=193E, 24 frame/superframe

YELMD CCR.3 **193S Yellow Alarm Mode Select:**
Determines yellow alarm type to be transmitted and detected while in 193S framing. If set, yellow alarms are a "1" in the S-bit position of frame 12; if cleared, yellow alarm is a "0" in bit-2 of all channels. Does not affect 193E yellow alarm operation.

B8ZS CCR.2 **Bipolar Eight Zero Substitution:**
0=Disable B8ZS
1=Enable B8ZS

B7 CCR.1 **Bit Seven Zero Suppression:**
If CCR bit-1=1, channels with an all zero content will be transmitted with bit-7 forced to "1". If CCR bit-1=0, no bit-7 stuffing occurs.

LPBK CCR.0 **Loop Back:**
When enabled, the device internally loops output transmit data into the incomming receive data buffers and TCLK is internally substituted for RCLK.

RECEIVE CONTROL REGISTER (RCR)
Programs device operating characteristics unique to the receive side.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ARC	00FC	RCI	RCS	SYNCC	SYNCT	SYNCE	RESYNC

ARC RCR.7 **Auto Resync Criteria:**
0=Resync on 00F or RCL event
1= Resync on 00F only

00FC RCR.6 **Out-of-Frame Condition Detected:**
0= 2 of 4 framing bits in error
1= 2 of 5 framing bits in error

RCI RCR.5 **Receive Code Insert:**
When set, the receive code selected by RCR.4 is inserted into channels marked by RMR registers. If clear, no code is inserted.

RCS RCR.4 **Receive Code Selection:**
0=idle code (7F HEX)
1=digital milliwatt

SYNCC RCR.3 **Sync Criteria:**
Determines the type of algorithm utilized by the receiver synchronizer and differs for each frame mode.

193S Framing (CCR.4=0)
0=Synchronize to frame boundaries using F_T pattern, then search for multiframe by using F_S.
1=Cross couple F_T and F_S patterns in sync algorithm.

193E Framing (CCR.4=1)
0=Normal sync. (Fps only)
1=Validate new alignment with CRC before declaring sync.

SYNCT RCR.2 **Sync Time:**
If set, 24 consecutive F-bits of the framing pattern must be qualified before sync is declared. If clear, 10 bits are qualified.

SYNCE RCR.1 **Sync Enable:**
If clear, the transceiver will automatically begin a resync if 2 of the previous 4 framing bits were in error, or if carrier loss is detected. If set, no auto resync occurs.

RESYNC RCR.0 **Resync:**
When toggled low to high, the transceiver will initiate resync immediately. The bit must be cleared, then set again for subsequent resyncs.

TRANSMIT CONTROL REGISTER (TCR)
selects additional transmit side modes.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ODF	FTPT	TCP	RBSE	TIS	193SI	TBL	TYEL

0DF TCR.7 **Output Data Format:**
0= Bipolar data at TPOS & TNEG
1= NRZ data at TPOS; TNEG = 0

FTPT TCR.6 **FT/FPS Pass Through:**
0= FT/FPS sourced internally
1= FT/FPS sampled at TSER during F-bit time

TCP TCR.5 **Transmit CRC Pass-Through:**
0= transmit CRC code internally generated.
1= TSER sampled at CRC F-bit time for external CRC insertion

RBSE TCR.4 **Robbed Bit Signaling Enable:**
1= Signaling inserted in all channels during signaling frames.
0= No signaling inserted. (The TTR registers allow the user to disable signaling insertion on selected DSO channels.)

TIS	TCR.3	**Transmit Idle Code Selection:** Determines idle code format to be inserted into channels marked by the TIR registers. 0=insert 7F (hex) into marked channels. 1=insert FF (hex) into marked channels.
TIS	TCR.2	**193S S-Bit Insertion:** Determines source of transmitted S- bit. 0=internal S-bit generator 1=external
193SI	TCR.1	**Transmit Blue Alarm:** 0=disabled 1=enabled
TYEL	TCR.0	**Transmit Yellow Alarm:** 0=disabled 1=enabled

TRANSMIT IDLE REGISTERS (TIR1-TIR3)

Each of these bit positions represents a DS0 channel in the outgoing frame. When set, the corresponding channel will output an idle code format determined by TCR bit-3.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

CH24	TIR3.7	**Channel 24 Transmit Idle Register**
CH1	TIR1.0	**Channel 1 Transmit Idle Register**

TRANSMIT TRANSPARENCY REGISTERS (TTR1-TTR3)

Each of these bit positions represents a DS0 channel in the outgoing frame. When set the corresponding channel is transparent.

TTR1	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

TTR2	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9

TTR3	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

CH24	TTR.3.7	**Channel 24 Transmit Transparent Register**
CH1	TTR1.0	**Channel 1 Transmit Transparent Register**

RECEIVE MARK REGISTERS (RMR)

Each of these bit positions represents a DS0 channel in the incoming T1 frame. When set the corresponding channel will output codes determined by RCR bit-4 and RCR bit-5.

RMR1	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

RMR2	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9

RMR3	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

CH24	RMR3.7	**Channel 24 Receive Mark Register**
CH1	RMR1.0	**Channel 1 Recieve Mark Register**

GLOSSARY

GENERAL FUNCTIONS

LINE CODING

T1 line data is transmitted in a bipolar alternative mark inverted line format; ones are transmitted as alternating negative and positive pulses and zeros are simply the absence of pulses. This technique minimizes DC voltage on the T1 span and allows clock to be extracted from data. The network currently has a one's density constraint to keep clock extraction circuitry functioning, which is usually met by forcing bit-7 of any channel consisting of all 0's to 1. The use of bipolar eight zero substitution (B8ZS) satisfies the one's density requirement, while allowing data traffic to be transmitted without corruption. This feature is known as clear channel and is explained more completely in ATT C.B. #144. When the B8ZS feature is enabled, any outgoing stream of eight consecutive zeros is replaced with a B8ZS code word. If the last "1" transmitted was positive, the inserted code is 0 0 0 + - 0 - +; if negative, the code word inserted is 0 0 0 - + 0 + -. Bipolar violations occur in the fourth and seventh bit positions, which are ignored by the XR-T5690 error monitoring logic when B8ZS is enabled. Any received B8ZS code word is replaced with all "0's" if B8ZS is enabled. Also, the receiver status register will report any occurrence of B8ZS code words to the host controller. This allows the user to monitor the link for upgrade to clear channel capability, and respond to it. The B8ZS monitoring feature works at all times and is independent of the state of CCR bit-7.

F-BITS

The use of the F-bit position in 193S is split between the terminal framing pattern (known as F_T bits) which provides frame alignment information, and the signaling framing pattern (known as F_S bits) which provides multiframe alignment information (See Table 2). In 193E framing, the F bit position is shared by the framing pattern sequence (FPS), which provides frame and multiframe alignment information, a 4 KHz data link known as FDL, and CRC (cyclic redundancy check) bits. The FDL bits are used for control and maintenance (inserted by the user at TLINK) and the CRC bits are an indicator of link quality and may be monitored by the user to establish error performance. (See Table 1)

SIGNALING

During frames 6 and 12 in 193S, A and B signaling information is inserted into the LSB of all channels transmitted (Table 2). In 193E, A and B data is inserted into frames 6 and 12, and C and D data is inserted into Frames 18 AND 24. This allows a maximum of 4 signaling states to be transmitted per superframe in 193S and 16 states in 193E (Table 1).

B8ZS

The XR-T5690 supports existing and emerging zero suppression formats. Selection of B8ZS coding maintains system "1's" density requirements without disturbing data integrity as required in emerging clear channel applications. B8ZS coding replaces 8 consecutive outgoing zeros with a B8ZS code word. Any received B8ZS code word is replaced with all zeros.

BIT SEVEN STUFFING

Existing systems meet one's density requirements by forcing bit 7 of all zero channels to 1. Bit 7 stuffing is "globally" enabled by asserting CCR bit-1, and may be disabled on an individual channel basis by setting appropriate bits in TTR1-TTR3.

LOOP BACK

Enabling loop back will typically induce an out of frame "OOF" condition. If appropriate bits are set in the receive control register, the receiver will resync to the looped transmit frame alignment. During the looped condition, the transmit outputs (TPOS, TNEG) will transmit unframed all "1's". All operating modes are available in loop back.

ALARMS

The XR-T5690 supports all alarm pattern generation and detection required in typical BELL system applications. These alarm modes are explained in ATT PUB 43801, ATT C.B. #142

TABLE 1

193E FRAMING FORMAT

Frame #	F-Bit Use			Bit Use per Channel		Signaling Bit Use		
	FPS[1]	FDL[2]	CRC[3]	Data Bits	Signaling Bits[4,5]	2 State	4 State	16 State
1	-	M	-	Bits 1-8				
2	-	-	C1	Bits 1-8				
3	-	M	-	Bits 1-8				
4	0	-	-	Bits 1-8				
5	-	M	-	Bits 1-8				
6	-	-	C2	Bits 1-7	Bit 8	A	A	A
7	-	M	-	Bits 1-8				
8	0	-	-	Bits 1-8				
9	-	M	-	Bits 1-8				
10	-	-	C3	Bits 1-8				
11	-	M	-	Bits 1-8				
12	1	-	-	Bits 1-7	Bit 8	A	B	B
13	-	M	-	Bits 1-8				
14	-	-	C4	Bits 1-8				
15	-	M	-	Bits 1-8				
16	0	-	-	Bits 1-8				
17	-	M	-	Bits 1-8				
18	-	-	C5	Bits 1-7	Bit 8	A	A	C
19	-	M	-	Bits 1-8				
20	1	-	-	Bits 1-8				
21	-	M	-	Bits 1-8				
22	-	-	C6	Bits 1-8				
23	-	M	-	Bits 1-8				
24	1	-	-	Bits 1-7	Bit 8	A	B	D

Notes: 1. FPS - Framing Pattern Sequence
2. FDL - Facility Data Link (4 KHz M = Message Bits)
3. CRC - Cyclic Redundancy Check Bits
4. In case of clear channel, bit 8 will be used for data and not signaling.
5. Users can support 2 state, 4 state or 16 state signaling with the following outputs (TMO, TSIGFR, TSIGSEL, RMSYNC, RSIGFR, RSIGSEL).

TABLE 2

193S FRAMING FORMAT

Frame #	F-Bit Use		Bit Use per Channel		Signaling
	FT[1]	FS[2]	Data Bits	Signaling Bits[4]	Bit Use
1	1	-	Bits 1-8		
2	-	0	Bits 1-8		
3	0	-	Bits 1-8		
4	-	0	Bits 1-8		
5	1	-	Bits 1-8		
6	-	1	Bits 1-7	Bit 8	A
7	0	-	Bits 1-8		
8	-	1	Bits 1-8		
9	1	-	Bits 1-8		
10	-	1	Bits 1-8		
11	0	-	Bits 1-8		
12	-	0[3]	Bits 1-7	Bit 8	B

Notes: 1. FT - Terminal Framing Bits provide frame alignment.
2. FS - Signaling Frame Bits provide multiframe alignment.
3. For clear channel, bit 8 is used for data and not signaling.
4. The S bit in frame 12 may be used for yellow alarm transmission and detection for some applications.

RECEIVER FUNCTIONS

RECEIVE CODE INSERTION

Incoming receiver channels can be replaced with idle (7F Hex) or digital milliwatt (u-LAW format) codes. The receiver mark registers indicate which channels are inserted. When set, RCR bit-5 serves as a "global" enable for marked channels, and RCR bit-4 selects inserted code format: 0=idle code, 1=digital milliwatt.

RECEIVER SYNCHRONIZER

RCR bit-0 through RCR bit-3 allow the user to control operational characteristics of the synchronizer. Sync algorithm, candidate qualify testing, auto resync, and command resync modes may be altered at any time in response to changing span conditions.

SYNC TIME

The RCR bit-2 determines the number of consecutive framing pattern bits to be qualified before SYNC is declared. If RCR bit-2 is set to "1", the algorithm will validate 24 bits; if RCR bit-2 is set to "0", 10 bits are validated. 24 bit testing results in superior false framing protection, while 10 bit testing minimizes reframe time (although in either case, the synchronizer will only establish resync when one and only one candidate is found).

RESYNC

A zero to one transition of RCR bit-0 causes the synchronizer to search for the framing pattern sequence immediately, regardless of the internal sync status. In order to initiate another resync command, this bit must be cleared and then set again.

SYNC ENABLE

When RCR bit-1 is cleared, the receiver will initiate automatic resync if any of the following events occur: A) an out of frame (OOF), or B) carrier loss (32 consecutive 0's appear at RPOS and RNEG). An OOF event occurs any time that 2 of 4 F_T or FPS bits are in error. When RCR bit-1 is set, the automatic resync circuitry is disabled; in this case, resync can only be initiated by setting RCR bit-0 to "1", or externally via a low to high transition on RST. Note that using RST to initiate resync resets the receiver output timing while RST is low; use of RCR bit-1 does not affect output timing until the new alignment is located.

RECEIVER LOSS OF SYNC OUTPUT

The RLOS output of XR-T5690 indicates the status of the receiver synchronizer circuitry: when high, an off line resynchronization is in progress and a high low transition indicates resync is completed. The RLOS bit (RSR bit-0) is a "latched" version of the RLOS output. If the auto resync mode is selected (RCR bit-1=0) RLOS is a real time indication of a carrier loss or OOF event occurrence.

RESET

A high to low transition on $\overline{RST}$ clears all registers and forces immediate receive resync when $\overline{RST}$ returns high. This reset has no effect on transmit frame, multiframe, or channel counters. $\overline{RST}$ must be held low on system power up to insure proper initialization of transceiver counters and registers. Following reset, the host processor should restore all control modes by writing appropriate registers with control data.

RECEIVE SIGNALING

Robbed bit signaling data is presented at RABCD during each channel time in signaling frames for all 24 incoming channels. Logical combination of clocks RMSYNC, RSIGFR and RSIGSEL allow the user to identify and extract AB or ABCD signaling data.

TRANSMITTER FUNCTIONS

TRANSMIT BLUE ALARM

The blue alarm is an unframed, all 1's sequence enabled by asserting TCR bit-1. Blue alarm overrides all other transmit data patterns and is disabled by clearing TCR bit-1. Use of the TIR registers allows a framed, all 1's alarm transmission if required by the network.

TRANSMIT YELLOW ALARM

In 193E framing a yellow alarm is a repeating pattern set of FF (HEX) and 00 (HEX) on the 4 KHz facility data link (FDL). In 193S framing, the yellow alarm format is dependent on the state of CCR bit- 3. In all modes, yellow alarm is enabled by asserting TCR bit-0 and disabled by clearing TCR bit-0.

TRANSMIT SIGNALING

When enabled (Via TCR bit-4) channel signaling is inserted in frames 6 and 12 (193S), or 6, 12, 18 and 24 (193E) in the 8th bit position of every channel word. Signaling data is sampled at TABCD on the falling edge of TCLK during bit 8 of each input word during signaling frames. Logical combination of clocks TMO, TSIGFR and TSIGSEL allow external multiplexing of separate serial links for A, B, or A, B, C, D signaling sources.

SERIAL ADDRESS/COMMAND FORMAT

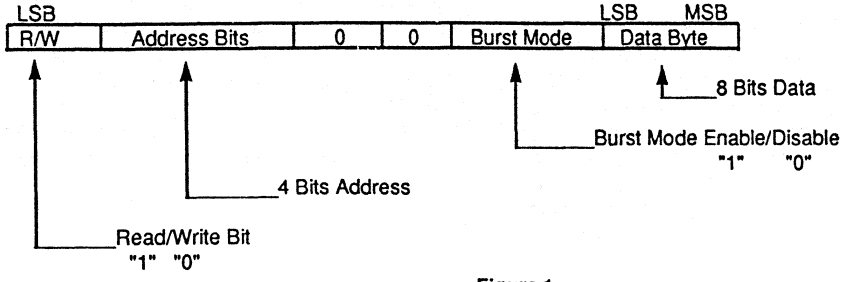


Figure 1

Reading or writing the control, configuration or status registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command word specifies register read or write. the following 4 bit nibble identifies register address. The next two bits are reserved and must be zero for proper operation. The last bit of the address/command word enables burst mode when set; the burst mode causes all registers to be consecutively written or read. Data is written to and read from the transceiver LSB first. (see Figure 1)

TRANSMIT CHANNEL TRANSPARENCY
Individual DS0 channels in the T1 frame may be programmed clear by setting the appropriate bits in the transmit transparency registers. Channel transparency is required in mixed voice/data or data only environments such as ISDN, where data integrity must be maintained.

TRANSMIT IDLE CODE INSERTION
Individual outgoing channels in the frame can be programmed with idle code by asserting the appropriate bits in the transmit idle registers. One of the two idle code formats, 7F (Hex) and FF (Hex) may be selected by the user via TCR bit-3. If enabled, robbed bit signaling data is inserted into the idle channel, unless the appropriate TTR bit is set for that channel. This feature eliminates external hardware currently required to intercept and stuff unoccupied channels in the DS1 bit stream.

SERIAL CONTROL INTERFACE
(See Figure 1 on previous page)

SERIAL PORT
Pin 14 through 18 of the XR-T5690 serve as a microprocessor or microcontroller compatible serial port. Sixteen on board registers allow the user to update operational characteristics and monitor device status via a host controller, minimizing hardware interfaces. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous read and/or writes by the host.

CHIP SELECT AND CLOCK CONTROL
All data transfers are initiated by driving the $\overline{CS}$ input low. Input data is latched on the rising edge of SCLK and must be valid during the previous low period of SCLK to prevent momentary corruption of register data during writes. Data is output on the falling edge of SCLK and held to the next falling edge. All data transfers are terminated if the $\overline{CS}$ input transitions high. Port control logic is disabled and SDO is tristated when $\overline{CS}$ is high.

DATA I/O
Following the 8 SCLK cycles that input an address/command byte to write, a data byte is strobed into the addressed register on the rising edge of the next 8 SCLK cycles. Following an address/command word to read, contents of the selected register are output on the falling edge of the next 8 SCLK cycles. The SDO pin is tristated during device write, and may be tied to SDI in applications where the host processor has a bidirectional I/O pin.

BURST MODE
The burst mode allows all on board registers to be consecutively read or written by the host processor. A burst read is used to poll all registers; RSR contents will be unaffected. This feature minimizes device initialization time on power up or system reset. Burst mode is initiated when ACB bit-7 is set and the address nibble is "0000". Burst is terminated by low to high transition on $\overline{CS}$.

HARDWARE MODE
For preliminary system prototyping or applications which do not require the features offered by the serial port, the transceiver can be reconfigured by the SPS pin. Tying this pin to Vss disables the serial port, clears all internal registers except CCR, TCR and redefines pins 14 through 18 as mode control inputs. The hardware mode allows device retrofit into existing applications where mode control and alarm conditioning hardware is often designed with discrete logic.

HARDWARE COMMON CONTROLS
In the hardware mode TCR bit-2, CCR bit-4, TCR bit-0, CCR bit-1 and CCR bit-2 map to pins 14 through 18. The loopback feature (CCR bit-0) is enabled by tying pins 17 (zero suppression) and 18 (B8ZS) to 1. (The last states of pins 17 and 18 are latched when both pins are taken high, preserving the current zero suppression mode). Robbed bit signaling (TCR bit-4) is enabled for all channels. The user may tie TSER to TABCD externally to disable signaling if so desired. CCR bit-3 is forced to 0, which selects yellow alarm bit-2 in 193S framing. Contents of the RCR, as well as the remaining bit locations in the CCR and TCR, are cleared in hardware mode. The RST input may be used to force immediate receiver resync, and has no effect on transmit.

ALARMS

ALARM OUTPUTS
The transceiver provides direct alarm outputs for applications when additional decoding and demuxing are required to supplement the on board alarm logic.

YELLOW ALARM OUTPUT
The RYEL output of XR-T5690 will go high when a yellow alarm is detected. A high to low transition indicates the alarm condition has been cleared. The RYEL bit

(RSR bit-5) is a "latched" version of the RYEL output. In 193E framing, the yellow alarm pattern detected is 16 pattern sets of 00 HEX and FF HEX received at RLINK or a "0" in the bit 2 position of all channels. In 193S framing the yellow alarm format is dependent on CCR bit-3: if CCR bit-3=0, the RYEL output transitions high if bit 2 of 156 or more consecutive channels is 0; if CCR bit-3=1, yellow alarm is detected when the S-bit received in frame 12 is 1.

BIPOLAR VIOLATION OUTPUT

The RBV output transitions high when accused bit emerges at RSER. RBV will go low at the next bit time if no additional violations are detected.

RECEIVE FRAME OUTPUT

The receive frame error output transitions high at the F-bit time and is held high for two bit periods when a frame bit error occurs. In 193S framing F_T and F_S patterns are tested. The FPS pattern is tested in 193E framing. Additionally, in 193E framing, RFER reports a CRC error by a low to high to low transition (one bit period wide) one half RCLK period before a low to high transition on RMSYNC.

RECEIVE ALARM REPORTING

Incoming serial data is monitored by the transceiver for alarm occurrence. Alarm conditions are reported in two ways: via transitions on the alarm output pins and registered interrupt. Interrupts may be direct, in which case the transceiver demands service for a real time alarm, or count overflow triggered, in which case an on board alarm event counter exceeds a user-programmed threshold. The user may mask individual alarm conditions by clearing the appropriate bits in the receive interrupt mask register.

ALARM SERVICING

The host controller must service the transceiver in order to clear an interrupt condition. Clear appropriate bits in the RIMR will unconditionally clear an interrupt. Direct interrupt will be cleared when the RSR is read, unless the alarm condition still exists. Count overflow interrupts will be conditionally cleared by reading the RSR; the next event will trigger interrupt unless the user presents the appropriate count register.

COUNTERS

ALARM COUNTERS

The three on board alarm event counters allow the transceiver to monitor and record error events without processor intervention on each event occurrence. All of these counters are presentable by the user, establishing an event count interrupt threshold. As each counter saturates, it will set a bit in RSR and generate an interrupt unless masked. The user may read these registers at any time; in many systems, the host will periodically poll these registers to establish link error rate performance.

OOF EVENTS AND ERRORED SUPERFRAMES

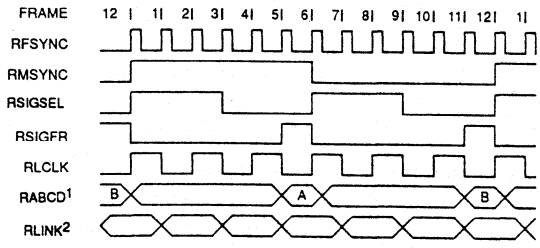
Out of frame is declared when two of four consecutive framing bits are in error. F_T bits are tested for OOF occurrence in 193S; the FPS bits are tested in 193E. OOF events are recorded by the 4 bit OOF counter in the error count register. In the 193E framing mode, the OOF event is logically "OR'ed" with an on chip generated CRC checksum. This event, known as errored superframe, is recorded by the 4 bit ESF error counter in the error count register. In the 193S framing mode, the 4 bit ESF error counter records individual F_T and F_S errors when RCR bit-3=1, or F_T errors only when RCR bit-3=0.

BIPOLAR VIOLATION COUNTER

This 8 bit binary up counter saturates at 255 and will generate an interrupt for each occurrence of a bipolar violation (RIMR bit-7=1). Presetting this register allows the user to establish specific count interrupt thresholds. The counter will count "UP" to saturation from the preset value, and may be read at any time. Counter increments occur at all times and are not disabled by resync.

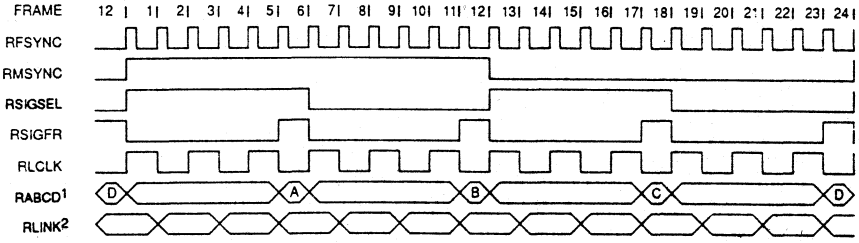
OOF AND ESF ERROR COUNTERS

These separate 4-bit binary up counters saturate at a count of 15 and will generate an interrupt for each occurrence of an OOF event or an ESF error event after saturation (RIMR bit-6=1). Presetting these counters allows the user to establish specific count interrupt thresholds. The counter will count "UP" to saturation from the present value, and may be read at any time. These counters share the same register address, and must be written to or read from simultaneously. The OOF counter records out of frame events in both 193S and 193E. The ESF error counter records errored superframes in 193E. In 193S the ESF counter records individual F_T and F_S errors when RCR bit-3=1; F_T errors only when RCR bit-3=0. ECR counter increments are disabled when resync is in progress (RLOS high).



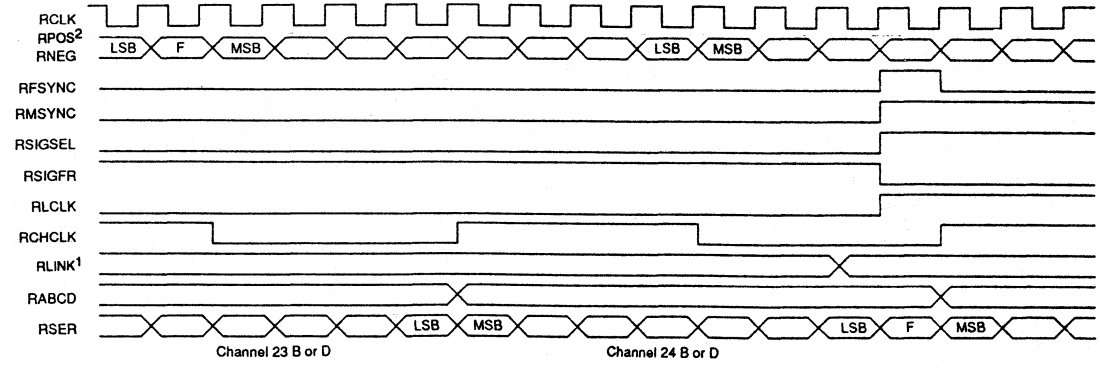
Note: 1. Signaling data is updated during signaling frames or channel boundaries. RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (S-bit) is updated one bit time prior to S-bit frames and held for two frames.

193S Receive Multiframe Timing



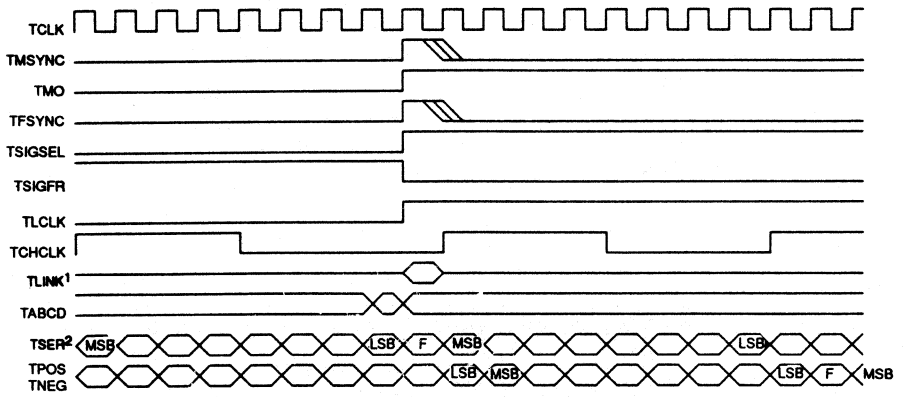
Note: 1. Signaling data is updated during signaling frames on channel boundaries. RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (FDL-bit) is updated one bit-time prior to S-bit frames and held for two frames.

193E Receive Multiframe Timing



Note: 1. RLINK timing is shown for 193E; in 193S RLINK is updated on even frame boundaries and is held across multiframe edges.
2. Total delay from RPOS and RNEG output is 13 clock periods.

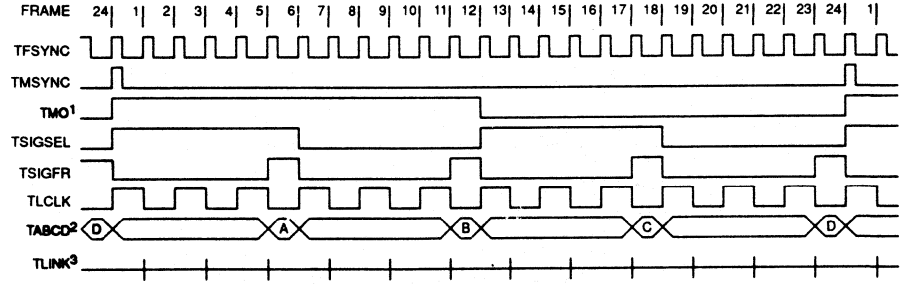
Receive Multiframe Boundary Timing



Note 1) TLINK timing shown is for 193 E framing; where TLINK is sampled as shown for insertion into F bit position of odd frames. When S-bit insertion is enabled in 193S, TLINK is sampled during even frames.

2. If TCR bit-S=1; TSER is sampled during the F-bit time of CRC frames for insertion into the outgoing data stream (193E Framing only).

Transmit Multiframe Boundry Timing

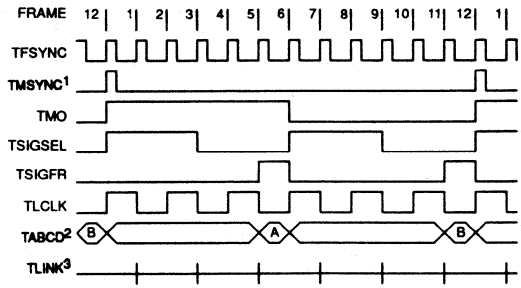


Notes: 1. Establishing frame and multiframe:
a) With TFSYNC tied low, TMSYNC may be pulsed high once every multiframe period to establish multiframe boundaries.
b) TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNC once establishes multiframe boundaries.
c) TMSYNC and TFSYNC may be continously pulsed to establish and reinforce frame and superframe timing.
d) If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.

2. Channels with Robbed Bit Signaling enabled will sample TABCD during the LSB bit time in the frames indicated

3. TLINK is sampled during the F-Bit time of odd frames and inserted into the outgoing data stream (FDL data).

193E Transmit Multiframe Timing

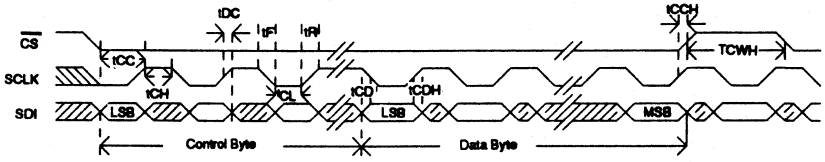


Notes: 1. Establishing frame and multiframe:
a) With TFSYNC tied low, TMSYNC may be pulsed high once every multiframe period to establish multiframe boundaries.
b) TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNC once establishes multiframe boundaries.
c) TMSYNC and TFSYNC may be continously pulsed to establish and reinforce frame and superframe timing.
d) If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.

2. Channels with Robbed Bit Signaling enabled will sample TABCD during the LSB bit time in the frames indicated.

3. When external S-bit insertion is enabled, TLINK will be sampled during the F-Bit time of even frames and inserted into the outgoing data stream.

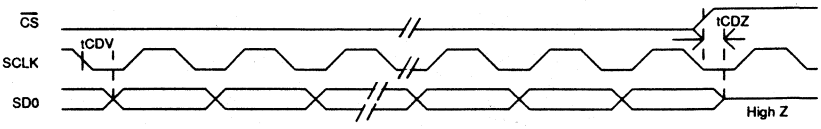
193S Transmit Multiframe Timing



Notes: 1. Data byte must be valid across low clock periods to prevent transients in operating modes.

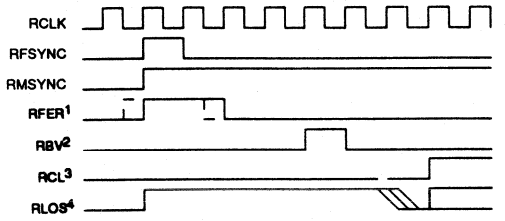
2. The shaded regions are don't care states of input data.

Serial Port Write AC Timing



Notes: 1. Serial port write must precede a port read to provide address information.

Serial Port Read[1] AC Timing



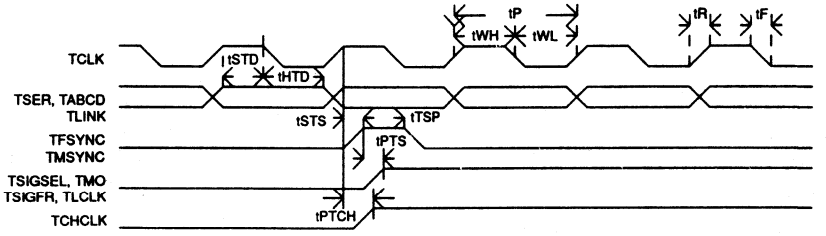
Note: 1. RFER goes high during F-Bit if framing pattern is in error (Frame 12 F-bits are ignored if CCR bit 3=1). Also, in 193E Format, RFER transitions half a bit period before the rising edge of RMSYNC to indicate a CRC error.

2. RBV indicates received bipolar violations and transitions high together with the accused bit on RSER. If B8ZS is enabled RBV does not report the zero replacement code.

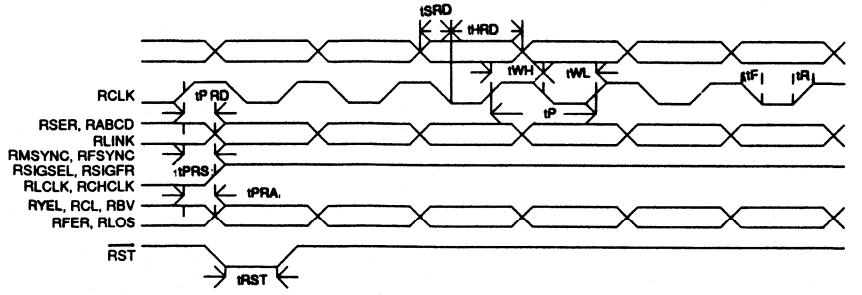
3. RCL transitions high after 32 consecutive "0" bits are received. It goes low when the next "1" is received.

4. RLOS transitions high during the F-bit time that caused the OOF event if autoresync mode is selected (RCR-1 = 0)(2 out of 4 consecutive F-T or FPS bits are in error). Resync will also occur when loss of carrier is detected (RCL = 1). When RCR-1=1 RLOS remains low until resync occurs, regardless of OOF carrier loss flags. In this situation, resync is initiated only when RCR-0 transitions low to high or RST pin transitions, high to low to high.

Alarm Output Timing



Transmit AC Timing



Receive AC Timing

T1 RECEIVE BUFFER

GENERAL INFORMATION

The XR-T5691 is designed to synchronize receive loop-timed T-carrier data streams to system side timing. It is very flexible and allows interfacing of incoming data to parallel or serial TDM backplanes. It is implemented using low power CMOS technology and is available in a "skinny" 24 lead plastic DIP & 24 pin PLCC packages. This device operates in conjunction with the XR-T5690 Framer and is capable of extracting, buffering and integrating ABCD Signaling.

FEATURES

Synchronizes T1 Data Streams To System Clocks
Two Frame Buffer Depth
Frame Slip Output At Frame Boundaries
Buffer Recentering Capability
Recommend Operating Frequency: 1.544 and 2.048 MBPS
Interfaces To Parallel and Serial Backplanes
Robbed-bit Signaling Extraction and Buffering
Inhibits Signaling Updates During Alarm or Slip Conditions
Integration Feature "Debounces" Signaling
Pin to Pin and Functionally Compatible to DS2176

APPLICATIONS

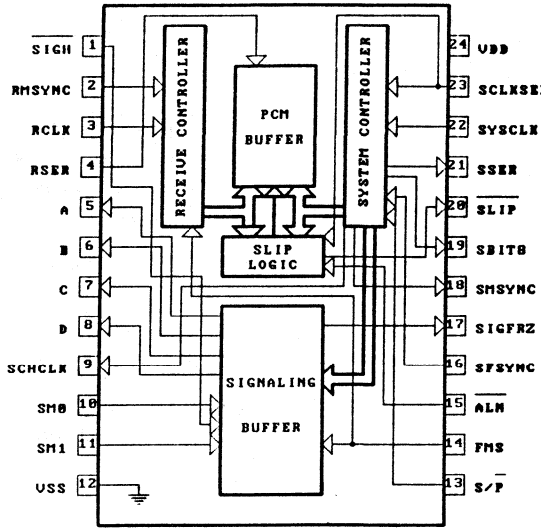
Digital Trunks
Drop and Insert Equipment
Transcoders
Digital Cross Connects
Private Network Equipment
PABX's
DMI's
CPI's

ABSOLUTE MAXIMUM RATINGS

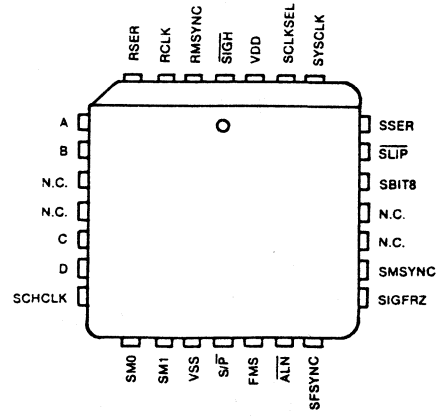
Input Voltage	-1.0V to 7.0V
Storage Temperature	-65°C to +150°C
Soldering Temperature	260°C for 10sec

NOTE: Stresses exceeding the ones specified above may cause permanent damage to the device or cause reliability problems.

PIN ASSIGNMENT



CP & 1P Pinout



CJ & 1J Pinout

ORDERING INFORMATION

Part Number	Package	Operating Temp
T5691 I P	Plastic	-40°C to +85°C
T5691 I J	PLCC	-40°C to +85°C
XR-T5691CP	Plastic	0°C to 70°C
XR-T5691CJ	PLCC	0°C to 70°C

PIN DESCRIPTION		
PIN	**SYMBOL**	**DESCRIPTION**
1	SIGH	SIGNALING INHIBIT When low it disables ABCD signaling updates for a period determined by SM0 and SM1 or until returned to high.
2	RMSYNC	RECEIVE MULTIFRAMES SYNC When high during multiframe boundaries it establishes frame and multiframe alignment
3	RCLK	RECEIVE CLOCK Extracted 1.544 MHz clock.
4	RSER	RECEIVE SERIAL DATA Sampled during the falling edge of RCLK.
5-8	A/B/C/D	ROBBED-BIT SIGNALING OUTPUT A-D
9	SCHCLK	SYSTEM CHANNEL CLOCK Needed for serial to parallel conversion of channel data. Transitions occur during channel boundaries.
10/11	SM0/SM1	SIGNALING MODES 0 and 1 Select signaling logic.
12	VSS	SIGNAL GROUND
13	S/P	SERIAL TO PARALLEL SELECT Parallel (tie to VSS) Serial (tie to VDD)
14	FMS	FRAME MODE SELECT For 193S Framing (tie to VSS) for 193E Framing (tie to VDD)
15	ALN	ALIGN. When forced low, it recenters the buffer on the next system side frame boundary.
16	SFSYNC	SYSTEM FRAME SYNC Rising edge establishes the start of the frame.
17	SIGFRZ	SIGNALING FREEZE. Indicates signaling updates when high. These can be caused internally via a slip or externally by forcing SIGH low.
18	SMSYNC	SYSTEM MULTIFRAME SYNC Slip-compensated multiframe output; indicates when signaling updates are made.
19	SBIT8	SYSTEM BIT 8. Intended to reinsert the extracted signaling into the outgoing data stream. It is high during the LSB time of each channel.
20	SLIP	FRAME SLIP. (Active low) Indicates a slip and held low for 64 SYSCLK cycles. Open collector output.
21	SSER	SYSTEM SERIAL OUT. Output data updated on the rising edge of SYSCLK.
22	SYSCLK	SYSTEM CLOCK. 1.544 MHz or 2.046 MHz clock.
23	SCLKSEL	SYSTEM CLOCK SELECT. 1.544MHz (tie to VSS); 2.048 MHz (tie to VDD)
24	VCC	POSITIVE SUPPLY VOLTAGE. 5.0V +/- 10%.

PRINCIPLES OF OPERATION

The XR-T5691 is designed to synchronize the received T1 PCM data (loop timed) to the host backplane, and also to supervise the robbed-bit signaling information embedded in the data stream. This device is intended to operate in conjunction with the XR-T5690 "T1 Framer" and the XR-T56L22 "T1 Line Receiver" to offer a complete system solution.

Synchronization

The XR-T5691 buffers the incoming PCM data from RSER into a 2-frame buffer (386 bits long). This data is sampled on the falling edge of RLCK and appears back at SSER where it is updated on the rising edge of SYSCLK. The frame and multiframe alignment on the receive side is established with the rising edge of RMSYNC. On the system side, a rising edge of SFSYNC establishes frame allignment. Buffer depth monitoring is done by an on board contention logic which signals a "slip" whenever the buffer is completely emptied or filled. After the occurance of a "slip", the SLIP output (open collector) is held low for 64 clock cycles and the buffer recenters automatically to a one-frame depth on the rising edge of a frame boundary. This configuration is adequate for most T-carrier applications which need to synchronize under short term jitter conditions. The XR-T5691 offers a good compromise between total delay and slip correction capability.

Buffer depth monitoring is achieved by sensing the distance between the rising edge of RMSYNC and SMSYNC real time. The output pulse SMSYNC which indicates the system side multiframe boundaries, is held high for 65 SYSCLK cycles.

This device is compatible with the two most common backplane frequencies (1.544 and 2.048MHz) which can be selected by strapping SCLKSEL to VSS for 2.048 MHz and to VCC for 1.544 MHz operation. In 1.544 MHz applications the F-bit is passed through the receive buffer and presented at SSER immediately after a rising edge on SFSYNC. For 2.048 MHz applications the F-bit is dropped, and MSB of channel 1 appears at SSER after a one bit period delay following the rising edge of SFSYNC. For the excess channels (greater than 24) the SSER pin is forced high. Also the slip criteria for 2.048 MHz applications is different than that used for 1.544MHZ in order to compensate for the faster system side read frequency.

The XR-T5691 is capable of interfacing to serial and/or parallel backplanes. For serial applications (S/P=1), the data from channel 1 appears at SSER after a rising edge at SFSYNC as illustrated in Figure 8. For parallel applications a look-ahead mechanism is used whereby data is made available 8 clock cycles prior to SCHCLK in order to convert parallel data externally.

Signaling

Robbed-bit signaling data is inserted into the LSB position of each channel during signaling frames. Depending on the type of frame format used (193S or 193E), the signaling information is first extracted from the incoming frames and then presented at the corresponding outputs (A, B, C or D). In 193S framing (FMS=0), the "A" signaling data is inserted into frame 6 and the "B" signaling data into frame 12. In 193E framing (FMS=1), four signaling bits are available, in which case the two additional bits "C and D" are inserted into frames 18 and 24 correspondingly The outputs A, B, C and D are valid for each individual channel time and are repeated per channel for all frames of the multiframes. In 193S applications, the two extra outputs "C and D" contain the previous "A and B" data. Signaling updates occur once per multiframe at the rising edge of SMSYNC unless prohibited otherwise by the freeze function.

This "freeze function", which occurs during a slip condition or by forcing SIGH low, inhibits any signaling updates during alarm or slip conditions. The duration of the freeze is dependent on SM0 and SM1. During this period "old" data is recirculated in the output registers, and SIGFRZ is held high until the next signaling update. The input to output delay of the signaling data is equal to 1 multiframe plus the current depth of the PCM buffer (1 multiframe +1 frame +/-1 frame).

Integration is another feature of the XR-T5691 which minimizes the impact of random noise and possible robbed-bit signaling corruption. This requires that the per channel signaling data be in the same state for 2 or more multiframes before appearing at A, B, C or D. As to what degree of integration is required can be selected by toggling SM0 and SM1. In order to minimize update delay, integration is limited to 2 multiframes during slip or alarm conditions. This is shown in Table 1.

Concerning ISDN applications and clear channel capability, in order to assure integrity of data, the XR-T5691 will not merge processed signaling information back into the outgoing PCM frame. SBIT8 indicates the LSB position of each channel which can be combined with off chip logic to selectively reinsert robbed-bit signaling data into the outgoing data stream.

TABLE 1. SIGNALING SUPERVISION MODES			
SM0	**SM1**	**FMS**	**SELECTED MODE**
0	0	0	193S framing, no integration, 1 multiframe freeze
0	0	1	193E framing, no integration, 1 multiframe freeze
0	1	0	193S framing, 2 multiframes integration & freeze
0	1	1	193E framing, 2 multiframes integration & freeze
1	0	0	193S framing, 5 multiframes integration & 2 multiframes freeze. (1)
1	0	1	193E framing, 3 multiframes integration & 2 multiframes freeze. (1)
1	1	0	Test mode.
1	1	1	Test mode.

NOTES: 1) During a slip or alarm condition, integration is limited to 2 multiframes to minimize signaling delay.

DC ELECTRICAL CHARACTERISTICS:
Test Conditions: VCC = 5V+/-10%, Ta = -40°C to +85°C unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYPE	MAX	UNIT	CONDITIONS
V IH	Logic 1	2.0		VDD+0.3	V	
V IL	Logic 0	-0.3		+0.8	V	
V CC	Pos Supply	4.5		5.5	V	
I CC	Current Input		6	10	mA	Note 1, 2
I IL	Leakage In	-1.0		+1.0	uA	
I OH	Current Output	-1.0			mA	Note 3
I OL	Current Output	+4.0			mA	Note 4
I LO	Leakage Output	-1.0		+1.0	uA	Note 5
C IN	Input Capacitance			5	pF	
C OUT	Output Capacitance			7	pF	

NOTES: 1) TCLK=RCLK=1.544MHz
2) Outputs open.
3) Measured @ 2.4V; all outputs except SLIP which is open collector.
4) All outputs.
5) Applies to SLIP when tri-stated.

AC ELECTRICAL CHARACTERISTICS:
Test Conditions: VCC = 5V+/-10%, Ta = -40°C to +85°C unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYPE	MAX	UNIT	CONDITIONS
t RCLK	RCLK Period	250	648		ns	Figure 1
t R, t F	RCLK, SYSCLK Rise/Fall Time			20	ns	Figure 1
t RWH t RWL	RCLK Pulse Width	125	324		ns	Figure 1
t SWH t SWL	SYSCLK Pulse Width	25100	244		ns	Figure 2
t SYSCLK	SYSCLK Period	200	488		ns	Figure 2
t SC	RMSYNC Setup to RCLK Rising	-tRWH/2		+tRWL/2	ns	Figure 1
t SC	SFSYNC Setup to SYSCLK Rising	-tSWH/2		+tSWL/2	ns	Figure 2
t PW	RMSYNC, SFSYNC, SIGH ALN Pulse Width	100			ns	Figure 1 & 2
t HD	RSER Hold from RCLK Falling	50			ns	Figure 1
t PVD	Propagation delay SYSCLK to SSER			100	ns	Figure 2
t PSS	Propagation delay SYSCLK to SMSYNC			75	ns	Figure 2

SYMBOL	PARAMETER	MIN	TYPE	MAX	UNIT	CONDITIONS
t PS	Propagation delay SYSCLK or RCLK to SLIP low			100	ns	Figure 1 & 2
t PSF	Propagation delay SYSCLK to SIGFRZ			75	ns	Figure 2
t SR	ALN, SIGH Setup to SFSYNC Rising	500			ns	Figure 2

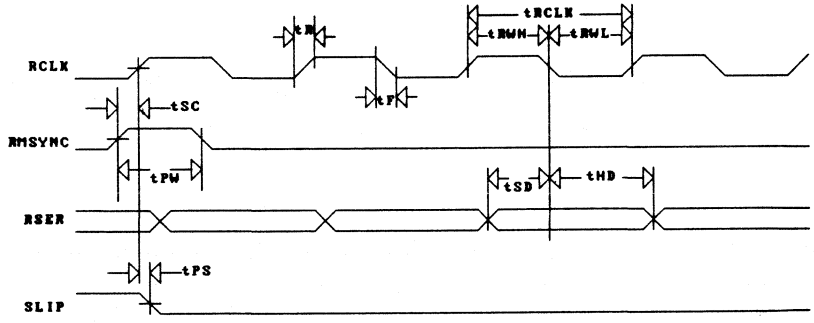


Figure 1. Receive A.C. Diagram

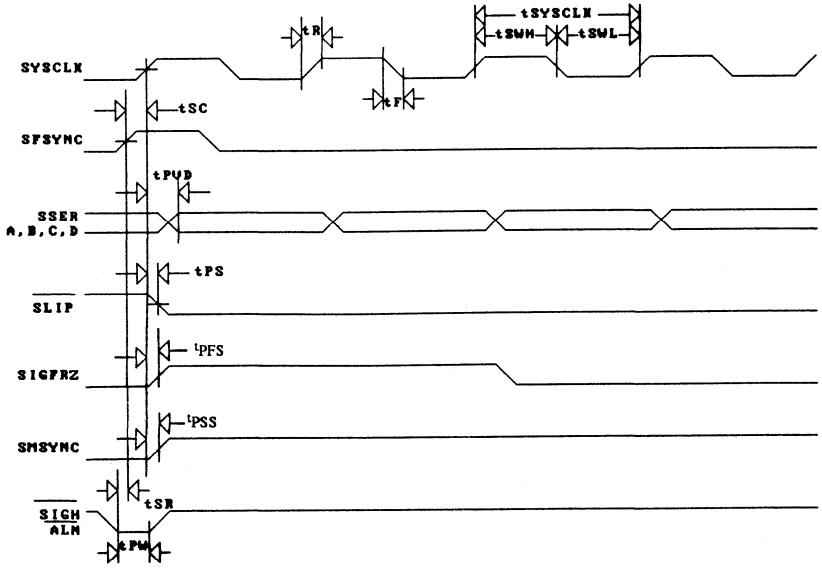


Figure 2. System AC Timing Diagram

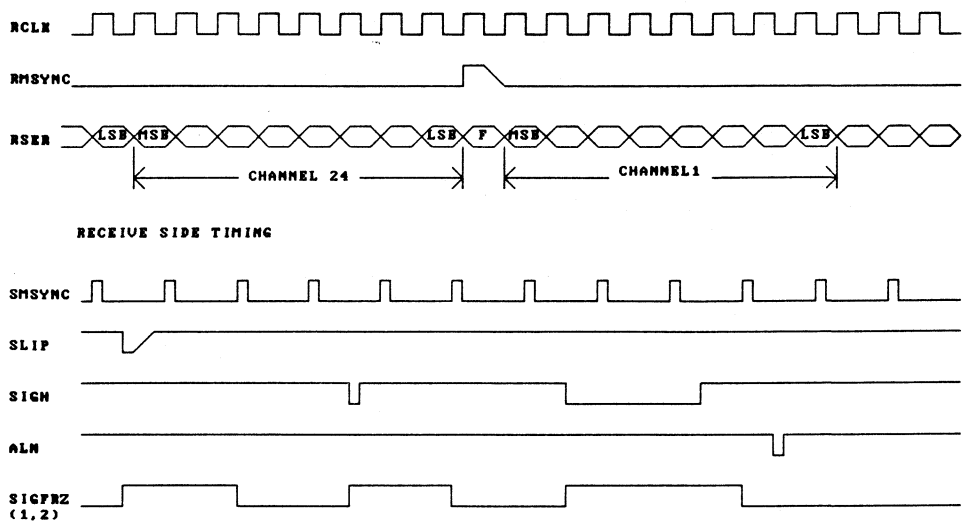


Figure 3. Slip and Signaling Supervision Logic Timing

NOTES: 1) Integration feature disabled (SMM=SMI=0) in timing set shown.
2) Depending on present buffer depth, forcing ALM low may or may not cause a slip condition.

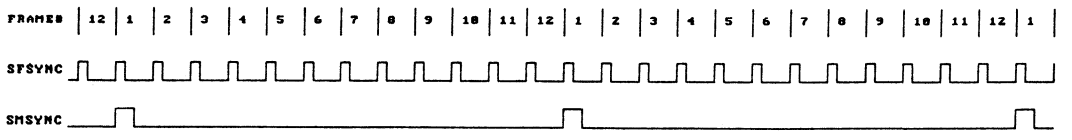


Figure 4. 193S System Multiframe Timing

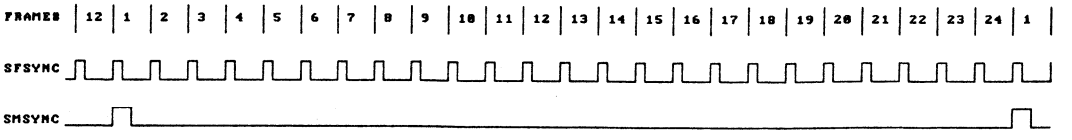


Figure 5. 193E System Multiframe Timing

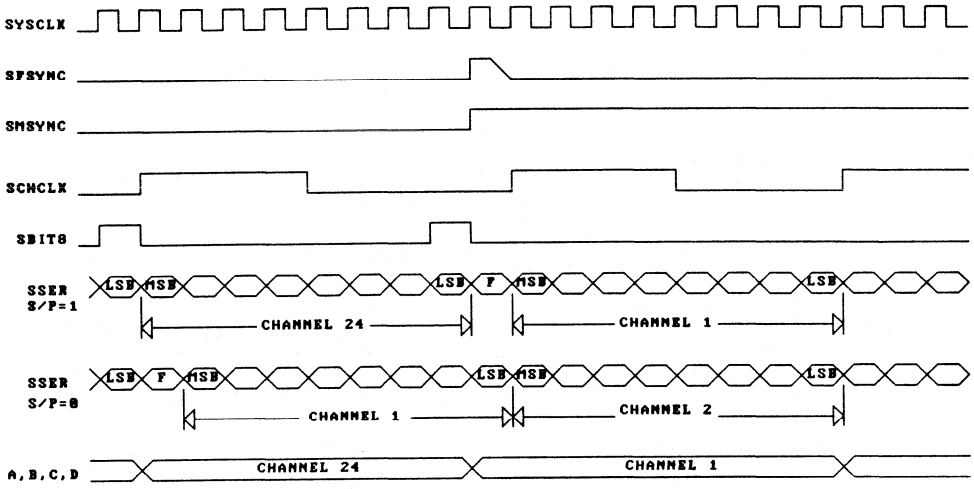


Figure 6. System Multiframe Boundry Timing (SYSCLM = 1.54 MHz)

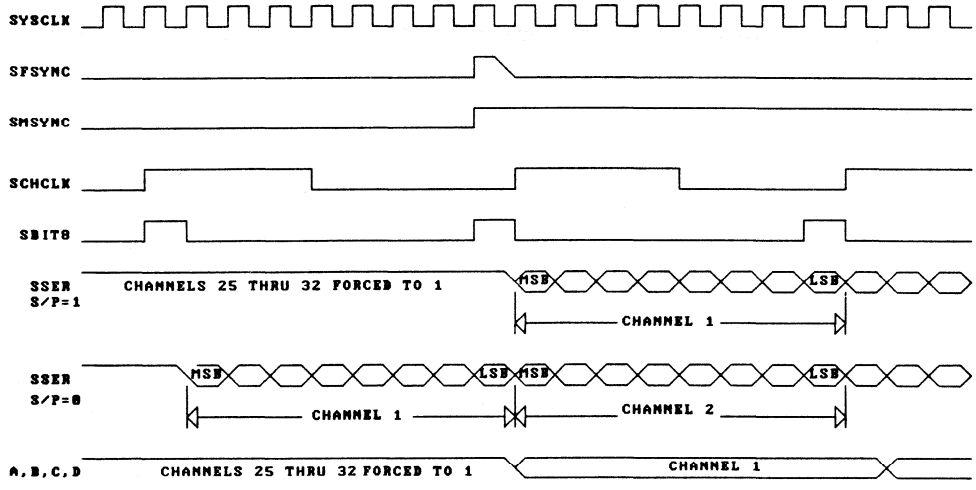


Figure 7. System Multiframe Boundary Timing (SYSCLK = 2.048 MHz)

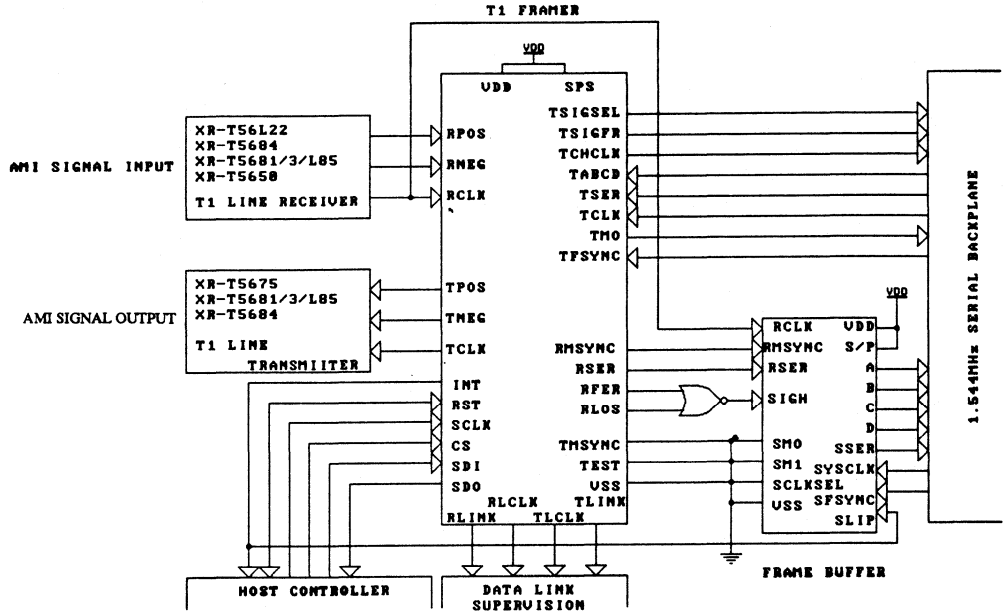


Figure 8. Typical Application using the XR-T5690 Framer and XR-T5691 Frame Buffer

Single Chip Codec/Filter Circuit

GENERAL INFORMATION

The XR-T3052/3053/3054/3057 are monolithic PCM CODER and DECODER integrated circuits, designed in CMOS technology, and intended to implement the transmit and receive functions in digital telecommunication circuits. The XR-T3052/3053/3054 have a companded μ-law PCM format as opposed to the XR-T3057 which uses the A-law PCM format. Each device contains separate D/A and A/D circuitry, all necessary sample and hold switched capacitor filters, precision voltage reference and internal auto zero circuitry.

On the transmit side, the analog signal is first amplified and then prefiltered by a distributed RC network to eliminate high frequency noise before entering a switched capacitor bandpass filter. The coder then samples the filtered signal and encodes this in the companded μ or A law. On the receive side, the decoder reconstructs the analog signal from the incoming digital PCM code. The analog signal goes through a low pass filter with sinx/x correction and a driver to handle low impedance loads. Included also is a timing and control section, which is upward compatible with 3052/3053/3054/3057 industry standard devices.

APPLICATIONS

Digital Telephone
Digital PABX'S
Digital PBX
ISDN Networks

FEATURES

Fully Differential Data Paths
Transmit High Pass, Low Pass Filtering
Receive Low Pass Filter with Sin x/x Correction
U-Law or A-Law COding and DECoding
Internal Auto-zero Circuitry
Dual Supply +/- 5 Volts
Serial I/O Interface
Low Operating Power (typ. 60 mW)
Power Down Stand by Mode (typ. 3 mW)
16 Pin Dual in Line Package (3054/3057)
TTL and CMOS Compatible Digital Interface
Automatic Power Down
Meets or Exceeds BELL/CCITT Specifications
Compatible with TP3052/3053/3054/3057
Precision Voltage Reference

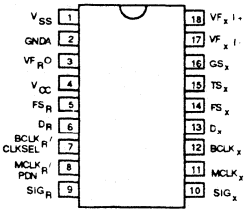
ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage V_{SS}/V_{DD}	+/- 7 Volts
Storage Temperature Range	-65° C to 150° C
Voltage at any pin	V_{SS}-.3 < V_{IN} < V_{DD} +.3

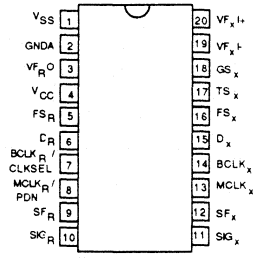
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T3052/53/54/57CP	Plastic DIP	0° C to +70° C
XR-T3052/53/54/57IP	Plastic DIP	-40°C to +85°C
XR-T3052/57CJ	PLCC	0° C to +70° C
XR-T3052/57IJ	PLCC	-40°C to +85°C
XR-T3052/53/54/57CN	Ceramic DIP	0°C to +70°C
XR-T3052/53/54/57IN	Ceramic DIP	-40°C to +85°C

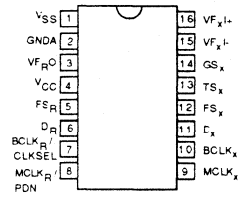
PIN ASSIGNMENT



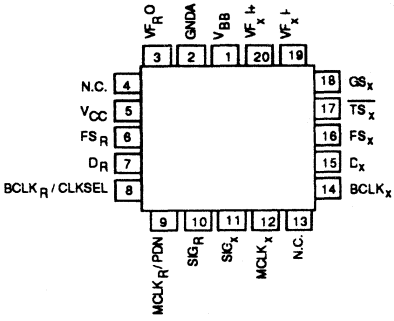
XR-T3052 CP/IN



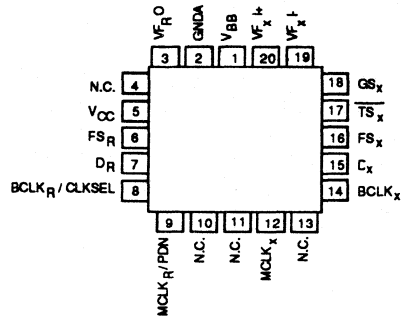
XR-T3053 CP/IN



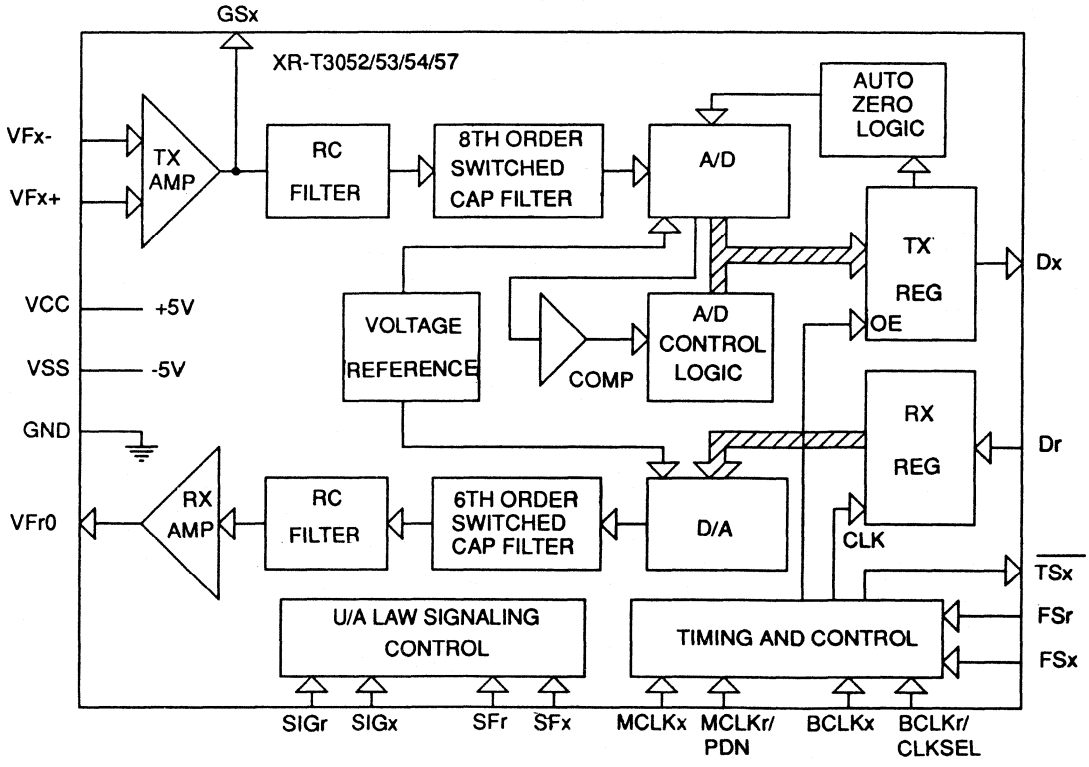
XR-T3054/57 CP/IN



XR-T3052 CJ



XR-T3054/57 CJ



PIN DESCRIPTION

	DESCRIPTION
VSS	**Negative Power Supply** pin. V_{SS} = -5V +/-5%.
GNDA	**Analog Ground**, all signals are referenced to this pin.
VFrO	**Analog Output** of the receive power amplifier.
VDD	**Positive Power Supply** pin. V_{DD} = +5V +/-5%
FSr	**Receive Frame Sync Pulse** which triggers extraction of PCM data into Dr. FSr is an 8KHz pulse train.
Dr	**Receive PCM Data Input** shifted into Dr following the FSr leading edge.
BCLKr/ CLKSEL	**Receive bit clock** which shifts data into Dr after the FSr leading edge. May vary from 64 KHz to 2.048 MHz. This pin can be selected as a master clock input for 1.536 MHz/1.544 MHz or 2.048 MHz. In the synchronous mode BCLKx is used for both receive and transmit directions.(See Table 1)
MCLKr/ PDN	**Receive Masterclock/ Powerdown.** This input must be a 1.536 MHz, 1.544 or 2.048 MHz clock which may be asynchronous with MCLKx but offers best performance when in the synchronous mode. If MCLKr is connected low, MCLKx is selected for all internal timing. If MCLKr is connected high the device is powered down.
SFr	**Receive Signaling Frame** When high during FSr, this input indicates a receive signal frame.

SYMBOL	DESCRIPTION
SIGr	**Receive Signaling Output** The eighth bit of the PCM data appears at this output after each receive signaling frame.
SIGx	**Transmit Signaling Input.** Data at this input is inserted into the 8th bit of the PCM word during transmit signaling frames.
SFx	**Transmit Signaling Frame** When high during FSx, this input indicates a transmit signaling frame.
MCLKx	**Transmit Masterclock** Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with MCLKr but offers best performance when in the synchronous mode.
BCLKx	**Transmit Bit Clock** which shifts out the PCM data on Dx. May vary from 64 KHz to 2.048 MHz.
Dx	**Transmit PCM Data Output** The three state PCM data output which is enabled by FSx.
FSx	**Transmit Frame Sync Pulse** input which enables BCLKx to shift out the PCM data on Dx. FSx is an 8 KHz pulse train. (See Figure 1 and 2)
TSx~	**Time Slot Output.** Open drain which pulses low during the encoded time slot.
GSx	**Transmit Amplifier Output** Used to set the gain of the transmit input amplifier.
VFxI-	**Inverting Input** of the transmit input amplifier.
VFxI+	**Non Inverting Input** of the transmit input amplifier.

DC ELECTRICAL CHARACTERISTICS:

Unless specified otherwise the following characteristics are guaranteed from T_A = -40°C to +85°C, V_{CC} = +5V ± 5%, V_{SS} = -5V ± 5%.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	Dx,IL = 3.2mA
				0.4	V	SIGr,IL = 3.2mA
				0.4	V	TSx,IL = 3.2mA (open drain)
V_{OH}	Output High Voltage	2.4			V	Dx,IH = -3.2mA
		2.4			V	SIGr,IH = -3.2mA
I_{IL}	Input Low Current	-10		+10	µA	GNDA≤VIN≤VIL
I_{IH}	Input High Current	-10		+10	µA	VIH≤VIN≤VCC
I_{OZ}	Output Current (High Z State)	-10		+10	µA	Dx,GNDA≤VO≤ VCC
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER						
I_{IXA}	Input Leakage Current	-200		+200	nA	-2.5V≤V≤+2.5V VFx+ or VFx-
R_{IXA}	Input Resistance	10			MΩ	-2.5V≤V≤+2.5V VFx+ or VFx-
R_{oXA}	Output Resistance		1	3	Ω	Closed loop
R_{IXA}	Load Resistance	10			KΩ	GSx
C_{IXA}	Load Capacitance			50	pF	GSx
V_{oXA}	Dynamic Range out	-2.8		+2.8	V	GSx,R_L≥10K
A_{VXA}	Voltage Gain	5000			V/V	VFx+ to GSx
F_{uXA}	Bandwidth (unity)	1	2		MHz	
V_{osXA}	Offset Voltage	-20		+20	mV	
V_{cmXA}	Common Mode Voltage	-2.5		+2.5	V	CMRRXA > 60db
CMRRXA	Rejection Ratio CM	60			dB	DC Test
PSRRXA	Rejection Ratio PS	60			dB	DC Test
ANALOG INTERFACE WITH RECEIVE FILTER						
R_{IRF}	Output Resistance		1	3	Ω	Pin VFrO
R_{IRF}	Load Resistance	600			Ω	VFrO = +/-2.5V
C_{IRF}	Load Capacitance			500	pF	
V_{OSrO}	Output DC Offset	-200		+200	mV	
POWER DISSIPATION						
I_{CC0}	Power Down Current		0.5	1.5	mA	No Load
I_{BB0}	Power Down Current		0.05	0.3	mA	No Load
I_{CC1}	Power Active Current		6.0	9.0	mA	No Load
I_{BB1}	Power Active Current		6.0	9.0	mA	No Load

TRANSMISSION CHARACTERISTICS

Unless specified otherwise the following characteristics are guaranteed from TA = -40°C to +85°C, V_{DD} = +5V ± 5%, V_{SS} = -5V ± 5%.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
	Absolute Levels		1.227		Vrms	0 dbm 0 = 4dbm
t_{MAX}	Max Overload Level		2.501		Vpk	XR-T3052/53/54
G_{XA}	Transmit Gain Absolute	-0.15		+0.15	db	XR-T3052/53/54/57 GSx = 0 dbm0 @ 1020Hz
G_{XR}	Transmit Gain Relative to GXA			-40	db	f = 16Hz
				-30	db	f = 50Hz
				-22	db	f = 60Hz
		-1.8		+0.15	db	f = 200Hz
		-0.15		+0.15	db	f = 300Hz to 3000Hz
		-0.35		+0.05	db	f = 3300Hz
		-0.7		0	db	f = 3400Hz
				-14	db	f = 4000Hz
				-32	db	f = 4600Hz and up
G_{XAT}	Transmit Gain Variations with Temperature	-0.1		+0.1	db	Relative to GXA
G_{XAV}	Absolute Gain Variations with Supply Voltage	-0.05		+0.05	db	Relative to GXA
G_{XRL}	Transmit Gain Variation with Level	-0.2		+0.2	db	VFx+ = -40 to +3dbm0
		-0.4		+0.4	db	VFx+ = -50 to -40dbm0
		-1.2		+1.2	db	VFx+ = -55 to -50dbm0 Sinusoidal Test
G_{RA}	Receive Gain, Absolute	-0.15		+0.15	db	Digital Code Input at 1020Hz @ 0dbm0
G_{RR}	Receive Gain, Relative to GRA	-0.15		+0.15	db	f = 0 to 3000Hz
		-0.35		+0.05	db	f = 3300Hz
		-0.7		0	db	f = 3400Hz
				-14	db	f = 4000Hz
G_{RAT}	Absolute Gain Variation (Receiver) over Temperature	-0.1		+0.1	db	Relative to GRA
G_{RAV}	Absolute Gain Variation (Receiver) over Supply Voltage	-0.05		+0.05	db	Relative to GRA
G_{RRL}	Receive Gain Variation with Level	-0.2		+0.2	db	-40 to 3dbm0
		-0.4		0.4	db	-50 to 3dbm0
		-1.2		1.2		-55 to -50dbm0 Sinusodial test method
V_{RO}	Receive Output Drive	-2.5		+2.5	V	Rl = 600Ω
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay (Abs)		290	315	µsec	f = 1600Hz
D_{XR}	Transmit Delay (Relative to DXA)		195	220	µsec	f = 500 to 600Hz
			120	145	µsec	f = 600 to 800Hz
			50	75	µsec	f = 800 to 1000Hz
			20	40	µsec	f = 1000 to 1600Hz
			55	75	µsec	f = 1600 to 2600Hz
			80	105	µsec	f = 2600 to 2800Hz
			130	155	µsec	f = 2800 to 3000Hz
D_{RA}	Receive Delay (Abs)		180	200	µsec	f = 1600Hz

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DRR	Receive Delay	-40	-25		µsec	f = 500 to 1000Hz
	Relative to DRA	-30	-20		µsec	f = 1000 to 1600Hz
			70	90	µsec	f = 1600 to 2600Hz
			100	125	µsec	f = 2600 to 2600Hz
			145	175	µsec	f = 2800 to 3000 Hz
NOISE						
N_{XC}	Transmit Noise C Message Weighted		12	15	dbmCO	XR-T3052/53/54
N_{XP}	Transmit Noise P Message Weighted		-74	-67	dbmCO	XR-T3057
N_{RC}	Receive Noise C Message Weighted		8	11	dbmOP	XR-T3052/53/84 PCM Code
N_{RP}	Receive Noise P Message Weighted		-82	-79	dbmOP	XR-T3057
N_{RS}	Noise, Single Frequency			-53	dbmO	f = 0 to 100KHz VFx+ = 0Vrms
PPSRx	Positve Power Supply Rejection, Transmit	40			dbC	VFx+ = -50dbm0 V_{CC} = 5Vdc+ 100mVrms, f = 0 to 50KHz
NPSRx	Negative Power Supply Rejection Transmit	40			dbC	VFx+ = -50dbm0, Vee = -5Vdc+100mV, f = 0 to 50KHz
PPSRr	Positive Power Supply Rejection,	40			dbC	f = 0 to 4000Hz
	Receive	40			db	f = 4KHz to 25KHz
		36			db	f = 25KHz to 50KHz
NPSRr	Negative Power Supply Rejection	40			dbC	f = 0 to 4000Hz
	Receive	40			db	f = 4KHz to 25KHz
		36			db	f = 25KHz to 50KHz
SOS	Spurious Out-of-band Signals at the Channel Output			-30	db	0 dbm0, 300Hz to 3400Hz, Input = Dr, Loop Around Measurement
				-30	db	f = 4600 to 7600Hz
				-40	db	f = 7600 to 8400Hz
				-30	db	f = 8.4 to 100KHz
DISTORTION						
STDx	Signal/Distortion	33			dbC	3 db level
STDr	Transmit or Receive Half	36			dbC	0 to -30db level
	Channel	29			dbC	-40dbm0 (XMT)
		20			dbC	-40dbm0 (RCV)
		14			dbC	-55dbm0 (XMT)
		15			dbC	-55dbm0 (RCV)
SFDx	Single Frequency Distortion, Transmit			-46	db	
SFDr	Single Frequency Distortion, Receive			-46	db	
IMD	Intermodulation Distortion			-41	db	VFx+ = -4 to 21dbm0, 300Hz< f<3400Hz

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
CROSSTALK						
CTx-r	Transmit To Receive Crosstalk, Level = 0dbm		-90	-75	db	f=300 to 3400Hz Dr = Quiet dbm Code
CTr-x	Receive to Transmit Crosstalk, Level = 0dbm		-90	-70	db	f=300 to 3400Hz VFx = Multitone

AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25° C, V_{SS} =-5V+/-5%, V_{DD} = 5V+/-5%, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
$1/t_{PM}$	Master Clock Frequency		1.536 1.544 2.048		MHz MHz MHz	See Table 1
t_{WMH}	Width (MCLK High)	160			ns	MCLKx, MCLKr
t_{WML}	Width (MCLK Low)	160			ns	MCLKx, MCLKr
(t_{SBFM})	Set-Up Time BCLK high to MCLK low	100			ns	Bit after FSx edge
t_{WBH}	Bit Clock Width	160			ns	VIH = 2.2V
t_{WBL}	Bit Clock Low	160			ns	VIL = 0.6V
t_{HBFL}	Hold Time (Bit Clock Low to FS)	0			ns	Long Frame Only
t_{HBFS}	Hold Time (Bit Clock High to FS)	0			ns	Short Frame Only
t_{SFB}	Set Up Time (FS to Bit Clock Low)	80			ns	Long Frame Only
t_{DBD}	Delay (BCLK high to Data Valid)	0	140		ns	Load = 150pF
t_{DBTS}	Delay (to TSx low)	140			ns	Load = 150pF
t_{DZC}	Delay (BCLKx low-Data Out Disabled)	50		165	ns ns	C = 0 to 150pF
t_{DZF}	Delay (Data Valid from FSx or BCLKx	20		165	ns	C = 0 to 150pF
t_{SSFF}	Set-Up (SFx/r to high to FSx/r)	60			ns	XR-T3053
t_{SSFB}	Set-Up (SF Sync to high to BCLKx/r	60			ns	XR-T3053
t_{SSGB}	Set-Up (SIGx to BCLKx)	100			ns	XR-T3052 & XR-T3053
t_{HBSG}	Hold Time (BCLK high to SIGx)	50			ns	XR-T3052 & XR-T3053
t_{SDB}	Set-Up (Dr valid to BCLKr/x low)	50			ns	
t_{HBD}	Hold Time (BCLKr/x low to Dr valid)	50			ns	
t_{HBSF}	Hold Time (BCLKx/r low to SF Sync)	100			ns	XR-T3053
t_{SF}	Set-Up Time (FSx/r to BCLKx/r low)	50			ns	Short Frame Sync Pulse
t_{HF}	Hold Time (BCLKx/r low to FSx/r low)	100			ns	Short Frame Sync Pulse
t_{HBFI}	Hold Time (Bit CLK 3rd Period to FSr or FSx)	100			ns	Long Frame Sync Pulse
t_{WFL}	Minimum Width of Frame Sync Pulse	160			ns	64Bit/sec
t_{RM}	Rise Time of MCLK	50			ns	MCLKr,MCLKx
t_{FM}	Fall Time of MCLK	50			ns	MCLKr,MCLKx
t_{PB}	Bit Clock Period	485	488	15725	ns	

ENCODING FORMAT		
	T3052/3053/3054	XR-T3057
V IN (at GSX) = +Full Scale	10000000	10101010
V IN (at GSX) = 0V	11111111	11010101
	01111111	01010101
V IN (at GSX) = -Full Scale	00000000	00101010

SYSTEM DESCRIPTION

The XR-T3052/53/54/57 consist of two major blocks; the COder or the transmit section and the DECoder or the receive section plus timing and control sections.

TRANSMITTER/RECEIVER SECTION

The encoder portion of each device consists of an input gain adjust amplifier with provisions for gain adjustment using two external resistors to set the required gain. This amplifier stage allows amplification of the audio signals in excess of 20 db across the audio passband with satisfactory low noise and wide bandwidth. The output of the amplifier drives a distributed RC network, followed by an eighth order switched capacitor band pass filter. The resulting band-pass characteristics meet the G.712 specifications. The sample and hold circuit follows this band pass filter and passes the sampled information to the analog to digital encoder. The circuitry used for coding and encoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and resistors to define steps. These steps are predefined according to U-law (XR-T3052/53/54) or A-law (XR-T3057) coding conventions. The frame sync pulse (FSx) is needed to control the sampling of the filter output, and start each encoding cycle. The 8-bit codes are then loaded into a buffer and shifted out through Dx at the next FSx pulse. The DC offset cancellation is achieved with an autozero logic circuitry which operates by integrating the sign bit of the PCM data and feeding it back to the noninverting input of the comparator.

The decode portion of each device consist of an expanding decoder, which reconstructs the analog signal from the companded U-law (XR-T3052/53/54) or A-law (XR-T3057) code. The output of this section drives a sixth order low pass filter, and is used to correct for the sinx/x response of the decoder output. The outputpower amplifier is capable of driving a 600 ohm load to a level of 7.2 dbm. Upon the occurrence of FSr, the data at the Dr input is clocked in on the falling edge of the next eight BCLKr periods. At the end of the decoder time slot, the decoding cycle begins, and the decoder digital to analog circuit output is updated.

SYNCHRONOUS/ASYNCHRONOUS OPERATION

In a synchronous operation, the same bit clock should be used for both transmitter and receiver. A bit clock must be applied to BCLKx and BCLKr/CLKSEL can be used to select the proper internal divider for a masterclock of 1.536 MHz, 1.544 MHz or 2.048 MHz as shown in table 1. If 1.544 MHz clock is supplied, the device automatically compensates for the 193rd framing bit pulse. BCLKx may vary from 64 KHz to 2.048 MHz. The FSx pulse starts the encoding cycle and it also enables the Dx output to shift out the previously encoded PCM bits on the positive edge of BCLKx. The tri-state Dx output then returns to a high impedance state. On the receive side PCM data from Dr is latched on the negative edge of BCLKx with an FSr pulse.

For asynchronous operation, separate transmit and receive clocks may be applied. Applying only static logic levels to the MCLKr/PDN pin will automatically connect MCLKx to all internal MCLKr functions. FSx starts each encoding cycle and must be synchronous with BCLKx. In the asynchronous mode the logic levels shown in table 1 do not apply anymore, but the bit clocks (BCLKr and BCLKx) may still operate from 64 KHz to 2.048 MHz. The FSr pulse starts each decoding cycle and must be synchronous with BCLKr.

	Master Clock Frequency Selected	
BCLKR/CLKSEL	TP3057	TP3052 TP3053 TP3054
Clocked	2.048MHz	1.536MHz or 1.544 MHz
0	1.536MHz or 1.544MHz	2.048MHz
1 (or Open Circuit)	2.048MHz	1.536MHz or 1.544MHz

Table 1. Selection of Master Clock Frequencies

FRAME SYNCHRONIZATION

The XR-T3052/53/54/57 can utilize either a short or long frame sync pulse. Upon power initialization, the device will be set to short frame mode. In this mode both FSx and FSr must be one bit clock period long. With FSx high during a falling edge of BCLKx, the next rising edge of BCLKx enables the Dx output. With FSr high during a falling edge of BCLKr, the next falling edge of BCLKr latches in the sign bit. The following seven falling edges latch in the seven remaining bits.

To use long sync frame mode, FSx or FSr, must be three or more bit clock periods long. Based on the transmit frame sync pulse (FSx), the XR-T3052/53/54/57 will sense whether short or long frame sync pulses are being used. For 64 KHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The Dx three state output buffer is enabled with the rising edge of FSx or the rising edge of BCLKx, whichever comes later, and the first bit clocked out is the sign bit. The following seven bits will be clocked out on next rising edge of the BCLKx. The Dx output is disabled by the falling BCLKx edge following the eight rising edges, or by FSx going low, whichever comes later. A rising edge on the receive frame sync pulse, FSr will cause the PCM data at Dr to be latched in on the next eight falling edges of BCLKr (BCLKx in the synchronous mode. The long frame sync pulse may be utilized in both, the synchronous and asynchronous mode.

SIGNALING

The XR-T3052 is a U-law CODEC intended to be used for short frame sync applications and be able to insert and extract signaling from the PCM data stream.

The XR-T3053 has the same characteristics as the XR-T3052 except it can be used for short and long frame sync pulses.

The XR-T3054 is also U-law but has no provisions for signaling.

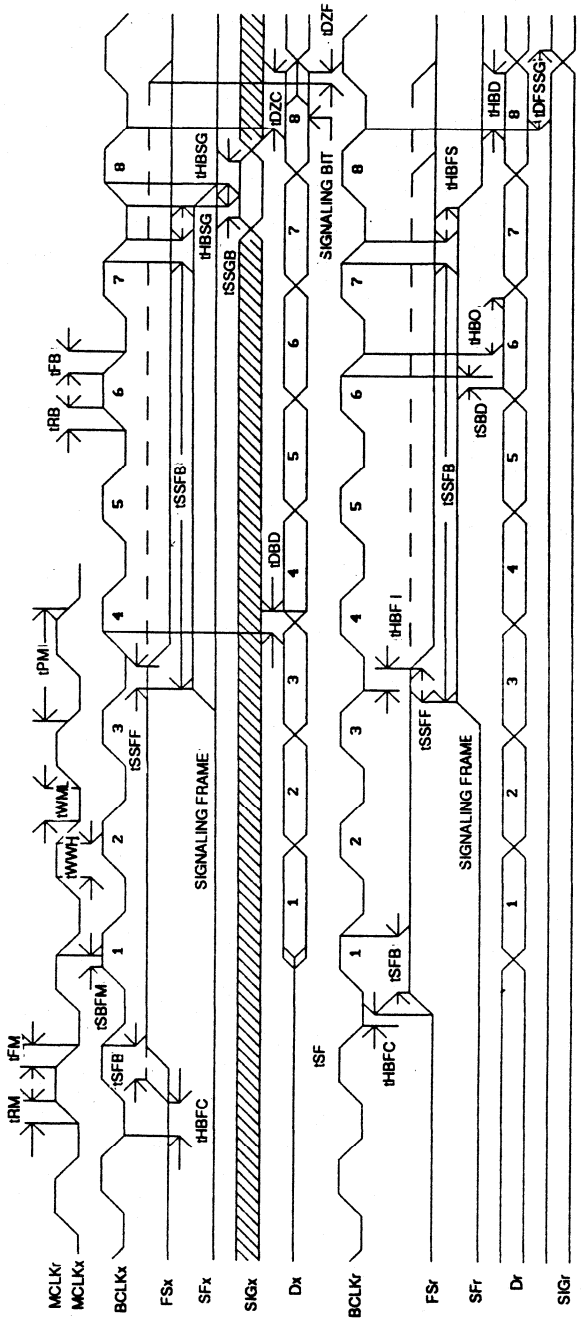
The XR-T3057 uses A-law companding technique and has no provisions for signaling.

Signaling is accomplished by insertion of the data present on the SIGx input, whenever a frame sync pulse (two bits long) is present. The signaling data is inserted LSB in the PCM data transmitted during that frame. Similar, with a FSr two bit clock periods long, the LSB of the PCM data read into the Dr input will be latched and appear on the SIGr output pin until updated following the next signaling frame.

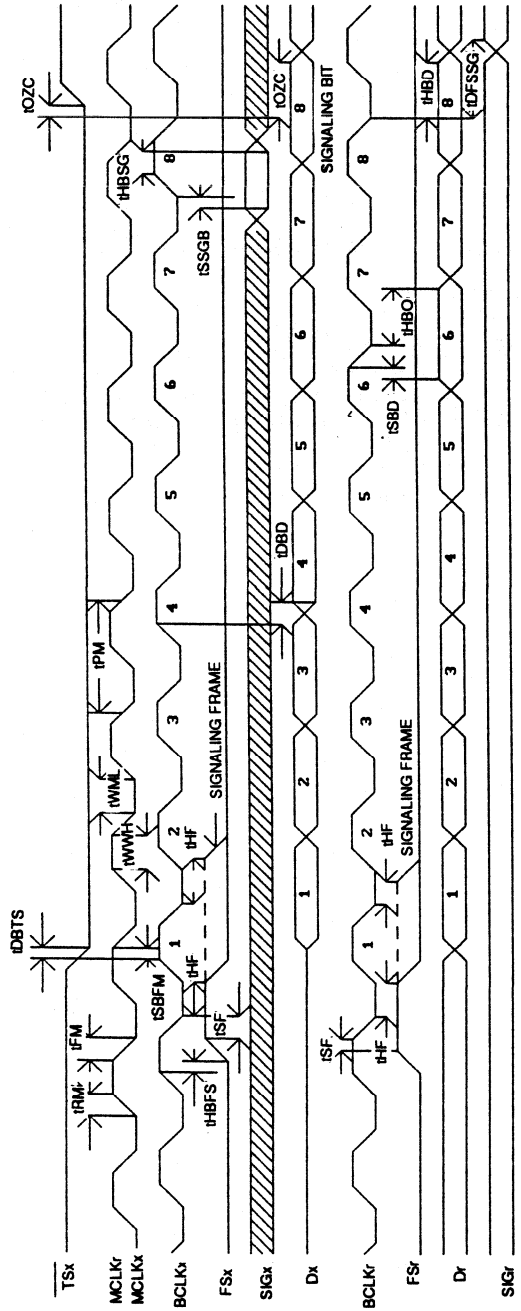
The short frame signaling may also be implemented using the XR-T3053, providing SFr and SFx are left open circuit or tied to ground. As mentioned prior, the XR-T3052 can not insert or extract signaling information in the long frame mode, while the XR-T3053 can in both modes. In the long framing mode, two additional frame sync pulses are required (SFx and SFr), which indicate the respective transmit and receive signaling frames. Operation is such, that the data present at the SIGx input will be inserted as the LSB into the PCM data transmitted during that frame. Similar, with a signaling frame sync (SFr), the LSB of the PCM data is latched at Dr and will appear on the SIGr output pin until the next signaling frame.

POWER UP

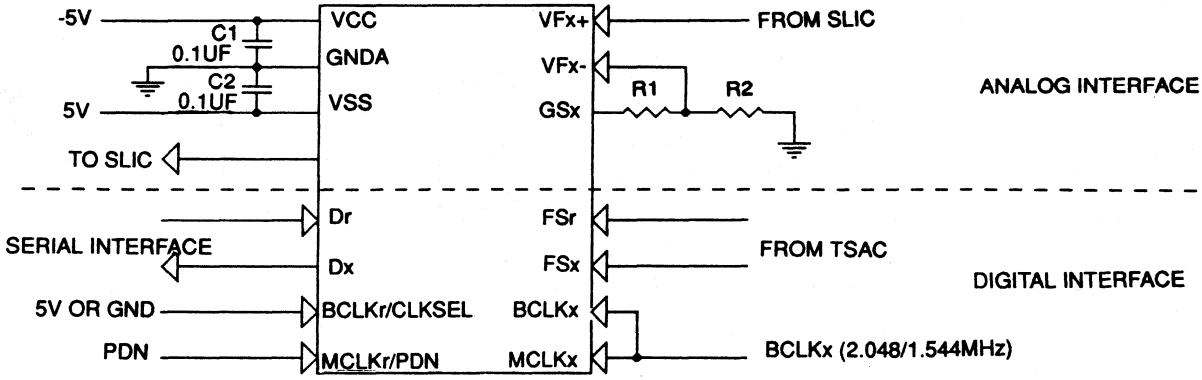
Initially, at power-up the COMBO is put into a power down state.This way all essential circuits are deactivated and the Dx and VFro outputs are put into a high impedance state. To activate the device [a logical low level or clock (MCLKr/PDN)] and [FSx or FSr pulses] need to be present. Note now that two different power-down control modes are available. One, to put MCLKr/PDN pin into a high state, and second, to keep both (FSr and FSx) continuously low. The approximate power-down delay after the last FSx or FSr pulse is 2msec. The first FSx or FSr pulse powers the device up but keeps the Dx output drive in a high impedance state until the next FSx pulse.



LONG FRAME SYNC TIMING



SHORT FRAME SYNC TIMING



Note: 1) Xmit Gain = 20 Log (R1 + R2) / R2 where (R1 + R2) > 10Kohm
2) C1 & C2 need to be connected as close as possible to the device for proper operation.

TYPICAL SYNCHRONOUS APPLICATION CIRCUIT FOR THE XR-T3052/53/54/57

B8ZS/AMI Line Transcoder

GENERAL DESCRIPTION

The XR-T5670 is an LSI CMOS integrated circuit which performs the B8ZS or AMI transmission coding and receiving decoding functions with error detection. It is intended for DS1 (1.544 Mbits/s) PCM transmission applications, but can operate at clock frequencies up to 6 MHz.

FEATURES

B8ZS Coding and Decoding for Data Rates up to 6 Mbits/s to AT&T Technical Advisory 69
B8ZS/AMI Transmission Coding/Reception Decoding with Code Error Detection
All Transmitter and Receiver Inputs/Outputs are TTL Compatible
Internal Loop Test Capability
Single 5 V ± 10% Supply Rail

APPLICATIONS

AMI Encoding/Decoding
B8ZS Encoding/Decoding

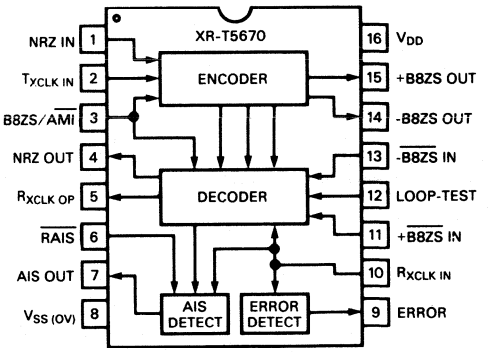
ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (V_{DD})	-0.3 to 7.0 V
Input Voltage Range (V_{IN})	-0.3 to V_{DD} + 0.3 V
Input Protection Current (I_D)	±10 mA
Storage Temperature Range	-55°C to 150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5670CP	Plastic	0°C to 70°C
XR-T5670CN	Ceramic	-40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

Coder

Binary data in "NRZIN" is clocked into the coder by a synchronous transmission clock "TXCLKIN" on the falling edge. The "+B8ZS" and "-B8ZS" output signals appear 8.5 clock cycles later to allow for the insertion of extra pulses due to sequences of eight consecutive zeros. These two signals are full width data and will be mixed with the "TX CLKIN" at the input of an external line driver to produce bipolar B8ZS signals for transmission.

Decoder

Received half width data on "+$\overline{\text{B8ZSIN}}$" and "-$\overline{\text{B8ZSIN}}$" are locked into the decoder on the rising edge of the received clock "RXCLKIN". The "NRZOUT" binary data output occurs on eight clock cycles later. Received signals not consistant with B8ZS coding rules are detected as errors. The error output "ERROR" is active high during one "RXCLKIN" clock period.

AIS (Alarm Indication Signal)

If the decoder inputs received a continuous of ones (all marks) over two consecutive periods of the external reset signal "$\overline{\text{RAIS}}$", the "AISOUT" output will be set high and latched in that state until one or more zeros are received when the next reset signal "$\overline{\text{RAIS}}$" occurs.

The number of received zeros required to reset "AISOUT" over two consectuive periods of "$\overline{\text{RAIS}}$" can be mask programmed to two or three.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = -40°C$ to $+85°C$, $V_{DD} = 4.5$ to 5.5 V, unless specified otherwise.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DYNAMIC CHARACTERISTICS						
T_{XCLKIN}	Clock Input Frequency			6	MHz	
R_{XCLKIN}	Clock Input Frequency			6	MHz	
t_{s1}	Data Set-Up Time	55			ns	NRZIN to T_{XCLKIN} See Figure 6
t_{h1}	Data Hold Time	25			ns	NRZIN to T_{XCLKIN} See Figure 6
t_{pd1}	Data Propagation Delay Time			65	ns	T_{XCLKIN} to B8ZS OUT See Figures 3 and 6, Note 1
t_{s2}	Data Set-Up Time	55			ns	B8ZSIN to R_{XCLKIN} See Figure 7, Loop Test = 0
t_{h2}	Data Hold Time	0			ns	B8ZSIN to R_{XCLKIN} See Figure 7, Loop Test = 0
t_{pd2}	Data Propagation Delay Time			90	ns	R_{XCLKIN} to NRZOUT See Figures 4 and 7, Note 2 Loop Test = 0
t_{pd3}	Clock Delay Time			50	ns	R_{XCLKIN} to $R_{XCLKOUT}$ See Figure 8, Loop Test = 0
t_{s3}	RAIS = 0 Set-Up Time	30			ns	RAIS to R_{XCLKIN} See Figure 7
t_{h3}	RAIS= 0 Hold Time	30			ns	RAIS to R_{XCLKIN}
STATIC CHARACTERISTICS, $V_{DD} = 5.0$ V						
I_{DD}	Quiescent Device Current			100	μA	
	Operating Current			4	mA	Input Clock Frequency = 2.0MHz
V_{DD}	Supply Voltage	4.5	5	5.5	V	
V_{IN}	Input Voltage 0	0		5.0	V	
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2			V	
V_{OL}	Output Low Voltage			0.1	V	$I_{OL} = 0$
V_{OH}	Output High Voltage	4.9			V	$I_{OH} = 0$
I_{OL}	Output Low Current	1.6			mA	$V_{OL} = 0.4$ V
I_{OH}	Output High Current	-1			mA	$V_{OH} = 4.6$ V
I_{IL}	Input Low Current			-10	μA	$V_{IL} = 0$ V
I_{IH}	Input High Current			10	μA	$V_{IH} = 5$ V

Note 1: The encoded B8ZS OUT are delayed by 8½ clock periods from NRZIN.
Note 2: The decoded NRZOUT are delayed by 7½ clock periods from B8ZS IN.

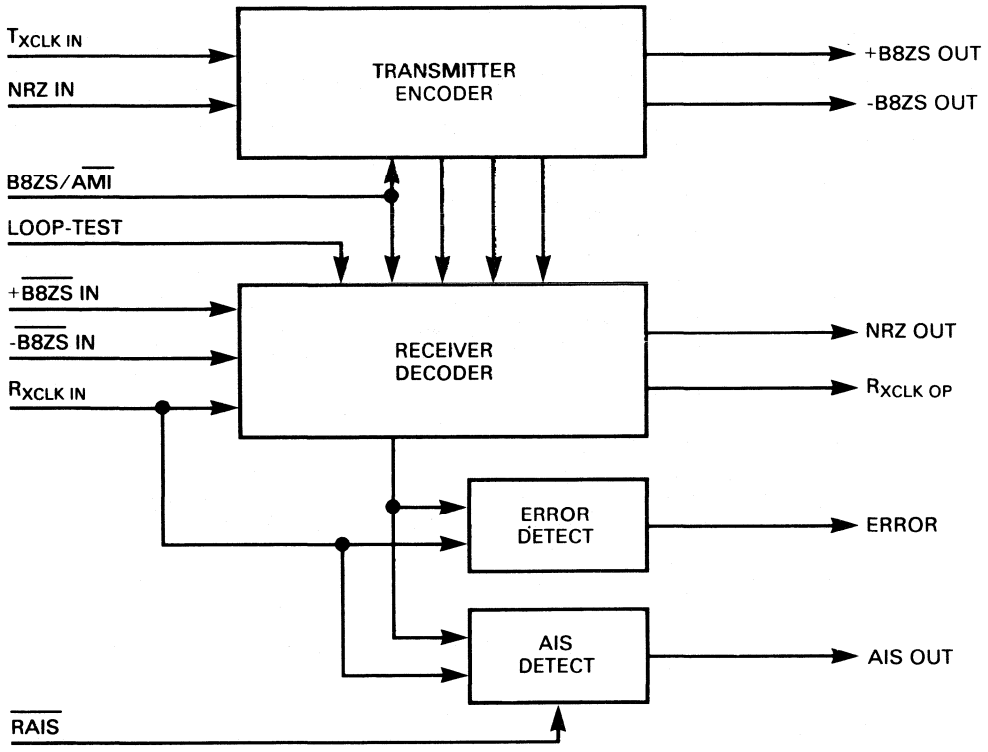


Figure 1. XR-T5670 Block Diagram

Loop Test

When the Loop Test control input is set high, a test mode is made in which the "+B8ZSOUT" and "-B8ZSOUT" are internally connected to the decoder inputs. The external B8ZS inputs and the "RXCLKIN" are disabled, and the "TXCLKIN" is used to control the decoder timing. The "NRZOUT" signals correspond to the "NRZIN" input, but delayed by 16 clock periods.

B8ZS/AMI

To operate the XR-T5670 in AMI mode, the B8ZS/AMI control input is driven low. In this mode, two consecutive pulses of the same polarity at the decoder inputs will be detected and flagged as an error at the "ERROR" output.

Definition of B8ZS Code Used in XR-T5670 Transcoder

With B8ZS coding, each block of eight consecutive zeros is removed and the B8ZS code is inserted. If the pulse preceding the inserted code is transmitted as a positive pulse (+), the inserted code is 000+−0−+. Bipolar violations occur in the fourth and seventh bit position of the inserted code. If the pulse preceeding the inserted code is a negative pulse (−), the inserted code is 000−+0+−. Bipolar violations again occur in the fourth and seventh bit positions as illustrated in Figure 2.

Binary Signal	1	0	0	0	0	0	0	0	0
B8ZS Signal	+1	0	0	0	+1	−1	0	−1	+1
or	−1	0	0	0	−1	+1	0	+1	−1

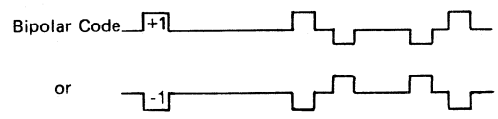


Figure 2. B8ZS Code

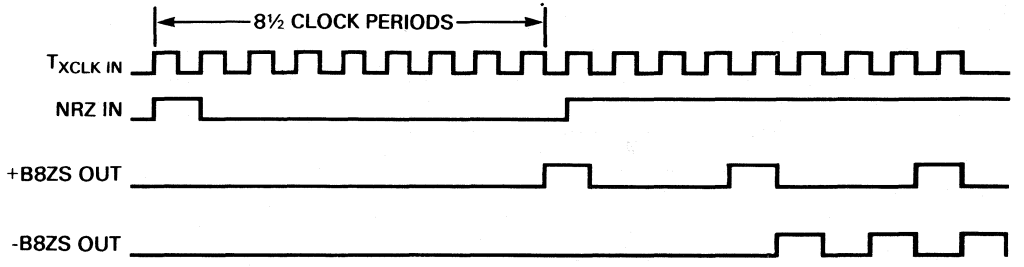


Figure 3. Encoder Waveforms

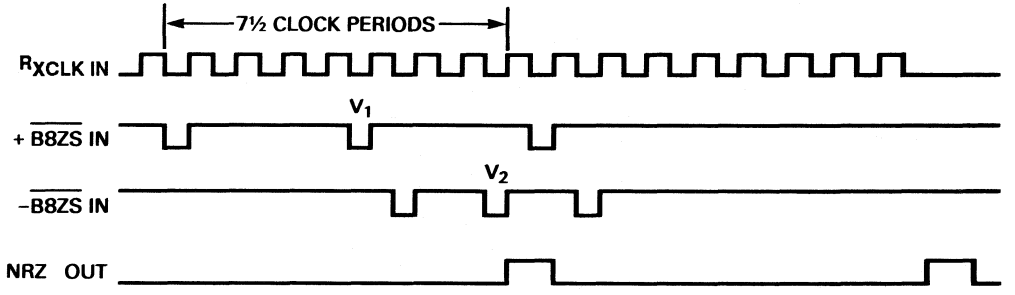


Figure 4. Decoder Waveforms

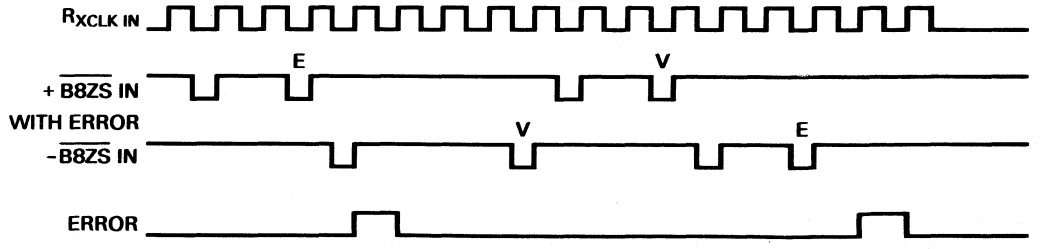


Figure 5. B8ZS Error Output Waveforms

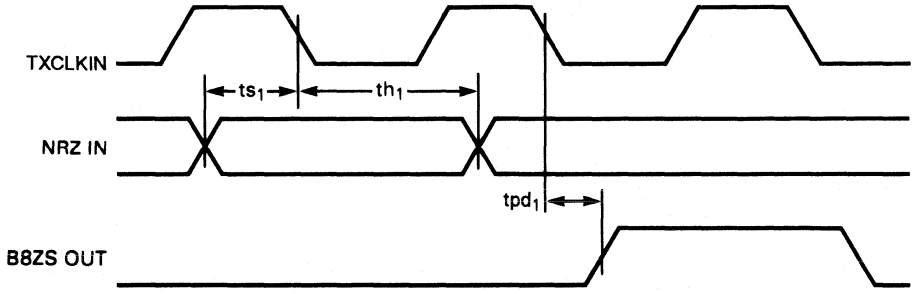


Figure 6. Encoder Timing Relationship

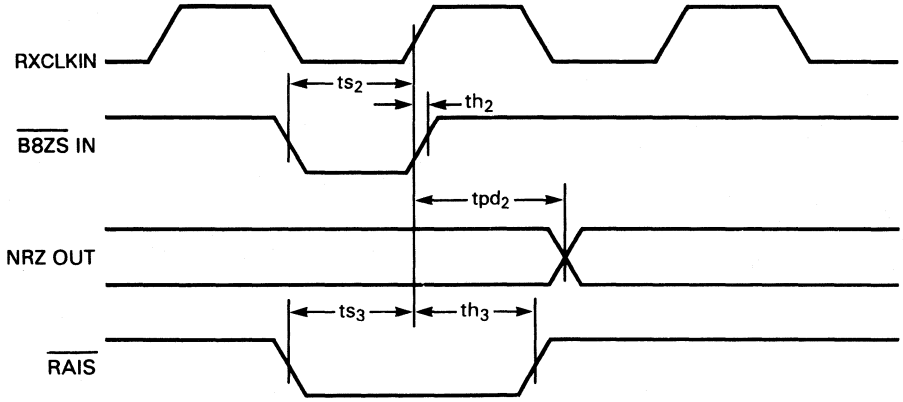


Figure 7. Decoder Timing Relationship

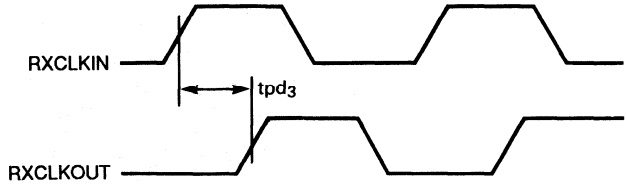


Figure 8. $R_{XCLK\ IN}$ to $R_{XCLK\ OUT}$ Relationship

Loopback Detector

GENERAL DESCRIPTION

The XR-T2713 is designed to be used in 4 wire maintenance terminating units in conjunction with manual or automatic testing systems in loopback mode to verify network performance.

Utilizing switched capacitor technology, the IC detects the 2713 or 2813Hz signal and performs a loopback function in accordance with BELL PUB 43004.

FEATURES

Bell Pub 43004 Compliant
Uses standard color TV crystal (3.58MHz)
Detection band 2713 or 2813 +/- 15Hz
Detection level -32 dbm
Complementary output signals
Low power (2 mA @ 12 Volts)
CMOS process
Pin Selectable 4/20 Minutes Time-out

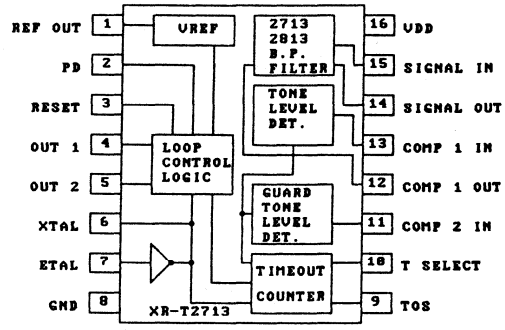
APPLICATION

4 wire maintenance terminating units

ABSOLUTE MAXIMUM RATINGS

DC Supply voltage	16 V
Voltage at any pin	GND -0.3V to V_{DD} +0.3V
Storage temperature range	-55°C to 150°C
Operating temperature range	0°C to 70°C
Power Dissipation	100 mW

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-T2713CP	Plastic DIP	0°C to 70°C

SYSTEM DESCRIPTION

The XR-T2713 contains the necessary band pass filters to meet the BELL PUB 43004 requirements on minimum and maximum detection levels and frequency rejection band. For the specified frequency detection band, a digital filter is used to maintain narrow bandwidth and decision making logic.

The tone detection output will be activated when a continuous tone of 2713/2813 +/- 15Hz is present for 1.8 seconds. Deactivation of the loopback signal will take place when a continuous tone of 2713/2813 +/- 15Hz is present for 0.45 seconds. If the deactivation tone is not received for 4 or 20 minutes (pin selectable), the XR-T2713 will reset automatically. The output signal is TTL compatible with a maximum output current capability of 1.5mA.

DC ELECTRICAL CHARACTERISTICS
Test Conditions: T_A = 25°C, V_{DD} = 12V±5% unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{DD}	Supply Voltage		12		V	
I_{DD}	Supply Current		4	5	mA	
I_P	Output Sink Current	1.5			mA	
V_T	Detection Level	-32		0	dBm	
T	Detection Frequency	2698	2713	2728	Hz	PIN 10 high
		2798	2813	2828	Hz	PIN 10 low
V_R	Tone Rejection Level	-38			dBm	
V_G	Signal to Guard Ratio	6	8	15	dB	

DC ELECTRICAL CHARACTERISTICS
Test Conditions: T_A = 25°C, V_{DD} = 12V±5% unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
t_{DD}	Tone Detection Time (on)		1.8		sec	Figure 1
t_{DF}	Tone Deactivation Time		.45		sec	Figure 1
t_{DO}	Detection on Time	20			msec	Figure 1
	Detection off Time	20			msec	Figure 1
t_{AB}	Tone Break			4	msec	Figure 1
t_F	Time Out		20		min	PIN 9 high, Figure 2
			4		min	PIN 9 low, Figure 2

PIN DESCRIPTIONS

Pin	Mnemonic	Description
1	REF OUT	Voltage reference output pin.
2	PD	The T2713 will be in power down mode when this pin is held high.
3	RESET	External power-up reset or manual loop back.
4	OUT-1	Upon detection of the 2713/2813 tone for a minimum of 1.8 seconds, pin 4 will go high to indicate that the system has entered the test mode. These outputs will be deactivated when a 2713/2813 tone is present for a minimum of 450 msec. If a deactivation tone is not received within 4 or 20 minutes (depending on the time out selection), the outputs will reset automatically.
5	OUT-2	Complementary output of OUT-1 (see pin 4).
6	XTAL	Crystal output pin.
7	ETAL	Crystal or external clock input pin.(Uses a standard color TV crystal at 3.58MHz)
8	GND	Most negative supply pin or ground.
9	TOS	Time Out selection pin. A low at this pin selects a 4 minute time out. A high level extends the time-out to 20 minutes.
10	T-SELECT	A high level at this pin selects the 2713Hz detection band and a low level selects the 2813Hz band.
11	COMP2 IN	Guardtone input coupled from pin 12.
12	COMP1 OUT	Guardtone output.
13	COMP1 IN	2713/2813 AC coupled frequency to tone and level detect circuitry.
14	SIGNAL OUT	2713/2813 Band pass filter output.
15	SIGNAL IN	Input of analog band pass filter
16	VDD	Most positive supply.

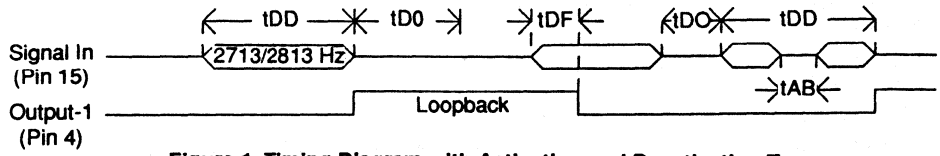


Figure 1. Timing Diagram with Activation and Deactivation Tones

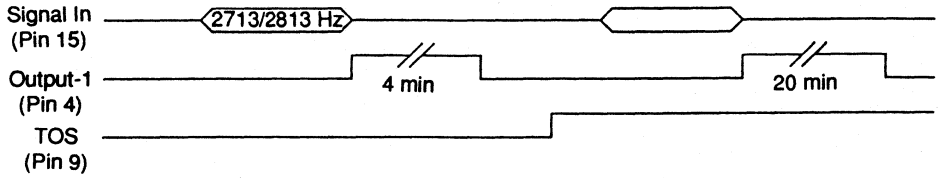


Figure 2. Timing Diagram without Deactivation Tone

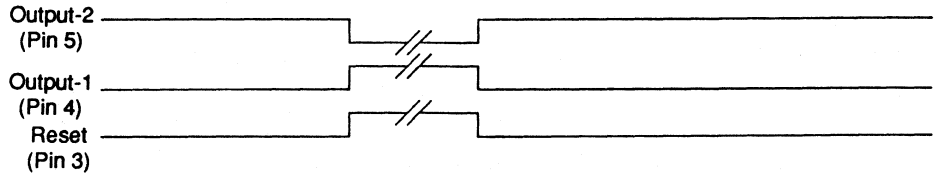
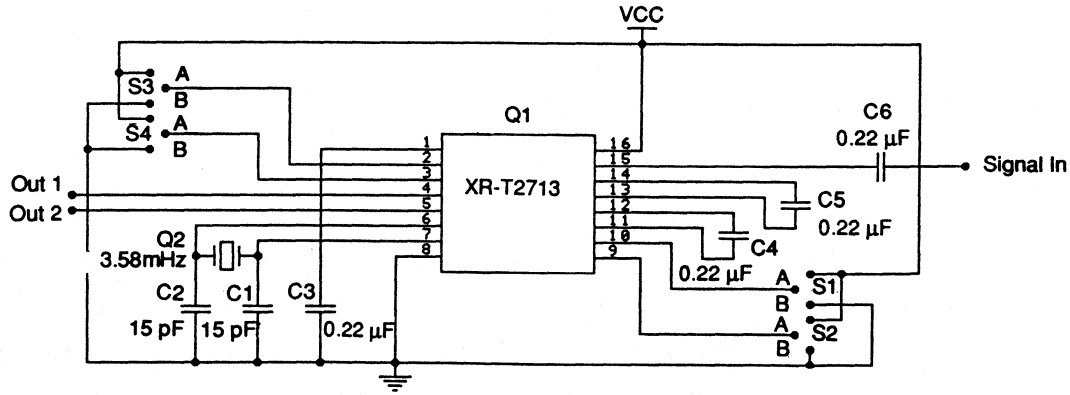


Figure 3. Manual Loopback Mode



	S4A	S4B
S3A	Factory Test	Power Down
S3B	Reset	Normal Op.

	A	B
S1	2813 Hz	2713 Hz
S2	20 min	4 min

Figure 4. Typical Application Circuitry

V.35 / Bell 306 Driver / Receiver

GENERAL DESCRIPTION

The V.35 chip set consists of two bipolar chips, one performing a receive function, the other a transmit function according to the specification requirements laid down in Appendix II of the V.35 CCITT Recommendation and Bell 306 modem interface specification.

Typical applications require three transmit and receive pairs to establish the link between distant DTE's at data rates ranging from 48Kbps to 10Mbps. To conserve power (especially in the case of the transmitter, which requires approximately 22mA for each output stage to meet CCITT specifications), power-down functions are included in both devices, allowing any of the three receive/transmit circuits to be disabled. All inputs and outputs are TTL compatible and designed to offer maximum versatility and performance.

Both the transmitter and receiver require termination resistors external to each device, to meet the V.35 specification tolerance.

FEATURES

Compatible with CCITT V.35 and Bell 306 Interface Requirements
TTL Input Compatibility
High Common Mode Output Voltage Range
Excellent Stability over Supply and Temperature Range
High Speed Operation (up to 10Mbps)
Individual Receive/Transmit Power-down capability

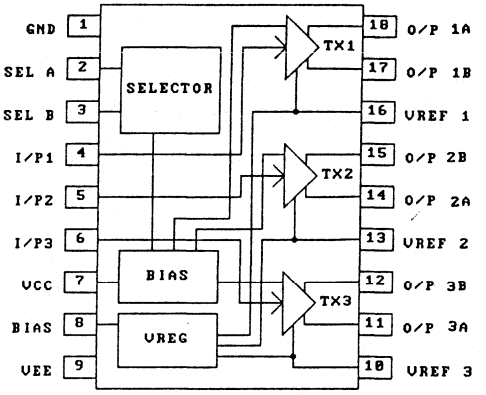
APPLICATIONS

High Speed Data Transmission Systems
Short Haul Modems
Signal Converters and Adapters
Network and Diagnostic Systems
Matrix Switches
Modem Emulators

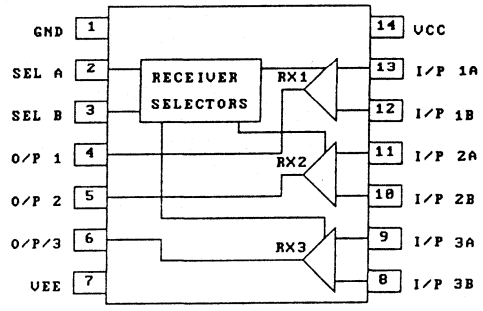
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+/- 7V
Storage Temperature	-65°C to +150°C
Power Dissipation	
XR-T3588 CN	1000mW
XR-T3589 CN	300mW

PIN ASSIGNMENT



XR-T3588



XR-T3589

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T3588CN	Ceramic	0°C to 70°C
XR-T3589CN	Ceramic	0°C to 70°C

TRANSMITTER: XR-T3588
SYSTEM DESCRIPTION

The function of the transmitter is to take a TTL input signal at a maximum bit rate of 10Mbps and output a balanced differential signal with a peak amplitude of 0.55V and a maximum DC offset of 0.6V. An internal buffer provides the regulated output voltage to set the mean level of the transmitters to less than 0.6V.

To meet the pulse shape and offset requirements laid down in the V.35 specification, the transmitter employs an internal temperature compensated voltage generator to provide reference voltages for both offset control and output current generation. Load resistors for the output stage, which provide the required source impedance for the transmitter, are external to the IC and are required to meet the V.35 specified tolerance.

To generate well defined output pulses, device current is set using an external resistor, which should be of the same type as the transmitter load resistors. Each device contains three independent transmit circuits.

Individual transmitters may be shut down to achieve power savings for applications not requiring three channels. Two TTL compatible inputs provide four combinations of transmitter configurations, as defined in table 1. If either of the select pins is left open a high state is adopted, hence with no inputs applied, all channels are powered up.

TRANSMITTER	SEL A	SEL B
1-2-3	HIGH	HIGH
1-2	HIGH	LOW
1	LOW	HIGH
ALL OFF	LOW	LOW

TABLE 1. TRANSMITTER SELECTORS

XR-T3588 DC ELECTRICAL CHARACTERISTICS (TRANSMITTER)
Test Conditions: V_{CC} = 5V ± 5%, V_{EE} = -5V ± 5%, T_A = 0°C -70°C

SYMBOL	PARAMETER	PINS	MIN	TYP	MAX	UNITS	CONDITIONS
V_{CC}	Positive Supply Voltage	7	4.75	5	5.25	V	
V_{EE}	Negative Supply Voltage	9	-4.75	-5	-5.25	V	
I_{CC}	Input Current	7		86	124	mA	
I_{EE}	Input Current	9	-133	-92	-132	mA	
I_{PD}	Power Down Input Current	2-6		0.4		mA	Per Transmitter
I_{PCCO}	Power Down I_{CC} Current			9.2		mA	No Termination Resistors
I_{PEEO}	Power Down I_{EE} Current			11.6		mA	No Termination Resistors
I_{PCCT}	Power Down I_{CC} Current			51		mA	With Termination Resistors
I_{PEET}	Power Down I_{EE} Current			11.6		mA	With Termination Resistors
V_{IH}	High Level Input Voltage		-2			V	
V_{IL}	Low Level Input Voltage				0.8	V	
V_{OL}	Output Low Voltage			-0.275		V	Note 1
V_{OH}	Output High Voltage			0.275		V	Note 1
Z_S	Source Impedance		90	100	110	0hm	per CCITT V.35 Note 2
R_{GND}	Resistance to GND		135	150	165	0hm	per CCITT V.35 Note 2
I_{INH}	Input Current High			-10		µA	
I_{INL}	Input Current Low			1		mA	
I_{ODIFF}	Output Current Differential			22		mA	with 3.9K bias resistor

NOTE 1. O/P Terminated with 100 Ohm Differential Load across external network pins 11, 12, 14, 15, 17, 18.
NOTE 2. O/P Terminated with External Network pins 11, 12, 14, 15, 17, 18.
NOTE 3. O/P Terminated with External Network, common mode resistance between any pari of generator outputs and ground.

AC CHARACTERISTICS Test Conditions: V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, T_A = 0°C to 70°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
$t_{(PLH)}$	Input (I/P to O/P)		25	50	nsec	Note1
$t_{(PHL)}$	Input (I/P to O/P)		25	50	nsec	Note1
t_R	TX Rise Time		10	20	nsec	Note1
t_F	TX Fall Time		10	20	nsec	Note1

NOTE 1. O/P Terminated with External Network

RECEIVER: XR-T3589 SYSTEM DESCRIPTION

The XR-T3589 Line Receiver contains three identical receive circuits to complement the XR-T3588 Line Transmitter. Received differential signals are converted into a single TTL compatible output. The input stage is designed to meet the full V.35 noise and common mode input specification, when connected to an external termination network.

Individual receivers may be shut down to achieve power savings for applications not requiring three channels. Two TTL compatible inputs provide four combinations of receiver configurations, as defined in in table 2. If either of the select pins is left open a high state is adopted, hence with no inputs applied, all channels are powered up.

RECEIVER	SEL A	SEL B
1-2-3	HIGH	HIGH
1-2	HIGH	LOW
1	LOW	HIGH
ALL OFF	LOW	LOW

TABLE 2. RECEIVER SELECTORS

XR-T3589 DC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V ± 5%, V_{EE} = -5V ± 5%, T_A = 25°C

SYMBOL	PARAMETER	PINS	MIN	TYP	MAX	UNITS	CONDITIONS
V_{CC}	Supply Voltage	14	4.75	5	5.25	V	
V_{EE}	Supply Voltage	7	-4.75	-5	-5.25	V	
I_{CC}	Input Current	14		40	60	mA	All Receives Selected
I_{EE}	Input Current	7		7	9	mA	All Receives Selected
I_{OH}	High Level Current	4,5,6	40			uA	@ VOUT = 2.4V
I_{OL}	Low Level Current	4,5,6			-1.6	uA	@ VOUT = 0.4V
V_{OH}	High Level Output	4,5,6	2.4			V	
V_{OL}	Low Level Output	4,5,6			0.4	V	
Z_{IN}	Input Impedance			8		Kohm	Differential Note 2
Z_{IN}	Input Impedance		90	100	110	Ohm	per CCITT V.35 Note 1,2
R_{GND}	Resistance to GND		135	150	165	Ohm	per CCITT V.35 Note 1,2
V_{TH}	Power-down Threshold Voltage			2		V	
I_{PCC}	Power Down I_{CC} Current			1.1		mA	
I_{PEE}	Power Down I_{EE} Current			0.3		mA	

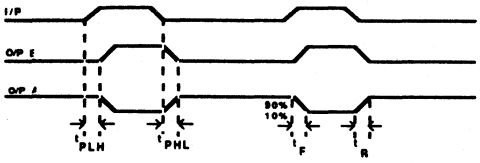
NOTE 1. I/P Terminated with External Network
NOTE 2. Pins (8,9), (10,11), (12-13)

AC CHARACTERISTICS

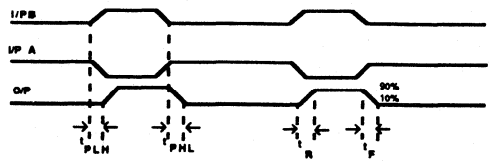
Test Conditions: V_{CC} = 5V ± 5%, V_{EE} = -5V ± 5%, T_A = 0°C to 70°C

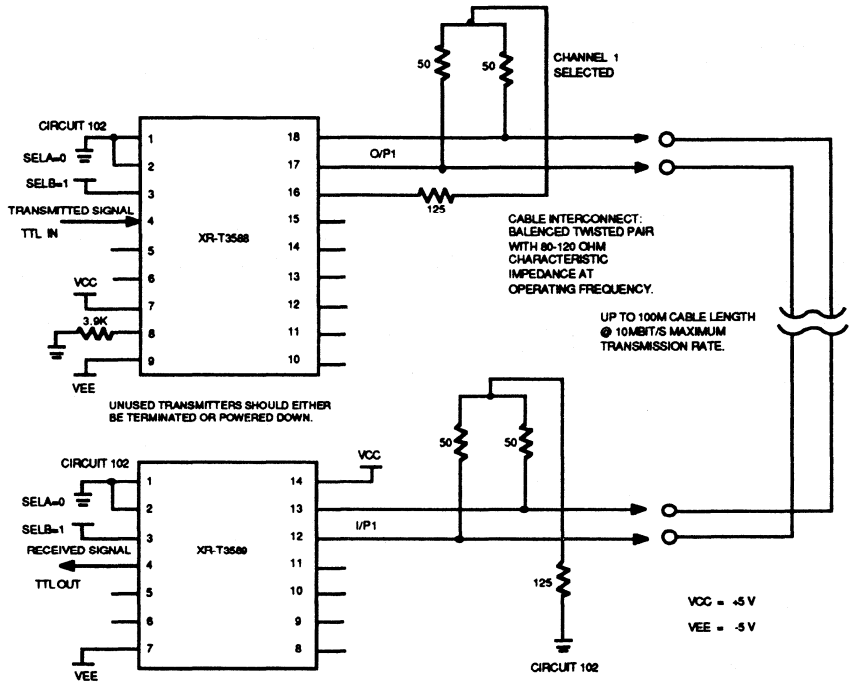
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
$t_{(PLH)}$	Input (I/P to O/P)		50	70	nsec	
$t_{(PHL)}$	Input (I/P to O/P)		50	70	nsec	
t_R	RX Rise Time		18	40	nsec	
t_F	RX Fall Time		12	30	nsec	

TRANSMITTER WAVEFORMS:



RECEIVER WAVEFORMS:





APPLICATION CIRCUIT XR-T3588, XR-3589.
(TERMINATION DIAGRAM)

PCM Line Receiver & Clock Recovery Circuit

GENERAL DESCRIPTION

The XR-T5650 is a monolithic bipolar IC designed for PCM type line receiver applications operating at T1. T148C, T1C and 2 M bit/s data rates. It provides all the active circuitry required to perform automatic line build out (ALBO), threshold detection, positive and negative data and clock recovery.

Clock recover using a crystal filter instead of an LC tank circuit is also available as XR-T5750.

FEATURES

On Chip Positive and Negative Data, Clock Recovery
Less than 10 ns Sampling Pulse over the Operating Range
Double Matched ALBO Ports
Single 5.1 V Power Supply
2 M Bit/s Capability

APPLICATIONS

T1 PCM Line Receiver
T148C Line Receiver
T1C PCM Line Receiver (requires external amplifier)
General Purpose Bipolar Line Receiver
HDB3 Line Receiver
B8ZS Line Receiver

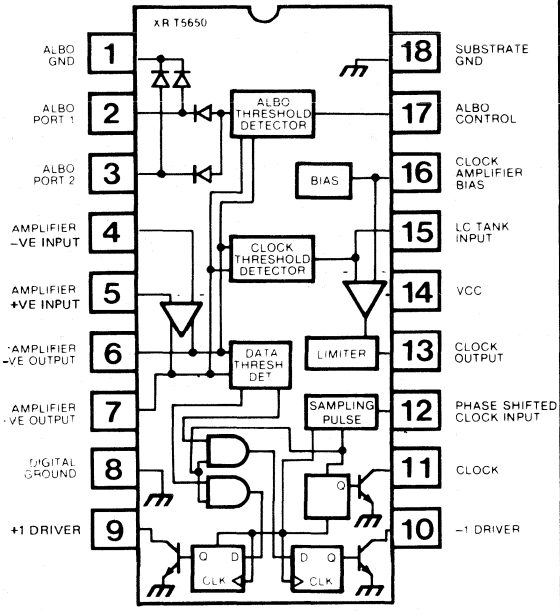
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	-40° to +85°C
Supply Voltage	-0.5 to +10 V
Supply Voltage Surge (10 ms)	+25 V
Input Voltage (except Pins 2,3,4,17)	-0.5 to 7 V
Input Voltage (Pins 2,3,4,17)	-0.5 to +0.5 V
Data Output Voltage (Pins 10,11)	20 V
Voltage Surge (Pins 5,6,10,11) (10 msec only)	50 V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5650	Ceramic	-40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-T5650 is designed for interfacing T1, T148C and 2 Mbit/s PCM carrier lines on plastic or pulp insulated cables. It can also be used at T1C rate (3.152 M bit/s) with external gain. Since it outputs plus and minus ones on a bipolar pulse stream together with the clock, it can be used to interface systems having different line codes like AMI, AMI-B8ZS or AMI-HDB3.

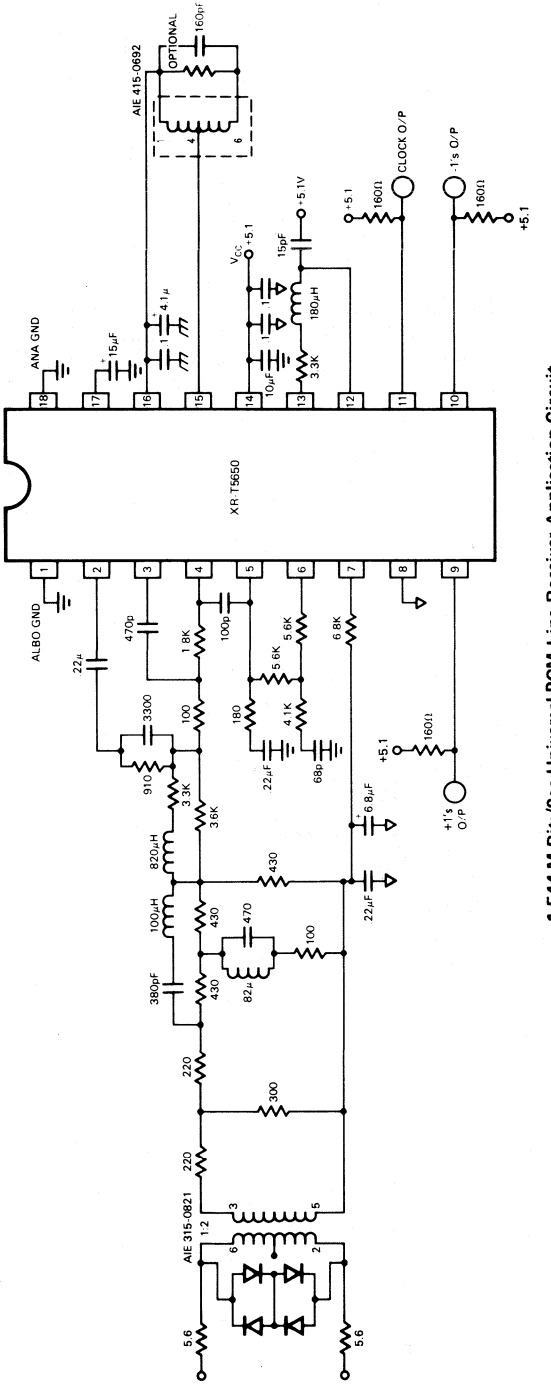
The XR-T5650 is a modified version of XR-T5620 PCM repeater IC. It contains all the active circuitry needed to build a PCM line receiver up to 6300 ft. cable length. The preamplifier, the clock amplifier, threshold detectors, data latches and output drivers are similar to the ones on XR-T5620. Clock extraction is done by means of an LC tank circuit.

In addition to plus and minus one outputs, a synchronous clock signal is made available at Pin 11 by deleting one of the ALBO ports on XR-T5620 thus leaving two matched ALBO ports. All outputs have high current open collector transistors.

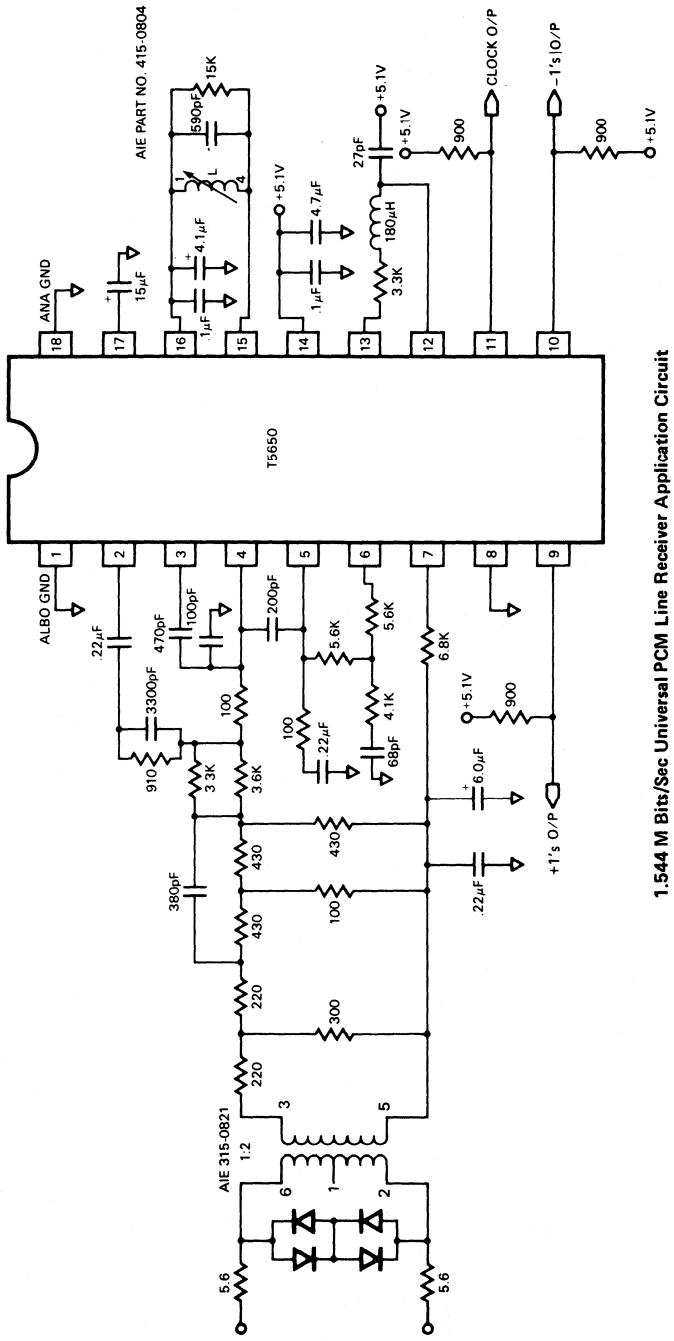
ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.1 V ± 5%, T_A = 25°C, unless specified otherwise.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Supply Current		26	34	mA	ALBO Off
	Clock & Data Output					
	Output Leakeage Current		0	100	μA	$V_{pull\text{-}up}$ = 15 V
	Amplifier Pin Voltages	2.4	2.9	3.4	V	At DC Unity Gain
	Amplifier Output					
	Offset Voltage	-50	0	50	mV	R_S = 8.2 kΩ
	Voltage Swing	2.2			V	Measured Differentially from Pin 7 to Pin 6
	Amplifier Input					
	Bias Current			5	μA	
	ALBO on Current	3			mA	
	Drive Current		1		mA	
AC CHARACTERISTICS						
	Pre Amplifier					
	AC Gain @ 1 MHz		50		dB	
	Input Impedance	20			kΩ	
	Output Impedance			200	Ω	
	Clock Amplifier					
	AC Gain		32		dB	
	-3 dB Bandwidth	10			MHz	
	Delay		10		ns	
	Output impedance			200	Ω	
	ALBO					
	Off Impedance	20			kΩ	
	On Impedance			25	Ω	
CLOCK DATA OUTPUT BUFFERS						R_L = 130Ω, $V_{pull\text{-}up}$ = 5.1 V ± 5%
	Rise Time		30		ns	
	Fall Time		30		ns	
	Output Pulse Width		244		ns	
	Sample Pulse Width		10		ns	
	V_{OL}		0.7		V	
	I_L sink		35		mA	
THRESHOLDS						
	ALBO	1.4	1.5	1.6	V	
	Clock Drive Current Peak		1.0		mA	At $V_O = V_{ALBO}$ Threshold
CLOCK THRESHOLD						
	% of ALBO	63	69	75	%	
DATA THRESHOLD						
	% of ALBO	40	46	52	%	



1.544 M Bits/Sec Universal PCM Line Receiver Application Circuit
Random Pattern – Max. Cable Loss 36 dB



1.544 M Bits/Sec Universal PCM Line Receiver Application Circuit

Maximum Cable Loss 25 dB

Dual Line Driver

GENERAL DESCRIPTION

The XR-T5675 is a bipolar monolithic dual line driver designed to drive PCM lines up to a 10 Mbits/s rate. The device is powered from a single 5V ± 5% source. Its current consumption is 14 mA (typical) and the output can be pulled up to 20VDC.

FEATURES

50 mA Output Drive Current Capability
Low Current Consumption (18 mA Max.)
High Speed Switching
Dual Matched Driver Outputs
High Output Voltage
TTL or DTL Compatible Inputs

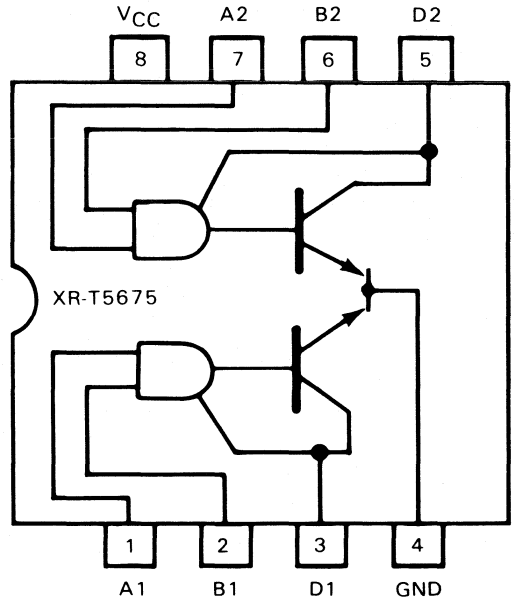
APPLICATIONS

T1, T1C, T2, 2048K and 8448K b/s PCM Line Driver
LAN Line Driver
Relay Driver
LED/Lamp Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	+7.0 V
Input Voltage (Pin 1,2,6,7)	−0.2 V to +V_{CC}
Output Pull-up Voltages (Pin 3,5)	+35.0 V
Power Dissipation	
Ceramic	700 mW
Plastic	600 mW
Storage Temperature	−65°C to 150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5675CP	Plastic	0°C to +70°C
XR-T5675CN	Ceramic	0°C to +70°C

SYSTEM DESCRIPTION

Figure 1 contains the Functional Block Diagram of the XR-T5675. The circuit consists of two AND logic gates with their outputs internally connected to the bases of the output transistors. The low level outputs are clamped at 1 VBE to ground to insure non-saturating operation for fast switching.

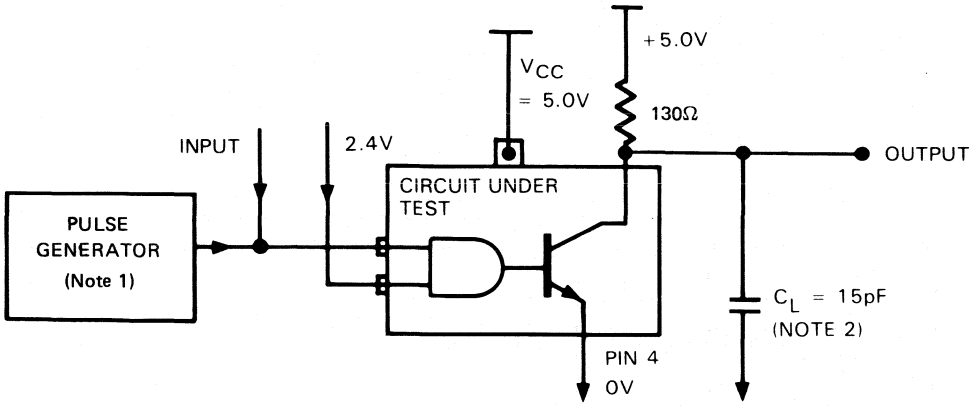
A	B	OUTPUT (D)
L	L	H (OFF)
L	H	H (OFF)
H	L	H (OFF)
H	H	L (ON)

Truth Table - XR-T5675
H = High Level, L = Low Level

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.0 V, T_A = 0°C to +70°C, unless specified otherwise.

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
V_{CC}	Supply Voltage	8	4.75	5.0	5.25	V	
V_{IH}	High Level Input Voltage	1,2,6,7	2.2			V	I_{OL} = 50 mA V_{OL} = 0.95 V
V_{IL}	Low Level Input Voltage	1,2,6,7			0.8	V	
I_{IH}	High Level Input Current	1,2,6,7			40	µA	V_{IH} = 2.7 V, Pins 3 & 5 Open
I_{IL}	Low Level Input Current	1,2,6,7			−1.2	mA	V_{IL} = 0.4 V, Pins 3 & 5 Open
V_{OL}	Low Level Output Voltage	3,5	0.6		0.95	V	V_{IH} = 2.2 V, I_{OL} = 50 mA
I_{OL}	Low Level Output Current	3,5			50	mA	V_{IH} = 2.2 V, V_{OL} = 0.95 V
I_{OH}	High Level Leakage Current	3,5			100	µA	Pins 3 & 5, Pull-up to +20 V
I_{ccH}	Supply Current Output High	8			3.0	mA	Pins 3 & 5 Open
I_{ccL}	Supply Current Output Low	8		14.0	18.0	mA	Pins 3 & 5 Open
SWITCHING CHARACTERISTICS, V_{CC} = 5.0 V ±5%, T_A = +25°C							
t_{pLH}	Propagation Delay, Low to High	3,5		15		ns	See Figure 2
t_{pHL}	Propagation Delay, High to Low	3,5		15		ns	
t_{rise}	Rise Time	3,5		15	24	ns	
t_{fall}	Fall Time	3,5		10	24	ns	
	Output Pulse Imbalance			2.5		ns	At 50% Output Level



NOTE 1. PULSE GENERATOR FREQUENCY = 2.0 MHz, Z_{OUT} = 50Ω

NOTE 2. CL INCLUDED — PROBE AND JIG CAPACITANCE

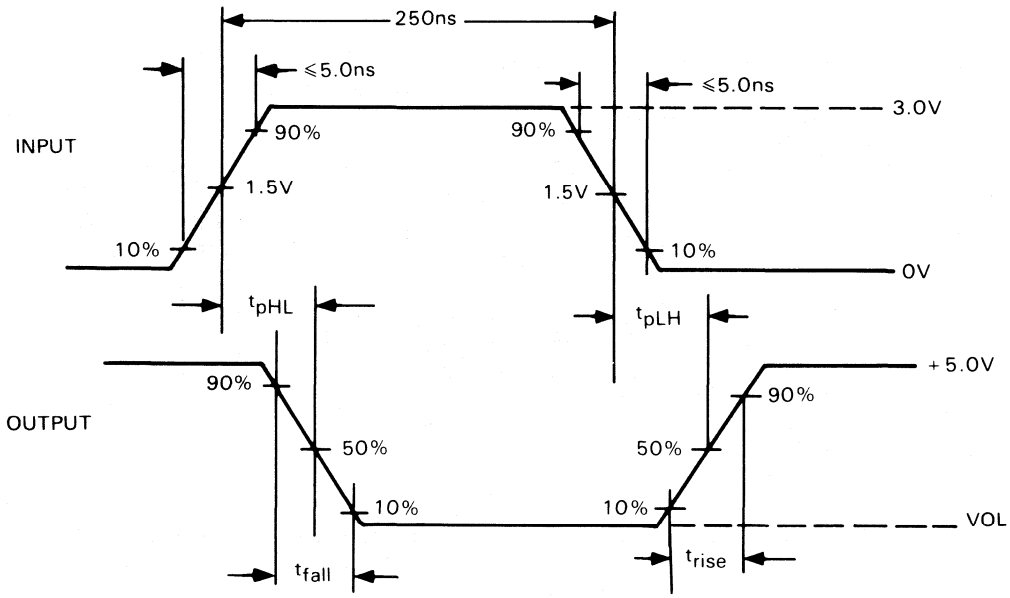
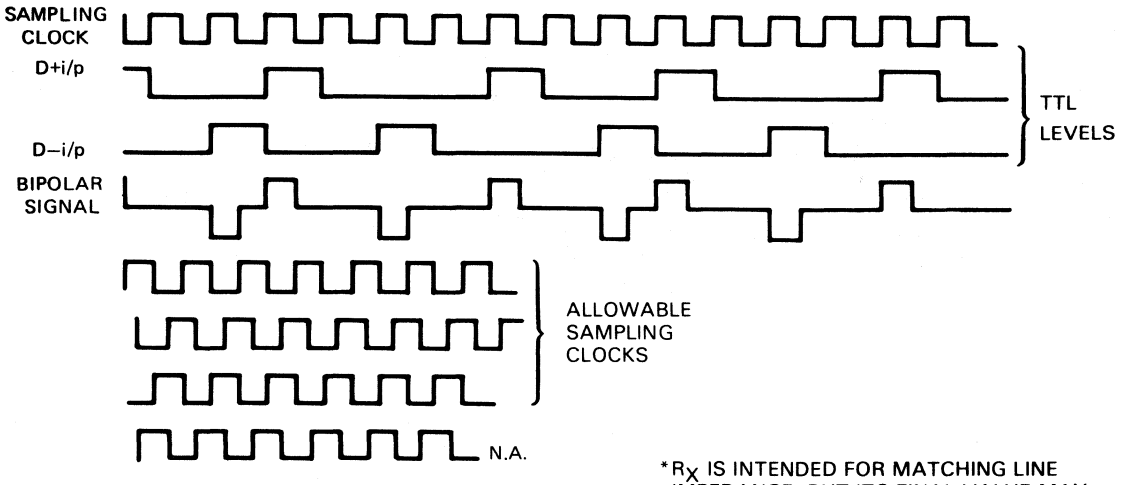
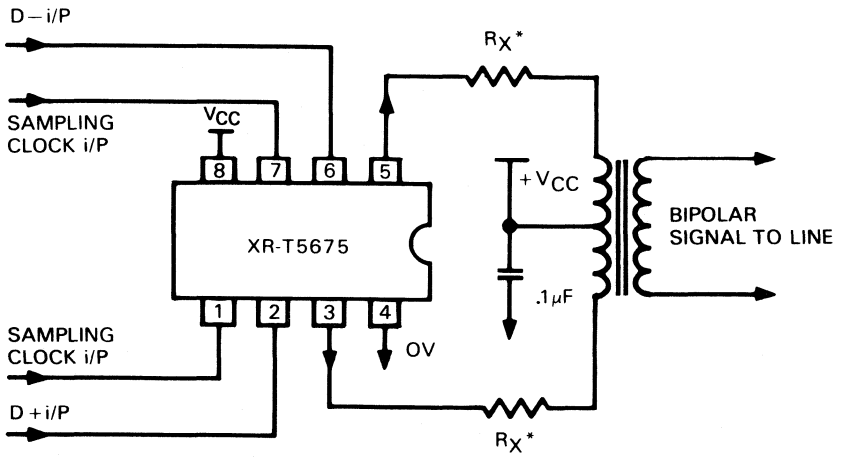


FIGURE 2. AC TEST CIRCUITS AND SWITCHING WAVEFORMS



*R_X IS INTENDED FOR MATCHING LINE IMPEDANCE, BUT ITS FINAL VALUE MAY BE DETERMINED BY THE OUTPUT SIGNAL AMPLITUDE REQUIRED.



IN THE CASE WHERE D+ AND D– ARE HALF WIDTH SIGNALS, PIN 1 AND PIN 7 SHOULD BE TIED TOGETHER AND RETURNED TO +5.0V VIA A 1K RESISTOR

FIGURE 3. XR-T5675 PCM LINE DRIVER APPLICATION CIRCUIT

Low Power PCM Line Receiver

GENERAL DESCRIPTION

The XR-T5676 is a low power PCM line receiver IC intended to operated up to 2.048 MBPS and a maximum signal level attenuation of -10db (cable loss) at half the bit rate. Because of it's small outline and low power consumption, this device is very well suited for mux/demux applications interfacing to several T1/CEPT lines.

FEATURES

Low Power (Typ 6mA)
Single +5.0V Supply
Up to 2.048 MBPS Operation
TTL Compatible Interface
Inputs: Balanced Transformer Single Coaxial
Capacitive Coupled Twisted Pair

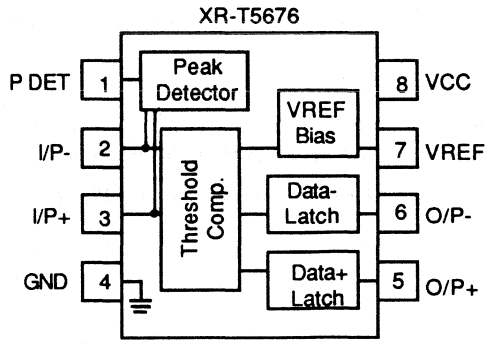
APPLICATIONS

Mux/Demux Equipment
T1 and CEPT Interfaces
CPI's
DMI's

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+20V
Storage Temperature	-65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5676IN	Ceramic	-40°C to + 85°C
XR-T5676IP	Plastic	-40°C to +85°C

SYSTEM DESCRIPTION

The XR-T5676 PCM line receiver IC accepts the incoming PCM signals which have been attenuated and distorted by the cable through a balanced transformer or a single capacitive coupled terminal. A peak detector which follows the input generates a DC reference voltage for the positive and negative threshold comparator. This voltage in turn is mirrored around a reference voltage to establish the threshold voltage for the negative pulses.

Pin	Name	DESCRIPTION
1	P DET	**Peak Detector Output.** Connects to a timing capacitor for signal peak detection.
2	I/P-	**Receiver Negative Input.**
3	I/P+	**Receiver Positive Input.**
4	GND	**Ground.** Most negatvie supply voltage (0V)
5	O/P+	**Data Positive Output.** (active low)
6	O/P -	**Data Negative Output.** (active low)
7	VREF	**Reference Voltage.** Establishes reference voltage for transformer coupled applications.
8	VCC	**Positive Supply Voltage.** (5.0V+/-5%)

DC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC = 5V+/-5%, Ta = 25°C unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	4.75		5.25	V	
Supply Current		6	10	mA	
Data Output Low		0.3	0.6	V	Pin 5 & 6 I_{OL} = 1.6 mA
Data Output High	3.0	3.6		V	Pin 5 & 6 I_{OH} = 400 µA

AC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V+/-5%, Ta = 25°C unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
Input Level		6	6.6	Vp-p	Pins 2 & 3
Loss Input Signal					
Alarm Level		0.6		Vp-p	Pins 2 & 3
Input Impedance		2.5		Kohm	@ 2.048 MBPS
Data Pulse Width	200	244	300	nS	Cable loss = 0 db

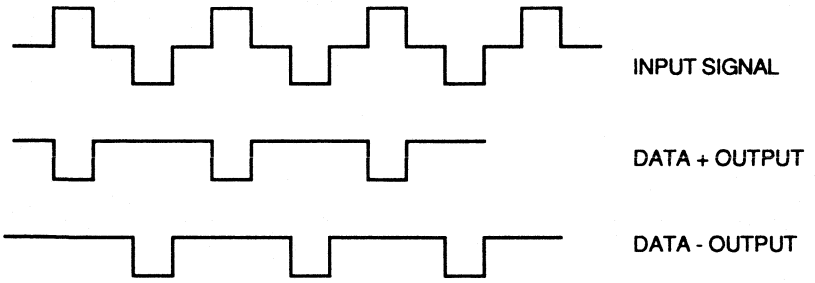


Figure 1. Receiver Output Timing Diagram with 1-1-1-1 Pattern

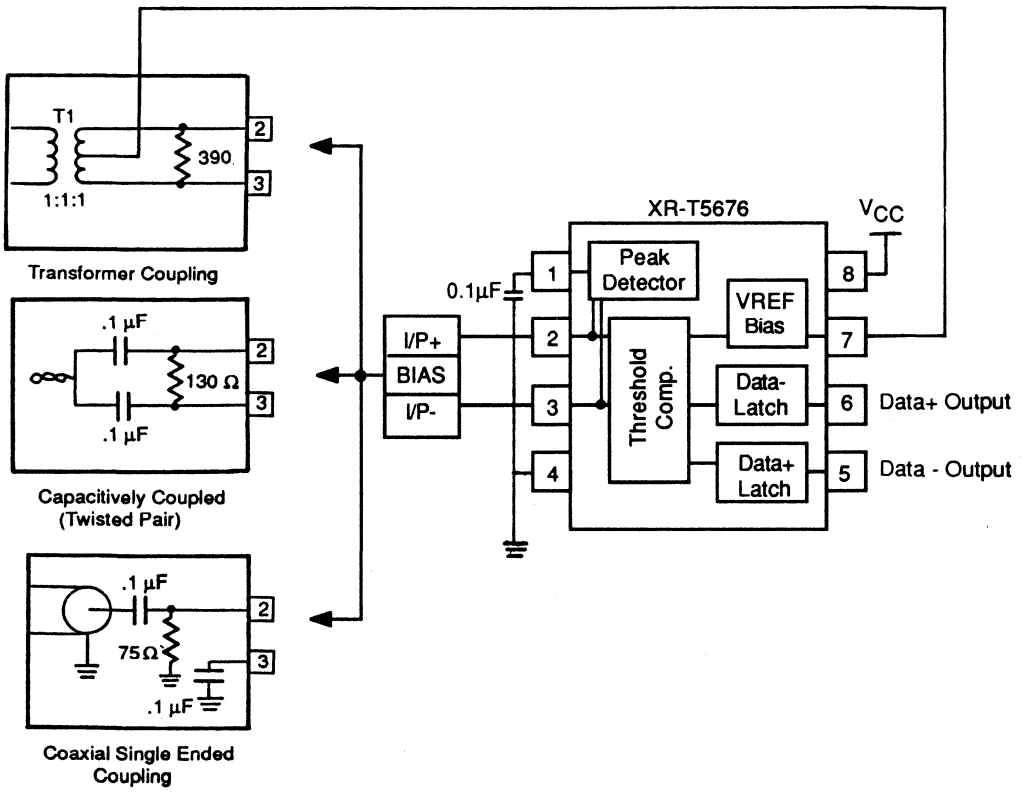


Figure 2. Typical Application Circuit

Speakerphone Audio Circuit

GENERAL DESCRIPTION

The XR-T6420-2 is a monolithic integrated circuit for use in high performance speakerphone systems. It is designed to be used with the XR-T6421 Speakerphone Control Circuit.

The XR-T6420-2 contains the audio paths comprising the following: Two variable gain cells, a microphone amplifier, a transmitting amplifier, a receive amplifier, and a speaker amplifier. Mute and enable control logic of the variable gains cells is provided internally.

FEATURES

Two Matched Variable Gain Cells
Internal Microphone Amplifier
Independent Control of Transmitting and Receiving Levels
External Control of Gains and Frequency Response
Enable and Mute Logic Pins

APPLICATIONS

Speakerphones
Intercoms
Voltage Controlled Amplifiers

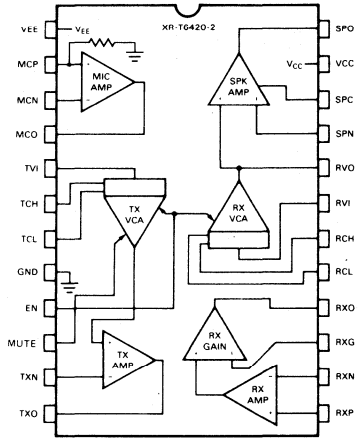
ABSOLUTE MAXIMUM RATINGS

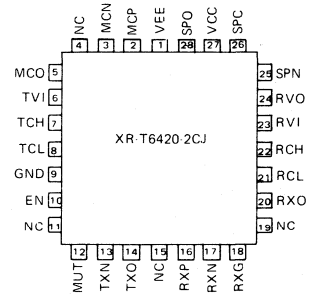
Power Supply ($V_{CC} - V_{EE}$)	+30 V
Power Dissipation	1 W
Derate Above +25°C	7 mW/°C
Any Input Voltage	V_{CC} – 0.5 V to V_{EE} + 0.5 V
Storage Temperature	**-65°C to +150°C**

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T6420-2CJ	PLCC	0°C to 70°C
XR-T6420-2CP	Plastic	0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM





SYSTEM DESCRIPTION

The speakerphone concept essentially requires that only one direction of sound transmission be permitted at any time. This restraint is brought about by the large gains required to provide loudspeaker volume and high microphone sensitivity. Owing to the inevitable acoustic coupling between loudspeaker and microphone, plus imperfections in the hybrid 2 to 4 wire conversion, it is necessary to lower the gain in either the transmitting or receiving path at any one time to avoid regeneration.

The XR-T6420-2 and XR-T6421 chip set enables the system designer to make a highly adaptive, high performance speakerphone. The XR-T6421 provides for all sensing and control functions, while the XR-T6420-2 contains all audio paths needed to switch the gain in either path and provide interfacing between the system and line.

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{CC} = +5 V, V_{EE} = −5 V, unless specified otherwise.

PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	3			V	
V_{EE}	3			V	
I_{CC}		4.9	8	mA	Pin 23
MICROPHONE AMPLIFIER					
V_{IN}		5	25	mV	Pin 2
R_{IN}		20		kΩ	Pin 2
V_{OFFSET}			5	mV	
I_{BIAS}		−.2	−0.5	μA	
Open Loop Gain	80			dB	
SPEAKER AMPLIFIER					
R_{IN}		10		kΩ	Pin 20
V_{OFFSET}			5	mV	
I_{BIAS}		−.2	-0.5	μA	
Open Loop Gain	80			dB	
I_{SOURCE}, I_{SINK}	100			mA	R_{LOAD} = 10Ω
V_{OUT} High	V_{CC} −1.6			V	R_{LOAD} = 5kΩ
V_{OUT} Low	V_{EE} +.8			V	R_{LOAD} = 5kΩ
TRANSMIT AMPLIFIER					
I_{BIAS}		−.2	−0.5	μA	
Open Loop Gain		90		dB	
RECEIVE AMPLIFIER					
I_{BIAS}		1.2	2	μA	Pin 13, Pin 14
Differential Mode Gain	−3	−1		dB	Pins 15 and 16 Shorted
Common Mode Gain	−40	−60		dB	Pins 15 and 16 Shorted
I_{BIAS}		−.2	−.5	μA	Pin 15
Open Loop Gain		90		dB	
VCAs TRANSMIT AND RECEIVE					
V_{OUT} DC			.3	V	Pins 11 and 20
Maximum Gain	−2		+2	dB	f = 1kHz, Pins 5 and 19
I_{BIAS} Control			.5	μA	Pins 6, 7, 17 and 18
MUTE AND ENABLE LOGIC					
I_{SOURCE}		−10	−20	μA	
Trip Voltage		V_{CC} −2.8	V_{CC} −2.1	V	

PRINCIPLES OF OPERATION

Power Supply

Normal operation is with two supplies. V_{CC} is the highest potential and V_{EE} is the lowest. The circuit can be operated from a single supply if the ground pin is connected to a low impedance source of approximately one half the supply voltage.

Microphone Amplifier

The microphone amplifier is an operational amplifier with the positive input internally connected to the ground pin through a 20 K ohm nominal resistance. Gain and frequency responses are set using external components.

Transmit Voltage Controlled Amplifier (T_X VCA)

The output of the microphone amplifier is normally capacitively coupled into the T_X VCA. The input impedance is nominally 10 K ohm. The gain of the T_X VCA is dependent upon the voltage difference between the TCH and TCL inputs on pins 6 and 7. The output is internally connected to the transmit amplifier.

Transmit Amplifier

This is an operational amplifier with a class AB output stage. Gain and frequency response are set with external components. This amplifier is used to drive the hybrid interface network.

Receive Amplifier

The input on pins 13 and 14 is a high input impedance differencing amplifier. The output is internally referenced to the ground pin and connected to the positive input of an operational amplifier. The gain and frequency response of the amplifier can be adjusted using external components on pins 15 and 16. This amplifier is normally connected to the hybrid interface network to detect the receive signal while rejecting the transmit signal.

Receive Voltage Controlled Attenuator (R_X VCA)

The output of the receive amplifier is capacitively coupled to the R_X VCA input on pin 19. The R_X VCA's input impedance is a nominal 10 K ohm. The gain of the R_X VCA is dependent upon the voltage difference between the RCH and RCL inputs on pins 17 and 18. The output of the R_X VCA is internally referenced to the ground pin through a 10 K ohm resistance and connected to the positive input of the speaker amplifier on pin 20.

Speaker Amplifier

This is an operational amplifier with a class AB power output stage. Gain and frequency response are set using external components. Depending on the load driven, compensation may be necessary using pin 22.

PIN DESCRIPTIONS

Pin 1 - V_{EE} – Negative DC supply.

Pin 2 - MCP – Microphone amplifier noninverting input. Internally connected to ground with a 20 K ohm resistance.

Pin 3 - MCN – Microphone amplifier inverting input.

Pin 4 - MCO – Microphone amplifier output.

Pin 5 - TVI – Transmit voltage controlled amplifier input. Input impedance is 10 K ohm.

Pin 6 - TCH – Transmit VCA gain control pin; high reference. Used with pin 7 to control VCA gain according to Figure 1.

Pin 7 - TCL – Transmit VCA gain control pin; low reference. Used with pin 6 to control VCA gain.

Pin 8 - GND –Ground reference pin for circuit.

Pin 9 - ENABLE – Active high; internally pulled high. When pulled low, causes an internal 200 mV difference between the gain control pins for both VCAs effectively causing minimum gain in both.

Pin 10 - MUTE – Internally pulled high. When pulled low, causes only the transmit VCA to be minimum gain.

Pin 11 - T_XN – Transmit amplifier inverting input.

Pin 12 - T_XO – Transmit amplifier output.

Pin 13 - R_XP – Receive amplifier positive input. High input impedance, must be DC referenced externally.

Pin 14 - R_XN – Receive amplifier negative input. Must be DC referenced to same source as pin 13.

Pin 15 - R_XG – Receive amplifier inverting input.

Pin 16 - R_XO – Receive amplifier op amp output.

Pin 17 - RCL – Receive VCA gain control pin low referenced used with pin 18 to control VCA gain according to Figure 1.

Pin 18 - RCH – Receive VCA gain control pin; high reference used with pin 17 to control gain of VCA.

Pin 19 - RVI – Receive VCA input. Input impedance is 10 K ohm.

Pin 20 - RVO – Receive VCA output. Impedance is 10 K ohm to ground.

Pin 21 - SPN – Speaker amplifier inverting input.

Pin 22 - SPC – Speaker amplifier compensation.

Pin 23 - V_{CC} – Positive DC supply.

Pin 24 - SPO – Speaker amplifier output.

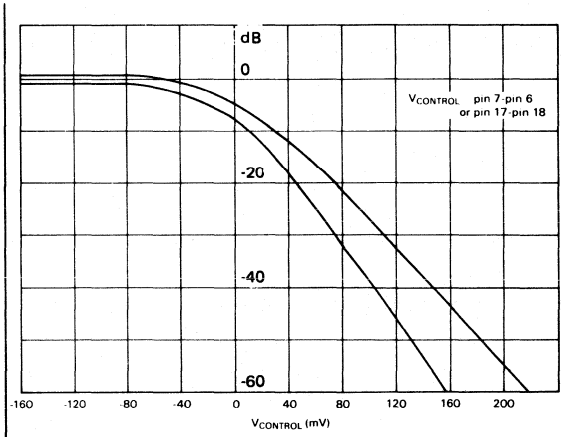


Figure 1. VCA Gain Characteristics

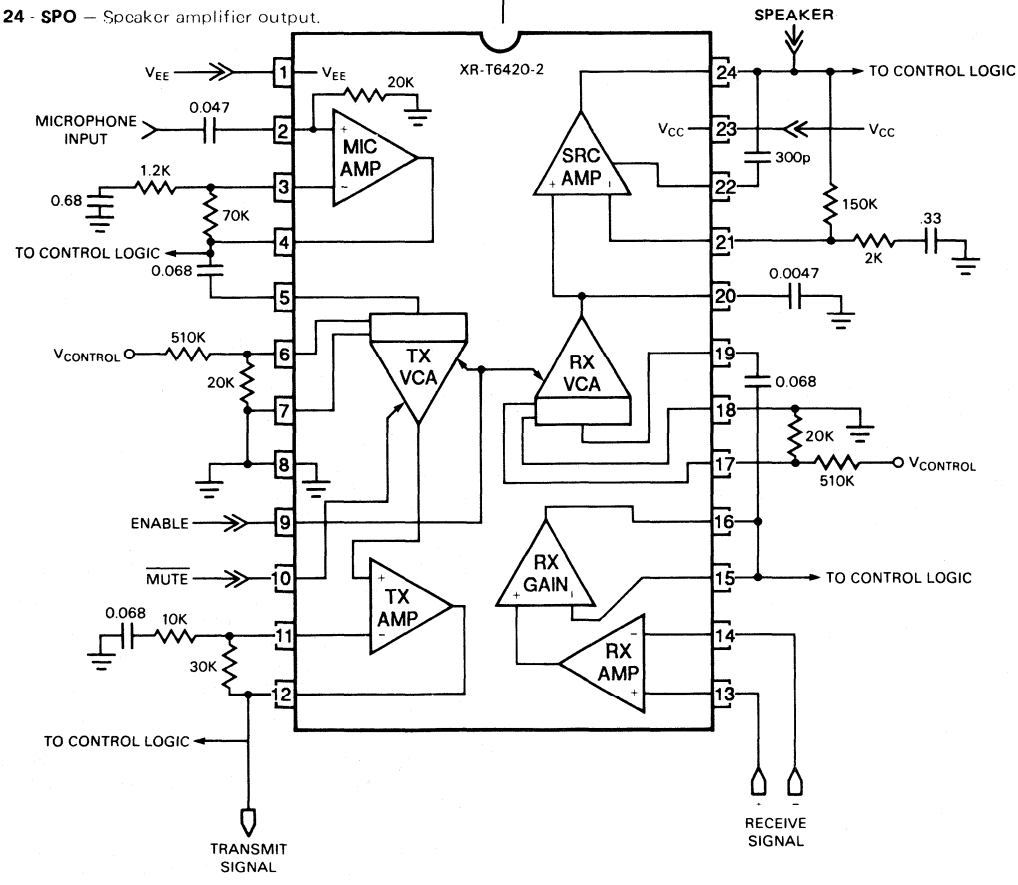


Figure 2. Typical Application Schematic

Speakerphone Control IC

GENERAL DESCRIPTION

The XR-T6421 is a monolithic integrated circuit for use in high performance speakerphone systems. It is designed to provide all control functions for the XR-T6420-2 speakerphone audio circuit.

The XR-T6421 contains the level sensors and logic necessary to change the attenuation in the transmitting or receiving path in order to avoid acoustic feedback.

Circuitry is included to detect background noise level and provide a preset amount of attenuation in each path when no voice is present.

FEATURES

Low Current
Background Noise Detection and Suppression
External Control of Attack and Decay Time Constants
Independent Control of Gain and Frequency Response
Provides Three Level Control of Transmit & Receive Paths

APPLICATIONS

Speakerphones
Intercoms
Voice Operated Switches

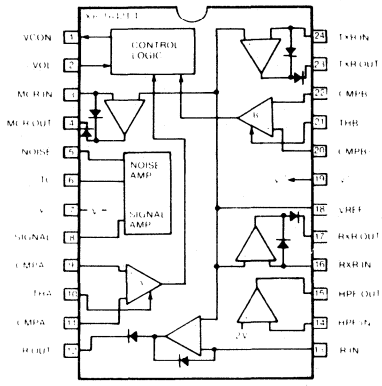
ABSOLUTE MAXIMUM RATINGS

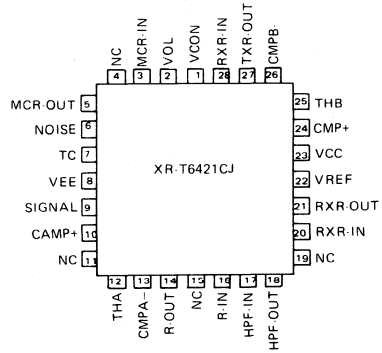
Power Supply	20 V
Power Dissipation	1 W
Derate Above +25°C	7 mW/°C
Any Input Voltage	V_{CC} +0.5 V to V_{EE} -0.5 V
Storage Temperature	**-65°C to 150°C**

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T6421CP	Plastic	0°C to 70°C
XR-T6421CJ	PLCC	0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM





SYSTEM DESCRIPTION

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ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{CC} = 10V$, unless specified otherwise.

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage Range	5		20	V	
Supply Current		1.4	3	mA	$V_{CC} = 10$ V
V_{REF}	1.85	2.1	2.25	V	
RECTIFIERS					
V_{OUT}	1.9	2.1	2.27	V	VAC = 0
V_{OUT} (High Level)		5.0		V	
V_{OFFSET} 1	-5		5	mV	Vpin 4 - Vpin 12
V_{OFFSET} 2	-5		5	mV	Vpin 17 - Vpin 23
A_{OL}	45			dB	
I_{bias}		0.2		µA	
HPF					
V_{OUT} DC	2.3	2.6	2.9	V	
Maximum Isource (Pin 15)		1.0		mA	
Maximum Isink (Pin 15)		1.0		mA	
A_{OL}	32			dB	
I_{bias}		0.25		µA	
VOICE CIRCUITRY					
Noise Amplifier Offset V6 - V5	-3		12	mV	V_{IN} =
Signal Offset V8 - V18			15	mV	V_{IN} =
Signal Gain	.8	1	1.2		$\frac{\text{Vpin 8 - Vpin 18}}{\text{Vpin 5 - Vpin 6}}$
CONTROL OUTPUT					
V_{CON} High	V_{CC}-.9		V_{CC}-.5	V	
V_{CON} Idle	4.9	5	5.1	V	20 kΩ to 5 V
V_{CON} Low Minimum			.95	V	
V_{CON},V_{OL} Offset	50		250	mV	
COMPARATORS					
I_{bias}		1		µA	
Offset	5		17	mV	$V_{POS} - V_{NEG}$

PRINCIPLES OF OPERATION

Rectifiers – All four rectifiers are operational amplifiers with the noninverting input connected to V_{REF}. The circuit contains the diodes internally to provide the function of a negative peak detector. Using the typical application schematic of Figure 1, the "gain" of the rectifier is R2/R1. The output is then filtered using another RC network. The attack time is given by R3.C and the decay time by (R2 + R3).C.

High Pass Filter – This is a simple gain stage with a class AB output stage. Pin 14 is about 2.6 V above V^-. This amplifier is normally used as a high pass filter to reduce line induced hum from the detection circuitry.

Noise Control Circuitry – This function provides a signal on Pin 8 related to the difference between Pins 5 and 6. Pin 5 is usually connected to the filter network of the microphone rectifier. This signal represents the speech plus noise from the microphone. Pin 6 has an external RC network and functions as a detector for the noise level. The output on Pin 8 is the difference between Pins 5 and 6, referenced to V_{REF}.

Comparators – Both comparators have internally generated offset of -10mVolts nominally. With no difference between the inputs, the output will be in the low state. The amount of offset can be increased by connecting a resistor between the threshold adjust pin and V^-.

Control Logic – The purpose of the logic is to derive the three speakerphone states, depending on Comparators A and B. The three states are:

1) Transmit → Pin 1 = V^+ -0.7V
2) Receive → Pin 1 ≅ Pin 2 + 0.1V
3) Idle → Pin 1 is High Impedance.

The truth table for the logic is:

Comparator		State
A	B	
0	0	Idle
0	1	Receive
1	0	Transmit
1	1	Idle

CIRCUIT DESCRIPTION

Pin 1 - V_{CON} – Provides three voltage states depending on input conditions. The first is a low impedance voltage about equal to V^+ -.7 Volt. The second state is a low impedance voltage equal to voltage on Pin 2. The third state is a high impedance state.

Pin 2 - V_{OL} – A high impedance input used to modify the control voltage (Pin 1) when in the low state.

Pin 3, 4 - MCR – Negative peak detector usually connected to microphone amplifier output. Gain, attack, and delay times are externally set.

Pin 5 - NOISE – High impedance input used to buffer speech plus noise input from microphone rectifier.

Pin 6 - TC – External RC network determines response to background noise level. RC network determines rise time, internal circuitry will discharge network if Pin 6 > Pin 5.

Pin 8 - SIGNAL – Provides voltage proportional to Pin 5, Pin 6 output impedance is nominally 36 K ohms.

Pin 9, 11 - CMP A – Used to compare signal level to level of speaker signal.

Pin 10 - TH A – Used to increase offset of comparator A. With TH A open, offset is approximately -10 mV.

Pin 12, 13 - R – Negative peak detector normally connected to speaker amplifier. Gain, attack, and decay times are externally set.

Pin 14, 15 - HPF – Inverting amplifier, normally connected as a high pass filter to reject low frequencies from received signals into the control circuitry.

Pin 16, 17 - R_XR – Negative peak detector normally connected after line receive amplifier. Gain, attack, and decay times are externally set.

Pin 18 - V_{REF} – Internal 2 Volt reference.

Pin 20, 22 - CMP B – Used to compare transmitted and received signal levels.

Pin 21 - TH B – Used to increase offset of comparator B with TH B open, offset is approximately -10 mV.

Pin 23, 24 - T_XR – Negative peak detector normally connected to transmit amplifier. Gain, attack, and decay times are externally set.

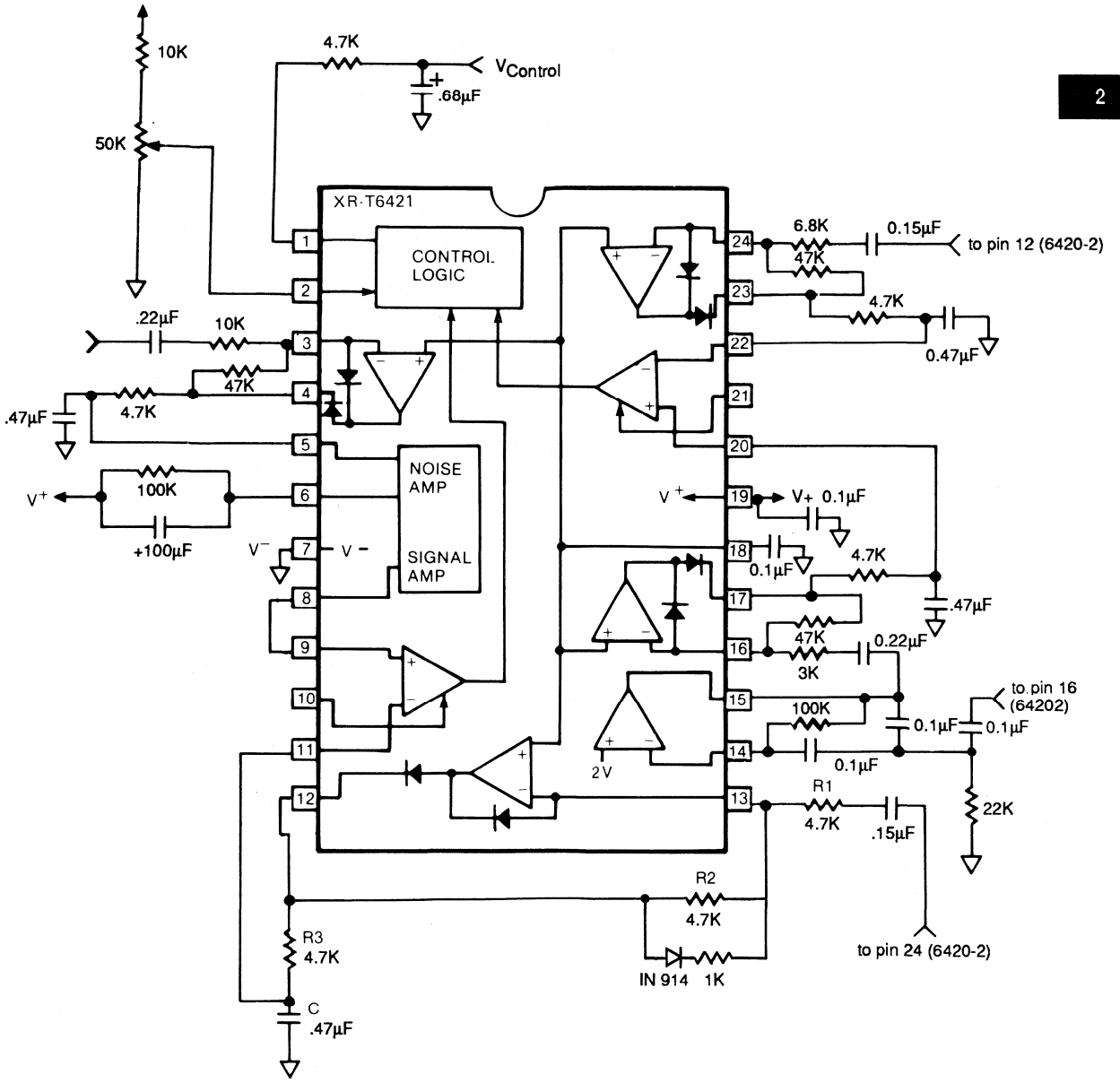


Figure 1. Typical Application Schematic

Speakerphone IC

GENERAL DESCRIPTION

The XR-T6425 speakerphone IC is a low cost solution for the implementation of a hands-free telephone. It is a convenient way of carrying on conversation without using the handset, while the user is talking into a microphone and listening from a loudspeaker located on the desk. It is ideal for hands-free conference calls.

The XR-T6425 contains most of the circuits to eliminate singing and excessive background noise in a single chip solution.

FEATURES

Low Operating Voltage (4.5 V)
Single Chip Speakerphone
No External Adjustments
Smooth T/R Switching
Background Noise Detection and Suppression
On-chip Hybrid Circuit

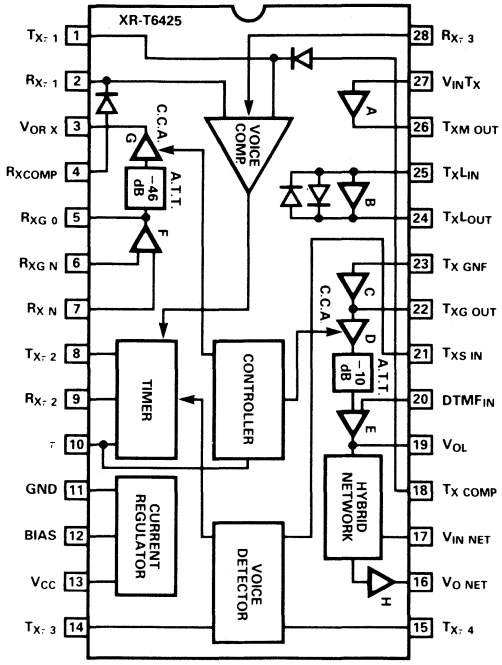
APPLICATIONS

Speakerphones
Intercoms
Voice Operated Switches

ABSOLUTE MAXIMUM RATINGS

Power Supply	16 V
Power Dissipation	700 mW
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to 150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T6425CP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-T6425 single chip speakerphone IC is designed to operate from the phone line and allows hands-free operation. The chip contains most of the necessary circuits to reduce external component count and performs half-duplex operation. The internal circuits consist of a transmitter, receiver and control logic. DTMF input is provided for Touch Tone operation. An adjustable threshold circuit is provided to separate voice from ambient noise.

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{CC} = 5 V, f = 1 kHz, unless otherwise specified.

SYMBOL	PARAMETERS	TYPICAL VALUE	UNIT	CONDITIONS
V_{CC}	Operating Voltage	4.5 - 6.5	V	
I_C	Operating Current	8.0	mA	No Input of T/R Signal
R_{XS}	Receiving Sensibility	–64	dBm	
T_{XS}	Transmitting Sensibility	–74	dBm	
G_VR_X	Receiving Gain	–22.5	dB	Receiving Mode
G_VT_X	Transmitting Gain	44	dB	Transmitting Mode
V_{INLIM}	Mic Input Level	–55	dBm	THD = 1%
$AttR_X$	Receving Loss	–50	dB	Receiving Transmitting Relative Value
$AttT_X$	Transmitting Loss	–50	dB	Transmitting Receiving Relative Value

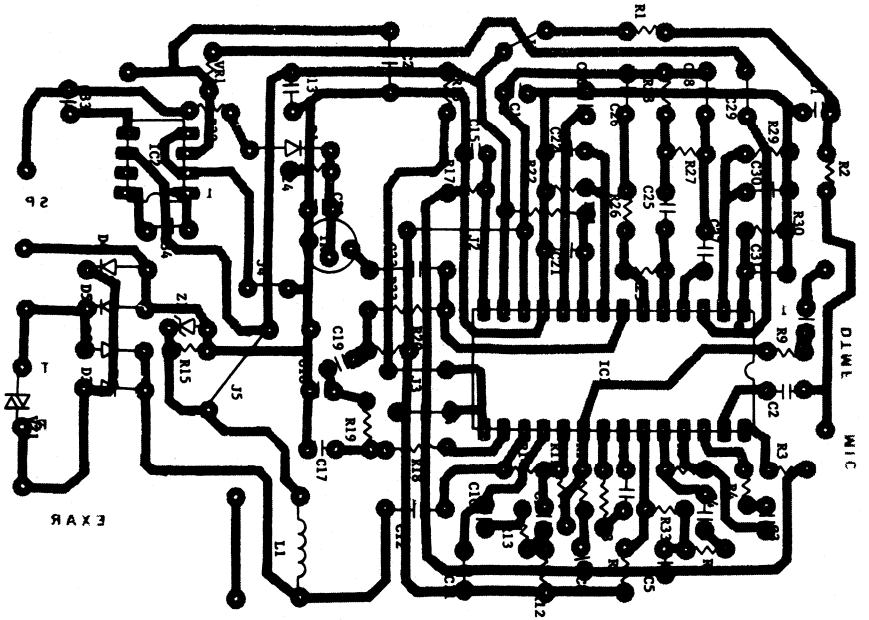


Figure 1. Circuit Board Layout

PIN DESCRIPTIONS

Pin	Symbol	Description
1	$TX_{\tau 1}$	Transmitter stabilization time constant.
2	$RX_{\tau 1}$	Receiver stabilization time constant.
3	$V_O R_X$	Receiver output.
4	R_X COMP	T/R comparator input for receiver.
5	$R_X G_O$	Receive buffer output.
6,7	R_{XGN},R_{XIN}	Receive buffer inputs.
8	$TX_{\tau 2}$	Transmitter holding time constant.
9	$RX_{\tau 2}$	Receiver holding time constant.
10	τ	T/R switching time constant
11	GND	Ground
12	BIAS	Mid-point of the supply voltage ($V_{CC}/2$).
13	V_{CC}	Most positive voltage.
14	$TX_{\tau 3}$	Voice rectifier time constant.
15	$TX_{\tau 4}$	Ambient noise and voice discriminator time constant.
16	V_{ONE}	Hybrid network output.
17	V_{IN} NET	Hybrid network input.
18	T_X COMP	T/R comparator input for transmitter.
19	V_{OL}	Transmit signal output.
20	DTMFIN	DTMF input terminal.
21	T_{XS} IN	Voice detector output.
22	T_{XG} OUT	Transmit amplifier output.
23	TXG NF	Transmit amplifier input.
24	$T_X L_{OUT}$	Transmit limiter amplifier output.
25	$T_X L_{IN}$	Transmit limiter amplifier input.
26	$T_X M_{OUT}$	Transmit buffer output.
27	$V_{IN} T_X$	Transmit buffer input.
28	$RX_{\tau 3}$	Receiver stabilizer.

FUNCTION DESCRIPTIONS

Transmitting Sections

The transmit path is divided into five sections: buffer, limiter, bandpass filter and amplifier, current control attenuator and mixer.

Buffer

The buffer is used to do impedance matching and gives 9 dB gain to signal.

Limiter

The output of the buffer is fed to limiting amplifier to increase the signal level. The gain can be set with two external resistors R_4, R_5 to obtain proper signal level.

Bandpass Filter and Amplifier

Filtering is performed in this section to eliminate unwanted signals. Gain of 20 dB is set for this section and output of this amplfier is capacitor coupled to control lgoic to eliminate DC components for decision making.

Current Control Attenuator

The current control attenuator is used to do smooth switching between transmitter and receiver to perform half-duplex operation.

Mixer

Additional input is provided for DIMF signaling and driving transmitting signals to telephone line through impedance matched resistance R_{14} (680Ω), and simultaneously inputs to the hybrid network for cancelling signals to receiving circuit.

Receiving Section

Incoming signals are amplified by AMP H and AMP F after passing through hybrid network. The result is fed to current control attenuator to control output level.

Ambient Noise and Voice Discrimination Section

This section discriminates voice signals from ambient noises of input signals from microphone at transmtting mode and gives the instruction signals to keep transmitting mode or changes the mode to T/R signal attenuator circuit through timer circuit.

Controller Section

This section compares transmit signal level (pin 18) with receive signal level (pin 4) according to the time settled by C_{31}, R_{30}, C_{30}, R_{29}, the result is applied to the timer circuit which is triggered with the resistor value of R_3 connected from Pin 28 to Ground.

Timer Section

This section generates the signals to T/R signal attenuator circuit and provides the time constant for T/R switching.

Transmit time constant is set by pin 8, receive time constant is set by pin 9, and T/R switching time constant is determined by pin 10. Pin 10 outputs 2.5V at transmit mode and +1.2V at receive mode.

Hybrid Network

Hybrid network is used to attenuate transmit signal going to the receive path. Equivalent circuit is shown below.

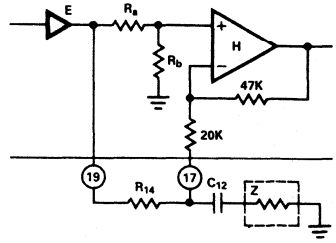


Figure 2. Equivalent Circuit

TIMING CALCULATIONS

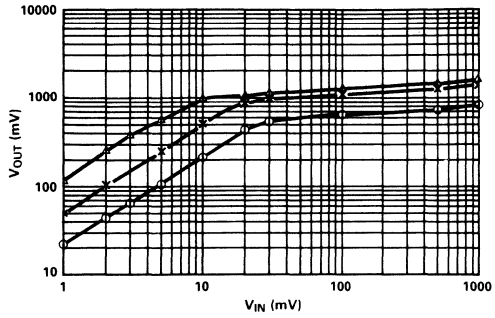
Transmit Rise Time = $C_{22} \times 10^4$	4.7 μF, τ = 47 ms
Transmit Hold Time = $C_{22} \times R_{22}$	4.7 μF, 470K, τ = 2.2S
Receive Rise Time = $C_{21} \times 10^3$	.47 μF, τ = .47 ms
Receive Hold Time = $C_{21} \times R_{21}$	.47 μF, 470K, τ = .22S

DESCRIPTION OF AMPLIFIERS

Type	Application	Gain	Remarks
A	TX amplifier	0 dB	For the impedance conversion (emitter-follower microphone) (Zin = 20 kΩ)
B	TX amplifier	R5/R 4	Negative input limiter amplifier, clamping at $\frac{1 VF}{\sqrt{2}}$ of Pin 24 output. (V0 = 700 mVrms)
C	TX amplifier	20 dB	Fixed gain amplifier.
D	TX amplfier	TX: 20 dB ST: –5 dB RX: –23 dB	Gain varies with transmitting (TX), receiving (RX) and standby (ST).
E	TX amplifier	R11/R10	Output gain - the signal applied as a negative input when DTMF is used.
F	RX amplifier	R25/R26	Differential input amplifier. Its output is connected to C.C.A. (amp G) through pin 5 and ATT.
G	RX amplifier	TX: –23 dB ST: –5 dB RX: 20 dB	Gain varies with transmitting (TX), receiving (RX) and standby (ST).
H	RX amplifier	7.5 dB	For the network loss correction of receving (RX) side.

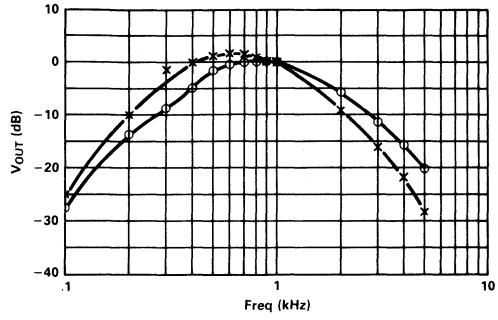
TYPICAL CHARACTERISTICS

XR-T6425 RECEIVING ALC CHARACTERISTICS
V_{CC} = 5.6V, APPLYING 12V BETWEEN L1 AND L2



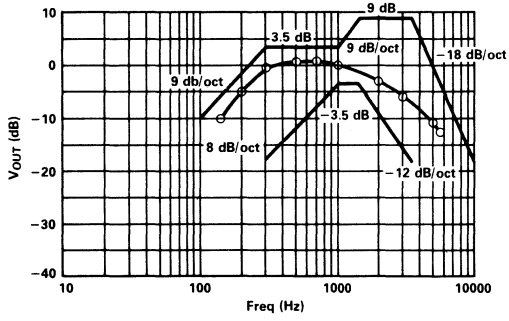
△ C × B ○ A

XR-T6425 RECEIVING FREQUENCY CHARACTERISTICS
V_{CC} = 5.6V, APPLYING 12V BETWEEN L1 AND L2



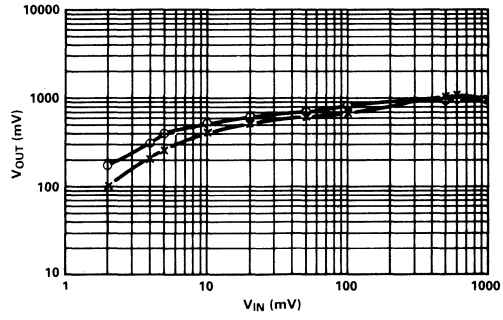
× BEFORE MOUNTING C32 ○ AFTER MOUNTING C32

XR-T6425 TRANSMITTING FREQUENCY CHARACTERISTICS
V_{CC} = 5.6V, APPLYING 12V BETWEEN L1 AND L2



❄ INDICATION VALUES OF M3

XR-T6425 MICROPHONE AMPLIFIER LIMITER CHARACTERISTICS
V_{CC} = 5.6V, APPLYING 12V BETWEEN L1 AND L2



× INDICATION VALUES OF M2 ○ INDICATION VALUES OF M3

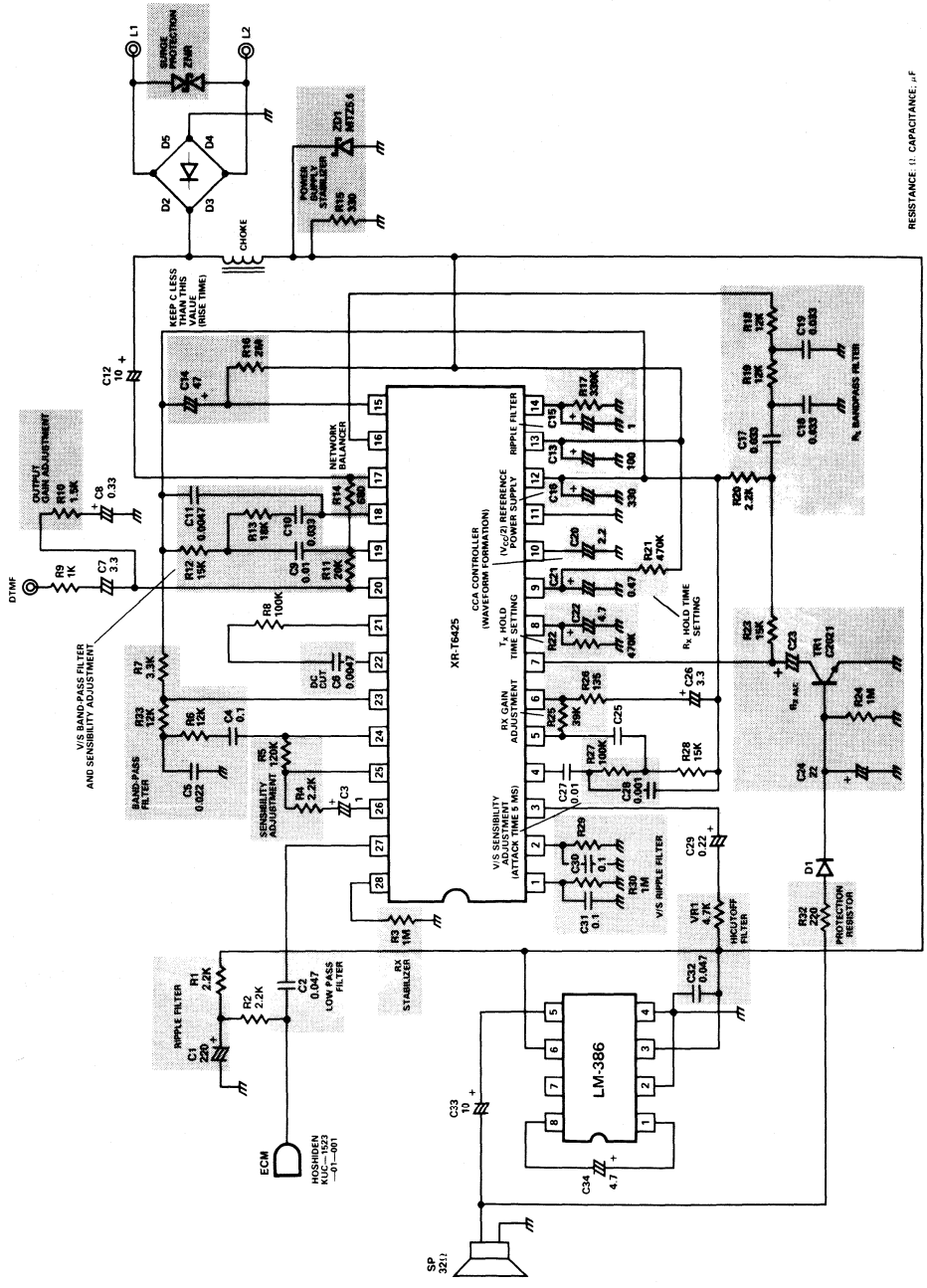


Figure 3. Typical Line Powered Application Circuit

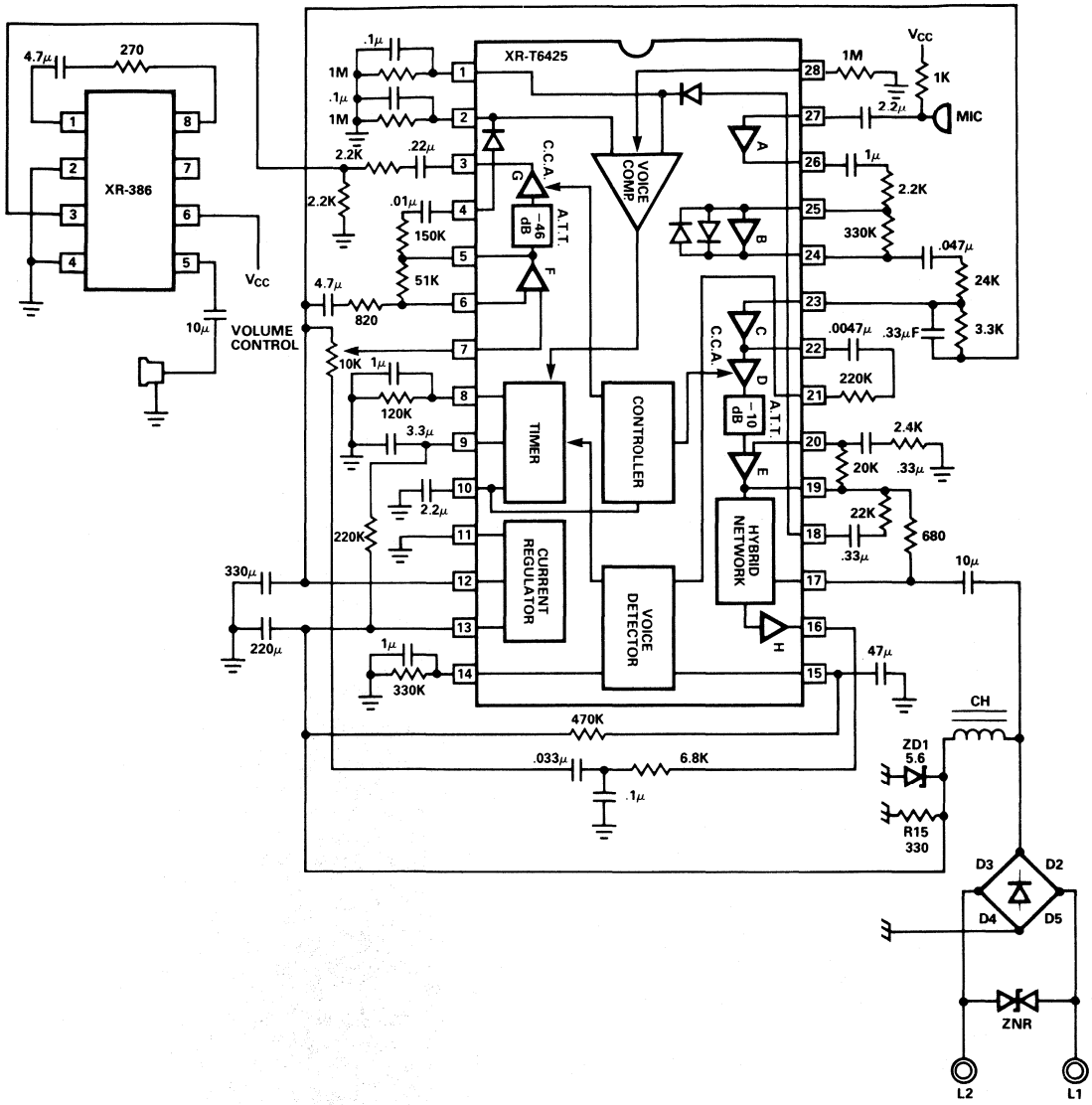


Figure 4. Simplified Application Schematic

Voice Switched Speakerphone Circuit

GENERAL DESCRIPTION

The XR-T34118 Voice Switched Speakerphone Circuit is designed to operate as a hands free speakerphone and include all the necessary amplifiers, attenuators, level detectors and control algorithms. Included are a microphone amplifier with adjustable gain and mute control, a transmit and receive attenuator, two level detectors - located at the input and output of the attenuators, and a background noise monitor for the transmit and receive channels. Also, part of the circuitry is a dial tone monitor which prevents the dial tone from being attenuated by the receive background noise monitor. The two line driver amplifiers at the output stage can be used to form a hybrid network in conjunction with an external coupling transformer. In the receive channel, a high pass filter can be used to filter out the 60Hz noise. Also, a chip disable pin permits powering down of the entire circuit in order to conserve power, specially on long loops where loop current is at a minimum.

The speakerphone IC can be powered from the telephone line or with an exterior power source (5mA typical power consumption). Applications of this IC are several and can vary as simple as a standalone product or used in conjunction with a handset speech network or a pulse/tone dialer.

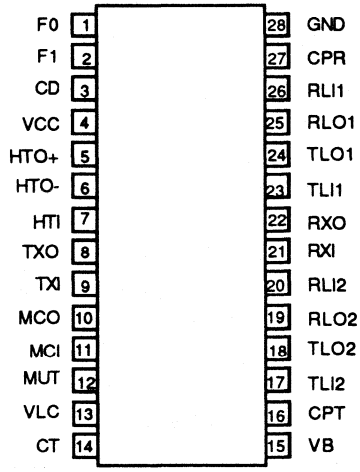
APPLICATIONS

Featurephones
Intercoms
Voice Operated Switches

FEATURES

Attenuator Gain Range: 52 db between Transmit and Receive.
Low Voltage Operation: 3.0 to 6.5V
Improved Sensitivity: 4 Point Signal Sensing Background Noise Monitor on Transmit and Receive Sides.
Mute Feature with Externally Adjustable Microphone Amplifier Gain
Chip Disable for Active/Standby Operation
On Board Filter Pinned Out For User Defined Function
Dial Tone Detector to Inhibit Receive Idle Mode During Dial Presence
Compatible with the XR-T34119 Speaker Amplifier

PIN OUT



XR-T34118
DIP PACKAGE

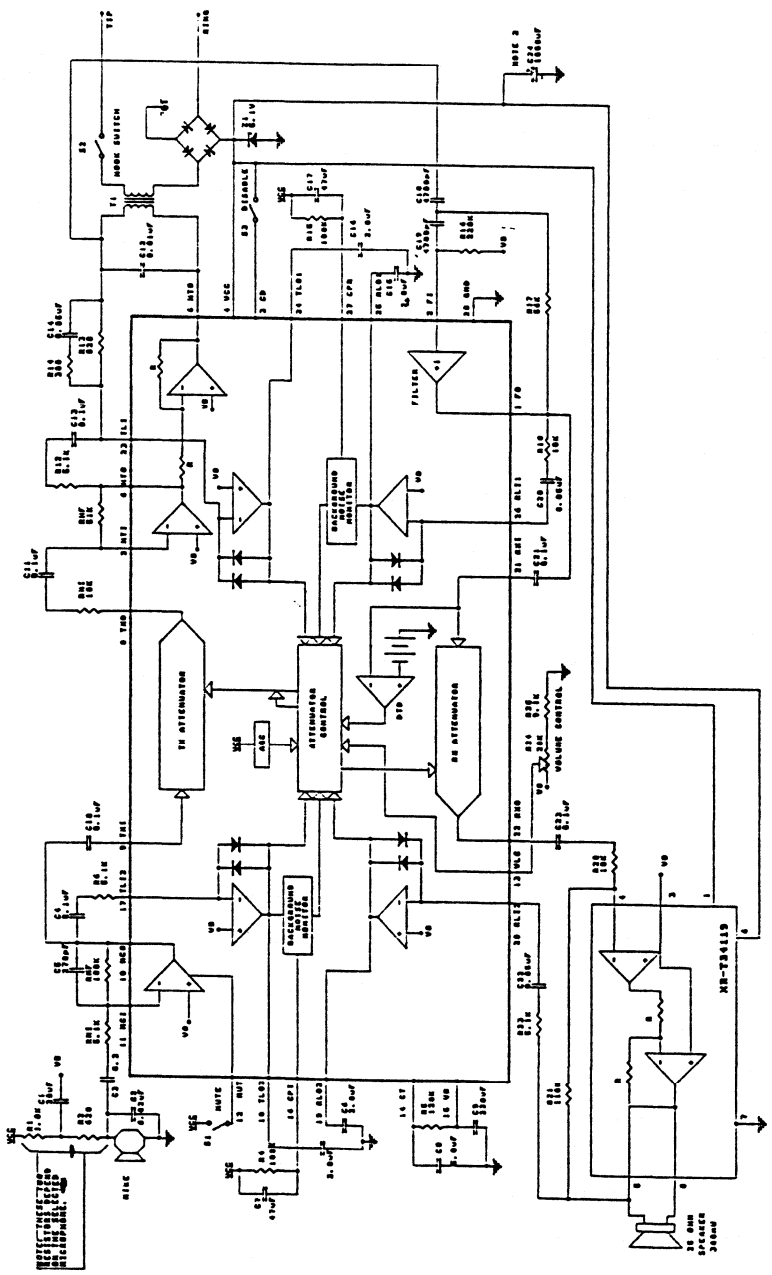
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-1V to 7.0V
Voltage at CD and MUT	-1V to V_{CC}+1V
Voltage at VLC	-1V to V_{CC} +0.5V
Voltage at TXI, RXI	-0.5V to V_{CC}+0.5V
Storage Temperature	-65°C to 150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T35118CP	Plastic	0C to +70°C
XR-T34118D	SOP	0C to +70°C

FUNCTIONAL BLOCK DIAGRAM



Note: 1- Component values are recommendations only and will vary in different applications.
2- This capacitor must be physically adjacent to pin 4 of the XR-T34118 for best performance.
3- Recommended transformer : Stancor TTPC-13, Microtran T5115

Low Power Audio Amplifier

GENERAL DESCRIPTION

The XR-T34119 is a low power audio amplifier designed primarily to operate in conjunction with the XR-T34118 Speakerphone IC. It's differential outputs are able to operate at low supply voltages (2.0V minimum) without coupling capacitors. The open loop gain can be set with two external resistors. Power down or muting of the input signal is possible with the Chip Disable pin which disconnects the internal biasing circuit to the amplifier.

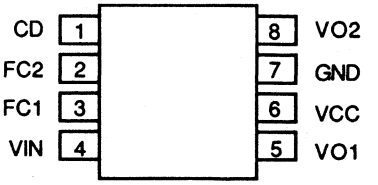
FEATURES

Wide Supply Voltage Range (2-16V, Telephone Line Powered Applications)
Low Quiescent Supply Current (2.7mA Typical-Battery Powered Applications)
Chip Disable Input for Power Down Applications
Low Power Down Quiescent Current (65µA Typical)
Wide Range Drive Capability (8-100 ohms)
Output Power (250mV with 32 Ohm Load)
Low Harmonic distortion (0.5% Typical)
Adjustable Gain (0 to 46db for Voice Band)
Few External Components

APPLICATIONS

Featurephones
Intercoms
Voice Operated Switches
High Performance Voice Amplifier

PIN OUT



XR-T34119

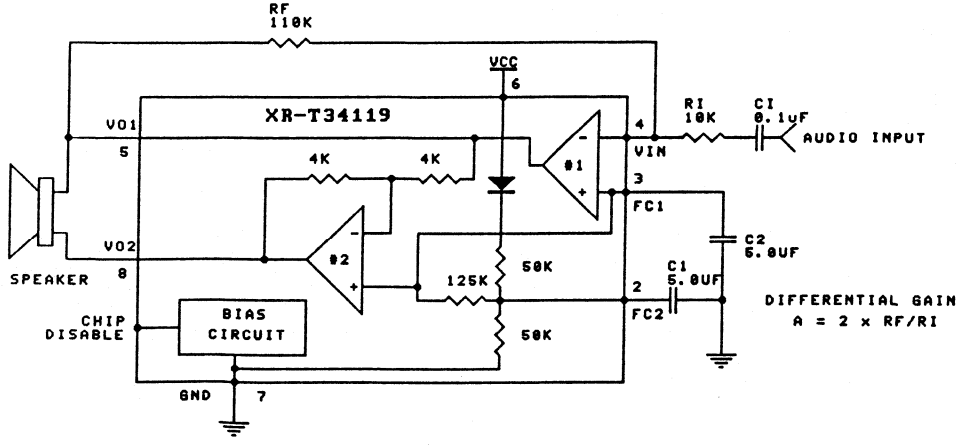
ABSOLUTE MAXIMUM RATINGS

Featurephones
Intercoms
Voice Operated Switches
High Performance Voice Amplifier

ORDERING INFORMATION

Part Number	Device	Operating Temperature
XR-T34119CP	Plastic	0C to 70°C
XR-T34119CD	SOIC	0C to 70°C

FUNCTIONAL BLOCK DIAGRAM



XR-C277/TMO44 EVALUATION DEMOBOARD

GENERAL DESCRIPTION

The XR-C277/TMO44 combination can be used as a T1/CEPT Receiver or Repeater capable of extracting, regenerating and retiming of AMI encoded data. With an additional comparator it is possible to extract the clock, which is generally required for receiver applications. Included in the XR-C277 monolithic repeater is a high performance preamplifier followed by a peak detector, a set of clock and data threshold detectors to extract the timing information, an ALBO (Automatic Line Build Out) circuit to insure that the preamplifier receives the correct amplitude and shape, a clock amplifier to generate a squarewave out of the sinusoidal tank waveform, and a set of latch circuits which sample and hold the received data. The outputs of the two data latches drive the two output driver stages which are designed to work with a nominal load of 100 ohm and be able to handle peak load currents of 30 mA.

FEATURES

1.544/2.048MBPS Repeater or Receiver
Space Saving Hybrid Equalizer
Complete ALBO and Smoothing Filter
Low Power Operation (13mA)
Improved Crosstalk and Noise Performance
Enhanced Performance (36DB Line Loss)
Operating Temperature Range (-40° to 85°C)
Available Packages (C277): Plastic, Ceramic and S.O.P.

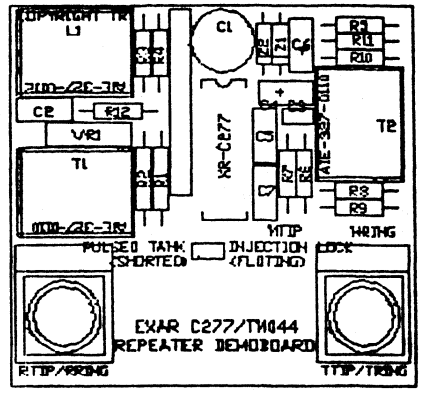
ASSEMBLY PROCEDURE

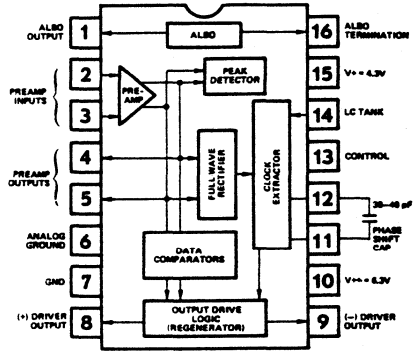
1) Attach four equal spacers to the corners of the Demoboard to ease the assembly procedure.

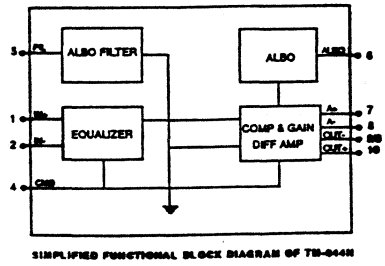
2) Insert and solder all capacitors as marked on the PC Board. Make sure you choose the correct component values, tolerances and polarity where applicable.

3) Insert and solder all resistors and diods in place and clip their leads.

4) Now insert the 16 pin integrated circuit socket. Notice the polarity to avoid damage to the IC when inserted.







SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM OF TS-044N

5) The magnetics used for the demoboard are manufactured by three qualified vendors which are:

a) AIE MAGNETICS (813) 347-2181
b) SCHOTT (612) 475-1173
c) PULSE ENGINEERING (619) 268-2400

For further information and specs on these components please contact the selected magnetic manufacturers. Insert and solder these parts. Notice the polarity of the transformers and tank coil.

6) Carefully insert the XR-C277 IC into the socket without bending the leads and choose the desired input and output connectors. The board is intended to use BNC connectors but can vary depending on the type of test equipment used.

7) Lastly, insert the hybrid network into the corresponding socket.

TEST AND ADJUSTMENT PROCEDURE:

The XR-C277/TMO44 Demoboard is designed to operate as a repeater, but with the small addition of a comparator it is possible to extract the clock output as shown in the applications schematic. It is left to the customers choice to perform the testing and evaluation of this circuitry depending on the type of test instrument and application they may have. The testing of this board was done with the Sierra (415-11) which tests the board in a repeater configuration.

INITIAL ADJUSTMENT

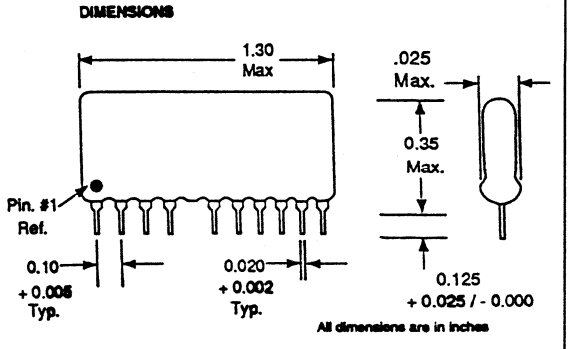
1) Connect the AMI encoded input signal from the Sierra Test Set to the RTIP/RRING input connector of the demoboard. Similarly connect the TTIP/TRING or output signal back to the return line of the test set.

2) Apply power to the test set and check for a: the correct feed through current (supplied by the test set, approx. 50mA and adjustable) and b: the voltage drop (approx. 5V) on the loop which in this case is generated by the exterior zeners.

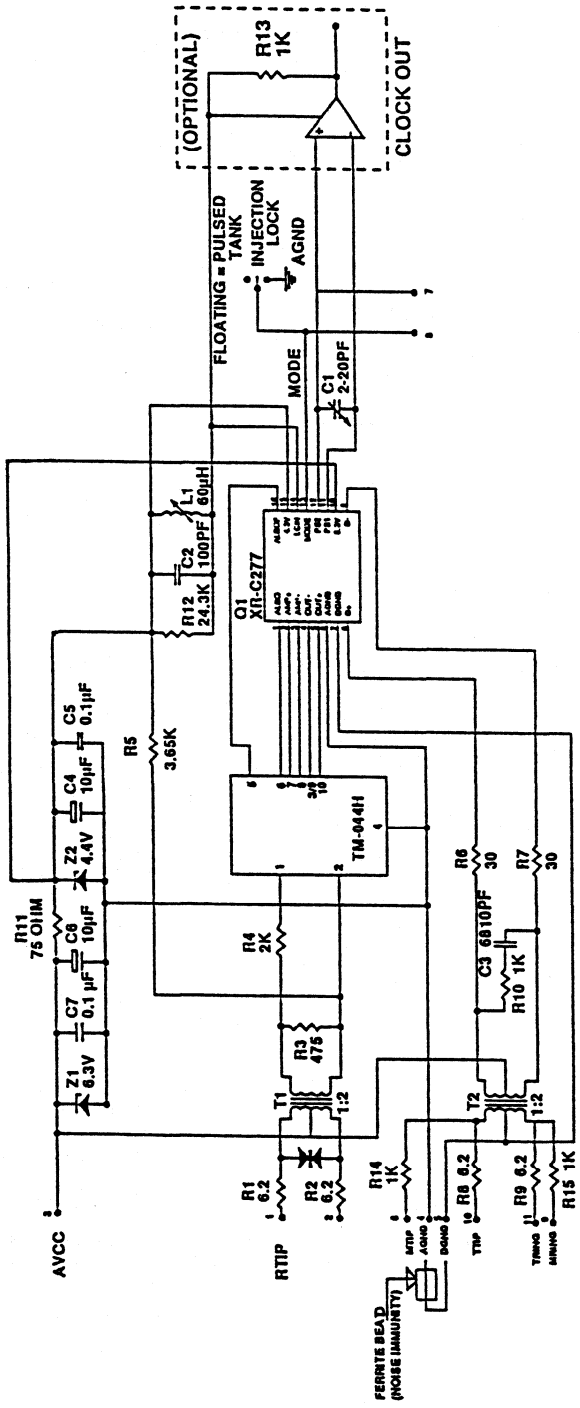
3) To be able to see the input and output waveforms with an oscilloscope, it is necessary to isolate the scope ground from the board ground with a small electrolytic capacitor. Connect this capacitor to the board ground and switch over to an all one's pattern on the test set. Check for a sign of life and look at the extracted data output (pin 8 or 9). Notice that it may look jittery since the board has not been adjusted so far.

4) Place another scope probe on pin 14 (LC Input Pin) and adjust the variable inductor until the sinusoidal output waveform reaches it's maximum amplitude.

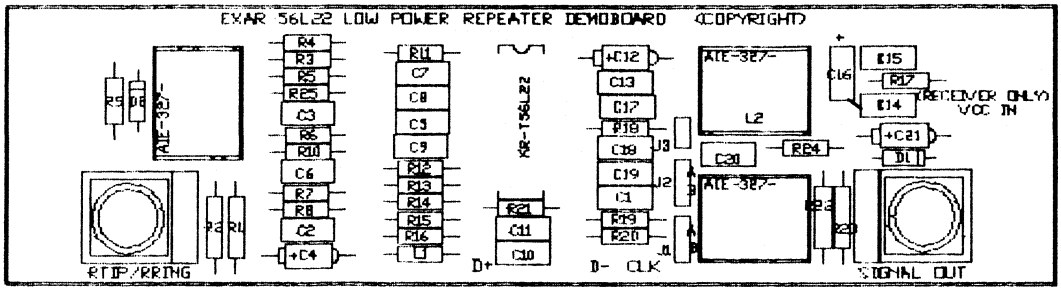
5) Switch the test instrument to generate a QRSS pattern sequence, and place a scope probe on one of the preamplifier output pins (4 or 5) and the other on the extracted data output (pin 8 or 9). Now adjust the phase shift capacitor (C1) until the falling or negative transition of the clock output waveform coinsides directly, or slightly less (30nses), with the top of the preamplifier output pulse (top of the eye.) At this point we should observe the least amount of errors under normal or noisy conditions. The board should be now operating satisfactorily from up to 36dB and approximately 11dB of noise.



7-FEB-1989 Bill of Material Print			
COMP NO.	**LABEL**	**PACKAGE**	**COMMENTS**
1	BNC1	BNC	
2	BNC2	BNC	
3	C1	VARCAP	2-20PF
4	C2	RAD0.2	100Pf
5	C3	RAD0.1	6.8NF
6	C4	RAD0.2	10UF TANT
7	C5	RAD0.2	0.1UF
8	C6	RAD0.2	10UF TANT
9	C7	RAD0.2	0.1UF
10	HYBRID1	HYB	XR-TM044
11	IND	TRANS	327-0112
12	J1	J2	JUMPER
13	R1	AXIAL0.6	6.2 OHM, 1/2W
14	R10	AXIAL0.5	1K, 1/4W
15	R11	AXIAL0.5	75, 1/4W
16	R12	AXIAL0.5	24K, 1/4W
17	R2	AXIAL0.6	6.2 OHM, 1/2W
18	R3	AXIAL0.5	475, I/4W
19	R4	AXIAL0.5	2K, 1/4W
20	R5	AXIAL0.5	3.65K, 1/4W
21	R6	AXIAL0.5	30.1, 1/4W
22	R7	AXIAL0.5	30.1, 1/4W
23	R8	AXIAL0.5	6.2, 1/2W
24	R9	AXIAL0.5	6.2, 1/2W
25	T1	TRANS	327-0110
26	T2	TRANS	327-0110
27	VAR1	RAD0.4	90V
28	XR-C277	DIP16	U1
29	Z1	DIODE0.4	ZENER 6.2V, 1/4W
30	Z2	DIODE0.4	ZENER 4.4V, 1/4W


(OPTIONAL)
R13
1K
CLOCK OUT
FLOATING = PULSED TANK
INJECTION LOCK
AGND
MODE
C1
2-20PF
L1
60µH
C2
100PF
R12
24.3K
Q1
XR-C277
R5
3.65K
C5
0.1µF
C4
10µF
Z2
4.4V
R11
75 OHM
C6
10µF
C7
0.1 µF
Z1
6.3V
TM-0441
R4
2K
R3
475
T1
1:2
R6
30
R7
30
C3
6810PF
R10
1K
T2
1:2
R1
6.2
R2
6.2
R14
1K
R8
6.2
R9
6.2
R15
1K
AVCC
RTIP
FERRITE BEAD
(NOISE IMMUNITY)

XR-T56L22 EVALUATION DEMOBOARD



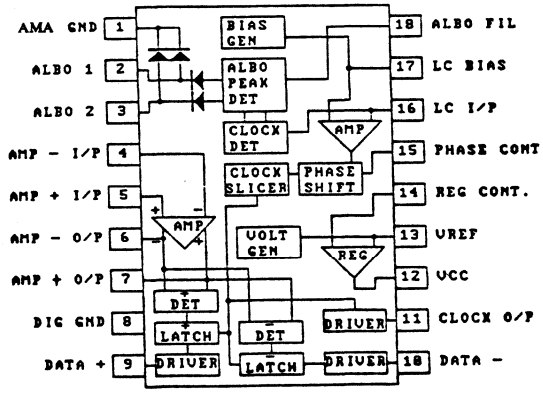
GENERAL DESCRIPTION

The XR-T56L22 is a T1/CEPT Receiver or Repeater capable of extracting, regenerating and retiming of AMI encoded data as well as providing the extracted clock output for applications where it is required. Included are a shunt regulator to generate +5V supply out of the phantom feed current, a high performance preamplifier followed by a set of clock and data threshold detectors to extract the timing information, an ALBO (Automatic Line Build Out) Circuit to insure that the preamplifier receives the correct amplitude and shape, a clock amplifier to generate a square-wave out of the sinusoidal tank waveform, a phase shift network which delays the extracted clock by 90 degrees, and a set of latch circuits which sample and hold the received data. The output stage is capable of driving up to 100mA and it's output is produced by ORing the latched preamplifier information with the inverse clock to insure the correct phase and output pulse shape.

FEATURES

Very Low Power Consumption (7 to 8.75mA)
Data and Clock Extraction up to 40 dB
Dual Matched ALBO Ports
Internal Adjustable Phase Shift Network
Internal Shunt Regulator
Operating Temperature Range (-40° to +85°C)
Available Packages: Plastic, Ceramic and S.O.P.

FUNCTIONAL BLOCK DIAGRAM



XR-T56L22

ASSEMBLY PROCEDURE

1) Attach four equal spacers to the corners of the Demoboard to ease the assembly process.

2) Insert and solder all capacitors as marked on the PC Board. Make sure you choose the correct component values, tolerances and polarity where applicable.

Included are the schematic and Bill of Material for 1.544MBPS and 2.048MBPS applications.

3) Insert and solder all resistors and diodes in place and clip their leads.

Note:
The magnetics used for the demo boards are manufactured by three qualified vendors which are:

a) AIE Magnetics 813-347-2181
b) Schott 612-475-1173
c) Pulse Engineering 619-268-2400

For further information and spec please contact the selected magnetics manufacturers. Insert and solder these parts. Notice the polarity of the transformers and tank coil.

4) Solder in an 18 pin socket and carefully insert the XR-T56L22 IC into it without bending the leads. Use BNC or other type of connectors as input and output ports.

5) Jumpers: Notice the jumper configuration between receivers and repeaters.

	RECEIVER	REPEATER
J1	A SHORTED	B SHORTED
J2	B SHORTED	A SHORTED
J3	SHORTED	OPEN
J4	DIG GND SHORT	DIG GND SHORT
R21	1K OHM	47 OHM
R20	1K OHM	47 OHM

TEST AND ADJUSTMENT PROCEDURE

The XR-T56L22 Demoboard can be configured as a receiver or as a repeater. It is left to the customers choice to perform the testing and evaluation of this circuitry depending on the type of test instruments they feel is most appropriate.

Again, depending on the application, the Sierra (415-11) was used to test the board as a repeater, and an H.P. Pattern Generator/Error Detector (3780A) was used to test the demoboard as a receiver. In both cases the adjustment procedure is very similar.

Initial Adjustment

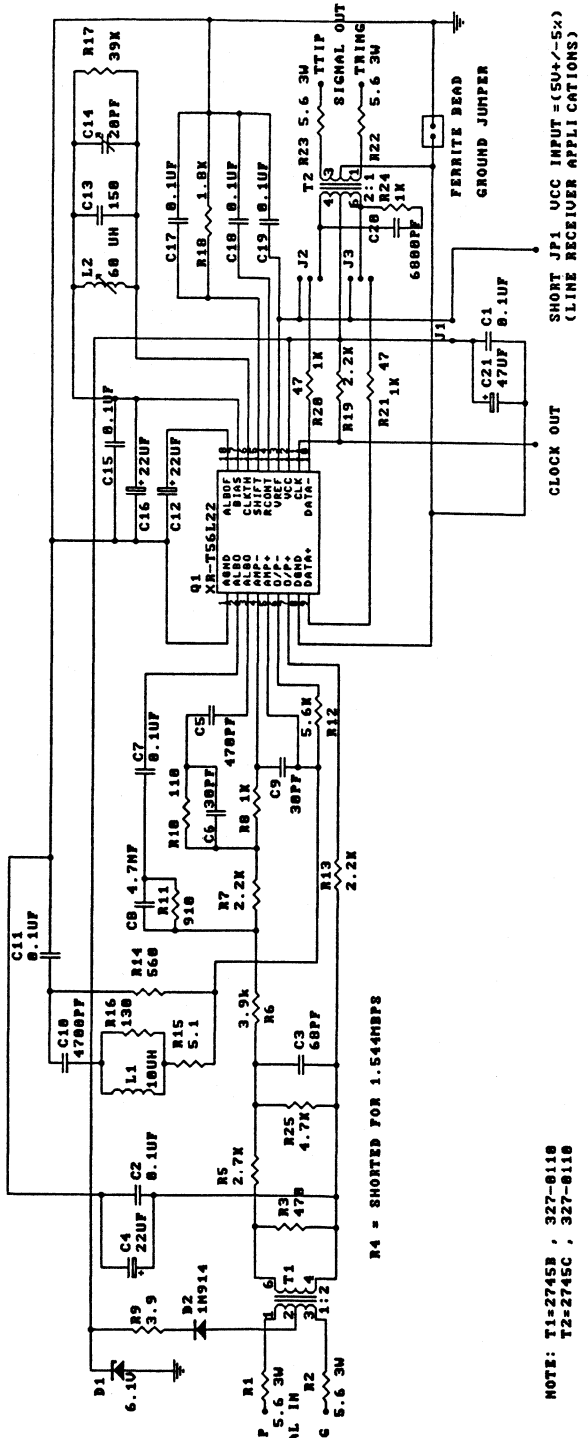
1) Connect the AMI encoded input signal from the Sierra Test Set to the RTIP/RRING input connector of the demoboard. Similarly connect the TTIP/TRING or output signal back to the return of the test set.

2) Apply power to it and check for a: the correct feed current supplied by the test set (approx. 50mA, adjustable) and b: the voltage drop (approx. 5V) on the loop which in this case is generated by the shunt regulator of the XR-T56L22.

3) To be able to see the input and output waveforms with an oscilloscope, it is necessary to isolate the scope ground from the board ground with a small electrolytic capacitor. Connect this capacitor to the board ground and switch over to an all one's pattern on the test set. Check the extracted clock output pin marked CLK. Notice that it may look jittery since the board has not been adjusted so far.

4) Place another scope on pin 16 (LC Input Pin) and adjust the variable inductor until the sinusoidal output waveform reaches it's maximum amplitude.

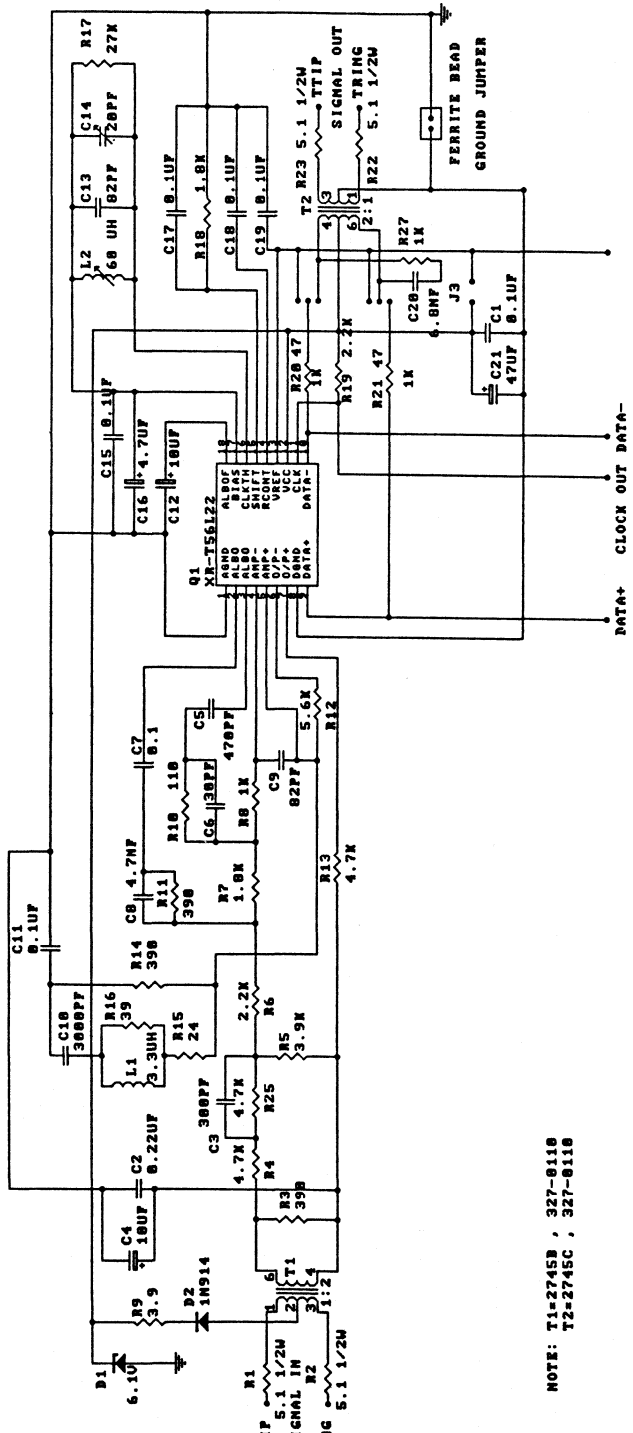
5) Switch the test instrument to generate a QRSS pattern sequence; place a scope probe on one of the preamplifier output pins (6 or 7) and the other on the extracted clock output (pin 11). Now adjust the phase shift resistor (R18) until the falling or negative transition of the clock output waveform coinsides directly, or slightly less (30nses), with the top of the preamplifier output pulse (top of the eye). At this point we should observe the least amount of errors under normal or noisy conditions. At this point the tank may need to be readjusted to operate error free from approximately 5 to 40 db of cable attenuation.



TYPICAL APPLICATION FOR THE XR-T56L22 AT 1.544 MBPS

Bill of Material for 1.544 MBPS Application Circuit

DESCRIPTION	QUANTITY	COMPONENT NAME (S)				
0.1UF	8	C1	C11	C15	C17	C18
		C7	C2			
		C19				
1.8K	2	R7	R18			
1:2	1	T1				
1K		2	R8	R27		
1N914	1	D2				
2.2K	2	R6				
2:1	1	T2				
3.3UH	1	L1				
3.9	1	R9				
3.9K	1	R5				
4.7K	3	R4	R13	R25		
4.7NF	1	C8				
4.7UF	1	C16				
5.1 3W	4	R1	R2	R22	R23	
5.6K	1	R12				
6.1V	1	D1				
6.8NF	1	C20				
10UF	2	C4	C12			
20PF	1	C14				
24	1	R15				
27K	1	R17				
30PF	1	C6				
39	1	R16				
47	2	R20	R21			
47UF	1	C21				
60UH	1	L2				
82PF	2	C9	C13			
110	1	R10				
300PF	1	C3				
390	3	R3	R11	R14		
470PF	1	C5				
3000Pf	1	C10				
XR-T56L22	1	Q1				



TYPICAL APPLICATION FOR THE XR-T56L22 AT 2.048 MBPS

NOTE: T1=27458 , 327-0118
T2=2745C , 327-0118

Bill of Material for 2.048 MBPS Application Circuit

DESCRIPTION	QUANTITY	COMPONENT NAME (S)				
0.1µF	8	C1	C2	C7	C11	C13
		C17	C18	C19		
1.8K	1	R18				
1:2	1	T1				
1K	2	R8	R24			
1N914	1	D2				
2.2K	3	R7	R13	R19		
2.7K	1	R5				
2:1	1	T2				
3.9	1	R9				
3.9K	1	R6				
4.7K	1	R25				
4.7NF	1	C8				
5.1	1	R15				
5.6 3W	4	R1	R2	R22	R23	
5.6K	1	R12				
6.1V	1	D1				
10UH	1	L1				
20PF	1	C14				
22UF	3	C4	C12	C16		
30PF	2	C6	C9			
39K	1	R17				
47	2	R20	R21			
47UF	1	C21				
60UH	1	L2				
68PF	1	C3				
110	1	R10				
130	1	R16				
150	1	C13				
470	1	R3				
560	1	R14				
910	1	R11				
4700PF	1	C10				
6800PF	1	C20				
XR-T56L22	1	Q1				
0.1	1	C7				
0.1UF	6	C1	C11	C15	C17	C18
		C19				
0.22UF	1	C2				
1.8K	2	R7	R18			
1:2	1	T1				

XR-T6421/6420-2 EVALUATION DEMOBOARD

GENERAL DESCRIPTION

The design of a speakerphone is particularly difficult as only one channel is permitted to be fully active at any one time.

Complementary attenuators have been considered to control the transmit and receive signal gain, when one is at maximum gain the other is at maximum attenuation, and vice versa. They are never both fully on or off. Some switching systems are required to operate to detect the presence or absence of speech, subsequently, switching action on the speech signal will subject that signal to clip. In other words, some portions of the signal will be removed.

The XR-T6420-2 and XR-T6421 speakerphone ICs permit the system designers to adjust the performance and operating points of the speakerphone to their specific requirements. Simple steps are provided to check and set the proper levels of transmit and receive channels and control logic.

Each audio path gain needs to be set when the VCA is set to maximum gain levels. The sum of attenuations introduced by both VCAs have to be equal to -50 dB and idle state for each VCA to be -25 dB.

The idle state is the condition where the control logic has not determined which channel should be on, and has placed the system in a wait state with both channels partially on until a decision has been made. To adjust the four rectifiers in the control circuitry, the effect of the noise circuitry needs to be disabled by tying pin 6 and pin 18 of XR-T6421 together.

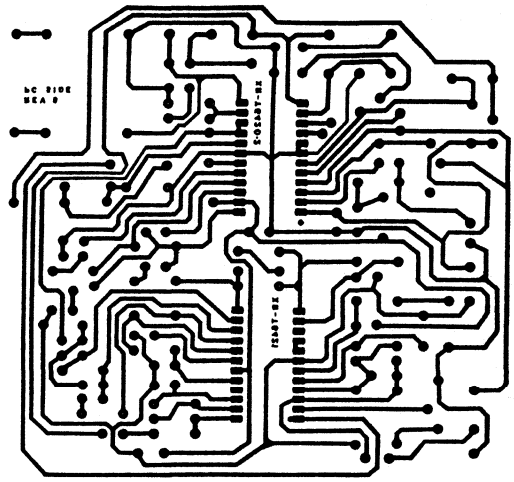
ADJUSTMENTS STEPS

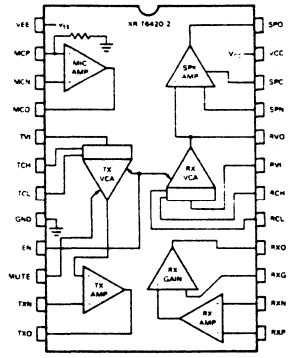
Step 1: Control Voltage Adjustments (Idle Stage)

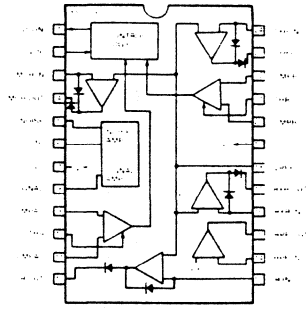
Connect the junction of C1 and R1 to ground. Adjust R3 to make the voltage on pin 17 of XR-T6420-2 between +80 and +90 mV. Adjust R2 to make the voltage on pin 6 of XR-T6420-2 between -80 to -90 mV.

Step 2: T_X Channel Adjustments

Connect the junction of C1 and R1 to V_{CC}. Adjust R4 and R5 to obtain proper levels of the telephone line according to system requirements. Normal gains for the microphone amplifier are in the range of +35 to +45 dB.







Step 3: R_X Channel Adjustments

Connect the junction of C1 and R1 to V_{EE}. Adjust R6 and F7 to obtain proper speaker amplifier gain for maximum level required from the system for normal signal gain levels on line.

Step 4: Receive Sensitivity

Disconnect the microphone. Adjust speaker volume to maximum. Connect a 600 ohm signal generator to the line and monitor the voltage at the junction of C1 and R1.

By monitoring the voltage while increasing the input level, the takeover point from idle (0 volts) to receive (-4.2 volts) can be found. The normal level is about -50 dBm input. The systems takeover point can be adjusted by varying R8. R9 can be changed, but R10 should be made the same value.

Step 5: Transmit Rectifier Adjustment

The transmit rectifier is adjusted to prevent comparator B from sensing a receive state due to the transmit sidetone from the hybrid circuitry. The gain from the transmit rectifier input to comparator B's negative input must be adjusted to be greater than the gain to comparator B's positive input by approximately 3 dB. The gain of the transmit rectifier is adjusted by R11 and R10, keeping in mind that R9 and R10 should be the same value.

Step 6: Microphone Rectifier Adjustment

The microphone rectifier can be adjusted by using a microphone or by applying an input from a signal generator to the microphone amplifier with the microphone disconnected. The background noise circuitry can be disabled if needed by connecting pin 6 to pin 18 of XR-T6421. By monitoring the voltage at the R1, C1 junction, the system takeover point from idle (0 volts) to transmit (+4.2 volts) can be determined. The sensitivity can be varied by adjusting R12 to R13. If R13 is changed, R14 must be changed to the same value.

Step 7: Speaker Rectifier Adjustment

The speaker rectifier is adjusted to prevent comparator A from sensing a transmit state due to acousitc coupling between the speaker and the microphone. The gain from the speaker rectifier input to comparator A's negative input must be greater than the gain from the speaker rectifier input to comparator A's positive input by at least +3dB over frequency. The second path includes the acoustic coupling gain of the microphone amplifier, and gain of the microphone rectifier. The speaker rectifier gain can be adjusted by R15 or R14, keeping in mind that R14 and R13 should be equal in value.

Step 8: Side Tone Cancellation

To prevent echoing and singing, hybrid circuits have been used in the speakerphone to cancel the side tone effects. R17, R18, and R16 determines side tone cancellation levels assuming impedance of the transformer is 600 ohms.

Step 9: Reference Guide

Transmit Rectifier	
Low Pass Filter	R11, C2
Rectifier Gain	R11, R10
Attack Time	R19, C3
Receive Rectifier	
Rectifier Gain	R20, R9
Attack Time	R20, C4
High Pass Filter	
2 Pole Unity Gain Filter	R21, R22, C5, C6, C7
Speaker Rectifier	
Low Pass Filter	R15, C8
Rectifier Gain	R14, R15
Attack Time	R23, C9
Noise Detection Filter	R24, C10
Microphone Rectifier	
Low Pass Filter	R12, C11
Rectifier Gain	R12, R13
Attack Gain	R25, C12
Volume Control	R26, R27
Microphone Amplifier	
Amplifier Gain	R4
VCA Threshold Levels	
R_X VCA	R28, R3
T_X VCA	R29, R2
T_X Line Level	R5, R30
Speaker Amplifier	
Amplifier Gain	R6, R7
Switching Time Const.	R1, C1

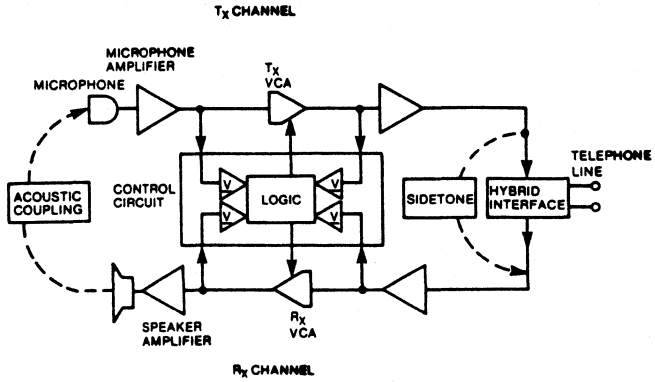


Figure 1. General Speakerphone Circuit

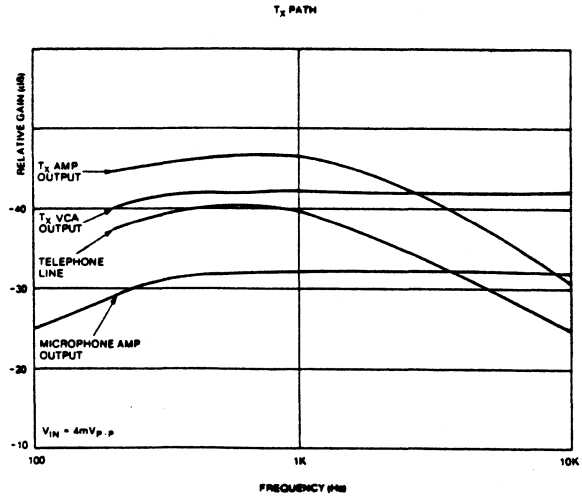
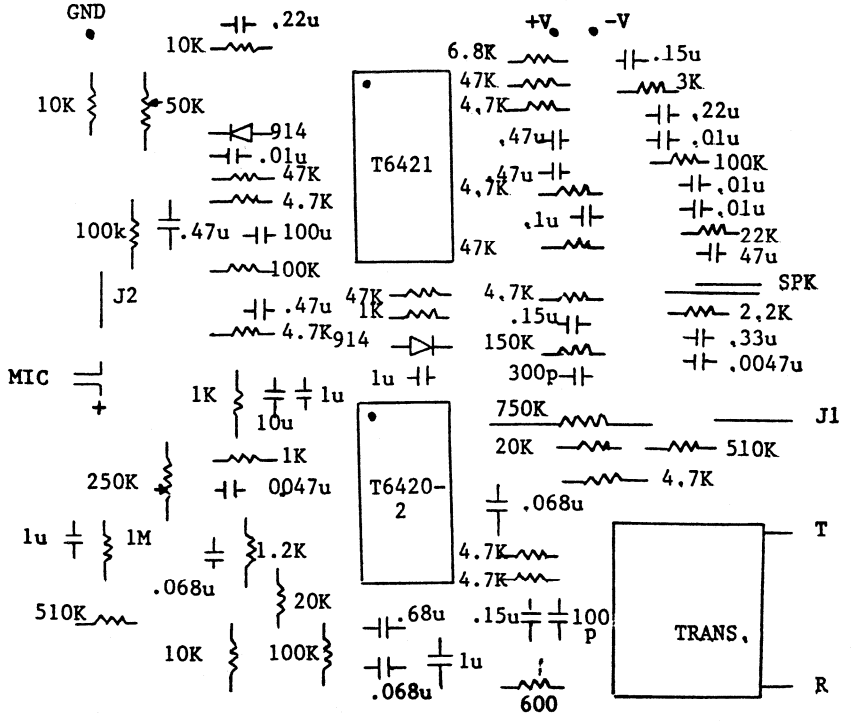
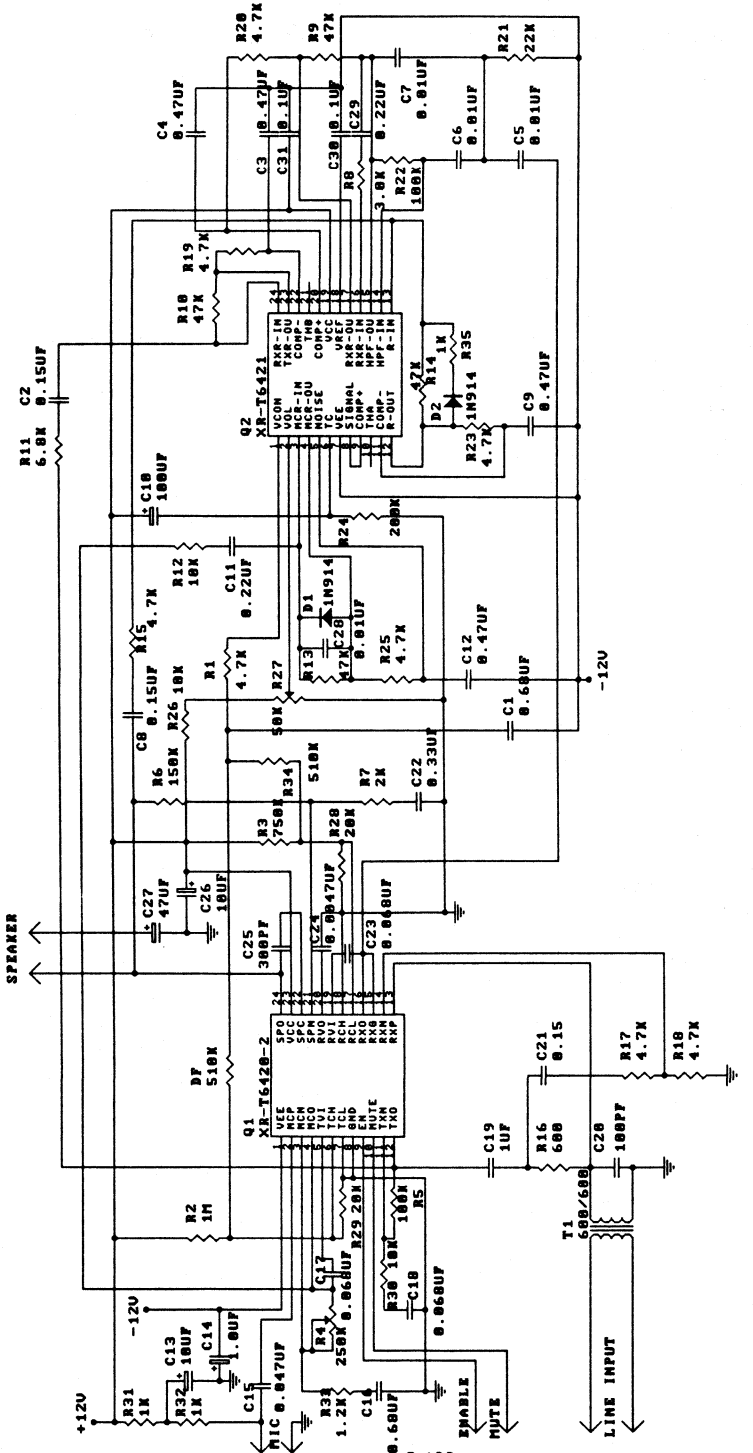


Figure 2. Frequency Response and Gain



T64230-2 and T6421 Speaker Phone Demo

TANGO-SCHEMATIC BILL OF MATERIAL FOR T6421						
DESCRIPTION	**QUAN.**	**COMPONENT**	**NAME(S)**	**NAME(S)**	**NAME(S)**	**NAME(S)**
0.01UF	4	C6	C7	C28	C5	
0.1UF	2	C30	C31			
0.15	1	C21				
0.15UF	2	C2	C8			
0.22UF	2	C11	C29			
0.33UF	1	C22				
0.47UF	4	C3	C4	C9	C12	
0.0047UF	1	C24				
0.047UF	1	C15	C17			
0.068UF	3	C23	C16	C18		
0.68UF	2	C1				
1.0UF	1	C14				
1.2K	1	R33				
1K	3	R31	R32	R35		
1M	1	R2				
1N914	2	D1	D2			
1UF	1	C19				
2K	1	R7				
3.0K	1	R8				
4.7K	8	R1	R15	R17		R19
		R20	R23	R25	R18	
6.8K	1	R11				
10K	3	R12	R26	R30		
10UF	2	C13	C26			
20K	2	R28	R29			
22K	1	R21				
47K	4	R9	R10	R13	R14	
47UF	1	C27				
50K	1	R27				
100K	2	R5	R22			
100PF	1	C20				
100UF	1	C10				
150K	1	R6				
200K	1	R24				
250K	1	R4				
300PF	1	C25				
510K	2	DF	R34			
600	1	R16				
600/600	1	T1				
750K	1	R3				
XR-T6420-2	1	Q1				
XR-T6421	1	Q2				


SPEAKER
LINE INPUT
ENABLE
MUTE
MIC
+12V
-12V
Q1 XR-T6428-2
Q2 XR-T6421
T1 600/600
D1 1N914
D2 1N914
R1 4.7K
R2 1M
R3 750K
R4 250K
R5 100K
R6 150K
R7 2K
R8 3.9K
R9 47K
R10 47K
R11 6.8K
R12 10K
R13 47K
R14 1K
R15 4.7K
R16 600
R17 4.7K
R18 4.7K
R19 4.7K
R20 4.7K
R21 22K
R22 100K
R23 4.7K
R24 200K
R25 4.7K
R26 10K
R27 50K
R28 20K
R29 20K
R30 10K
R31 1K
R32 1K
R34 510K
R35 47K
DF 510K
C1 0.68UF
C2 0.15UF
C3 0.47UF
C4 0.47UF
C5 0.01UF
C6 0.01UF
C7 0.01UF
C8 0.15UF
C9 0.47UF
C10 100UF
C11 0.22UF
C12 0.47UF
C13 10UF
C14 1.0UF
C15 0.047UF
C16 0.68UF
C17 0.068UF
C18 0.068UF
C19 1UF
C20 100PF
C21 0.15
C22 0.33UF
C23 0.068UF
C24 0.0047UF
C25 300PF
C26 10UF
C27 47UF
C28 0.01UF
C29 0.22UF
C30 0.1UF
C31 0.1UF

XR-C240 Monolithic PCM Repeater

INTRODUCTION

The XR-C240 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Mega bits per second (Mbps) data rates on T-1 type PCM lines. The device is packaged in hermetic 16-pin DIP package and is designed to operate over a temperature range of $-40°C$ to $+85°C$. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Build-out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities. Compared to conventional repeater designs using discrete components, the XR-C240 monolithic repeater IC offers greatly improved reliability and performance and provides significant savings in power consumption and system cost.

THE T-1 REPEATER SYSTEM:

The T-1 Repeater Line is designed to provide a transmission capability for 24 two-way voice frequency signals which are transmitted digitally using a Pulse-Code Modulation (PCM) technique. The system operates at a data rate of 1.544 Mbps, with bipolar data pulses. It can operate on either pulp- or polyethylene-insulated paired cable that is either pole mounted or buried. Operation is possible with a variety of wire gauges, provided that the total cable loss at 772 kHz is less than 36 dB. Thus, the system can operate satisfactorily on nearly all paired cables which are used for voice frequency trunk circuits.

The transmission system is designed to operate with both directions of transmission within the same cable sheath. The system performance is limited primarily by near-end crosstalk produced by other systems operating within the same cable sheath. In order to insure that the probability of a bit error is less than 10^{-6}, the maximum allowable repeater spacing, when used with 22-gauge pulp cable, is approximately 6000 feet.

The details of the T-1 type PCM systems are well covered in the literature listed in References 1 through 5.

Figure 1 shows the block diagram of a bi-directional PCM repeater system consisting of two identical digital regenerator or repeater sections, one for each direction of transmission. These repeaters share a common power supply. The dc power is simplexed over the paired cable and is extracted at each repeater by means of a series zener diode regulator.

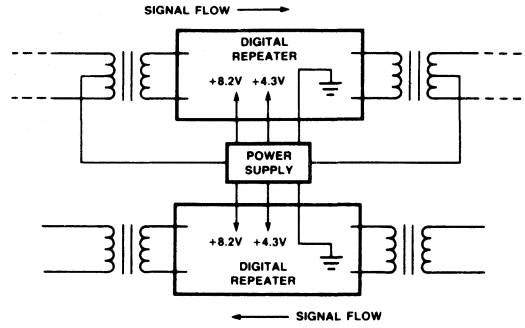


Figure 1. Block Diagram of a Bi-directional Digital Repeater System.

The XR-C240 monolithic IC replaces about 90% of the electronic components and circuitry within the "digital repeater" sections of Figure 1. Thus, a bi-directional repeater system would require two XR-C240 ICs, one for each direction of information flow.

Figure 2 shows the functional block diagram of one of the digital repeater sections, along with the external zener regulator. The basic system architecture shown in the figure is the same as that utilized in the design of the XR-C240 monolithic IC.

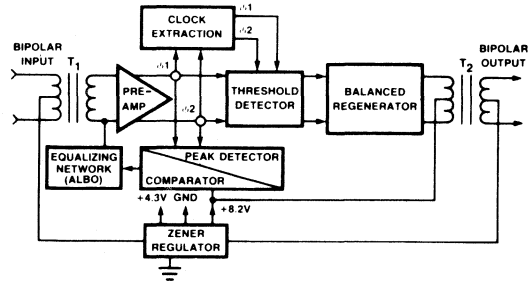


Figure 2. Functional Block Diagram of a Digital PCM Repeater Section.

In terms of the functional blocks shown in Figure 2, the basic operation of the repeater can be briefly explained as follows:

The bipolar signal, after traversing through a dispersive, noisy medium is applied to a linear amplifier and automatic equalizer. It is the function of this circuit to provide the necessary amount of gain and phase equalization and, in addition, to band limit the signal in order to optimize the performance of the repeater for near-end crosstalk produced by other systems operating within the same cable sheath.

The output signals of the preamplifier which are balanced and of opposite phases are applied to the clock extraction circuit and also to the pulse regenerator. The signals applied to the clock extraction circuit are rectified and then applied to a high-Q resonant circuit. This resonant circuit extracts a 1.544 MHz frequency component from the applied signal. The extracted signal is first amplified and then used to control the time at which the output signals of the preamplifier are sampled and also to control the width of the regenerated pulse.

It is the function of the pulse regenerator to perform the sampling and threshold operations and to regenerate the appropriate pulse. The regenerated pulse is in turn applied to a discrete switch which is used to drive the next section of the paired cable.

REFERENCES ON PCM REPEATERS:

1. Mayo, J. S., "A Bipolar Repeater for Pulse Code Signals," B.S.T.J., Vol. 41, January, 1962, pp. 25-97.
2. Aaron, M. R., "PCM Transmission in the Exchange Plant," B.S.T.J., Vol. 41, January, 1962, pp. 99-143.
3. Davis, C. G., "An Experimental Pulse Code Modulation System for Short-Haul Trunks," B.S.T.J., Vol. 41, January, 1962, pp. 1-25.
4. Fultz, K. E., and Penick, D. B., "The T-1 Carrier System," B.S.T.J., Vol. 44, September, 1965, pp. 1405-1452.
5. Tarbox, R. A., "A Regenerative Repeater Utilizing Hybrid IC Technology," Proceedings of International Communications Conference, 1969, pp. 46-5 — 46-10.

OPERATION OF THE XR-C240

The XR-C240 combines all the functional blocks of a PCM repeater system in a single monolithic IC chip. The pin connections for each of the functional circuits within the repeater chip are shown in Figure 3, for a 16-pin dual-in-line (DIP) package.

The circuit is designed to operate with two positive supply voltages, V^{++} and V^{+} which are nominally set to be 8.2V and 4.3V, respectively. Figure 4 gives a typical recommended power supply connection for the circuit.

The supply currents I_A and I_B drawn from the two supply voltages applied to the chip are specified to be within the following limits:

a. Current from 8.2V supply voltage, I_A:

$$1.1mA \leq I_A \leq 2.5mA$$

b. Current from 4.3V supply voltage, I_B:

$$6mA \leq I_B \leq 11mA$$

The external components necessary for proper operation of the circuit are shown in Figure 5, in terms of the

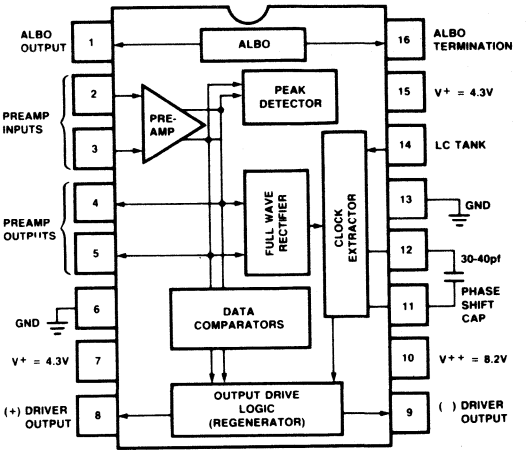


Figure 3. Package Diagram of XR-C240 Monolithic PCM Repeater.

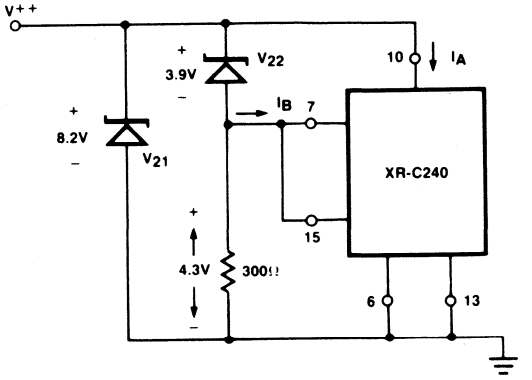


Figure 4. Recommended supply Voltage Connection for XR-C240 (Note: See Figure 6 for Recommended bypass capacitors).

ELECTRICAL CHARACTERISTICS
(Measured at 25°C with V++ = 8.2V, V+ = 4.3 V, unless specified otherwise.)

PARAMETER	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS
Supply Voltage:				
$V++$	7.79	8.61	V	Measured at Pin 10
$V+$	4.085	4.515	V	Measured at Pins 7 and 15
Supply Current:				See Figure 4
I_A	1.1	2.5	mA	Supply = 8.2V
I_B	6	11	mA	Supply = 4.3V
Total Current	7.1	13.5	mA	
Preamplifier				
Input Offset Voltage, V_{OS}		15	mV	
Open Loop Differential Gain, A_O	50	54	db	
Input Bias Current, I_B		4	μA	
Input Offset Current, I_{OS}		2	μA	
Input Impedance, R_{in}	50		kΩ	
Comparator Thresholds				See Figure 8 Measured Differentially Across Pins 4 and 5
Peak Detector (ALBO) Threshold	±1.3	±1.6	V	
Full-Wave Rectifier Threshold	±0.9	±1.15	V	
Data Threshold	±0.28	±0.48	V	
Clock Extractor Section				See Figure 10
Tank Drive Impedance	50		kΩ	At Pin 14
Tank Drive Current				
"Zero" Signal Current	12	24	μA	
"One" Signal Current	80	220	μA	
Recommended Tank Q	100			
Phase Shifter Offset Voltage	−18	+18	mV	Voltage applied to Pins 7 and 14 to reduce differential voltage across Pins 11 and 12 to zero.
Output Drive Section				See Figure 12 Voltage levels referenced to Pin 7
Output Voltage Swing	3.0		V	R_L = 100 Ω
Low Output Voltage	0.65	0.95	V	Referenced to Pin 7, I_L = 30 mA
Output Leakage Current		50	μA	
Output Pulse				See Figure 13
Maximum Pulse Width Error		±30	ns	
Rise and Fall Times		80	ns	

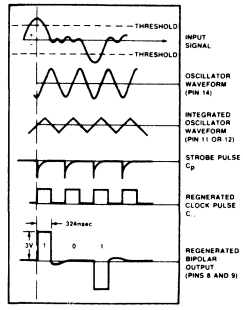


Figure 13. Typical Timing Waveforms for a 1—0—1 Input Data Pattern

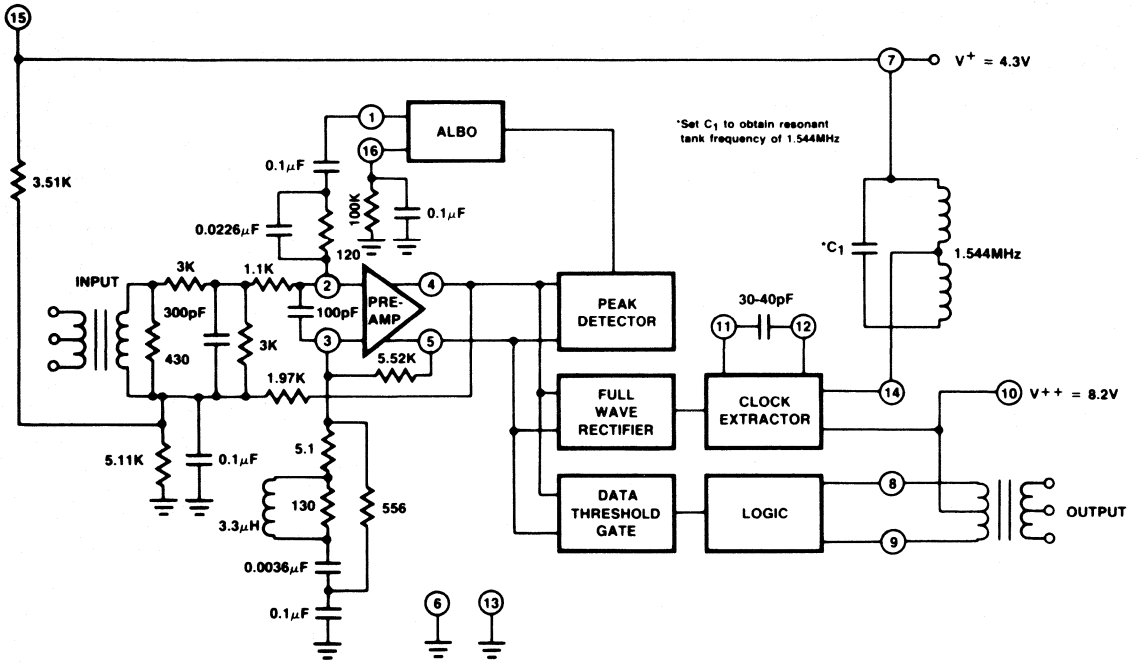


Figure 5. External Components Necessary for Circuit Operation.

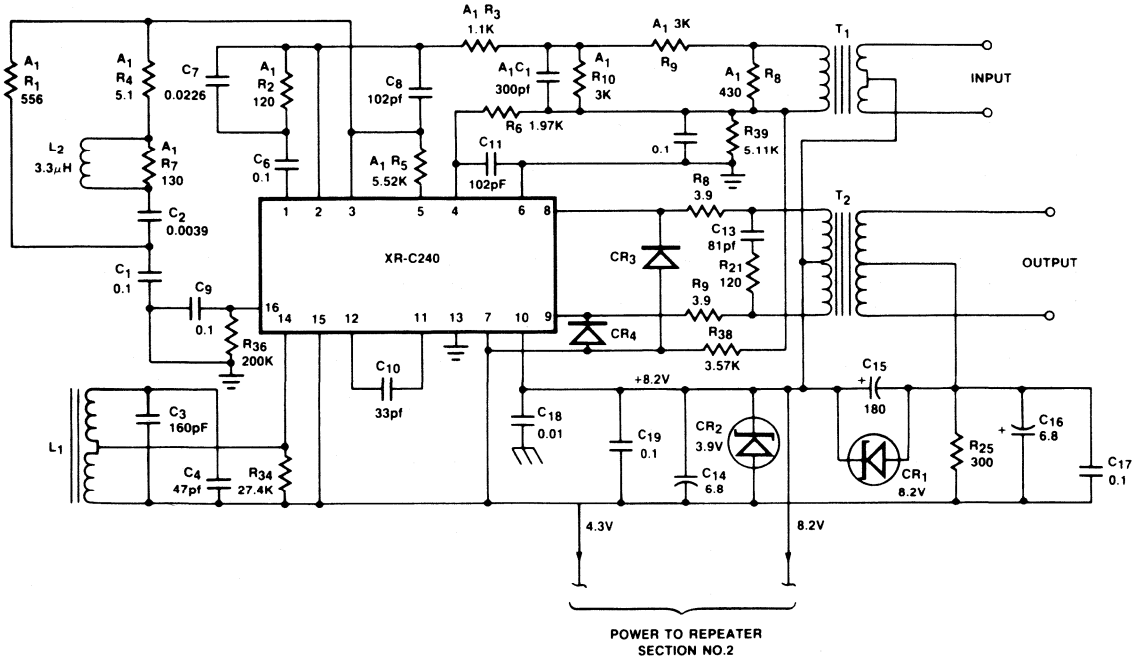


Figure 6. A Typical Circuit Connection for XR-C240 in 1.544 MHz T-1 Repeater System.

system block diagram. Note that all the blocks shown in Figure 6 are a part of the monolithic IC; and the numbered circuit terminals correspond to the IC package pins (see Figure 4).

Figure 6 shows a practical circuit connection for the XR-C240 in an actual PCM repeater application for 1.544 Mbps T-1 Repeater application. For simplification purposes, the lightening protection circuitry and the second repeater section are not shown in the figure.

DESCRIPTION OF CIRCUIT OPERATION:

This section gives a brief description of the internal circuitry contained within the XR-C240 monolithic IC.

The circuit diagram of the preamplifier section is shown in Figure 7. This section is designed as a two-stage differential amplifier with a broadband voltage gain of 52db. The differential outputs of the preamplifier (Pins 4 and 5) are internally connected to the peak-detector,

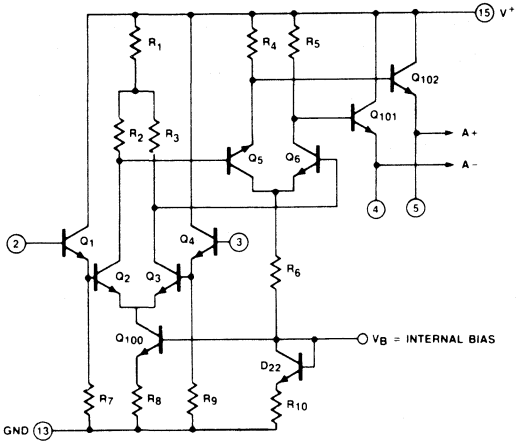


Figure 7. Circuit Diagram of Preamplifier Section.

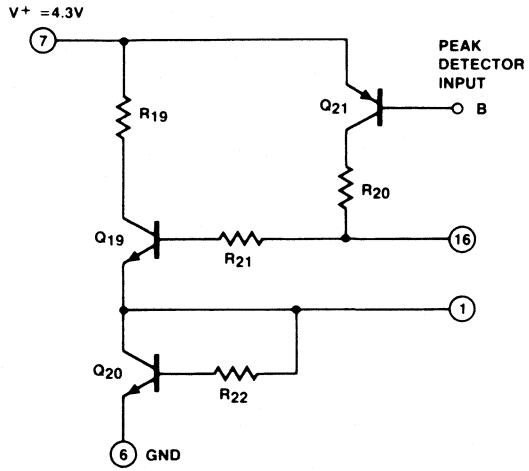


Figure 9. Automatic Line Build-Out (ALBO) Section.

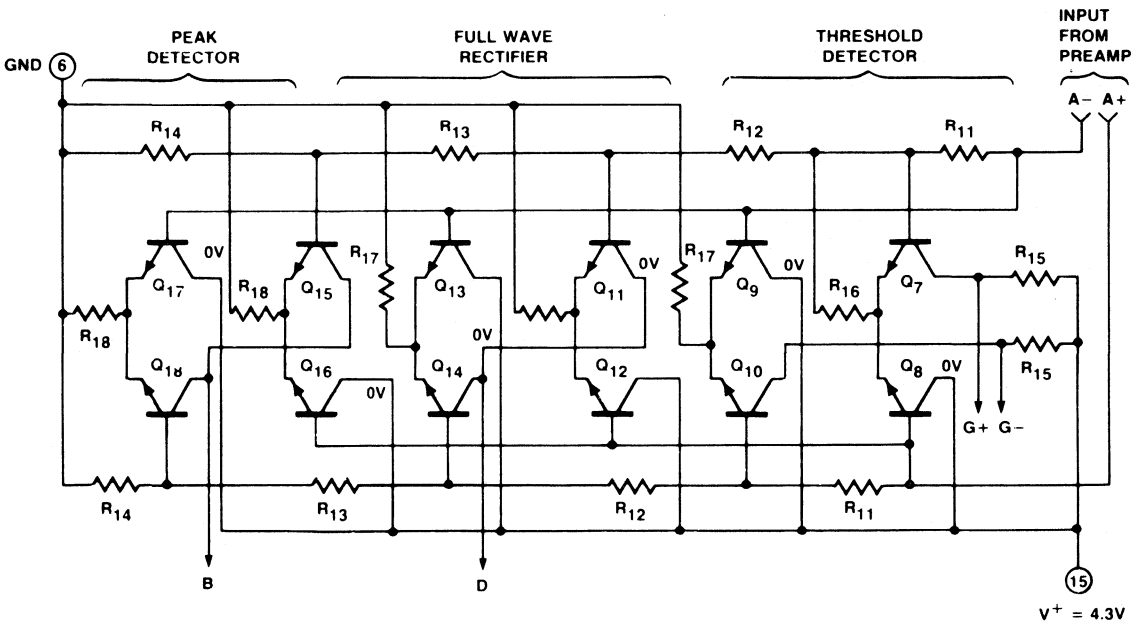


Figure 8. Circuit Diagram of Threshold-Detector, Full-Wave Rectifier and Peak-Detector Sections.

full-wave rectifier and the threshold detector sections of the XR-C240 as shown in Figure 8.

The peak-detector output (terminal B of Figure 8) is internally connected to the Automatic Line Build-out (ALBO) section of the circuit and controls the DC bias current through the ALBO diodes Q_{19} through Q_{20}, as shown in Figure 9.

The full-wave rectifier output (output D of Figure 8) is internally connected to the clock-extractor section of the repeater and provides the excitation signal for the L-C tuned tank circuit (Pin 14) of the injection locked oscillator. The threshold-detector outputs (G+ and G− of Figure 8) provide the differential logic drive to the data latches of the logic section of XR-C240.

The clock-extractor section of XR-C240 is designed as an injection locked oscillator as shown in the circuit schematic of Figure 10. The excitation is applied to the emitter of Q_{23}, through terminal D which is internally connected to the output of the threshold comparator. This signal in turn controls the current in the resonant L-C tank circuit connected to Pin 14. The sinusoidal waveform across the tank is then amplified and squared through the cascaded differential gain stages made up of Q_{31}, Q_{32} and Q_{35}, Q_{36}. The output swing of the second gain stage is "integrated" by the phase-shift capacitor, C_1, externally connected to Pins 11 and 12. (See timing diagrams of Figure 13.) The nominal value of this capacitor is in the 30 to 40pf range. The triangular waveform across Pins 11 and 12 is at quadrature phase with the sinusoidal voltage swing across the L-C tank circuit. This waveform is then used to generate the "strobe" signal, C_p, and the clock pulse C_ϕ, which is applied to the data latches of the logic section.

The strobe and clock pulses out of the clock-regenerator section are applied to the output data latches shown in Figure 11. The two parallel output R-S flip-flops are driven by the differential inputs (G+ and G−) from the data comparator of Figure 8. The two sets of differential data signals, F_1, $\overline{F_1}$ and F_2, $\overline{F_2}$ are then applied to the output driver amplifier shown in Figure 12. The high-current outputs of the driver stage (Pins 8 and 9) are connected to the center-tapped output transformer as shown in Figure 5. The voltage swing across the output is one diode drop (V_{BE}) less than the supply voltage spread, i.e.:

$$\text{Peak Output Swing} = (V^{++}) - (V^{+}) - (V_{BE}) \simeq 3.2V$$

The output stage is designed to work into a nominal load impedance of 100 ohms, and can handle peak load currents of 30mA.

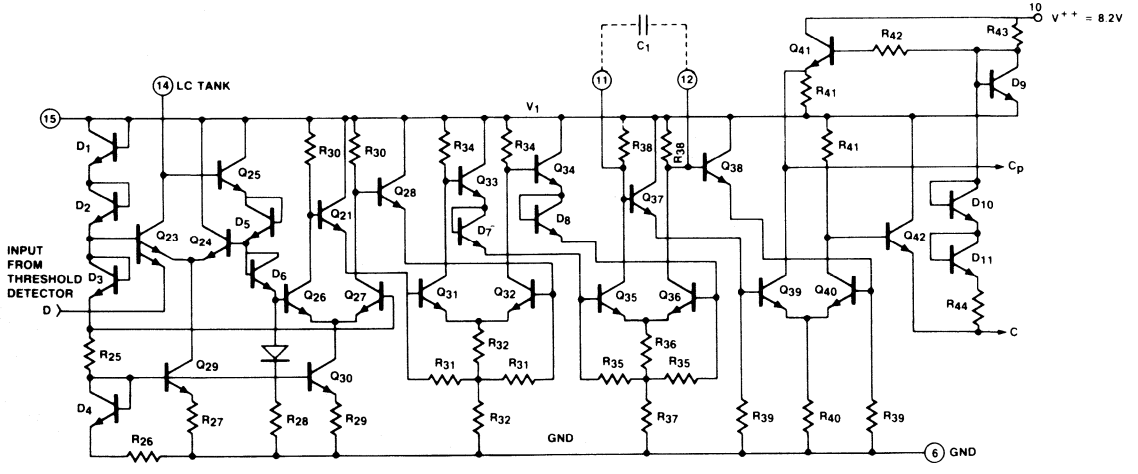


Figure 10. Circuit Diagram of Clock Extractor Section.

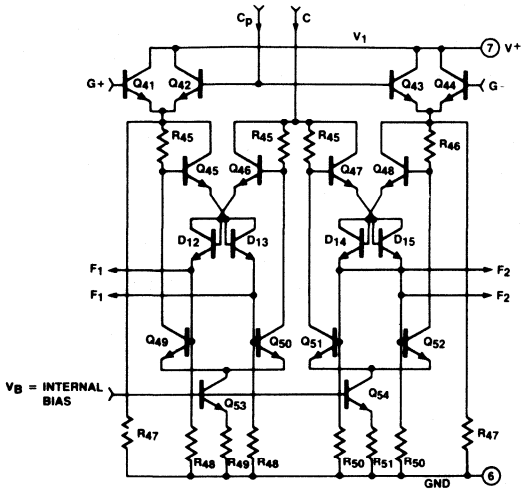


Figure 11. Data Output Latches (Logic Section).

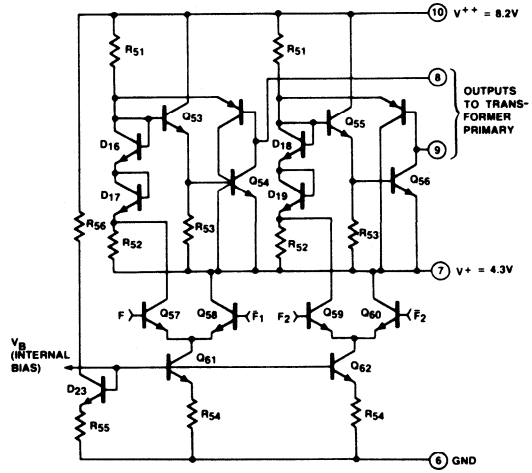


Figure 12. Output Driver Section.

XR-C277 Low-Voltage PCM Repeater IC

INTRODUCTION

The XR-C277 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Mega bits per second (Mbps) data rates on T-1 type PCM lines. It is packaged in a hermetic 16-pin CERDIP package and is designed to operate over a temperature range of −40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Build-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

The key feature of the XR-C277 is its ability to operate with low supply voltages (6.3 volts and 4.4 volts) with a supply current of less than 13 mA. Compared to conventional repeater designs using discrete components, the XR-C277 monolithic repeater IC offers greatly improved reliability and performance and provides significant savings in power consumption and system cost.

FUNDAMENTALS OF PCM REPEATERS

Figure 1 shows the block diagram of a bi-directional PCM repeater system consisting of two identical digital regenerator or repeater sections, one for each direction of transmission. These repeaters share a common power supply. The DC power is simplexed over the paired cable and is extracted at each repeater by means of a series zener diode regulator. The XR-C277 monolithic IC replaces about 90% of the electronic components and circuitry within the digital repeater sections of Figure 1. Thus, a bi-directional repeater system would require two XR-C277 IC's, one for each direction of information flow.

Figure 2 shows the functional block diagram of one of the digital repeater sections, along with the external zener regulator. The basic system architecture shown in the figure is the same as that utilized in the design of the XR-C277 monolithic IC.

In terms of the functional blocks shown in Figure 2, the basic operation of the repeater can be briefly explained as follows:

The bipolar signal, after traversing through a dispersive, noisy medium, is applied to a linear amplifier and automatic equalizer. It is the function of this circuit to provide the necessary amount of gain and phase equalization and, in addition, to band limit the signal in order to optimize the performance of the repeater for near-end crosstalk produced by other systems operating within the same cable sheath.

The output signals of the preamplifier which are balanced and of opposite phases are applied to the clock extraction circuit and also to the pulse regenerator. The signals applied to the clock extraction circuit are rectified and then applied to a high-Q resonant circuit. This resonant circuit extracts a 1.544 MHz frequency component from the applied signal. The extracted signal is first amplified and then used to control the time at which the output signals of the preamplifier are sampled and also to control the width of the regenerated pulse.

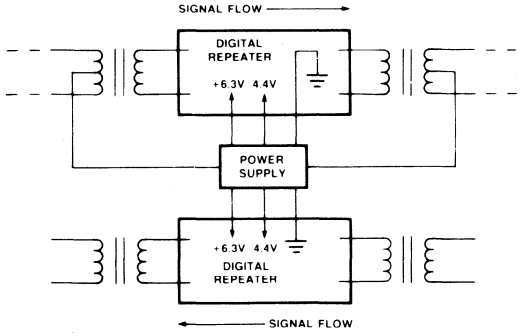


Figure 1. Block Diagram of a Bi-Directional Digital Repeater System

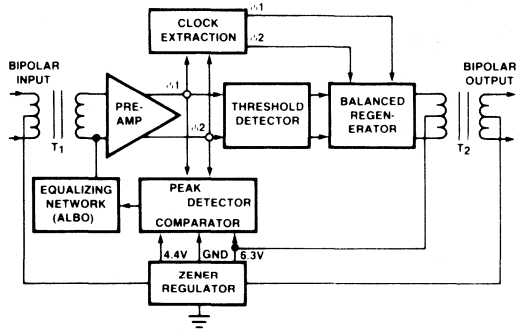


Figure 2. Functional Block Diagram of a Digital PCM Repeater System

It is the function of the pulse regenerator to perform the sampling and threshold operations and to regenerate the appropriate pulse. The regenerated pulse in turn applied to a discrete output transformer which is used to drive the next section of the paired cable.

Additional References on PCM Repeaters:

1. Mayo, J. S., "A Bipolar Repeater for Pulse Code Signals," B.S.T.J., Vol. 41, January, 1962, pp. 25-97.
2. Aaron, M. R., "PCM Transmission in the Exchange Plant," B.S.T.J., Vol. 41, January, 1962, pp. 99-143.
3. Davis, C. G., "An Experimental Pulse Code Modulation System for Short-Haul Trunks," B.S.T.J., Vol. 41, January, 1962, pp. 1-25.
4. Fultz, K. E. and Penick, D. B., "The T-1 Carrier System," B.S.T.J., Vol. 44, September, 1965, pp. 1405-1452.
5. Tarbox, R. A., "A Regenerative Repeater Utilizing Hybrid IC Technology," Proceedings of International Communications Conference, 1969, pp. 46-5 — 46-10.

OPERATION OF THE XR-C277

The XR-C 277 combines all the functional blocks of a PCM repeater system in a single monolithic IC chip. The pin connections for each of the functional circuits within the repeater chip are shown in Figure 3, for a 16-pin dual-in-line package.

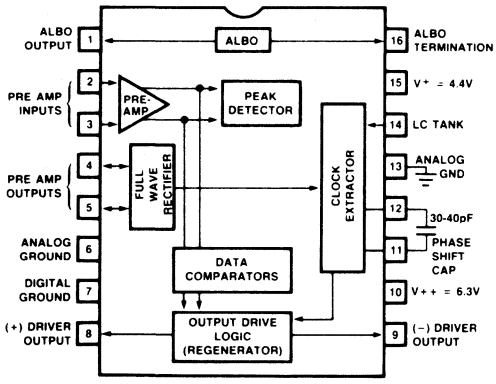


Figure 3. Package Diagram of XR-C277 Monolithic PCM Repeater

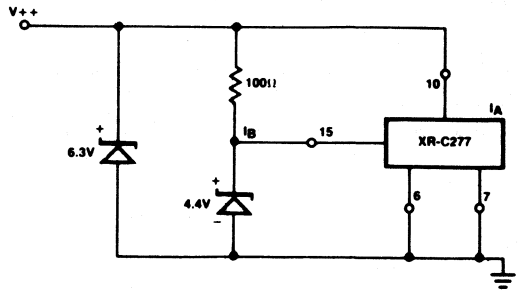


Figure 4. Recommended Supply Voltage Connection for XR-C277 (Note: See Figure 6 for Recommended Bypass Capacitors)

The circuit is designed to operate with two positive supply voltages, V^{++} and V^{+} which are nominally set to be 6.3V and 4.4V, respectively. Figure 4 gives the recommended power supply connection for the circuit.

The supply currents 1_A and 1_B drawn from the two supply voltages applied to the chip are specified to be within the following limits:

a. Current from 6.3V supply voltage, I_A:

$$2.5\ mA \leq I_A \leq 4.0\ mA$$

b. Current from 4.4V supply voltage I_B:

$$7\ mA \leq I_B \leq 9\ mA$$

The external components necessary for proper operation of the circuit are shown in Figure 5, in terms of the system block diagram. Note that all the blocks shown in Figure 5 are a part of the monolithic IC; and the numbered circuit terminals correspond to the IC package pins (see Figure 3).

Figure 6 shows a practical circuit connection for the XR-C277 in an actual PCM repeater application for 1.544 Mbps T-1 Repeater application. For simplification purposes, the lightning protection circuitry and the second repeater section are not shown in the figure.

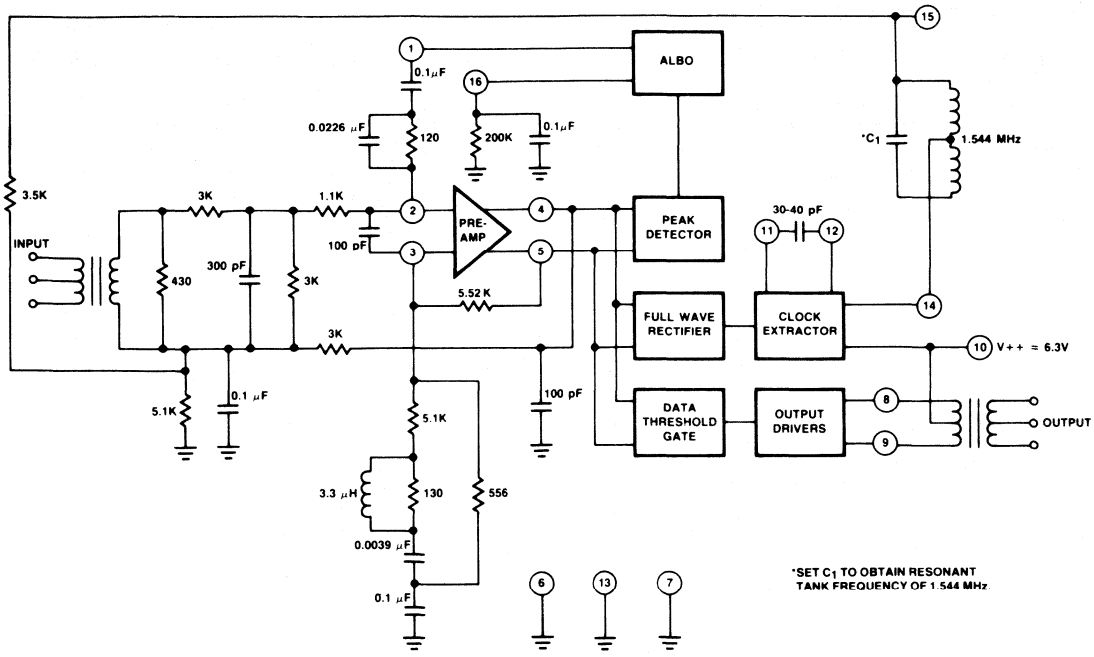


Figure 5. External Components Necessary for Circuit Operation in 1.544 MHz T-1 Repeater

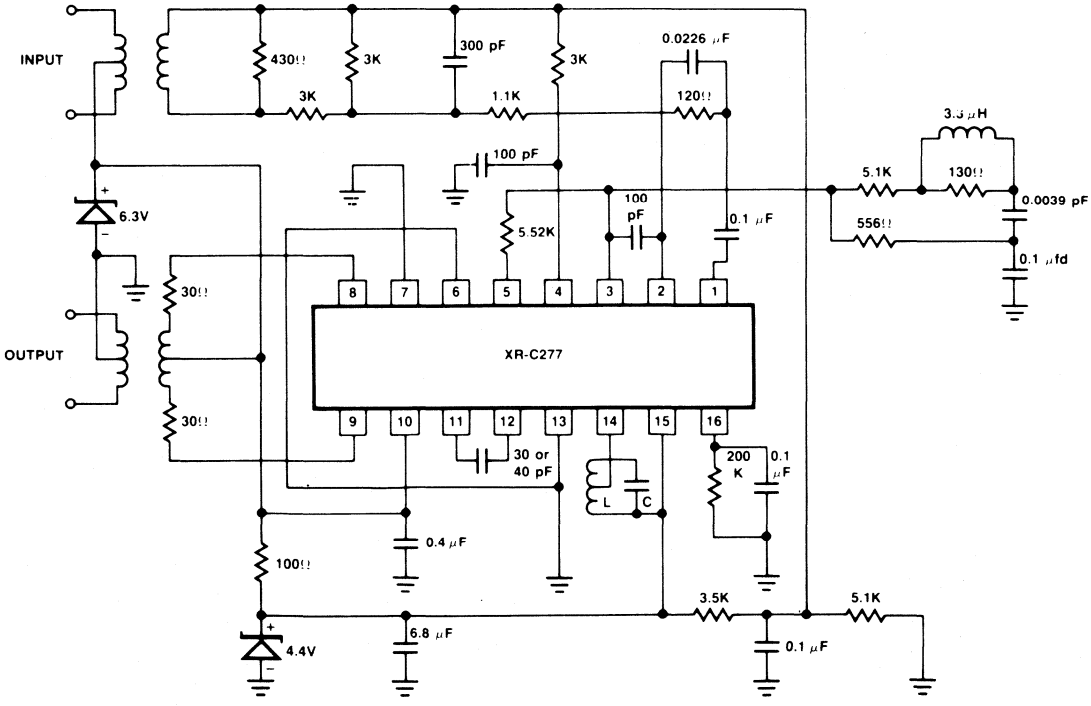


Figure 6. Typical Circuit Connection of XR-C277 in 1.544 MHz T-1 Repeater System. (Note: Set L and C to Form a High Q Tank Resonant at 1.544 MHz. It is Recommended that Q∂100, and C≈pF for most applications).

DESCRIPTION OF CIRCUIT OPERATION

Preamplifier Section (Fig. 7):

The circuit diagram of the preamplifier section is shown in Figure 7. This section is designed as a two-stage differential amplifier with a broadband differential voltage gain of 52 dB. The differential outputs of the preamplifier, Pins 4 and 5, are internally connected to the peak-detector, full-wave rectifier and the data threshold detector sections of the XR-C277.

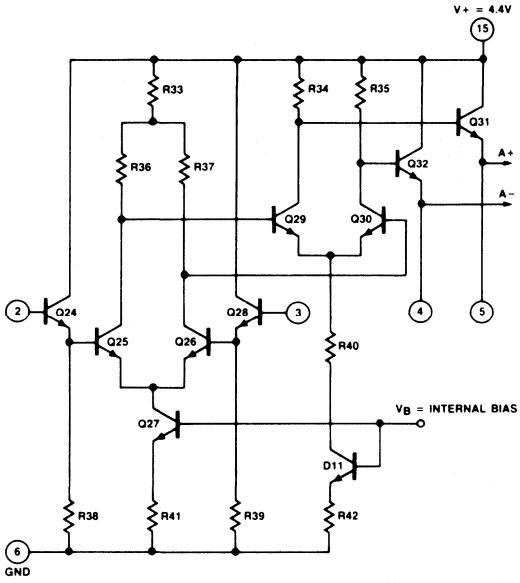


Figure 7. Circuit Diagram of Preamplifier Section

Automatic Line Build-Out (ALBO) Section (Fig. 8):

The ALBO function is achieved by controlling the dynamic impedance of ALBO diodes (Q_{21} and Q_{22}). The current which sets this dynamic impedance is supplied through Q_{21} and is controlled by the peak-detector output level applied to base of Q_{23}.

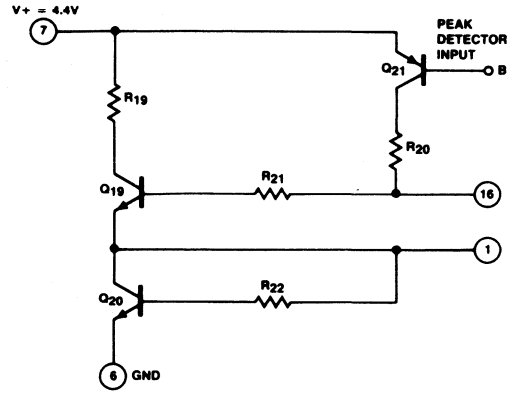


Figure 8. Automatic Line Build-Out (ALBO) Section

Data-Threshold Detector; Full-Wave Rectifier and Peak Detector Sections (Figure 9):

The level detector and peak rectifier sections of the XR-C277 are made up of two sets of gain stages which are driven differentially with the (A^+) and ($A-$) outputs of the preamplifier section. The outputs of the data threshold comparators, D^+ and D^- activate the data latches shown in Figure 11.

The peak-detector output, terminal B of Figure 9, is internally connected to the Automatic Line Build-Out (ALBO) section of the circuit and controls the dc bias current through the ALBO diodes Q_{21} through Q_{22}, as shown in Figure 8.

The full-wave rectifier output is internally connected to the clock-extractor section of the repeater and provides the excitation signal for the L-C tuned tank circuit (Pin 14) of the injection locked oscillator. The detection thresholds of the comparators are set by the resistor chains (R_{45}, R_{47}, R_{51}, R_{55}) and (R_{46}, R_{48}, R_{52}, R_{56}). The resistor ratios are chosen such that the data threshold is 50% of the ALBO threshold; and the clock extractor threshold is 73% of the ALBO threshold.

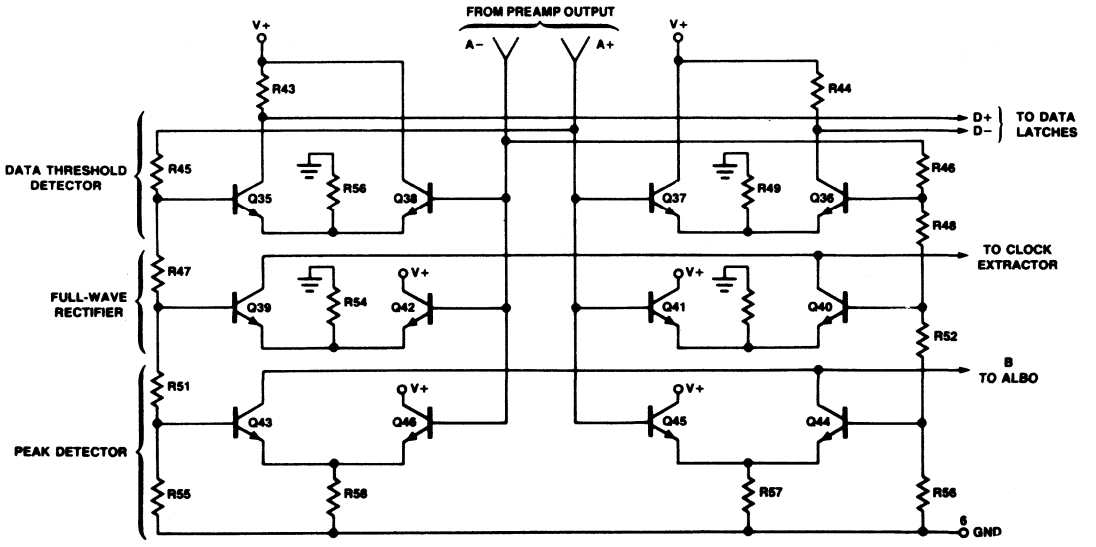


Figure 9. Data-Threshold Detector, Full-Wave Rectifier and The Peak Detector Sections of XR-C277

Clock Extractor Section (Figure 10):

The clock-extractor section of XR-C277 is designed as an injection locked oscillator as shown in the circuit schematic of Figure 10. The excitation is applied to the emitter of Q_{1B}, from the output of the full-wave rectifier. This signal in turn controls the current in the resonant L-C tank circuit connected to Pin 14. The sinusoidal waveform across the tank is then amplified and squared through two cascaded differential gain stages made up transistors Q_3 through Q_9. The output swing of the second gain stage is integrated by the phase-shift capacitor, C_1, externally connected to Pins 11 and 12. See timing diagrams of Figure 13. The nominal value of this capacitor is in the 30 to 40 pF range. The triangular waveform across Pins 11 and 12 is at quadrature phase with the sinusoidal voltage swing across the L-C tank circuit. This waveform is then used to generate the strobe signal, C_p, and the clock pulse C_ϕ, which are applied to the data latches of the logic section.

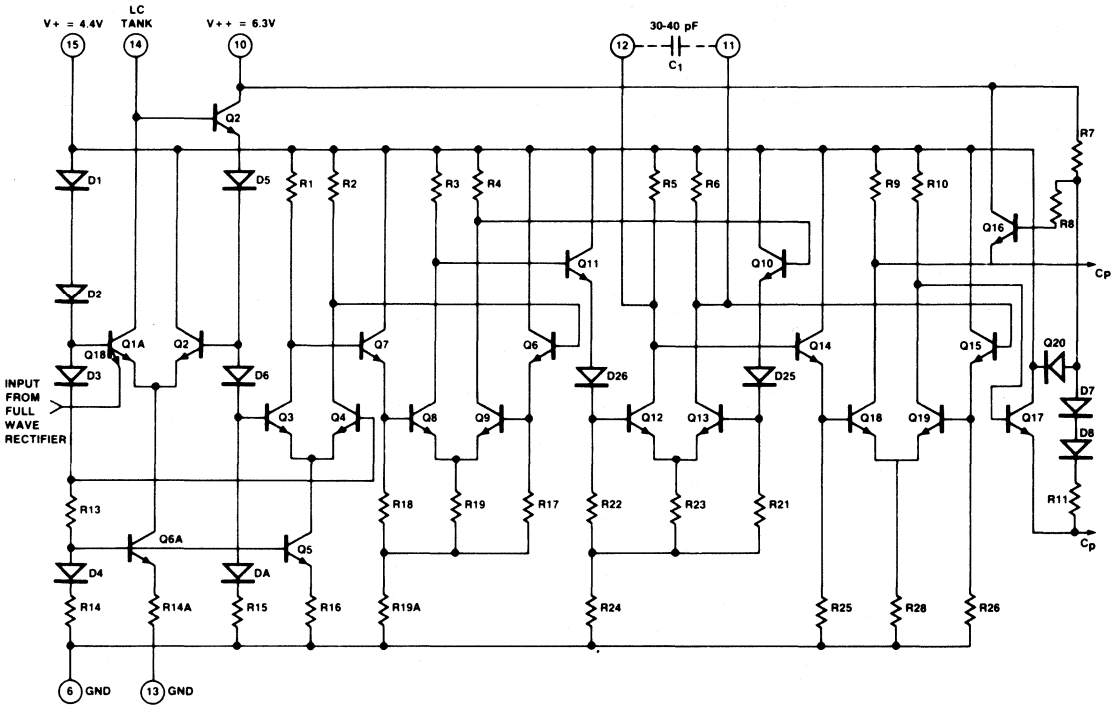


Figure 10. Circuit Diagram of Clock Extractor Section

Data-Latch and Output Driver Sections (Figures 11 and 12):

The data-latch section consists of two parallel flip-flops, driven by the D^+ and D^- inputs from the data-threshold detector. When the D^+ input is at a low state, the sampling or strobe pulse, C_p, is steered through Q_{47A} and sets Flip-Flop 1, on the leading edge of C_p. Conversely, when D^- input is at a low state, the sampling pulse is steered through Q_{47B} to set Flip-Flop 2. Each flip-flop section is then reset at the trailing edge of the clock pulse input, C_ϕ. The flip-flop outputs, (F_1, F_1) and F_2, F_2) are then used to drive the output drivers. This logic arrangement results in an output pulse width which is the same as the extracted clock pulse width (See timing diagram of Figure 13.)

The outputs of the two data latches drive the two output driver stages shown in Figure 12. The high-current outputs of the driver stage, Pins 8 and 9, are connected to the center-tapped output transformer as shown in Figure 5. The voltage swing across the output is one diode drop (V_{BE}) less than the supply voltage at Pin 10. The output stages are designed to work into a nominal load impedance of 100 ohms, and can handle peak load currents of 30 mA.

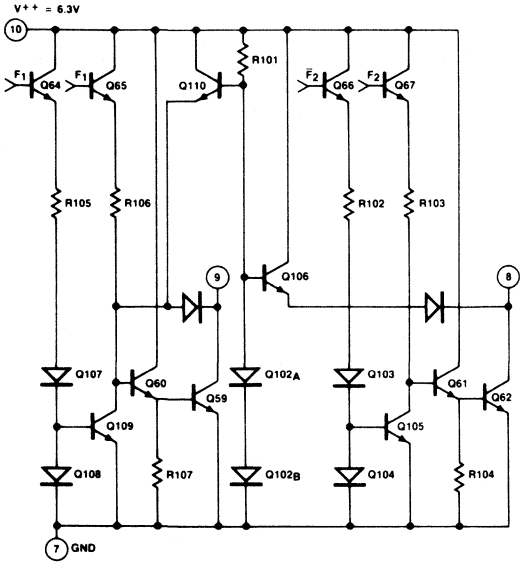


Figure 11. Data-Latch Section of XR-C277

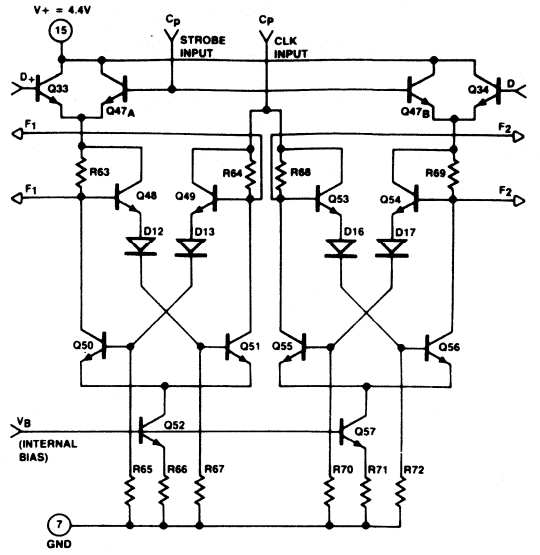


Figure 12. Output-Driver Section

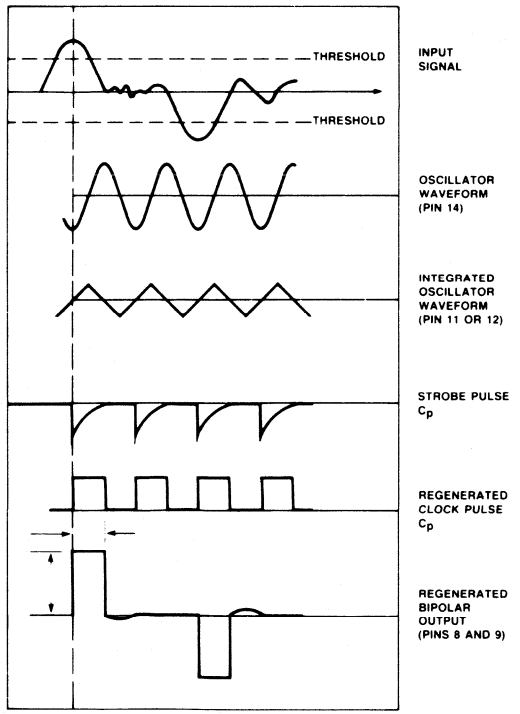


Figure 13. Typical Timing Waveforms for a 1—0—1 Input Data Pattern

XR-C262 High-Performance PCM Repeater IC

INTRODUCTION

The XR-C262 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (Mbps) data rates on T-1 type PCM lines. It is packaged in a hermetic 16-pin CERDIP package and is designed to operate over a temperature range of -40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Built-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

The XR-C262 operates with a single 6.8-volt power supply, and with a typical supply current of 13 mA. It provides bipolar output drive with high-current handling capability. The clock extractor section of XR-C262 uses the resonant-tank circuit principle, rather than the injection-locked oscillator technique used in earlier monolithic repeater designs. The bipolar output drivers are designed to go to "off" state automatically when there is no input signal present. Compared to conventional repeater designs using discrete components, the XR-C262 monolithic repeater IC offers greatly improved reliability and performance and provides significant savings in power consumption and system cost.

This application note outlines the basic design principles and the electrical characteristics of the XR-C262 monolithic repeater IC. In addition, circuit connections and applications information are provided for its utilization in T-1 type 1.544 Megabit PCM repeater systems.

FUNDAMENTALS OF PCM REPEATERS

The Pulse-Code Modulation (PCM) telephone systems are designed to provide a transmission capability for multiple-channel two-way voice frequency signals which are transmitted in a digital PCM format. In order to minimize error rates, and provide transmission over long distances, this digital signal must be regenerated at periodic intervals, using a regenerative repeater system. Figure 1 shows the block diagram of a bi-directional PCM repeater system consisting of two identical digital regenerator or repeater sections, one for each direction of transmission. These repeaters share a common power supply. The DC power is simplexed over the paired cable and is extracted at each repeater by means of a series zener diode regulator.

In the United States, the most widely used PCM telephone system is the T-1 type system which operates at a data rate of 1.544 Mbps, with bipolar data pulses. It

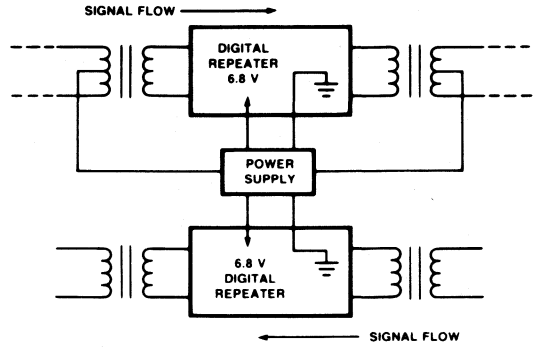


Figure 1. Block Diagram of a Bi-Directional Digital Repeater System.

can operate on either pulp- or polyethylene-insulated paired cable that is either pole-mounted or buried. Operation is possible with a variety of wire gauges, provided that the total cable loss at 772 kHz is less than 36 dB. Thus, the system can operate satisfactorily on nearly all paired cables which are used for voice frequency trunk circuits.

The T-1 type transmission system is designed to operate with both directions of transmission within the same cable sheath. The system performance is limited primarily by near-end cross-talk produced by other systems operating within the same cable sheath. In order to insure that the probability of a bit error is less than 10^{-6}, the maximum allowable repeater spacing, when used with 22-gauge pulp cable, is approximately 6000 feet.

The XR-C262 monolithic IC replaces about 90% of the electronic components and circuitry within the digital repeater sections of Figure 1. Thus, a bi-directional repeater system should require two XR-C262 ICs, one for each direction of information flow.

OPERATION OF THE XR-C262

The XR-C262 monolithic repeater is packaged in a 16-pin dual-in-line hermetic package, and is fabricated using bipolar process technology. The functions of the circuit terminals are defined in Figure 2, in terms of the monolithic IC package.

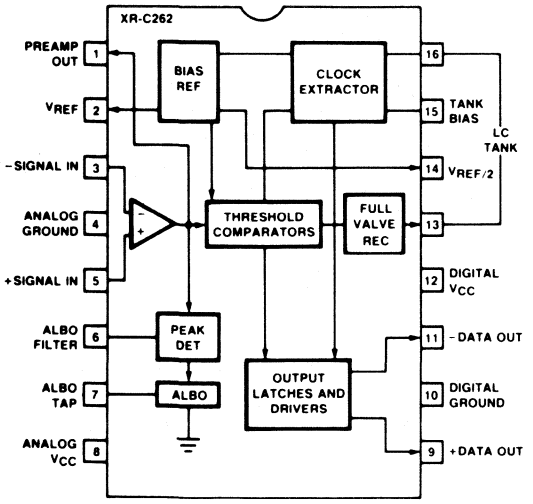


Figure 2. Package Diagram of XR-C262 Monolithic PCM Repeater.

A more detailed system block diagram for the monolithic repeater system is given in Figure 3. The system blocks shown within the dotted area are included on the monolithic chip. The numbers on the circuit terminals correspond to the pin numbers of the 16-pin IC package containing the repeater chip. In terms of the system block diagram of Figure 3, the overall repeater operation can be briefly explained as follows.

The bipolar PCM signals which are attenuated and distorted due to the preceding transmission medium are applied to the input of a preamplifier (Block 1) through an Automatic Line Build-Out (ALBO) circuit. The impedance, Z_1, corresponds to the passive section of the ALBO network. The preamplifier section, along with the passive equalizer networks Z_2 and Z_3 connected in feedback around it, provides gain to compensate for line losses and band-limiting to reject unwanted noise as well as gain and phase equalization to shape received pulses.

The ALBO circuitry provides attenuation and shaping to automatically adjust for varying cable characteristics. The output of the preamplifier is controlled to swing between two established peak levels. This is accomplished by feedback circuitry, and is similar in concept to automatic gain control. When the preamplifier output passes through the peak thresholds it is detected by the peak detector (Block 2) and produces a signal which is used to control a feedback loop establishing

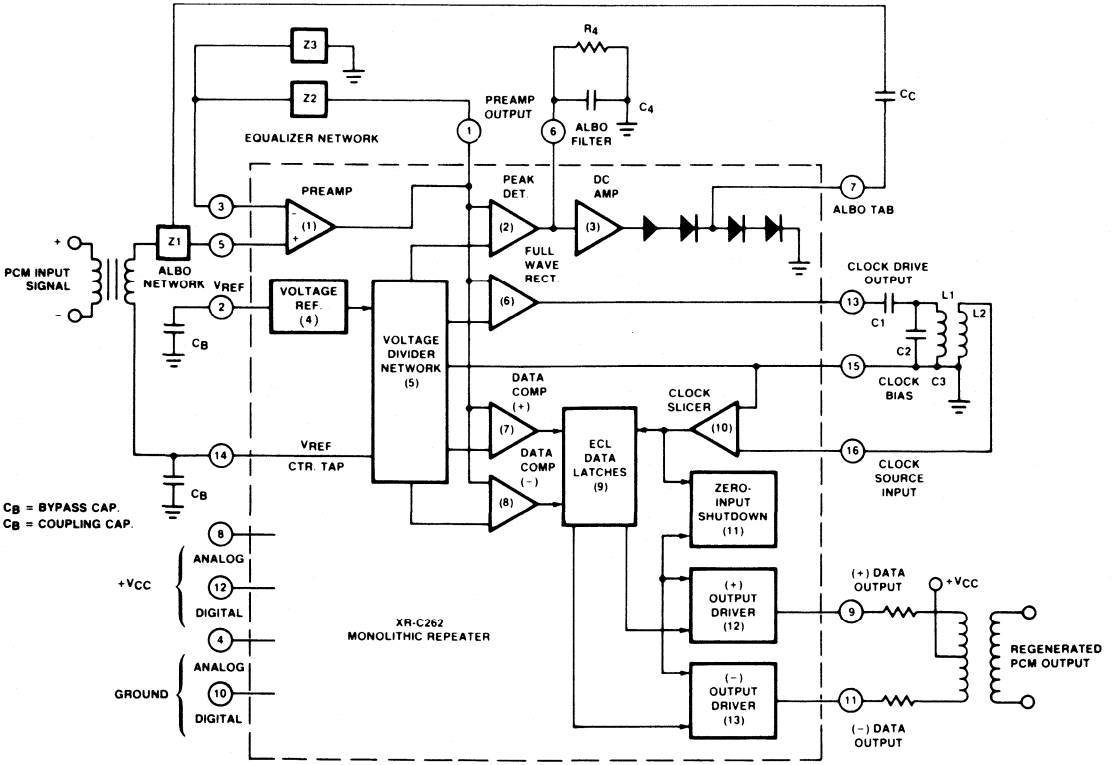


Figure 3. Detailed Block Diagram of the XR-C262 Monolithic Repeater System.

the attenuation and shaping of the ALBO network. The actual circuit design associated with this function is described in more detail in the discussion of peak detection and ALBO circuitry.

The output of the preamplifier drives a set of data comparators which are internally biased from a voltage reference (Block 4) and the precision voltage divider network (Block 5). Thus, the preamplifier output is "sliced" at various voltage levels to eliminate the effects of the baseline noise. This output is full-wave rectified and amplified through Block 6 of Figure 3. The resulting signal has a strong Fourier component at the clock frequency and is used to drive a high Q ($\approx$100) resonant circuit tuned to that frequency. The output of the resonant circuit is transformer-coupled to a zero-crossing detector and clock limiter (Block 10). The resultant output is the desired recovered timing. This resonant circuit is driven by a low impedance amplifier, and the resulting clock edges are in phase with the peak of the received pulses.

The regeneration of the data is achieved through the two data comparators (Blocks 7 and 8) and the ECL latches (BLock 9) which function as tracking flip-flops. The positive and negative data paths are separate; and, with the exception of the data limiter and slicer levels, identical in design. The preamplifier output is sliced at about 45 percent of the peak voltage and its amplitude is limited to provide digital data pulses. The data is applied to one of the inputs to the tracking flip-flop, whose state is latched and unlatched by the clock. During acquisition, the flip-flop acquires data; during hold, further data transitions are ignored and the state of the flip-flop output determines whether an output pulse is transmitted. The implication of using the clock to perform data sampling is that path delays of the data and clock must be controlled to be equal. The monolithic integrated circuit technology affords this control. The advantage of this technique is that the need for clock shifting or strobe pulse generating circuitry for accurate sampling alignment is eliminated. Actual circuit implementation resulted in a 40-nsec misalignment of clock and data. This 40-nsec error in sampling time amounts to less than 0.4 dB degradation in SNR performance. Figure 4 shows the idealized timing and signal waveforms within the circuit.

The output drivers use latched data and clock to produce an output pulse-width which is accurately controlled by the duration of the clock. Non-saturating output drivers (Blocks 12 and 13) insure that output pulse rise and fall times are less than 100 nsec. The zero input shut-down circuitry (Block 11) guarantees that in the event incoming data disappears, the output switches will not latch in the "on" state. When no input signal is present, the absence of clock is sensed and the output drivers are held in the "off" state.

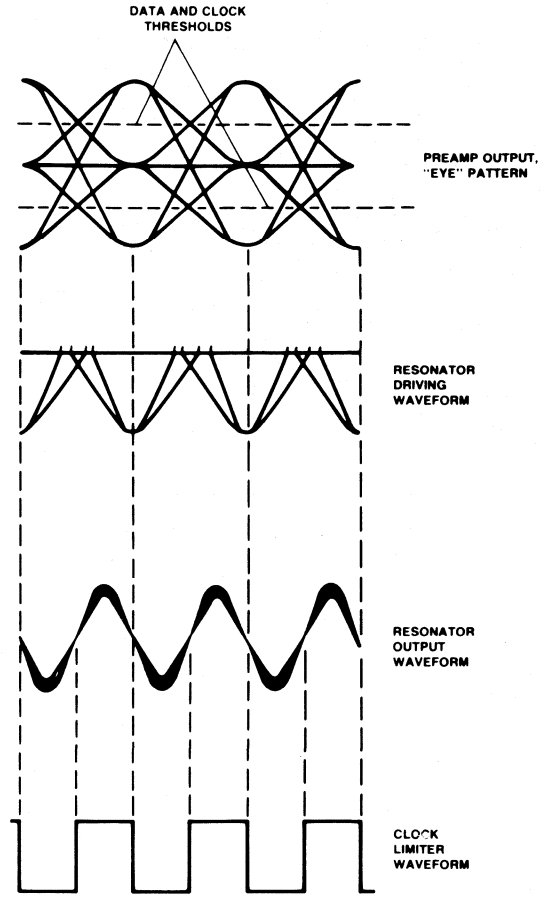


Figure 4. Timing Diagrams of Voltage Waveforms within the Clock Regeneration Section.

Figure 5 shows a practical circuit connection for the XR-C262 in an actual PCM repeater application for 1.544 Mbps T-1 repeater system. For simplification purposes, the lightening protection circuitry and the second repeater section for the reverse channel are not shown in the figure.

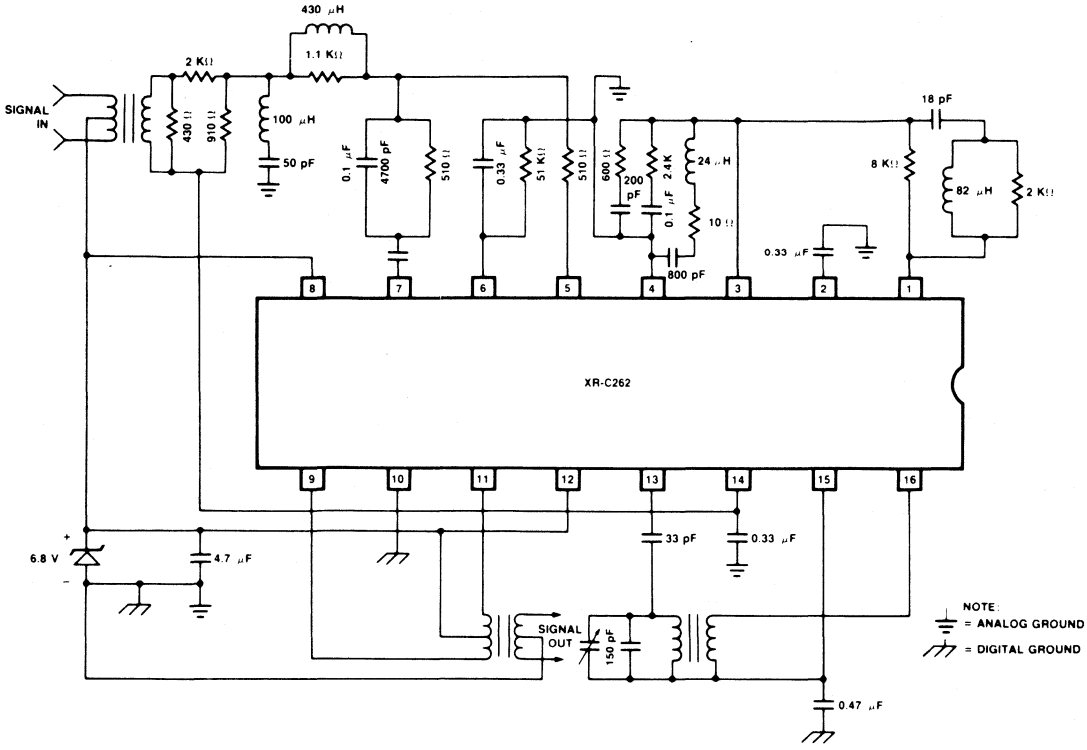


Figure 5. A Recommended Circuit Connection Diagram for T-1 Type Repeater Application.

DESCRIPTION OF CIRCUIT OPERATION

Preamplifier Section (Figure 6):

The circuit diagram of the preamplifier section is shown in Figure 6. This section is designed as a single-stage high-gain amplifier with differential inputs and a single-ended output. The amplifuer output is internally connected to the peak-detector, full-wave rectifier and the data-comparator sections. The circuit exhibits a high differential input resistance ($\approx 10^6$ ohms) and a low output impedance ($\approx$80 ohms). It has a nominal voltage gain of 69 dB at DC and $\geq$50 dB at 1 MHz. The frequency response of the circuit exhibits a single-pole roll-off characteristic.

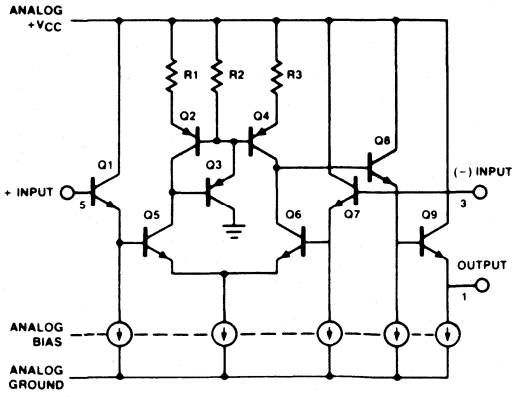


Figure 6. Circuit Diagram of Preamplifier Section.

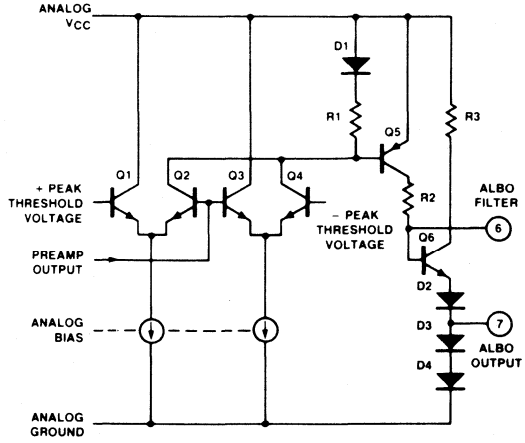


Figure 7. Circuit Diagram of the Peak-Detector and the ALBO Sections.

Peak-Detector and ALBO Section (Figure 7):

The peak-detector circuit is designed to detect the peaks of the preamplifier output, provided that these peaks exceed the internal detection threshold levels. This peak information is then low-pass filtered and is used to control the current in a diode string which acts as a variable-loss or "variolosser' element in a feedback path. In the circuit, the comparators conduct whenever the preamp output exceeds the (+) threshold in a positive direction or the (-) threshold in a negative direction. Transistor Q_5 then injects a pulse of current into the ALBO filter. In the steady state, DC level across the ALBO filter controls the current through the diode string; and the dynamic resistance of the diodes acts as the variolosser element. The usable linear resistance range in this application is almost three orders of magnitude ranging from 11 Ω to ≈ 6 KΩ.

Data Latches (Figure 8):

The data latches are required to be impervious to data transitions in the latch mode, and to be "transparent," (i.e., tracking the input data) during the tracking mode. Figure 8 shows the basic circuit configuration used in the XR-C262, which meets the above-mentioned performance requirements. During the time when the clock pulse is high, the acquisition transistors Q_1 and Q_2 are differentially switched with data transitions, and the data is coupled to the respective bases of Q_3 and Q_4. When the clock pulse goes low at the sample time (see Figure 4), the information is regeneratively latched into Q_3 and Q_4. While the clock is low, further data transitions have no effect upon the state of the flip-flop. A more detailed description of the timing waveforms is given in Figure 13.

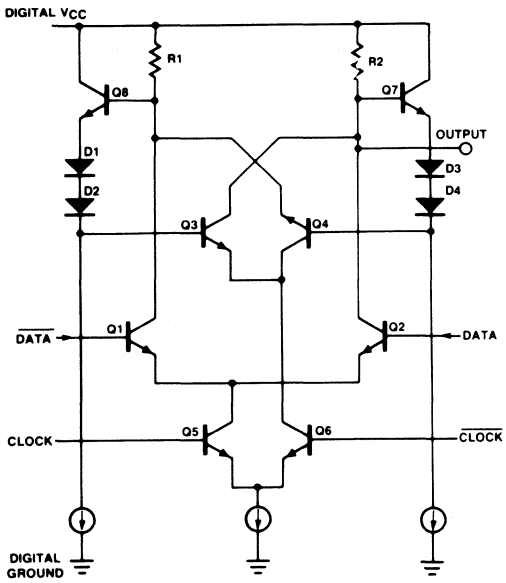


Figure 8. Circuit Configuration for Tracking Data Latches.

Threshold Circuitry (Figure 9):

Threshold circuitry is a low impedance voltage-divider circuit corresponding to Block 5 of Figure 3, and it establishes the fixed levels required for data, clock and peak detection. It is important that the thresholds are insensitive to temperature variations, and that they are of sufficiently low impedance to guarantee that there is no threshold variation due to changing signal conditions. The reference voltages of the peak-detector, data, and clock thresholds are set by a resistor chain which divides down the voltage of the on-chip zener diode. The ratios of data threshold to peak-detector threshold and that of clock threshold to peak-detector threshold are both set at 45 percent. In the actual circuit implementation, as shown in Figure 10, a compound connection of PNP's and NPN's are used to reduce the output impedance of the reference levels. The currents through the NPN and PNP transistor strings are set so as to insure that the base emitter voltage drops of the NPN's and PNP's are nominally the same. The output impedance of the resulting reference voltage taps are about 300 ohms. The center tap of the buffered divider is brought to a separate package terminal (Pin 14 of Figure 3) for biasing the preamplifier input.

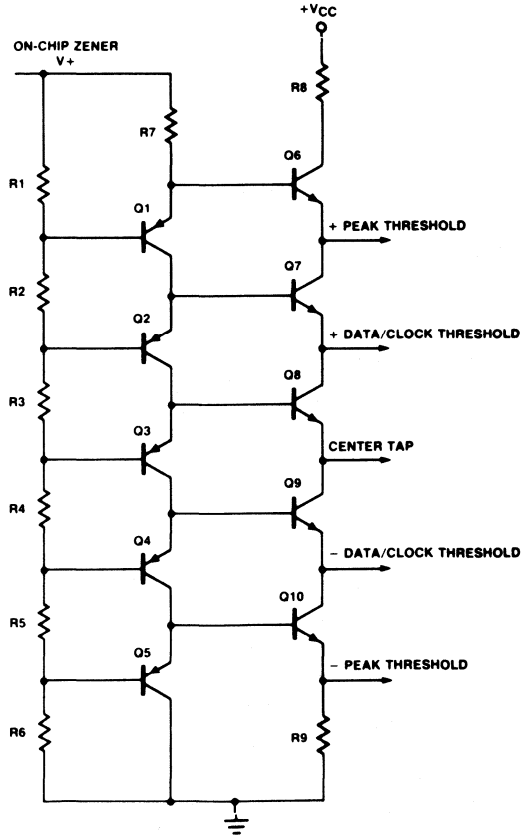


Figure 9. Internal Voltage-Divider Network for Comparator Threshold Setting.

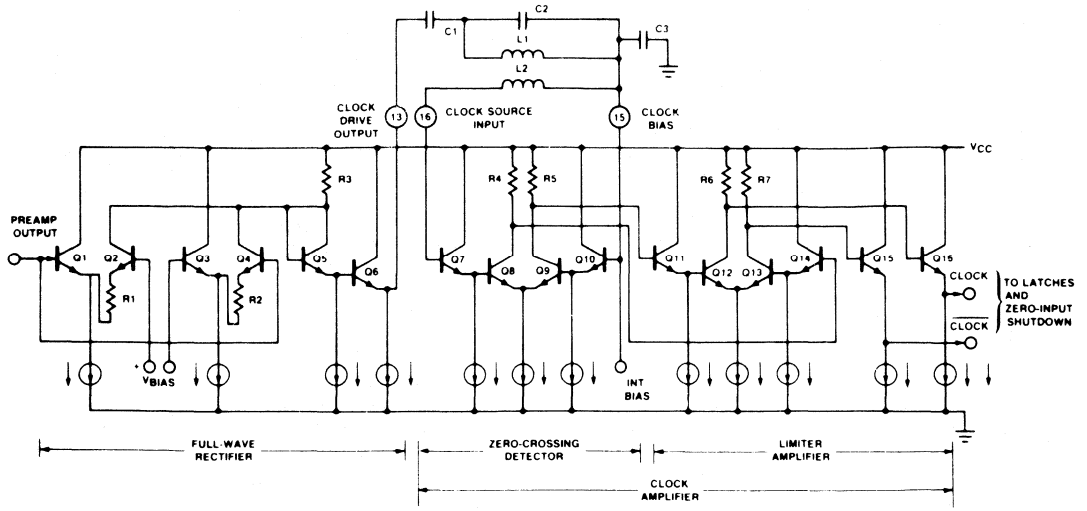


Figure 10. Circuit Diagram of the Clock Recovery Section.

Clock Recovery Section (Figure 10):

Clock recovery circuity consists of a full-wave rectifier, an external L-C resonant circuit, a zero crossing detector, and limiting amplifier, as shown in Figure 10. The full-wave rectifier circuit, comprising of cross-coupled transistor pairs Q_1 through Q_4 has a net voltage gain of 2, which is obtained by setting $R_1 = R_2 = (1/2)R_3$. The rectified output is then buffered by the Darlington emitter-follower stage made up of Q_5 and Q_6, and applied to the external L-C resonant circuit. Q_6 is operated at a high bias current level to provide an output impedance of less than 15Ω. This low impedance is required to insure that the L-C tank-drive circuitry looks like a voltage source.

The inductor of the resonant tank circuit is also a transformer which couples the sine wave signal to the zero crossing detector and limiting amplifier. The zero crossing detector is a differential amplifier with a nominal voltage gain of 20 and input impedance of 4 MΩ. The sine wave from the resonant circuit is sliced to produce a square wave with sharp transitions at the zero crossings. This eliminates timing variations that may be caused by amplitude changes of the sine wave signal. The output of the zero crossing detector is further enhanced by the limiter which is another differential pair with a nominal voltage gain of 30. The output of this amplifier is a 1.5 V peak-to-peak square wave clock which drives the data latches and the output drivers.

Zero-Input Protection Circuit (Figure 11):

The zero input protection circuitry accomplishes the dual task of preventing the output switches from latching in an "on" state, as well as reducing the likelihood of output pulses with no input signal. The data, clock, and regenerator circuitry are all balanced DC coupled circuits. Controlling the steady state, no-signal condition of these circuits without building an unacceptable offset into the path is not practical. Instead, a retrigerable one-shot that uses the saturation characteristics of PNP transistors is used to control the level of the clock into the output switches. This technique uses the bandpass characteristics of the timing recovery resonant circuit to reject out of band signals, thus minimizing the chance of producing output pulses with no input signal and the presence of noise. Figure 11 shows the basic implementation of the zero-input protection circuit. $Q_1$and Q_2 function as a simple retriggerable one-shot. The transistor Q_2 is a lateral PNP device with a limited frequency capability and long storage-time delay. The existence of the 1.544 MHz clock causes Q_2 to saturate and remain in saturation while clock pulses are present. The comparatively long time constant associated with Q_2 coming out of saturation ($\approx$5 μsec) insures that, when data is present, the zero input protection has no effect upon operation. When data disappears there is no clock to retrigger the one-shot, thus Q_2 comes out of saturation, causing Q_3 to saturate which pulls the respective clock lines high, and disables both output drivers in their "off" state.

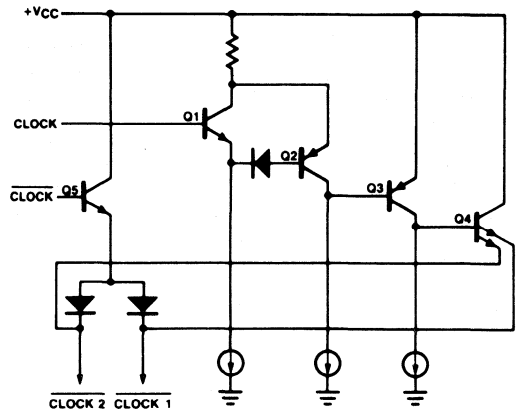


Figure 11. Zero-Input Shutdown Circuit for Output Protection.

Output Drive Circuitry (Figure 12):

The output drive circuitry is made up of two identical channels as indicated in the block diagram of Figure 2. The circuit configuration for each of these driver sections is shown in Figure 12. The output would follow the data input from the latches only when the clock input is at a "high" state, i.e., with Q_2 off and Q_3 on. In this manner, the output pulse-width is controlled by the clock. To provide the fast turn-on and turn-off of the output drivers, all the transistors operate in a nonsaturating state. Q_4 forms an active clamp to reduce voltage swing at the base of Q_6, and the clamp diode D_5 prevents the saturation of the output driver Q_7. Because of the biasing scheme mentioned above, the amplitude of the clock and the latched data are insensitive to supply voltage and temperature changes. Thus, the variations of the regenerated pulse-width over temperature and supply are minimized.

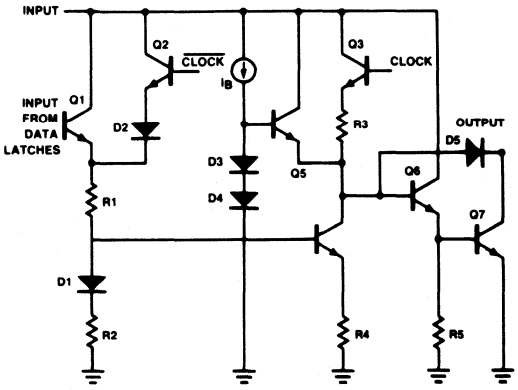


Figure 12. Circuit Configuration for the Output Drivers.

Timing Waveforms (Figure 13):

Figure 13 illustrates the relative time and phase relationships between the signal levels at various points within the circuit. For the purpose of illustration an input data pattern comprised of a string of "ONE"s is assumed, which looks like a nearly sinusoidal input after having traveled through a dispersive transmission medium such as a long cable. Waveform (1) is the output of the preamplifier; Waveforms (2) through (5) are the outputs of the two data comparators driven by the preamplifier output (see Figure 3). Waveform (6) is the low-level clock signal obtained from the resonant tank circuit, at Pin 16 which is then amplified and sliced by the clock-recovery circuit (see Figure 11) and appears as the internal clock signals shown as Waveforms (7) and (8). Waveform (9) shows the output of one of the data latches (Figure 8) as a function of the clock and data inputs. The output of the latch tracks +DATA when the clock is low, and stays latched in that condition when the block goes high. The output drive at Pin 9, which is shown as Waveform (10) will then go low only when the Waveforms (8) and (9) are low. Waveform (11) shows the second output available at Pin 11. These two outputs are then differentially combined by the output transformer (see Figure 3) to provide the regenerated bipolar output pulses shown in Waveform (12) of Figure 13.

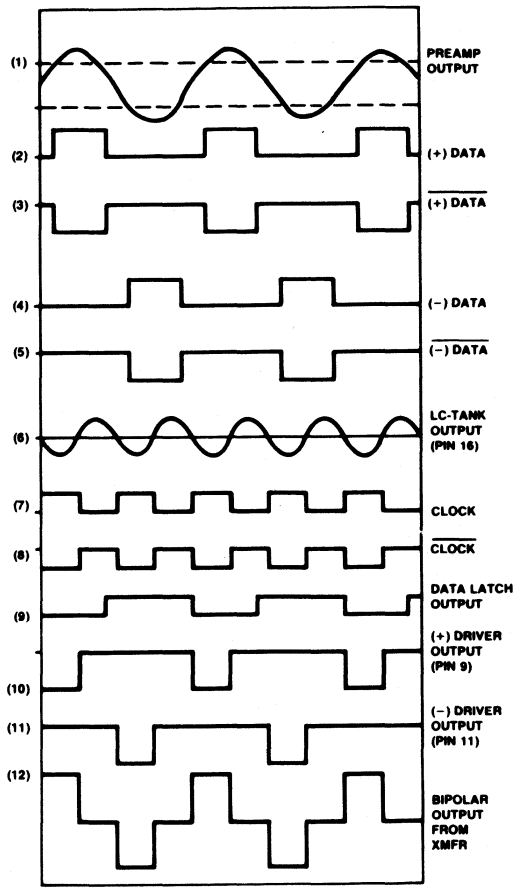


Figure 13. Timing Diagram of Circuit Waveforms for a 1-1-1 Input Data Pattern.

AN-10

ELECTRICAL CHARACTERISTICS $+V_{CC}$ = 6.8 Volts, T_A = −40°C to +85°C.

CHARACTERISTICS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
Supply Current					
Digital Current	7	10	13	mA	Measured at Pin 12
Analog Current	2	3.5	5	mA	Measured at Pin 8
Total Current		13	17	mA	
Preamplifier					
Input Offset Voltage	−15		+15	mV	Measured between Pins 3 and 5
DC Gain	60	69	74	dB	
Output High Level	4.3			V	Measured at Pin 1
Output Low Level			0.5	V	Measured at Pin 1
Clock Recovery Section					
Clock Drive Swing (High)	5.1			V	Measured at Pin 13
Clock Drive Swing (Low)			3.8	V	Measured at Pin 13
Clock Bias	3.8	4	4.2	V	Measured at Pin 15
Clock Source Input Current		0.5	4	μA	Measured at Pin 16
Comparator Thresholds					Measured at Pin 1 relative to Pin 14
ALBO Threshold	0.75	0.9	1.1	V	
Clock Threshold	0.323	0.4	0.517	V	
Internal Reference Voltages					
Reference Voltage	5.2	5.45	5.55	V	Measured at Pin 2
Divider Center Tap	2.6	2.78	2.85	V	Measured at Pin 14
ALBO Section					
Off Voltage		10	75	mV	Measured at Pin 7
On Voltage	1.2		1.7	V	Measured at Pin 7
On Impedance			15	Ω	Measured at Pin 7
Filter Drive Current	0.7	1	1.5	mA	Drive current available at Pin 6
Output Driver Section					Measured at Pins 9 and 11
Output High Swing	5.9	6.8		V	R_L = 400 Ω
Output Low Swing	0.6	0.7	0.9	V	I_L = 15 mA
Leakage Current			100	μA	Measured with output in off state
Output Pulse Width	294	324	354	nsec	
Output Rise Time			100	nsec	
Output Fall Time			100	nsec	
Pulse Width Unbalance			15	nsec	

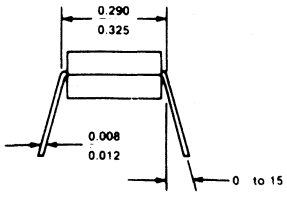
ABSOLUTE MAXIMUM RATINGS

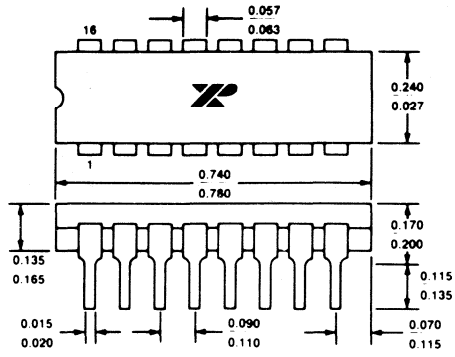
Supply Voltage	+10 V
Power Dissipation	750 mW
Derate above +25°C	6 mW/°C
Storage Temperature Range	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-C262	CERDIP	−40°C to +85°C

PACKAGE INFORMATION





PCM Short Haul Line Interface

INTRODUCTION

XR-T5681 is a PCM Transceiver chip consisting of both transmit and receive circuit in a CERDIP 18 pin package. The transceiver is designed primarily for short line (<10 dB) PCM transmission applications such as in Digital Private Branch Exchange (PBX) environment, Digital Multiplexed Interface (DMI), and Standard PCM data interface circuit. The maximum frequency of operation is 3 Mb/s, so it cover T1, T148, T1C and Europe's CEPT 2048K b/s data rates. The device is designed to operate over the temperature range of 0°C to +70°C.

PRINCIPLES OF OPERATION

Figure 1 contains a functional block diagram of the XR-T5681. The circuit consists of two separate sections: one is the line receiver and the other is the line transmitter. The receiver accepts incoming bipolar signal and converts it intc TTL D+ and D– data streams. It also produces a clock output from the input data. In the transmit direction, full width, TTL compatible D+ and D– signals at the input, and a 50% duty cycle clock are combined to form the bipolar line signal at the output of a transformer for transmission.

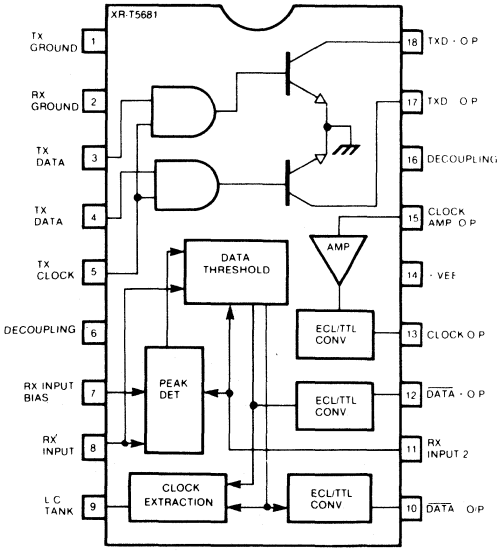


Figure 1. Block Diagram

RECEIVER CIRCUIT DESCRIPTION

The receiver is designed to handle a maximum of 10 dB line loss. This means the incoming signal will not suffer from severe attenuation and distortion caused by the cable, and, therefore, it can be reliably retrieved without preamplication circuit and equalizing network placed at the input of the receiver.

The receiver in this design consists of a peak detector which converts the incoming signal amplitude into a variable threshold. The variable threshold is arranged to slice the input signal at 50% level in the data comparator (See Figure 2) for D+ and D– data extraction. This scheme guarantees a maximum tolerance in interference immunity and ensures a nominal output pulse width change at different input signal level. However, as the data outputs are not regenerated pulses, their width will somewhat depend on the input pattern and cable loss. D+ and D– are active low data and they both go through similar level shifting circuit to be converted into TTL compatible signals.

CLOCK EXTRACTION

Since timing information is extracted from the data and the input spectrum does not carry any frequency component around the transmission rate, input waveform is full wave rectified to obtain all the transition pulses before applied to an external LC resonant circuit. If the input signal is a random data, the tank output looks like a amplitude modulated sine wave. Figure 2 depicts the clock extraction process with a known input patter. The clock output shown in Figure 2 has the rising edge coincided with the center of the D+ and D– data. This timing relation is essential for the external digital circuit to convert the half-width data into a full width signal when using a positive edge triggered D/FF as that shown in Figure 3. To achieve the 90° phase difference between the data and the clock, the tank output is coupled through a small value capacitor to the input of a common base amplifier (see Figure 4), followed by a zero crossing detector to obtain a square wave with sharp transitions. The emitter of Q10 is a low impedance point, hence, the coupling capacitor C_C forms part of the tank circuit.

ELECTRICAL CHARACTERISTICS

Test Conditions: $+V_{CC}$ = 5.0 V, operating temperature 0°C to +70°C.

PARAMETERS	PIN NO.	MIN	TYP	MAX	UNITS	CONDITIONS
DC Supply	14	4.75	5.0	5.25	V	
Supply Current	9,14		35.0	45.0	mA	Transmitter Drivers Open
Tank Drive Current	9	1.7	2.0	2.3	mA	Pin 8 & 11 = 0 V, Supply 3.0 V to Pin 6
Clock Output Low	13		0.3	0.8	V	I_{OL} =1.0 mA
Clock Output High	13	3.0	4.3		V	I_{OH}= −400μA
D+, D− Output Low	12,10		0.4	0.8	V	I_{OL} = 1.0 mA
D+, D− Output High	12,10	3.0	4.5		V	I_{OH} = 400μA
Driver Low Voltage	17,18	0.6		0.05	V	I_{OL} = 40 mA
Driver Sinking Current	17,18			40	mA	V_{OL} = 0.95 V
Driver Output Rise Time	17,18		20	30	nS	With 150Ω Pull-Up to +5.0 V, CL = 15 pF
Driver Output Fall Time	17,18		20		nS	With 150Ω Pull-up to +5.0 V, CL = 15 pF
Pulse Width at 2048K	17,18	219	244	269	nS	With 150Ω Pull-Up to +5.0 V
Pulse Width Imbalance at 2048K	17,18		5	10	nS	At 50%
Clock Duty Cycle at 2048K	13	40	50	60	nS	%
Clock Rise Time	13		25		nS	10-90%

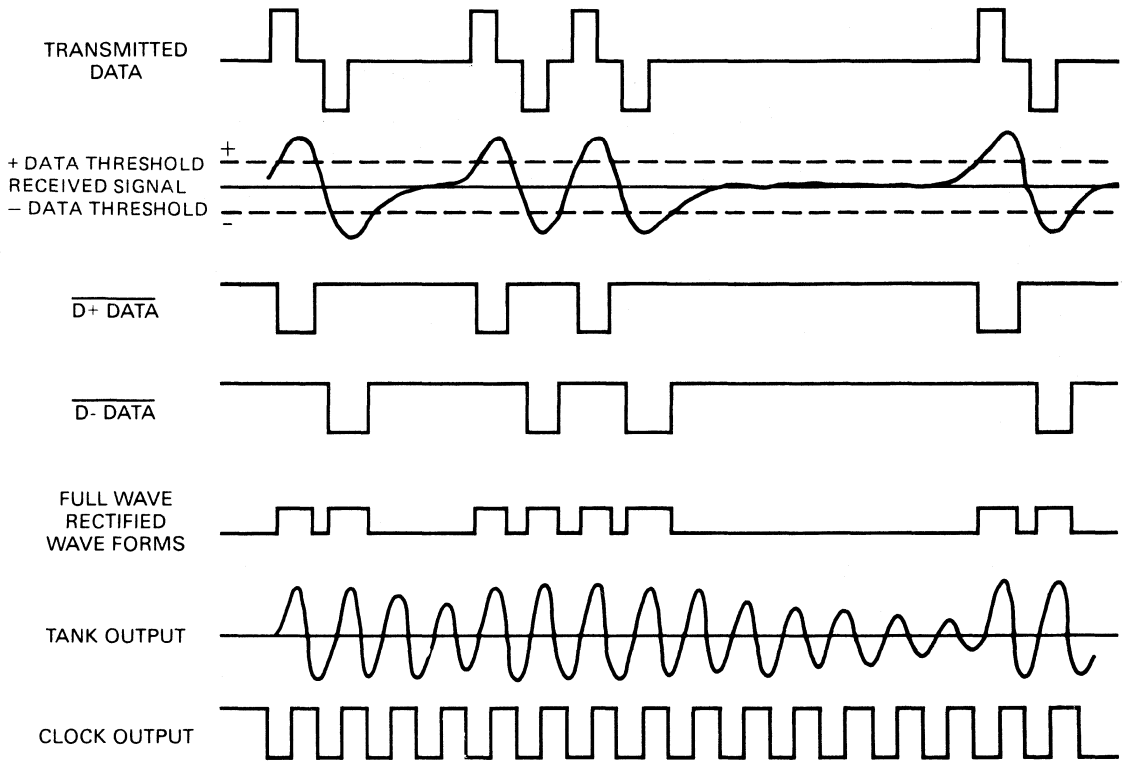


Figure 2. XR-T5681 Clock Extraction Timing Waveforms

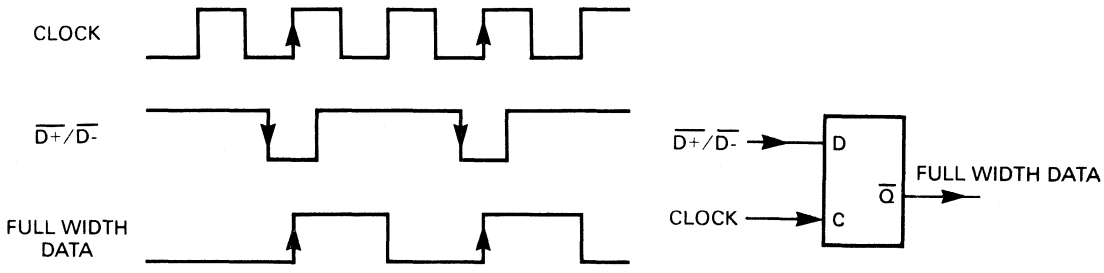


Figure 3. To Convert Half-Width Data into a Full-Width Data, A Positive Edge Triggered D/FF is Commonly used.

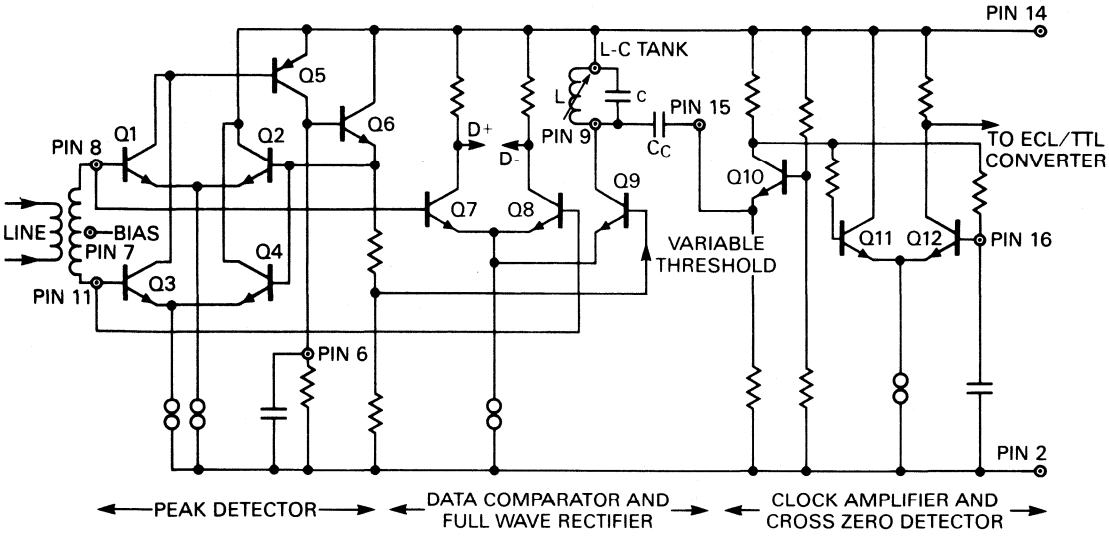


Figure 4. Simplified Schematic of XR-T5681 Receiver

TRANSMITTER

The transmitter consists of two identical TTL input open collector NAND gates. The output driver has a nonsaturating stage and can handle a maximum current of 40 mA. If the inputs are half width signals, Pin 5 should be returned to $+V_{CC}$ via a 1KΩ resistor. If the input data are full width signals, a synchronized 50% duty cycle TTL clock is needed at Pin 5 to obtain a bipolar signal at the output of a center tapped transformer (See Figure 5). The output pulse conforms to CCITT G.703 recommendation. A circuit connection diagram for 1.5Mb/s line interface is shown in Figure 6.

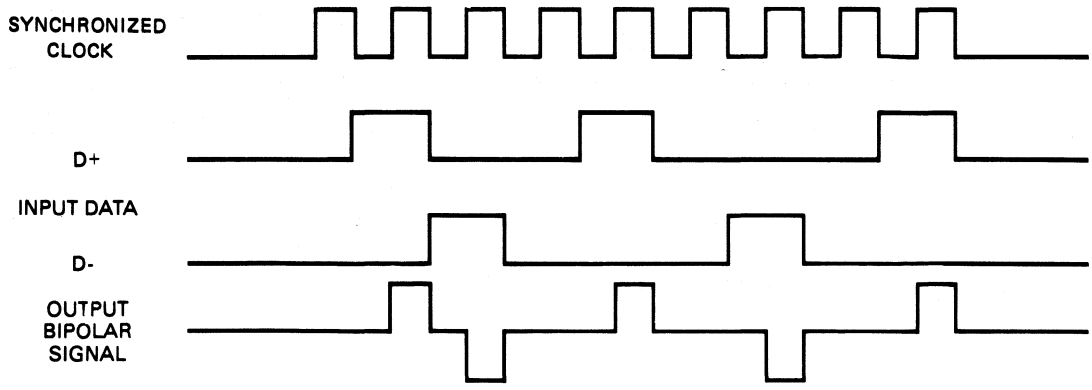
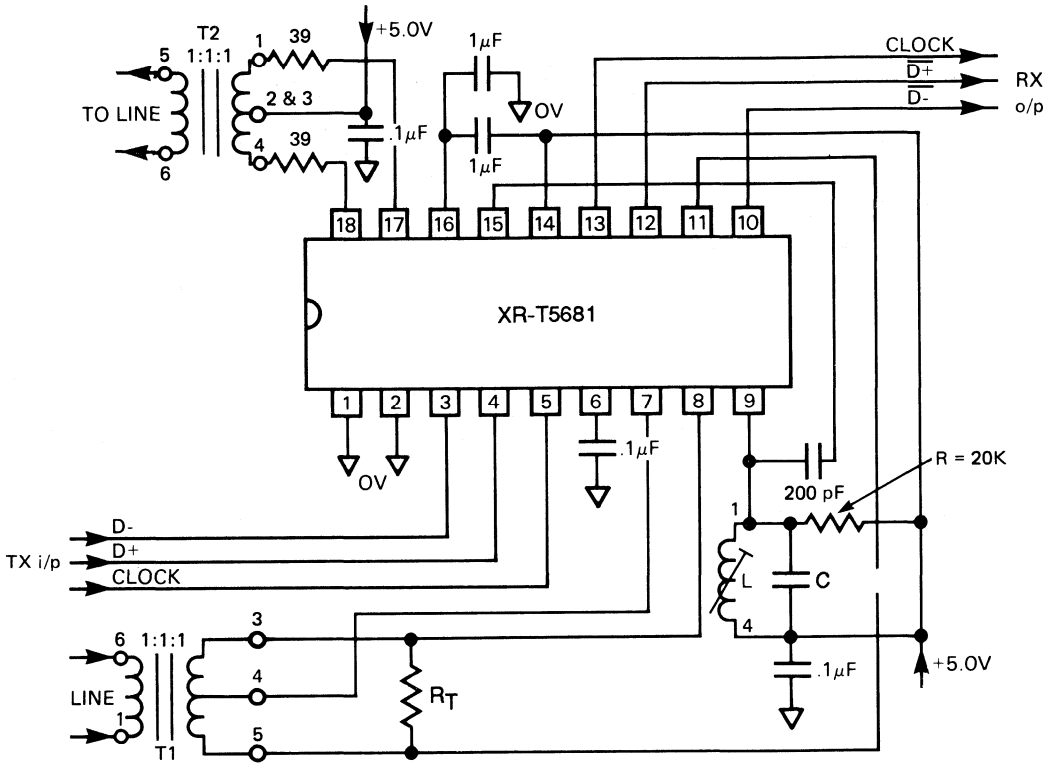


Figure 5. XR-T5681 Transmitter Section Timing Diagram



★ Q OF TANK CIRCUIT = 80-100

L = Tank coil AIE part no. 415–0804
T1 = AIE input transformer part no. 315–0765
T2 = AIE part no. 318–0696
Max. input voltage to T1 primary = 6 Vp-p at 5-0 V supply

Device	1.544 MBPS	2.048 MBPS
L	~60μH	60μH
C	600 pF	200 pF
R_T	470	390

Figure 6. Circuit Connection Diagram for XR-T5681

Long Haul PCM Line Receiver & Clock Recovery Circuit using the XR-T5650

INTRODUCTION

The XR-T5650 is a monolithic bipolar IC designed for PCM line receiver applications operating at T1, T148, T1C, and 2 Mbits/s data rates. It provides all the active circuitry to perform automatic line build out (ALBO), positive and negative data extraction, and clock recovery. For applications requiring crystal clock extraction, the XR-T5750 is recommended. Some of the features included in this IC are a double matched ALBO, a less than 10 ns sampling pulse over the operating range, a 5.1 volt power supply for easy interfacing with CMOS and TTL circuitry. This device is designed as a general purpose line receiver for bipolar line codes such as HDB3, B8ZS, or AMI formats, and is packaged in a hermetic 18 pin CERDIP.

PRINCIPLES OF OPERATION

Figure 1 illustrates the functional block diagram for XR-T5650. For ease of analysis, the internal structure of the receiver is divided into the following circuit blocks:

a. Preamplifier
b. Data threshold detector
c. Clock threshold detector
d. ALBO threshold detector
e. Clock amplifier and bias network
f. Limiter and sampling pulse generator
g. Retiming logic and drivers for clock and data outputs

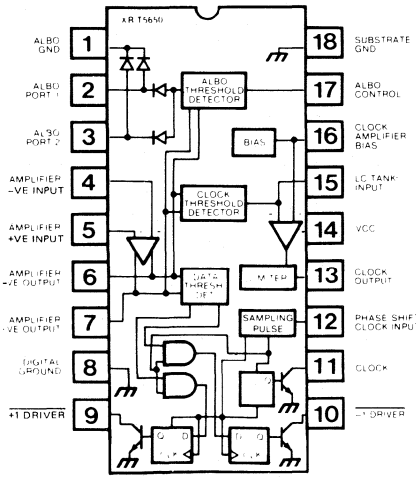


Figure 1. Functional Block Diagram

The basic function of the receiver is to reshape, regenerate, and retime the incoming pulse code modulated signal. The system operates on either pulp or polyethylene insulated paired cable that is either pole mounted or buried. Operation is compatible with a variety of wire gauges, provided that the cable loss at 772 KHz is less than 36 dB. Thus, the system can operate satisfactorily on nearly all paired cables which are used for voice frequency circuits. It is the function of the amplifier to provide the necessary gain and phase on a pre-equalized signal in order to insure proper recovery of clock and data. The circuit diagram of the preamplifier, as shown in Figure 2, is designed as a two stage differential broadband amplifier with a differential voltage gain of 50 dB. The differential outputs of the preamplifier, pin 6 and 7, are internally connected to the peak detector for the ALBO loop and also to the data and clock threshold detectors.

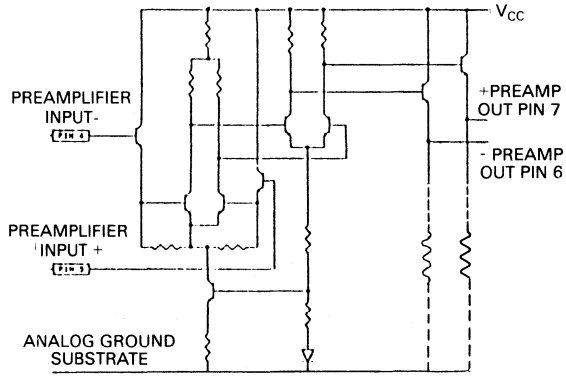


Figure 2. Preamplifier

The data, clock and ALBO threshold detector circuits as shown in Figure 3 are made up of two sets of gain stages which are driven differentially by the preamplifier outputs.

The outputs of the data comparators, D+ and D—, are gated with the sampling pulse to set the data latches. The peak detector output is internally connected to the automatic line build out section (see Figure 4) of the circuit, whose voltage controls the current through the ALBO diodes. This, in turn, varies the small signal resistance, r (II), which is used to control the attenuation characteristics of the ALBO network to provide shaped loss dependent on the line loss as well as automatic gain control function.

The clock recovery section, as shown in Figure 5, consists of an amplifier and an LC tank circuit whose resonant frequency is equal to the incoming data rate. The excitation that comes from the clock threshold detector is applied internally both to the input of clock amplifier and the tank

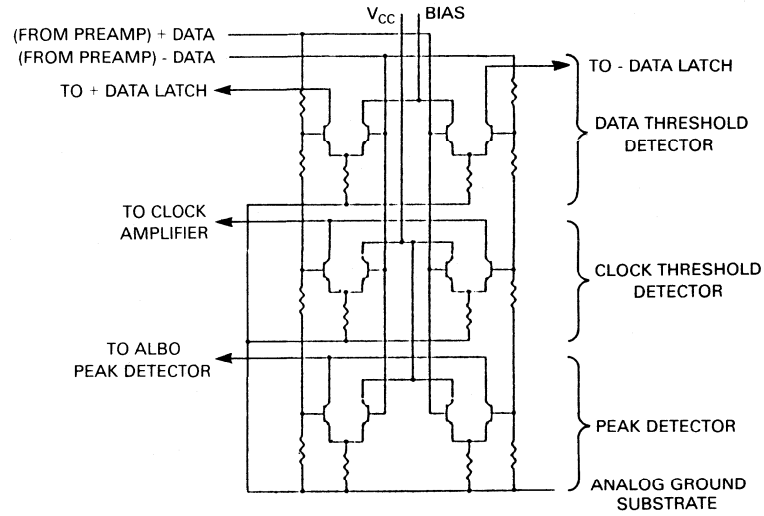


Figure 3. Data, Clock and Peak Threshold Detectors

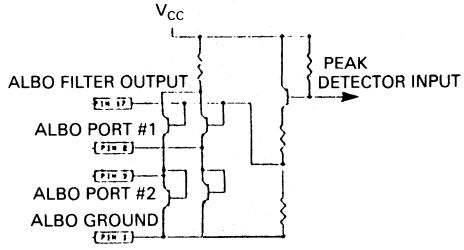


Figure 4. ALBO (Automatic Line Build Out)

circuit at Pin 15. Pin 16 is used to bias the tank circuit which has a Quality factor (Q) from 60 to 120 to track incoming jitter and to sustain oscillations when successive zeros are transmitted. The spectrum of bipolar signal does not contain any components at the data rate, therefore, clock threshold detector full wave rectifies the preamplifier output signal to double the equalized spectrum. This signal, when applied to the LC resonant circuit generates click at 1.544 MHz. The oscillations are applied to the input of the amplifier and sustained for a maximum number of 15 zeroes. It is therefore essential to maintain a sufficient one's density to keep the clock running (Bell Pub 62411 requires a minimum of 12.5% one's density). The clock amplifier (32 dB open loop gain and 3 dB roll off at 10 MHz) regenerates the **clock signal and** feeds this squarewave through a phase shift network. This network consists of an RLC combination which is located externally and integrates this square waveform into a triangle waveform. The objective in creating this triangle waveform is to generate a 90° phase shift so that the eye can be sampled in the middle. To do so, a sampling pulse

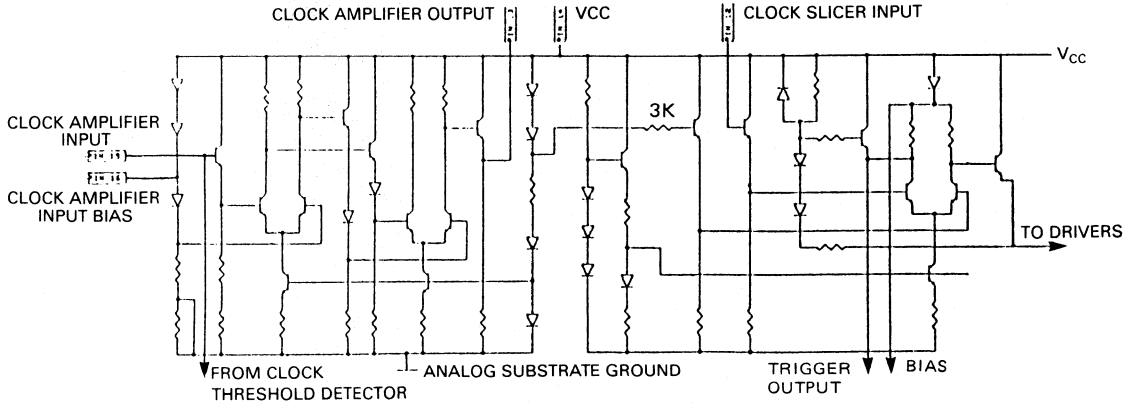


Figure 5. Clock Amplifier and Slicer Circuit

is generated on the positive edge of the clock and gated with the data threshold detector outputs to drive the data latches.

When D+ is low, the sampling pulse sets flip-flop 1 on the leading edge of this pulse. Similarly when D– is low, the sampling pulse sets flip-flop 2. The flip-flop outputs are then used to drive the output drivers as shown in Figure 7. The output stage is designed to drive a nominal load of 100 ohm, and can handle a **peak current of 50mA.**

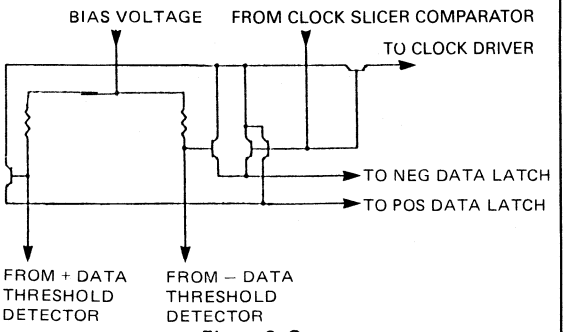


Figure 6. Gates

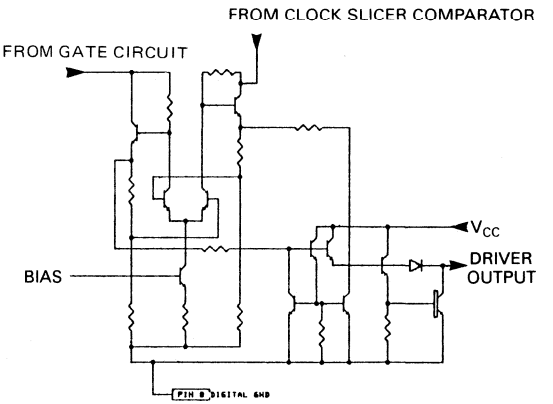


Figure 7. Output Driver & Data Latch Section

WAVEFORM AND TIMING DIAGRAM

A) Input Signal (Pin 4)
B) Oscillator Waveform (Pin 15)
C) Oscillator Output Waveform (Pin13)
D) Integrated Waveform from Pin 13 (Pin 12)
E) Strobe Pulse
F) Regenerated Clock Output (Pin 11)
G) Data+ (Pin 9)
H) Data– (Pin 10)

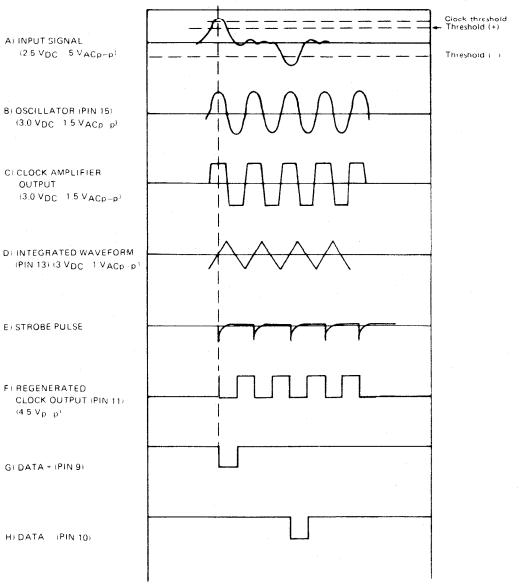


Figure 8. Waveform and Timing Diagram

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.1 V ± 5%, T_A = 25°C, unless specified otherwise.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Supply Current		26	34	mA	ALBO Off
	Clock & Data Output					
	Output Leakeage Current		0	100	μA	$V_{pull\text{-}up}$ = 15 V
	Amplifier Pin Voltages	2.4	2.9	3.4	V	At DC Unity Gain
	Amplifier Output					
	Offset Voltage	-50	0	50	mV	R_S = 8.2 kΩ
	Voltage Swing	2.2			V	Measured Differentially from Pin 7 to Pin 6
	Amplifier Input					
	Bias Current			5	μA	
	ALBO on Current	3			mA	
	Drive Current		1		mA	
AC CHARACTERISTICS						
	Pre Amplifier					
	AC Gain @ 1 MHz		50		dB	
	Input Impedance	20			kΩ	
	Output Impedance			200	Ω	
	Clock Amplifier					
	AC Gain		32		dB	
	-3 dB Bandwidth	10			MHz	
	Delay		10		ns	
	Output impedance			200	Ω	
	ALBO					
	Off Impedance	20			kΩ	
	On Impedance			25	Ω	
CLOCK DATA OUTPUT BUFFERS						
	Rise Time		30		ns	R_L = 130Ω, $V_{pull\text{-}up}$ = 5.1 V ± 5%
	Fall Time		30		ns	
	Output Pulse Width		244		ns	
	Sampling Pulse Width		10		ns	
	V_{OL}		0.7		V	
	I_L sink		35		mA	
THRESHOLDS						
	ALBO	1.4	1.5	1.6	V	
	Clock Drive Current Peak		1.0		mA	At V_O = V_{ALBO} Threshold
CLOCK THRESHOLD						
	% of ALBO	63	69	75	%	
DATA THRESHOLD						
	% of ALBO	40	46	52	%	

APPLICATION CIRCUIT PRINCIPLES

For ease of analysis, the application circuit shown in Figure 9 will be broken down into the following sections:

1. Pulse isolation transformer section
2. Impedance matching pad
3. Equalizer
4. Preamplifier
5. ALBO network
6. LC tank
7. Phase shift network

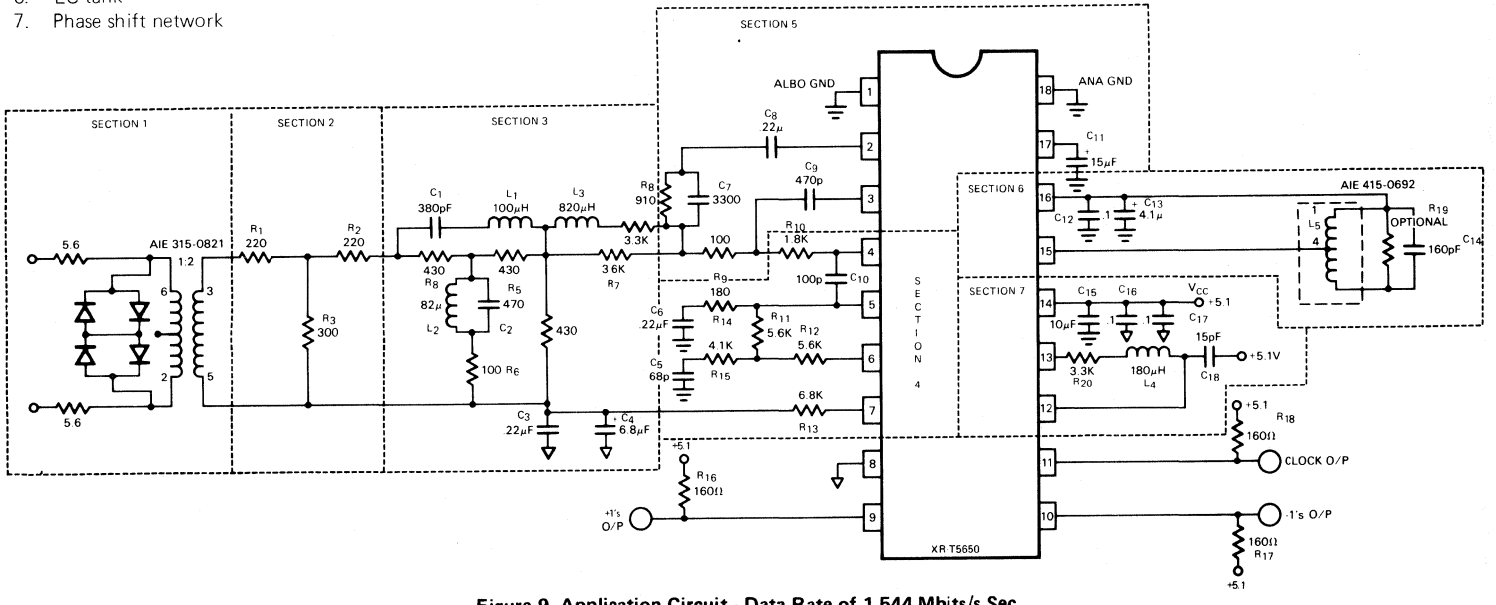


Figure 9. Application Circuit - Data Rate of 1.544 Mbits/s Sec

APPLICATION CIRCUIT PRINCIPLES

The receiver configuration as shown in Figure 9 will accept signals encoded in AMI, B8ZS, HDB3 and other bipolar line codes. Note that T1 transmission is done over balanced twisted pair for each direction of transmission and terminated by characteristic load impedance of 100 ohm ±5%.

1. Given the above constraints, the pulse isolation transformer shown in Figure 10 uses a set of 5.6Ω resistors to limit the current, and a diode clamping configuration. to protect the receiver from electrical differential disturbances that could be present on the line. Note that these diodes will clamp the voltage if the line loss is less than 6 dB at the primary side of the transformer.

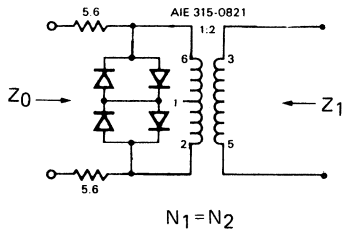


Figure 10. Isolation Transformer

Note: The transformer used in this application is an AIE 3150821 which has a 1:2 turns ratio.

2. Given the characteristic impedance of 100 ohm ±5%, it is first necessary to scale the impedance of the secondary of the transformer

$$\frac{Z0}{Z1} = \left(\frac{N0}{N1}\right)^2$$

Knowing the impedance on the secondary of the transformer, we can use the pad shown in Figure 11 to first match the impedance and also attenuate the incoming signal to an acceptable level.

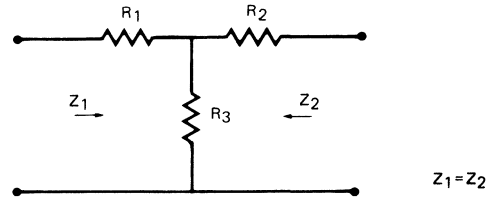


Figure 11. Attenuator Pad

Given a condition where the pad loss needs to be increased or decreased, the following set of formulas can be used:

$$R1 = R2 = \frac{(k-1)Z}{(k+1)}$$

$$R3 = \frac{k\,2Z}{k2-1}$$

The "k" factor in this case is the ratio of current, voltage, or power corresponding to a given value of attenuation expressed in decibels. To simplify the calculation of attenuator networks, the following table is helpful in finding the desired resistor values.

n(dB)	$\frac{k-1}{k+1}$	$\frac{k}{k^2-1}$	n(dB)	$\frac{k-1}{k+1}$	$\frac{k}{k^2-1}$	n(dB)	$\frac{k-1}{k+1}$	$\frac{k}{k^2-1}$
0.05	0.0028783	86.8618	8.0	0.43051	0.47309	28.5	0.92755	0.037636
0.1	0.0057562	43.4303	8.5	0.45366	0.43765	29.0	0.93147	0.035526
0.2	0.011512	21.713	9.0	0.47622	0.40592	29.5	0.43518	0.033534
0.3	0.017268	14.473	9.5	0.49817	0.37730	30.0	0.93869	0.031655
0.4	0.023022	10.854	10.0	0.51950	0.35137	31.0	0.94518	0.028207
0.5	0.028774	8.6810	10.5	0.54020	0.32775	31.5	0.94817	0.026627
0.6	0.34525	7.2327	11.0	0.56026	0.30616	32.0	0.95099	0.025135
0.7	0.040274	6.1974	11.5	0.57969	0.28635	33.0	0.95621	0.022398
0.8	0.046019	5.4209	12.0	0.59848	0.26811	34.0	0.96088	0.019961
0.9	0.051763	4.8268	12.5	0.61664	0.25127	34.5	0.96302	0.018843
1.0	0.057502	4.3335	13.0	0.63416	0.23568	35.0	0.96506	0.017788
1.1	0.063237	3.9376	13.5	0.65105	0.22123	36.0	0.96880	0.015853
1.2	0.068968	3.6076	14.0	0.66733	0.20780	37.0	0.97214	0.014128
1.3	0.074695	3.3283	14.5	0.68298	0.19529	37.5	0.97368	0.013338
1.4	0.080418	3.0888	15.0	0.69804	0.18363	38.0	0.97513	0.012591
1.5	0.086132	2.8809	15.5	0.72250	0.17275	39.0	0.97781	0.0112216
1.6	0.091846	2.6991	16.0	0.72639	0.16257	40.0	0.98020	0.0100010
1.7	0.097551	2.5384	16.5	0.73970	0.15305	40.5	0.98130	0.0094414
1.8	0.103249	2.3956	17.0	0.75246	0.14413	41.0	0.98233	0.0089134
1.9	0.108939	2.2676	17.5	0.76468	0.13577	42.0	0.98424	0.0079436
2.0	0.11463	2.1523	18.0	0.77637	0.12792	43.0	0.98594	0.0070795
2.2	0.12597	1.9531	18.5	0.78755	0.12055	43.5	0.98672	0.0066834
2.4	0.13728	1.7867	19.0	0.79823	0.11363	44.0	0.98746	0.0063096
2.5	0.14293	1.7133	19.5	0.80844	0.10713	45.0	0.98887	0.0056234
2.6	0.14856	1.6457	20.0	0.81818	0.10101	46.0	0.99003	0.0050119
2.8	0.15980	1.5245	20.5	0.82747	0.095255	46.5	0.99058	0.0047315
3.0	0.17100	1.4192	21.0	0.83634	0.089841	47.0	0.99111	0.0044668
3.2	0.18215	1.3269	21.5	0.84478	0.084739	48.0	0.99207	0.0039811
3.4	0.19326	1.2453	22.0	0.85282	0.079935	49.0	0.99293	0.0035481
3.5	0.19879	1.2079	22.5	0.86048	0.075411	50.0	0.99370	0.0031623
3.6	0.20432	1.1725	23.0	0.86777	0.071148	51.0	0.99438	0.0028184
3.8	0.21532	1.1072	23.5	0.87470	0.067133	52.0	0.99499	0.0025119
4.0	0.22627	1.0483	24.0	0.88130	0.063348	54.0	0.99602	0.0019953
4.5	0.25340	0.92323	24.5	0.88756	0.059778	55.0	0.99645	0.0017783
5.0	0.28013	0.82241	25.0	0.89352	0.056413	56.0	0.99684	0.0015849
5.5	0.30643	0.73922	25.5	0.89917	0.053238	57.0	0.99718	0.0014125
6.0	0.33228	0.66932	26.0	0.90455	0.050246	58.0	0.99749	0.0012589
6.5	0.35764	0.60964	26.5	0.90965	0.047422	60.0	0.99800	0.0010000
7.0	0.38246	0.55801	27.0	0.91448	0.044757	65.0	0.99888	0.00056234
7.5	0.40677	0.51291	27.5	0.91907	0.042245	70.0	0.99937	0.00031623
			28.0	0.92343	0.039874			

3. The equalizer exhibits shaped attentuation characteristics to compensate for the line loss which varies with cable size, cable length and applied frequencies. Spectrum components attenuated by the line cannot be recovered. However, a flat (or equalized) response can be obtained by attenuating predominant spectrum components with an equalizer having inverse line loss characteristics. For the equalizer shown below in Figure 12, the two resistors, R4 and R5, are equal to the circuit impedance (400 ohm). Resistor R6 is varied in order to obtain different values of loss. As the frequency is increased, the reactance of C1 and C2 decreases and the reactance of L1 and L2 increases. At resonance given by the formula:

$fr = \frac{1}{2\pi\sqrt{LC}}$ $f1=f2$ $f1 = \frac{1}{2\pi\sqrt{L1C1}}$ $f2 = \frac{1}{2\pi\sqrt{L2C2}}$

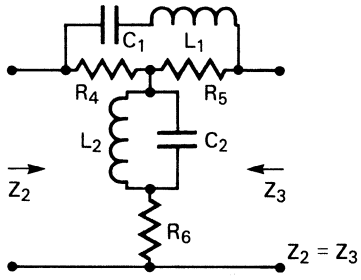


Figure 12. Equalizer Network

R4 and R5 are for all intent and purposes shorted and R6 is opened up. Thus, the pad loss is theoretically zero. The response of the equalizer needs to be shaped to the line loss characteristic of the cable in order to obtain as flat a response as possible at the output of the equaiizer. Twenty dB of equalization is about all that can be obtained with a single equalizer of this configuration. If a greater amount of equalization is required two or more equalizers may be connected in tandem. The typical response of this network is shown in Figure 13. It is important to note about this circuit is the characteristic impulse response which may cause a ringing effect on the incoming data waveform.

If the shape of the equalizer response needs to be adjusted for a steeper response (going from 2 to 1), choose a higher inductance and a lower capacitance for the series resonant circuit and a lower inductance, higher capacitance for the parallel resonant circuit.

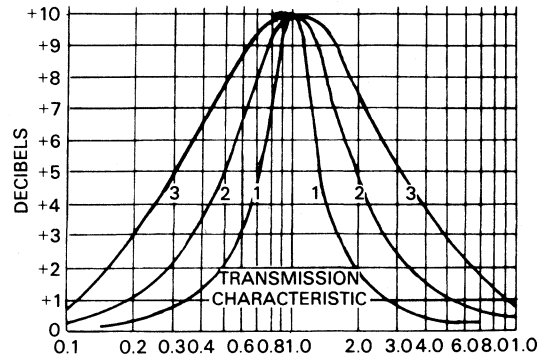


Figure 13. Transmission Characteristics of Equalizer Network

4. For ease of analysis concerning the preamplifier section, the following characteristics should be noted:

a. The input impedance of the preamplifier at 1.544 MHz (pins 4 and 5) is approximately 10 kohms.

b. The preamplifier closed loop AC gain is approximately equal to the ratio of (R11 + R12) over R14 as shown in Figure 15. For the application circuit shown in Figure 9, this value is calculated to be approximately 36 dB. Capacitor C6 is an isolation capacitor and will be in the order of 1 μF or higher.

c. In order to minimize the noise at the input of the preamplifier, a small RC low pass filter is placed between pins 4 and 5 (R10 C10). Notice that the dynamic range and stability of the preamplifier is very susceptible to the capacitance between 4 and 5.

d. R13 is chosen in order to minimize the offset of the preamplifier outputs. Its value is dependent on the resistor values used for the preamplifier gain adjust and the total series resistance between pin 7 and 4. C4 is a decoupling capacitor and forms a low pass filter together with R13.

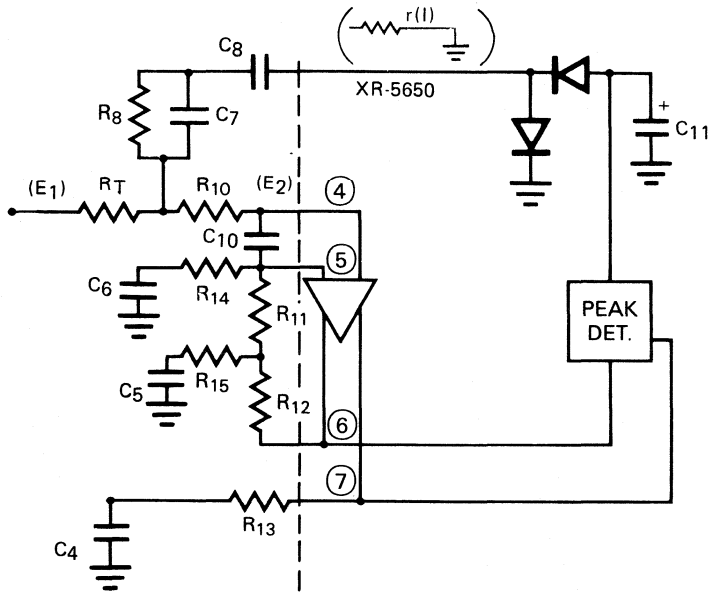


Figure 15. Preamplifier and ALBO Network Equivalent Circuit

5. The ALBO section usually preceeds the preamplifier and acts as a variable cable length simulator so that overall loss introduced by the cable and ALBO network equals to the loss of 6000 ft. long 22 AWG cable. The circuit implementation is based on the following characteristics:

a. The energy of the pulse generated is constant.

b. The gain phase characteristics of the preamplifier are fixed as shown in the application circuit.

Automatic equalizer adjusts its amplitude characteristics based on the peak value of the input signal. Figure 16 shows typical loss characteristics for 22 AWG cable for different lengths. It is important to notice that the location of the single pole and the low frequency loss are both **a function of cable length.**

To obtain these characteristics it is necessary to generate an adjustable single zero and an adjustable flat gain for varying cable lengths.

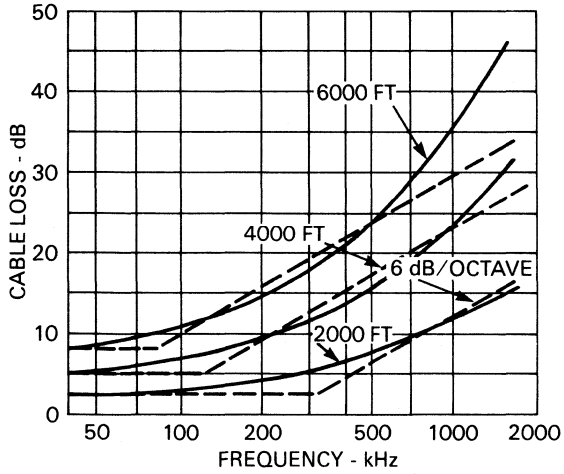


Figure 16. Loss of 22 Gauge Cable vs. Frequency

The combination of the ALBO equalizer network and the cable loss will give a first order approximation, to produce a flat gain and linear phase below 772 KHz. The feedback amplifier has an unbalanced input, a balanced output and contains fixed equalization in the feedback network. It also provides a fixed real zero below 772 kHz and one beginning about at 800 kHz to optimize the immunity of the receiver for nearend crosstalk (NEXT) produced by other systems operating within the same cable sheath. The ouput of the preamplifier is fed to a peak detector whose output voltage generates a control current (I), which in turn varies the small signal resistance, r(I). When diodes are fully on r(I) is guaranteed to be less than or equal to 25 ohms. See Figure 15.

The capacitor C8 is used to block the DC from the input to the amplifier. Capacitor C11 is part of the ALBO filter circuit and together with R_{INT} sets ALBO time constant and AGC droop rate. It also smooths out on current of the variolosser diodes. Assuming that the input impedance to the amplifier is sufficiently large so that it does not load down the output of the ALBO, we get the following transfer function:

(1)
$$\frac{E2}{E1} = \frac{+r(I)}{RT+r(I)} \cdot \frac{s + \dfrac{r(I) + R8}{r(I)\ R8\ C7}}{s + \dfrac{1}{R8\ C7}}$$

where $r(I) = \approx 25\Omega$ when fully on

this transfer function has a fixed pole at

(2)
$$s = -\frac{1}{R8\ C7}$$

and adjustable zero at

(3)
$$s = \frac{r(I) + R8}{r(I)\ R8\ C7}$$

and a variable flat loss at

(4)
$$\frac{R8 + r(I)}{RT + r(I)}$$

Notice that the feedback network as shown in Figure 15 has also a fixed real zero at S = 1/R15C5 that cancels out the pole of the ALBO and is equal to S = 1/R8C7.

6. An LC resonator is used to recover the clock from the incoming PCM pulse stream. Since the spectrum of bipolar signal passes through zero at the clock frequency, the spectrum is doubled by full wave rectifying the signal above the clock threshold. This brings the peak of the rectified spectrum on top of the clock frequency. The resonator is then driven by the output of the full wave rectifier to produce a stable clock signal.

Frequency of resonance is given by

$$fo = \frac{1}{2\pi\sqrt{LC}}$$

The 3 dB bandwidth of the tank is related to the resonant frequency by the following expression:

$$B = \frac{fo}{Q}$$

and the Q is related to circuit components as follows:

$$Q = \frac{R}{WoL}$$

Two important criteria need to be taken into account when receiving PCM signals. First, the tank has to have enough bandwidth so that the jitter in the recovered clock follows the jitter in the data in order not to cause any errors in the reception process. Second, the tank has to have enough Q to sustain the clocksignal when 15 successive zeros are received. These two factors are in contradiction with each other, however, in practice, Qs in the range of 60-120 are used to meet the jitter and clock recovery requirements.

7. To achieve a minimum bit error rate, the eye pattern needs to be sampled in the middle where it has the largest opening. Since sampling is performed on the positive edge of the internal clock, this edge needs to be aligned with the peak of the eye pattern. To achieve this, an external RLC network is used to phase shift the clock signal by 90 degrees. R is chosen as 3.3k to cancel out the offset caused by an internal resistor. An RC combination could be used for phase shifting purposes as well. However, use of inductor L improves and emphasizes the clock transitions. In practice, the driver outputs are observed to turn on roughly 30-40 nsec after the peak of the eye pattern. This is due to the delay of the clock signal through the slicer and output driver circuits.

Output drivers are designed with open collector outputs which can handle 50 mA peak currents to drive lines with characteristic impedance of 100 ohms. The data output pulses are 50 percent duty cycle.

Short Haul PCM Line Interface Using the XR-T5683/L85

INTRODUCTION

The XR-T5683/L85 Monolithic PCM Transceivers are designed primarily for short line (<10dB) PCM transmission applications such as in digital Private Branch Exchange's (PBXs), Digital Multiplexed Interfaces (DMI) and standard PCM data interface circuits. Both of these devices are identical in pinout but intended to operate in slightly different applications. The XR-T5683 is a higher frequency device (10MBPS), capable of extracting and transmitting data and clock from the AMI encoded data stream. The XR-T56L85 is capable of performing the same function up to 2.048MBPS and only consume one forth the power. Also, because of a different preamplifier input stage, the XR-T56L85 is capable of accepting either single coaxial, a twisted pair capacitive coupled or a balanced transformer input.

Both of these devices are packaged in a hermetirc 18 pin CERDIP and designed such that there is no phase difference between the extracted clock and data outputs.

PRINCIPLES OF OPERATION

Figure 1 contains a Functional Block Diagram of the XR-T5683 and XR-T56L85. The Circuit consists of two separate sections: one is the line receiver, and the other is the line transmitter. The receiver accepts incoming bipolar signals and converts them into TTL D+ and D- data streams. The main difference between the XR-T5683 and the XR-T56L22 preamplifier is that the XR-T56L85 is capable of accepting a single ended capacitive coupled AMI signal as well as a balanced transformer coupled signal. In order to successfully recover the data from the capacitive coupled signal, the receiver relies on the peak detector, which converts the positive signal amplitude into a DC variable threshold. This variable threshold is then mirrored around 2.5V (Voltage Reference) in order to be able to detect the negative coupled pulses. It also produces a clock output from the input data. In the transmit direction, full width, TTL compatible D+ and D- signals at the inputs and a 50% duty cycle clock are combined to form the bipolar line signal at the outputs of a transformer. The power supplies for the two sections of the circuit are internally isolated to avoid crosstalk problems.

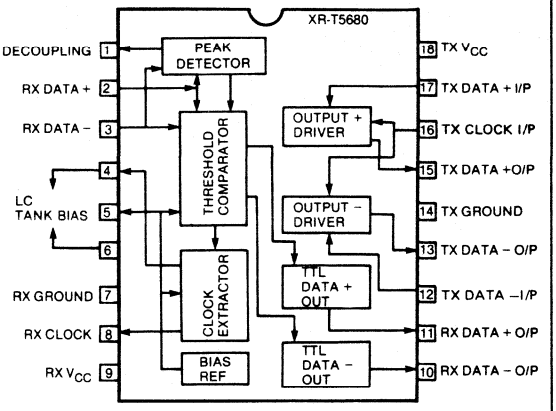


Figure 1. Functional Block Diagram for the XR-T5683 or XR-T56L85

Receiver Circuit Description:

The receiver is designed to handle a maximum of 10 dB line attenuation. This condition allows the design to adopt a relatively simple approach as compared with long transmission line receivers which usually require ALBO circuits and equalization networks to function properly.

The operation of the XR-T5683 receiver relies on the peak detector which converts the incoming signal amplitude into a DC variable threshold. The variable threshold is arranged to slice the input signal at half amplitude point of the peak voltage (see figure 3), so that D+ and D- data can be accurately extracted under the worst expected condition. It also ensures a constant output pulse width, over the nominal 10 dB of line attenuation. The D+ and D- data pulses go through similar level shifting circuits to be converted into TTL compatible output signals.

Clock Extraction and Timing

Since the input does not carry any frequency components around the transmission rate, the input wave-form is full wave rectified and applied to an external L-C resonant circuit for clock extraction. The amplitude modulated sine wave at the resonant circuit is coupled through a capacitor to a zero crossing detector before being applied to the input of an ECL/TTL converter as shown in Figure 2.

To convert the half-width data at the receiver outputs into full width signals for digital processing, it is common practice to use positive edge triggered D/FFs. This requires the mid-point of the data to be aligned with the rising edge of the clock so that no error will result. Should the data be jittered with a max. amplitude of ±0.25 UI relative to the clock (see Figure 5). The disadvantage of this scheme is additional hardware that is needed to ensure the two signals have the correct timing relationship. It is possible by means of an alternative retiming circuit as shown in Figure 6 to perform the same function while still keeping the data and the clock in the same phase. This circuit has twice the jitter tolerance under the same condition as compared with a single D-type counterpart and is recommended to be used with the XR-T5683/L85. It is anticipated that no glitches due to crosstalk, etc., should exist at the receiver data output terminals under the intended short line applications.

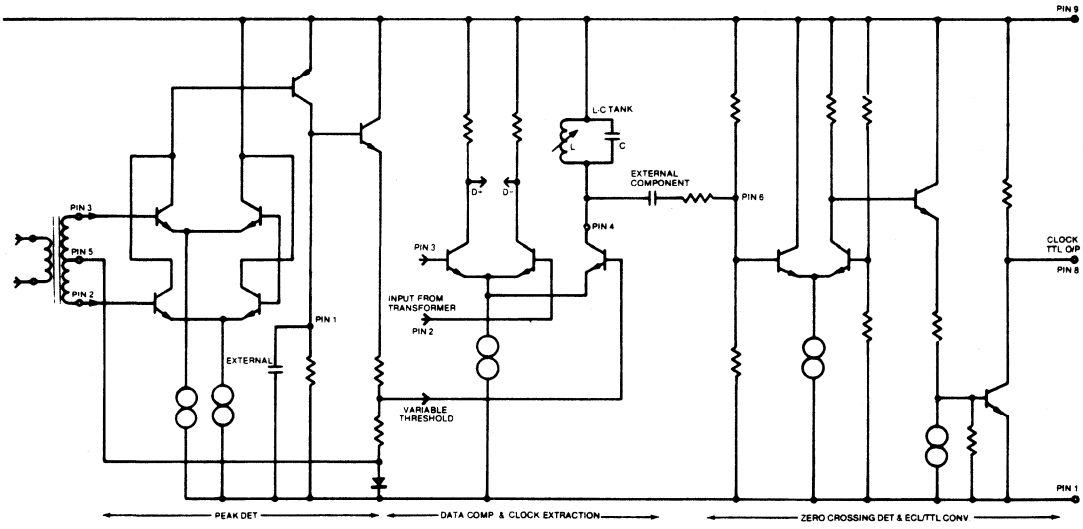


Figure 2A. Simplified Circuit of XR-T5683 Receiver

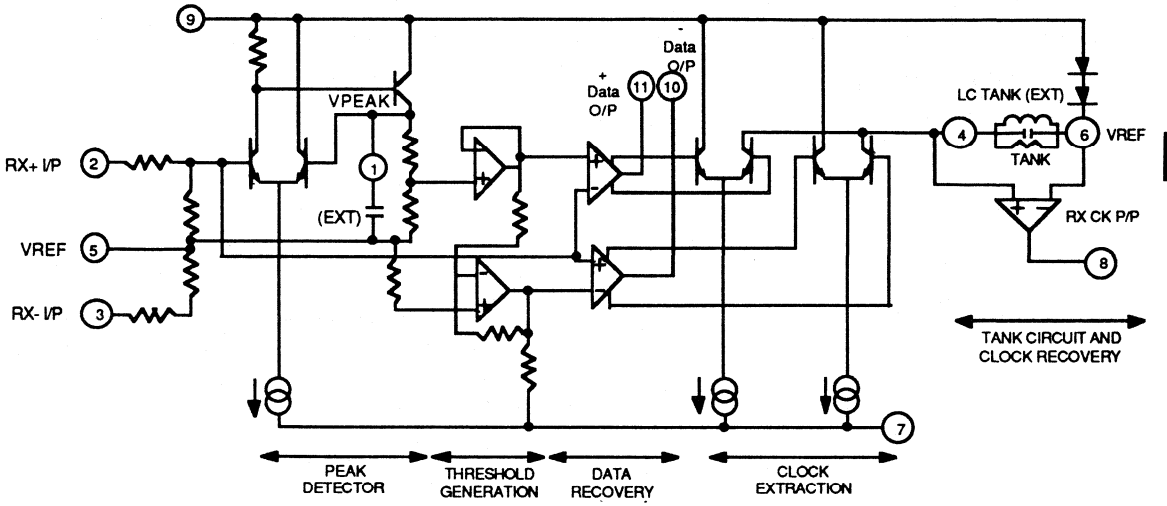
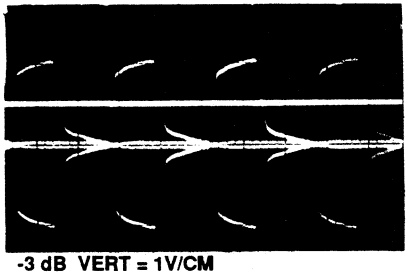
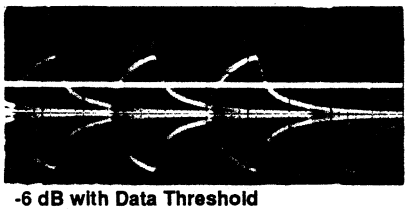


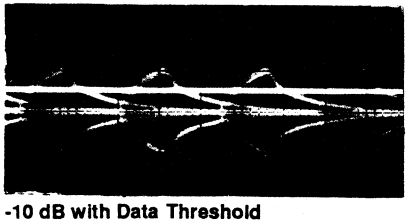
Figure 2B. Simplified Circuit of XR-T56L85 Circuit.



-3 dB VERT = 1V/CM
HORZ. = 200 nS/CM

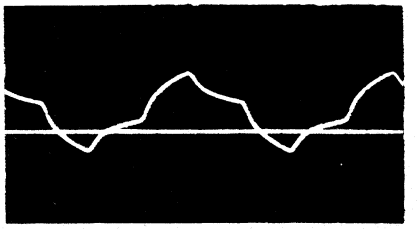


-6 dB with Data Threshold

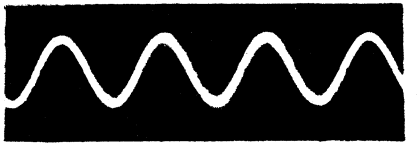


-10 dB with Data Threshold

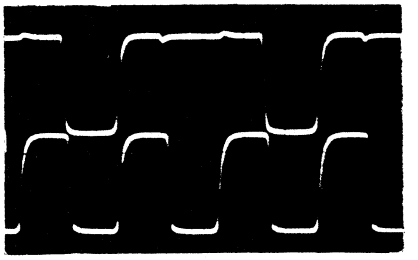
Figure 3. Typical Eye Pattern obtained at Pin 2 or 3 for Coaxial Cable at Various Line Length. Bit Rate = 2048 K Bits/s.



-10 dB (1-1-1 Pattern) with Data Threshold



Tank Circuit Waveform at Pin 4



Receiver Data and Clock Outputs

Figure 4. Timing Diagram of Circuit Waveforms for a 1-1-1 Input Data Pattern.

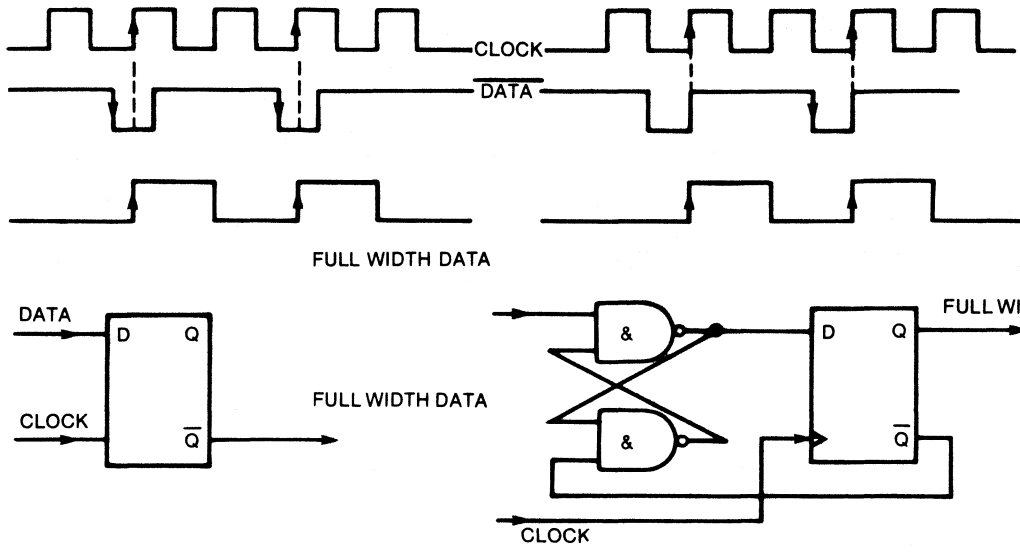


Figure 5. Retiming Circuit Requires Clock to be phase advanced by 90°C relative to data for optimum operations

Figure 6. Retiming Circuit to be used with XR-T5680

Transmitter:

The transmitter consists of two identical TTL input open-collector NAND gates. The output drivers are capable of handling a maximum current of 40 mA for the XR-T5683 and 80 mA for the XR-T56L85. If the input D+ and D- are half width signals, Pin 16 should be returned to $+V_{CC}$ via a 1K resistor. If the input data are full width signals, a synchronized 50% duty cycle TTL clock is needed at Pin 16 to obtain a bipolar signal at the output of a centre-tapped line transformer (see Figure 7). The output signal conforms to CCITT G.703 recommendation. A circuit connection diagram for 2048 Kbits/s line interface application is shown in Figure 8.

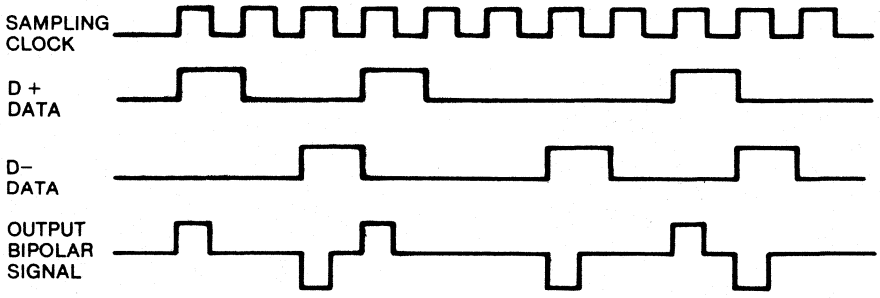
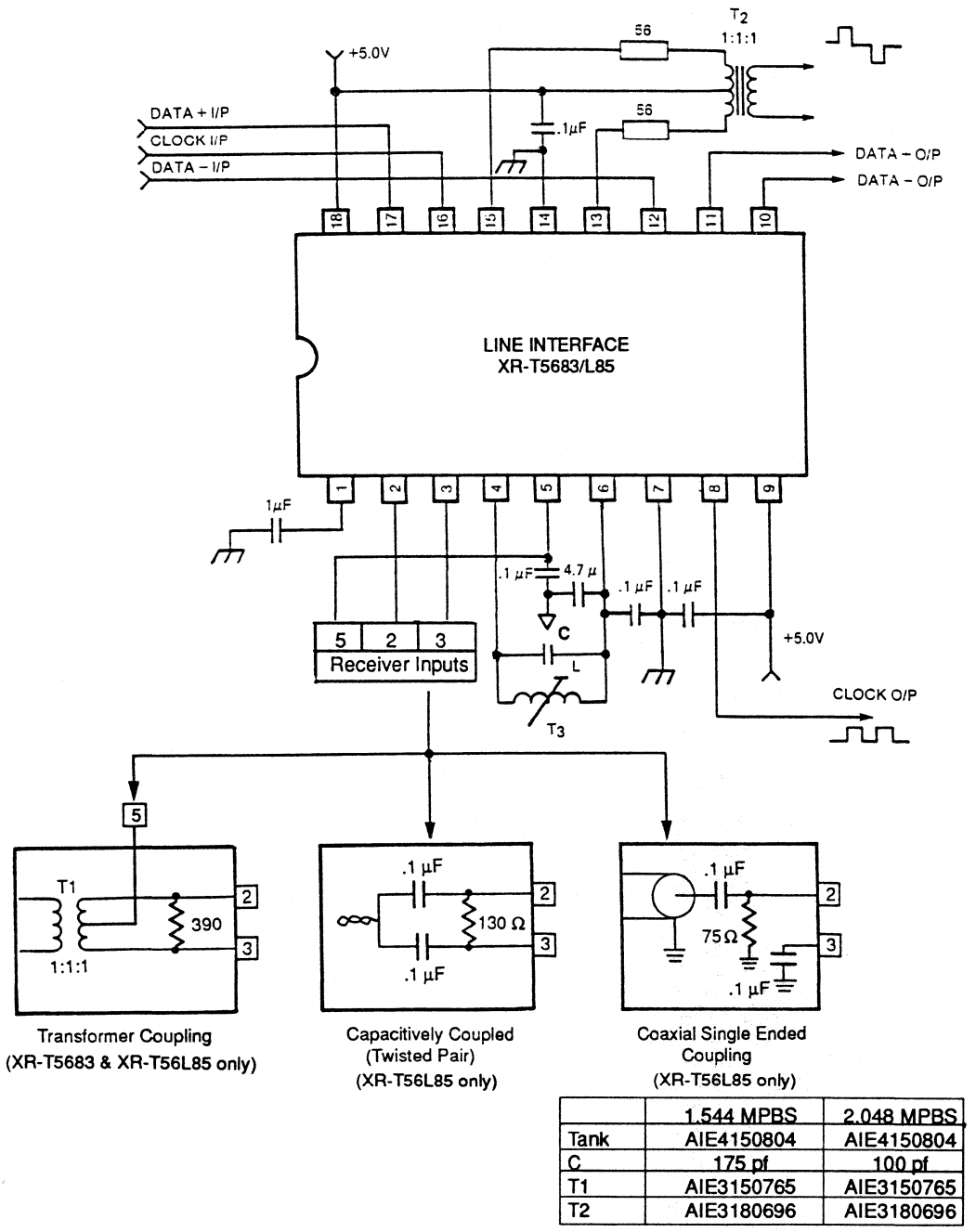


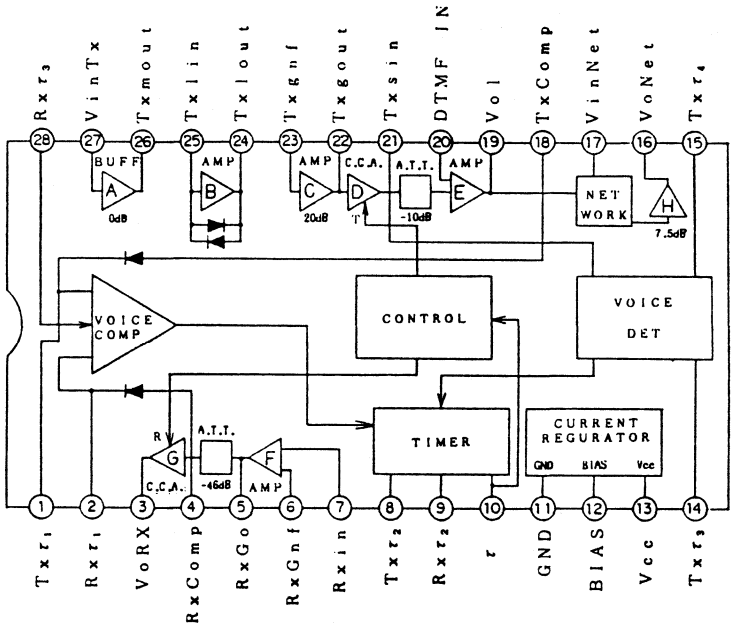
Figure 7. Input Timing Diagram for Transmitter.



	1.544 MPBS	2.048 MPBS
Tank	AIE4150804	AIE4150804
C	175 pf	100 pf
T1	AIE3150765	AIE3150765
T2	AIE3180696	AIE3180696

Figure 8. Recommended Circuit for XR-T5683/L85

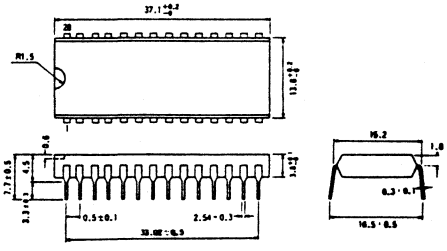
SPEAKERPHONE DESIGN USING THE XR-T6425



Features

Hands-free phone is available with one chip solution.
Using no-adjustment circuit, no need for level adjustment.
No inharmonious feeling because of smooth T/R switching.
Operating by line voltage.
Connection with lines is easy because of built-in network circuit.
Capable of low voltage operation. (4.5V Min)
Built-in microphone amplifier
Includes ambient noise and voice discrimination

Dimension (mm)



Pin Connections

1. Transmitter stabilization time constant input terminal ..... $Tx\tau_1$
2. Receiver stabilization time constant input terminal ..... $Rx\tau_1$
3. Receiving signal output terminal ..... VoRX
4. Receiving comparison signal input terminal ..... RxComp
5. Receiving amplifier gain adjustment terminal (output) ..... RxGo
6. Receiving amplifier gain adjustment terminal (input) ..... RxGnf
7. Receiving input terminal ..... Rxin
8. Transmitting holding time constant input terminal ..... $Tx\tau_2$
9. Receiving holding time constant input terminal ..... $Rx\tau_2$
10. T/R switch timing time constant input terminal ..... τ
11. GND ..... GND
12. Bias power supply output (Vcc/2) ..... BIAS
13. Vcc (4.5~6.5V) Vcc
14. Voice rectification time constant input terminal ..... $Tx\tau_3$
15. Ambient noise and voice discrimination time constant input terminal ..... $Tx\tau_4$
16. Receiving signal network output terminal ..... VoNet
17. T/R signal network input/output terminal ..... VinNet
18. Transmitting comparison signal input terminal ..... TxComp
19. Transmitting signal output terminal ..... Vol
20. DTMF input terminal ..... DTMF IN
21. Transmitting signal, noise and voice comparison input terminal ..... Txsin
22. Transmitting amplifier gain adjustment terminal (output) ..... Txgout
23. Transmitting amplifier gain adjustment terminal (input) ..... Txgnf
24. Transmitting limiter-amplifier gain adjustment terminal (output) ..... Txlout

GENERAL DESCRIPTION

1) Transmitter Section

(Pins 27, 26, 25, 24, 23, 22, 20, 19)
This section transfers the input signal from the ECM (microphone) to the buffer A and outputs to pin 26 at unity gain. Amplifier B has a negative input with a diode limiter, and it's gain is determined by the ratio of R4 and R5. The output of pin 24 connects to the input of amplifier C through a bandpass filter. The signals obtained through the filter get amplified by nearly 20db with amplifier C. One of the outputs from this amplifier (pin 22) is ac-coupled through C6 back to pin 21. The other output connects to the CCA (Current Control Attenator) internally and is used to attenuate signals with respect to the receive side signals. Lastly, the Amplifier E drives the transmitting signals onto the telephone line through the impedance matched resistance R14 (680 ohm). This signal is also used as an input to the network pad whose function is to generate a control signal for the receive control circuitry.

2) Receiver Section

This section amplifies the received signals from the network with amplifier H and F and feeds these signals back to the CCA. Here the signal is attenuated relative to the control signal from the transmit side. The outputs appear at pin 3, from which they can be further amplified with IC2 (see Figure 2).

3) Ambient Noise and Voice Discrimination Section

The purpose of this section is to discriminate between voice signals and ambient noise signals. The logic is such that it allows for a clean switch between the transmitter and the receiver by first comparing the transmit path signal time constant at pin 14 to the ambient noise time constant generated at pin 1 and 2. The output is then connected to the timer section which provides for smooth T/R switching.

5) Voltage Regulator Section

This section supplies power and the necessary reference voltages to all the sections of the XR-T6425.

6) Timer Section

This section generates control signals for the T/R attenuator and also provides the time constant for T/R switching. The RC network on pin 8 sets the transmitting time constant and the one on pin 9 sets the receiving time constant. Pin 10 sets the timing for T/R switching and should be around 1.2V for transmitting and -1.2V for receiving. The calculations for transmitting and receiving are as follows:

Transmitting rise-time = $C_{22} \times 10^4$ 4.7µF, τ = 47ms
Transmitting hold-time = $C_{22} \times R_{22}$ 4.7µF; 470k, τ = 2.2s
Receiving rise-time = $C_{21} \times R^3$ 0.47µF, τ = 47ms
Receiving hold-time = $C_{21} \times R_{21}$ 0.47µF; 470k, τ = 0.22s

7) Network Section

The internal equivalent circuit for the Network section is shown below.

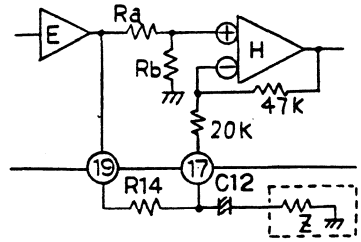


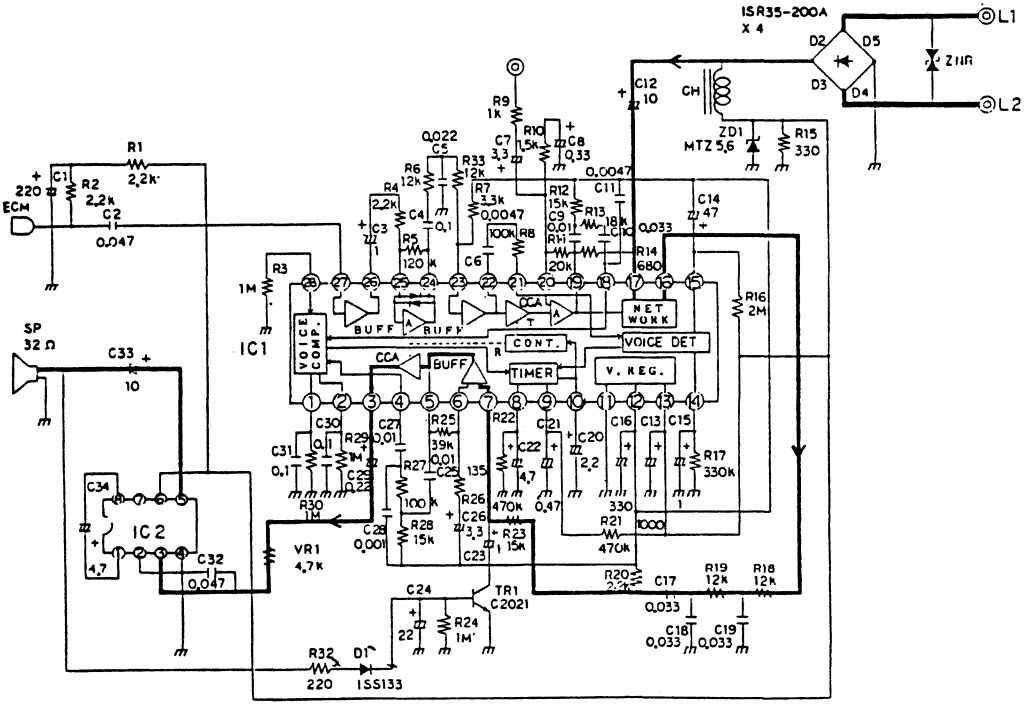
Figure 1. Network Section Equivalent Circuit

Transmitter section:

The transmit signals which are driven to the telephone line by the amplifier marked E also feed part of the signal to amplifier H through R14 as shown in the diagram. Internally, the signals from amplifier E are connected to the positive input of amplifier H through Ra and Rb. In case Ra = Rb, and R14 = 680 ohm, then none of the transmit signals should be output on pin 16.

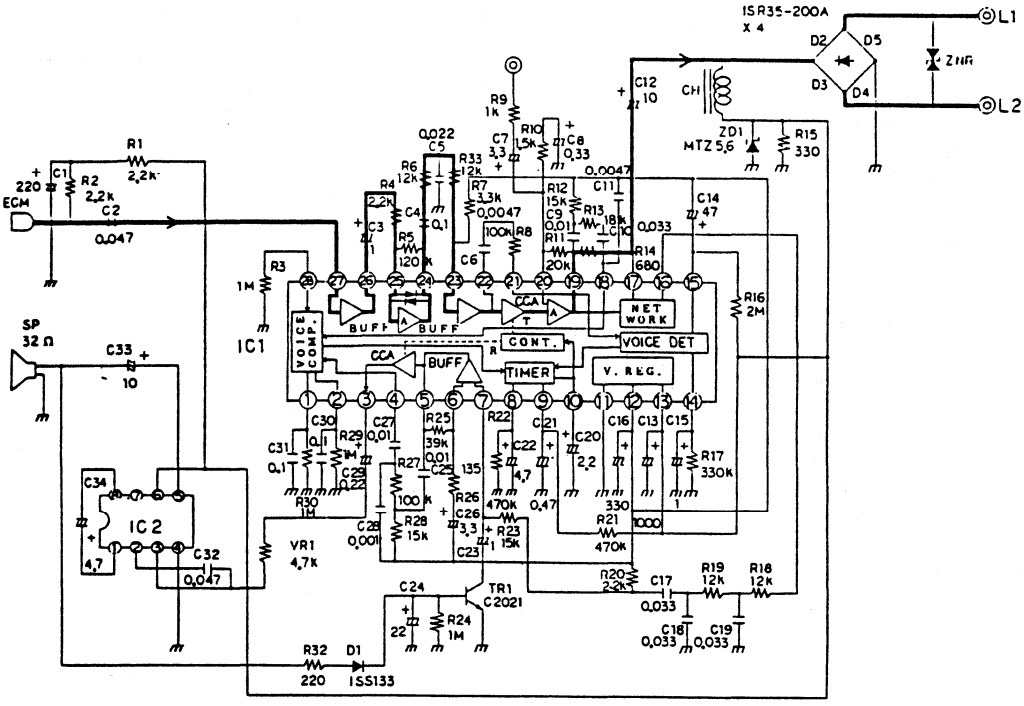
Receiver section:

The received signals are input to the negative side of the amplifier H and also to the positive side through R14. Because of the low output impedance of the E amplifier, the received signals are so small that they do not contribute to the composite signal of amplifier H. The T/R isolation degree of this network depends on R14 and the telephone line impedance.



Resistance: Ω, Capacitance: μF

Figure 2. Receiving Signaling Channel



Resistance: Ω, Capacitance: μF

Figure 3. Transmitting Signaling Channel

Table 1. Amplifiers

AMP. TYPE	APPLICATION	GAIN	REMARKS
A	TX amplifier	0dB	For the impedance conversion of emitter-follower microphone (Zin = 20kΩ)
B	TX amplifier	R5/R4	Negative input limiter amplifier, clamping at $\frac{1V}{\sqrt{2}}$ of 24pin output (Vo = 700mVrms)
C	TX amplifier	20dB	Fixed gain amplifier
D	TX amplifier	TX:20dB ST:-5dB RX:-23dB	Gain varies with transmit (TX), receive (RX) and stand-by (ST)
E	TX amplifier	R11/R10	The output of amplifier D is connected internally. It applies the signal to the negative input it when DTMF is used.
F	RX amplifier	R25/R26	Differential input amplifier. It's output is connected to the C.C.A. (amp G) through pin 5 and ATT.
G	RX amplifier	TX:-23dB ST:-5dB RX:20dB	Gain varies with transmit (TX), receive (RX) and stand-by (ST) operation.
H	RX amplifier	R7.5dB	Intended for the network loss correction of receiving (RX) side.

Absolute Maximum Ratings (Ta = 25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	Vcc	16	V
Permissible dissipation	Pd	700*	mW
Operating temperature range	Topr	-25~+75	°C
Storage temperature range	Tstg	-75~+125	°C

*When used at Ta = 25°C, 7mW is reduced for each degree.

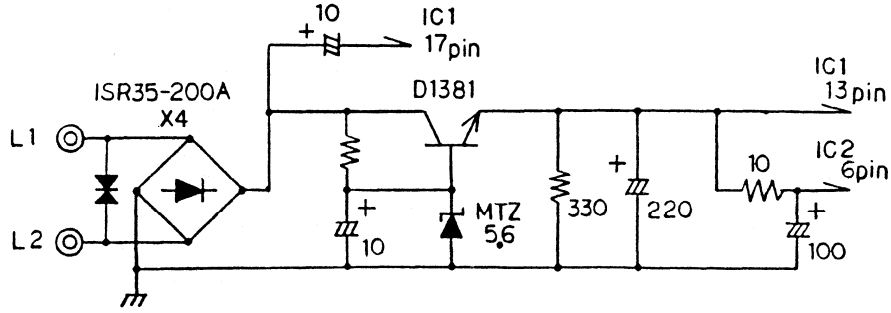
DC Electrical Characteristics
Test Conditions: Ta = 25 C, V_{CC} = 5V +/- 10% , f = 1 kHz unless otherwise specified.

PARAMETER	SYMBOL	STANDARD VALUE	UNIT	CONDITIONS
Recommended supply voltage range	Vcc op	4.5 ~ 6.5	V	
Quiescent circuit current	I_q	8.0	mA	No input of T/R signals
Receiving sensibility	Rxs	-64	dBm	
Transmitting sensibility	Txs	-74	dBm	
Receiving gain	Gv Rx	-22.5	dB	Receiving mode
Transmitting gain	Gv Tx	44	dB	Transmitting mode
Mic input level	Vin Lim	-55	dBm	THD = 1%
Receiving loss	Att Rx	-50	dB	Receiving ← → Transmitting relative value
Transmitting loss	Att Rx	-50	dB	Transmitting ← → Receiving relative value

Application Recommendations

1. In case of applying line voltage, pin 13 voltage should not be less than 4.5V.

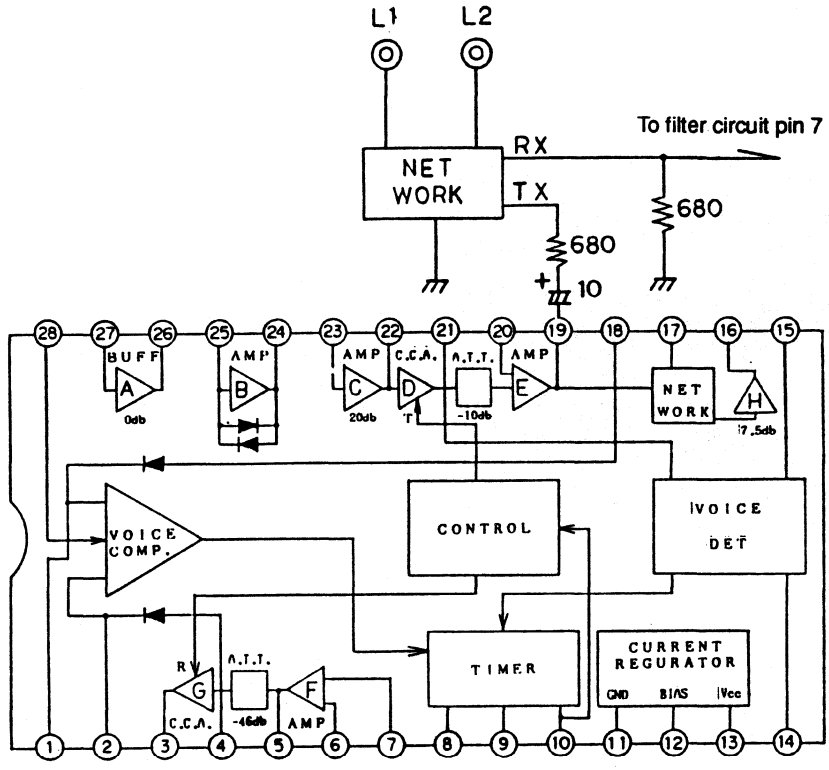
circuit below operates at line voltages of 6 to 7V.



Resistance: Ω Capacitance: μF

Figure 4. Supply Voltage Circuit

2. When using no internal network, refer to application circuit below.



3. When inputting a waveform of regular amplitude such as a sinusoidal waveform to the transmit side, the ambient and voice descrimination circuit will produce a mute after a certain amount of time. To solve this, put a 10kΩ between pin 15 and GND.

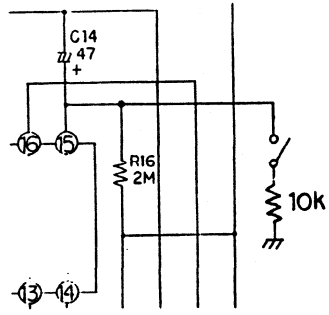
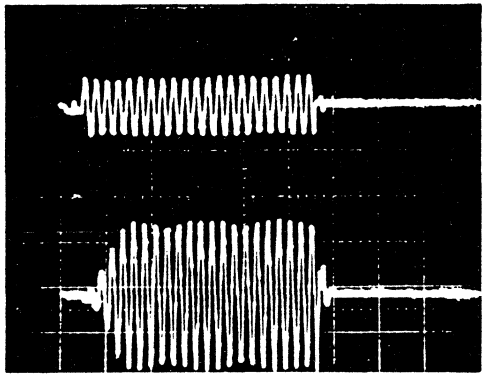


Figure 5. Voice Detector Circuit

4. This picture shows the delay time of IC1 - pin 17 to IC2 - pin 5. (Switching time from transmitting mode to receiving mode).



f =2 400Hz
CH1;m2 input waveform
CH2;m1 output waveform
t = 10ms/div
CH1 = 50mV/div, coupling;AC
Ch2 = 500mV/div, coupling;AC

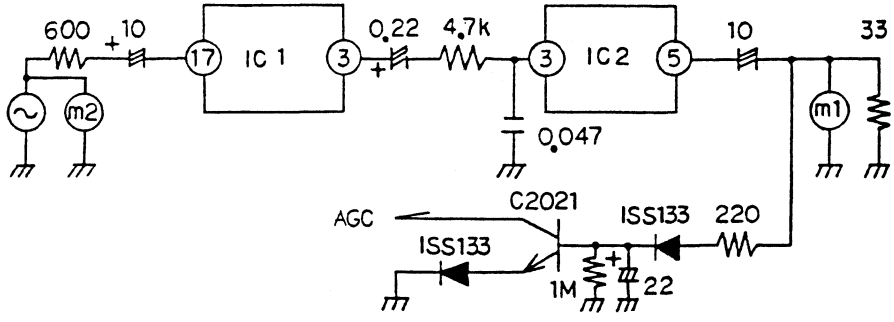
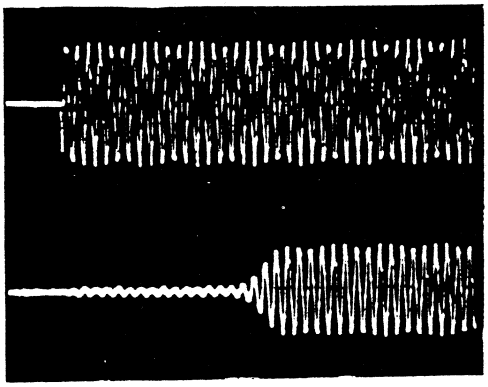


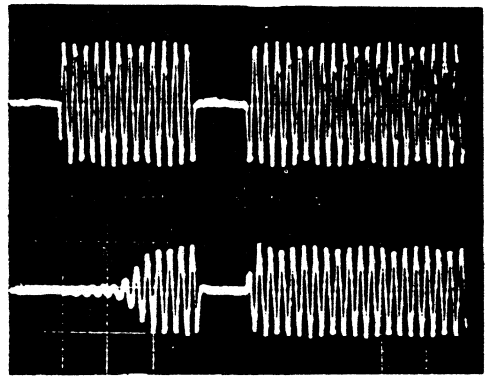
Figure 6. Measurement Diagram 1

5. Picture (1) shows the delay time of pin 17 to pin 19 (Circuit diagram used is shown in figure 7).

6. Picture (2) shows the second output waveform under the following conditions (please refer to figure 7). f = 400Hz, CH1;m1 input waveform, CH2;m3 output waveform



Picture (1)



Picture (2)

t = 10ms/div
CH1;200mV/div, coupling;AC
CH2;500mV/div, coupling;AC

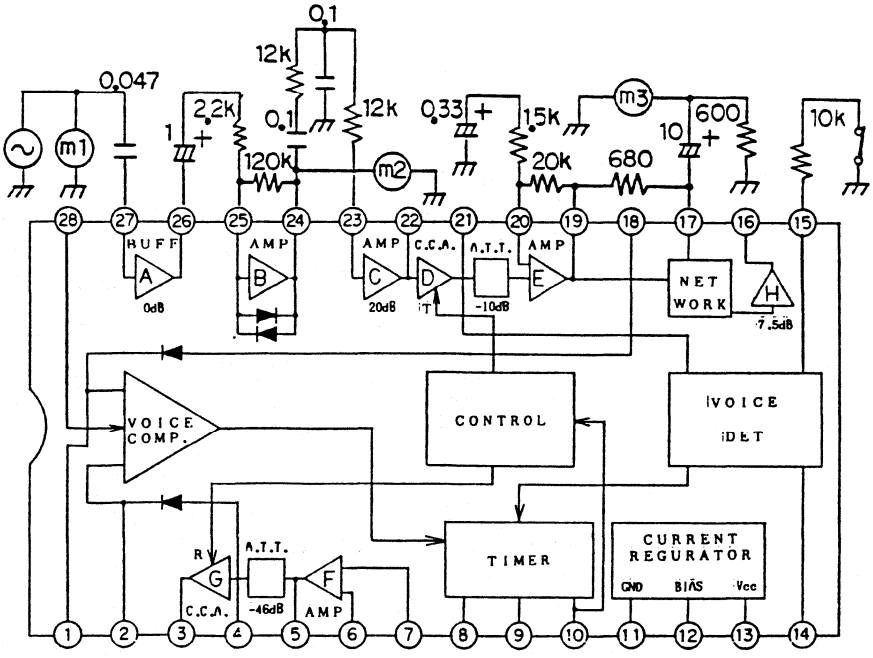
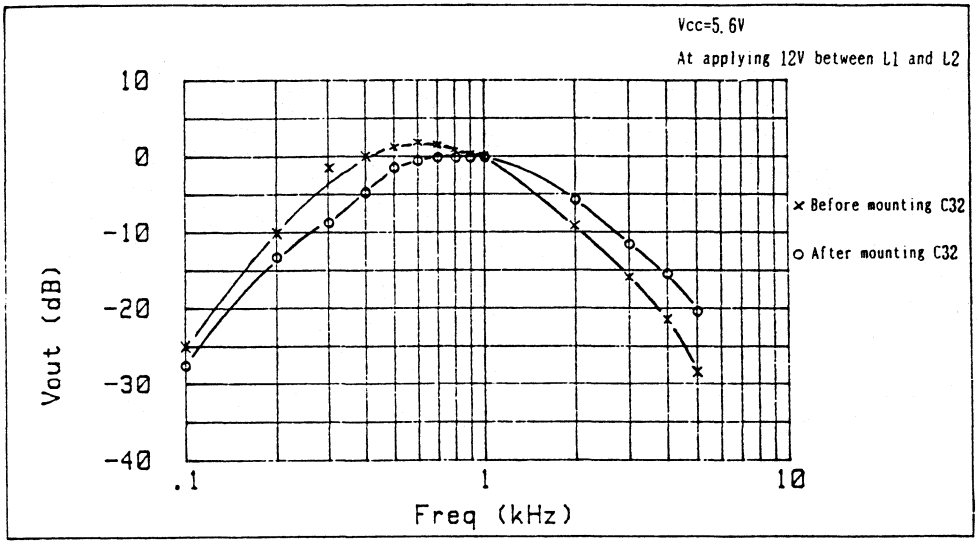


Figure 7. Measurement Circuit Diagram 2

Characteristics Data

Receiving Frequency Characteristics



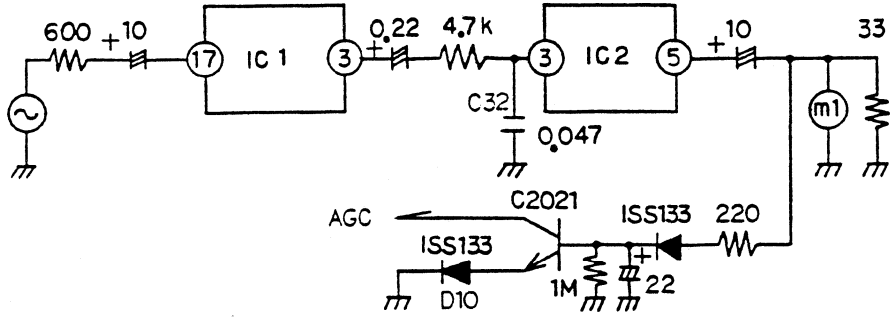
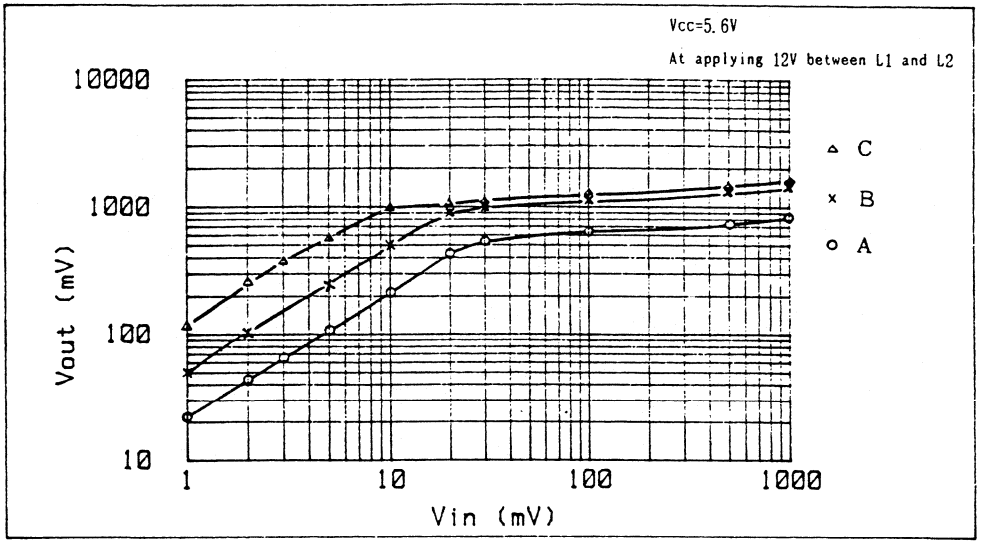
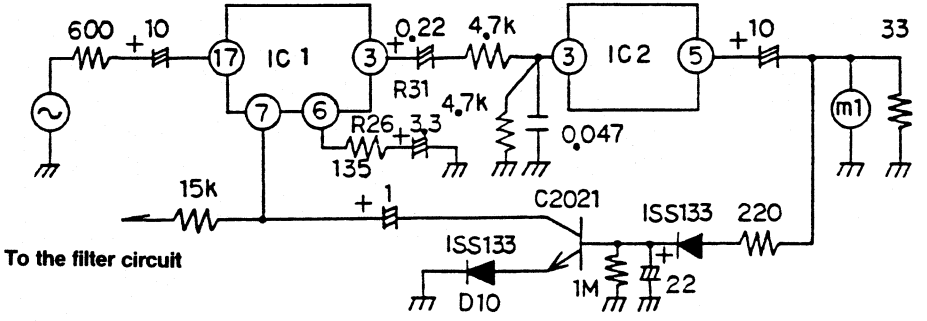


Figure 8. Measurement Circuit Diagram 3

Characteristics Data

Receiving ALC Characteristics



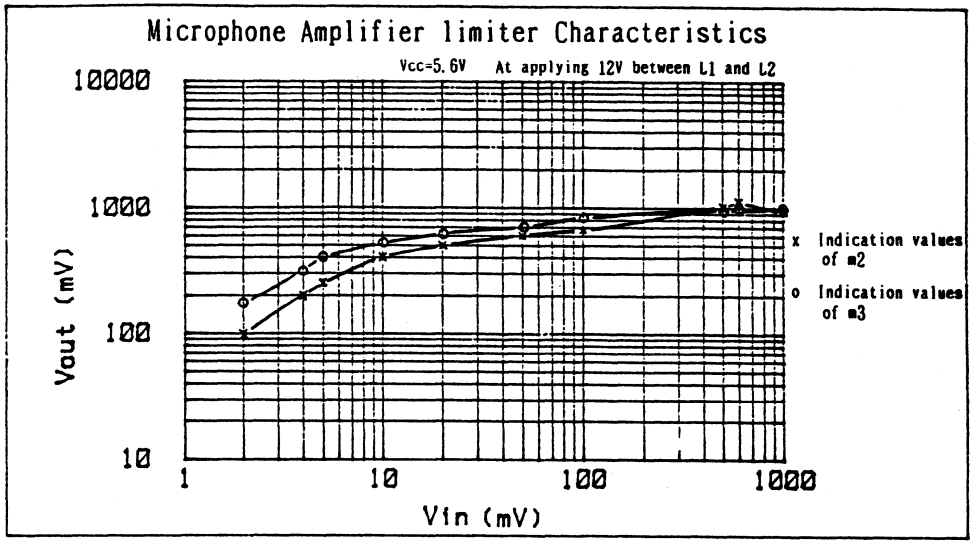


A;R20 = 2. 2k, R26 = 270Ω, R31 = 4.7Ω, D10 (no mounting)
B;R20 = 2. 2k, R26 = 135Ω, R31 (No mounting), D10 (mounting)
C;R20 = 2. 2k, R26 = 135Ω, R31 (No mounting), D10 (mounting)

Figure 9. Measurement Circuit Diagram 3

Characteristics Data

Microphone Amplifier Limiter Characteristics



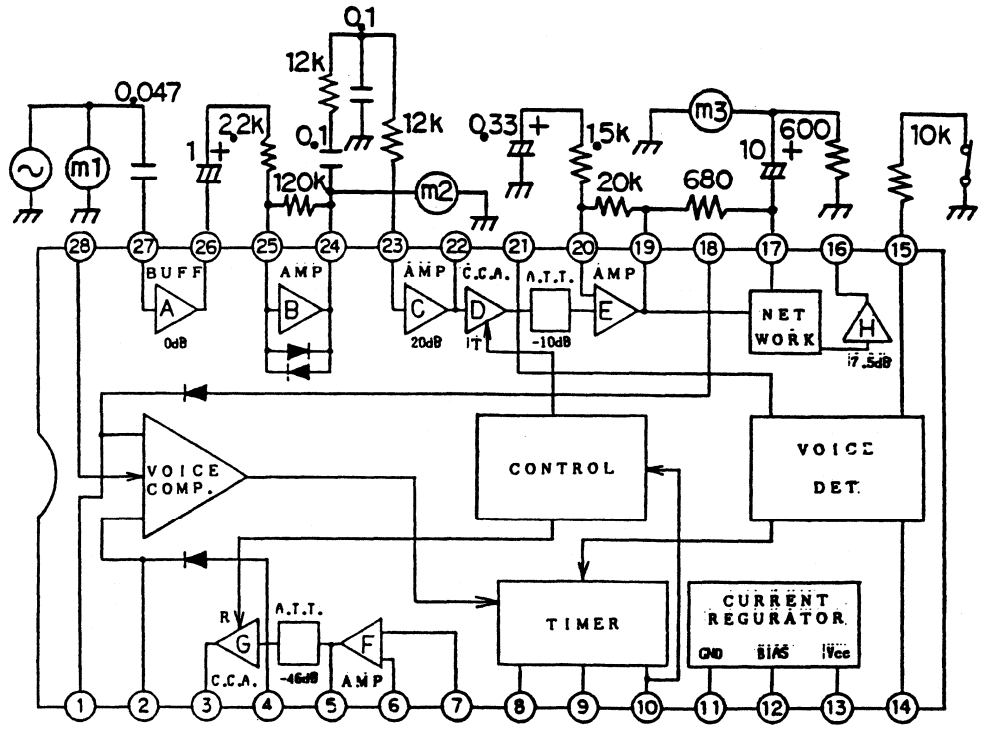
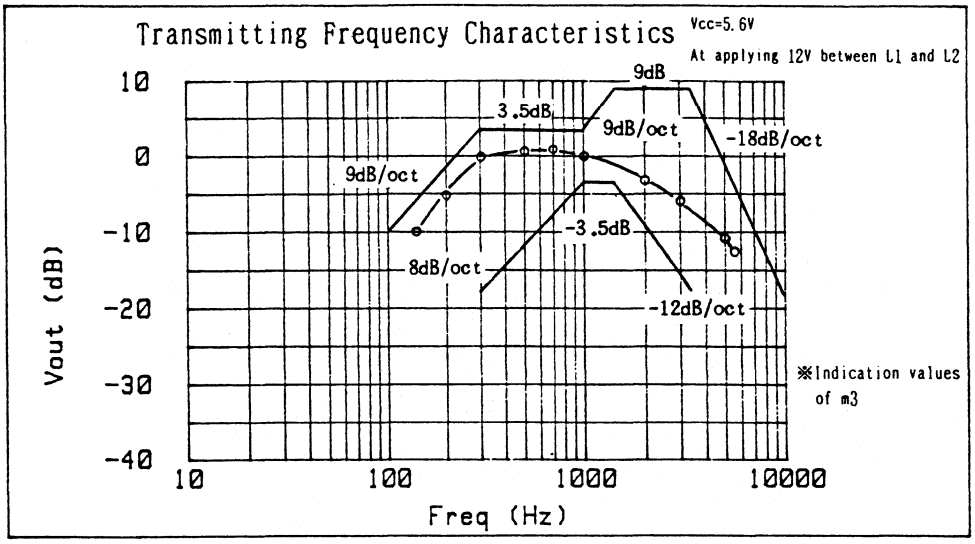


Figure 10. Measurement Circuit Diagram 4

Characteristics Data



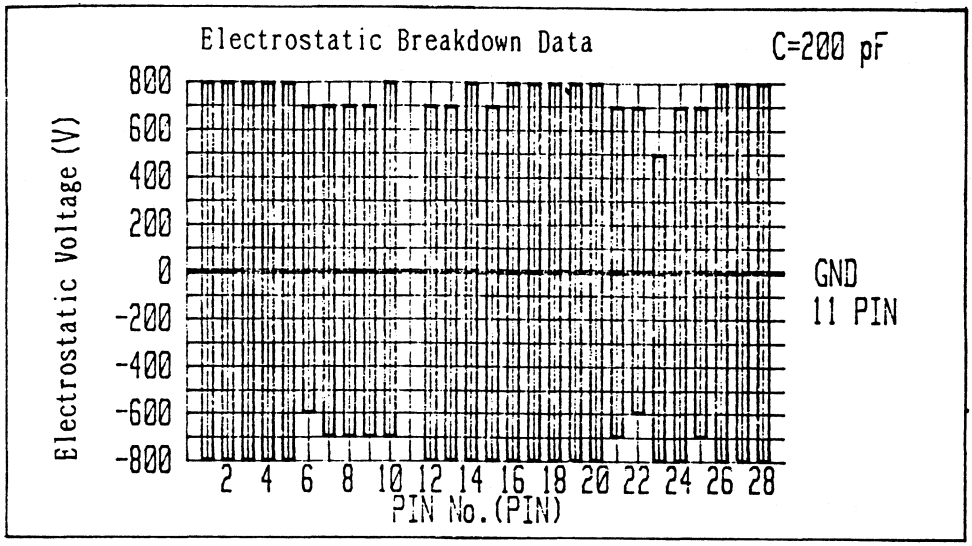


Figure 11. Electronic Breakdown (200pF)

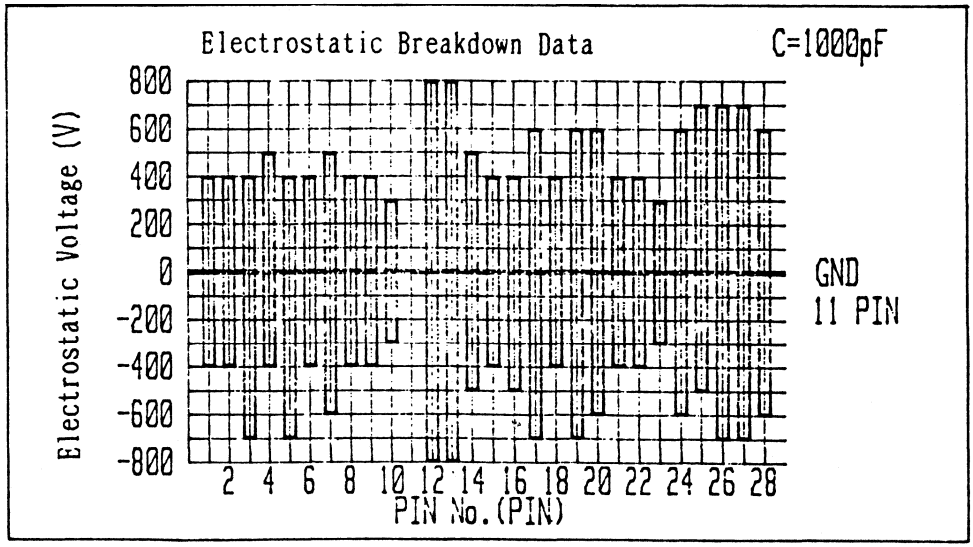


Figure 12. Electronic Breakdown (C = 1000pF)

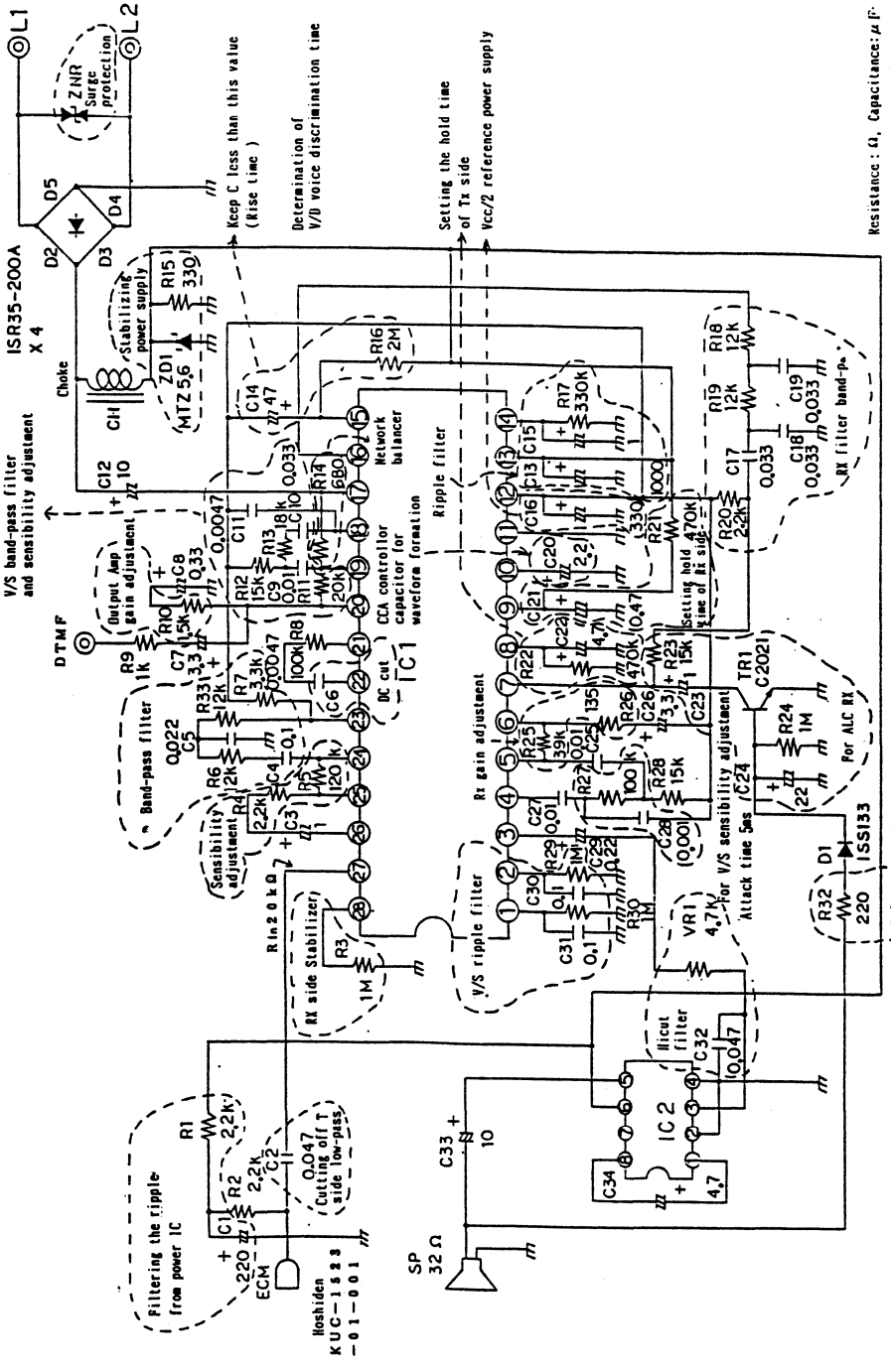


Figure 13. Typical Application Schematic

EXAR ...the analog plus™ company

Modem Product Selection Guide

Part Number	Description	Standards		Supply Voltages	Package	
		CCITT	Bell		DIP	PLCC
XR-3200	V.32 Modem	V.32 V.29 V.27ter V.22bis V.23 V.21	212A 103	±5V	Consult Factory	
XR-2900	Fax/Data Modem	V.29 V.27ter V.22bis V.22 V.21 ch 2	212A 103	+5V XR-2901 ±5V XR-2902	40 48	44 52
XR-2400	V.22bis Modem	V.22bis V.22	212A 103	+5V XR-2401 ±5V XR-2402	40 48	44 52
XR 2402A	Enhanced AFE	V.22bis V.22	212A 103	±5V	48	52
XR-2403B	MNP5 Microcontroller		MNP 2-5	+5V	40	44
XR-2405	'AT' Command Set Modem Controller		'AT' Commands	+5V	40	44
XR-2321	V.23/V.21 Modem	V.23 V.21		±5V	20	20
XR-2100	V.21 Modem	V.21		±5V	20	20
XR-2123A	Bell 212A Type Modem		212A	+5V	28	
XR-2135A	Improved Bell/CCITT Data Buffer			+5V	14	
XR-14412	Bell 103 Type Modem	V.21	103	+5V	16	
XR-2103	Bell 103 Type Modem Filter		103	+5V	20	
XR-2120	Bell 212A Type Modem Filter	V.22bis V.22	212A 103	±5V	22	
ADVANCED INFORMATION - CONSULT FACTORY FOR AVAILABILITY						
XR-2442	V.42/MNP5 Microcontroller	V.42	MNP5	+5V	40	44
XR-2442B	V.42bis/MNP5 Microcontroller	V.42bis	MNP5	+5V	40	44

Other Data Communication Product Selection Guide

Part Number	Product Description	Features	Supply Technology	Voltages	Package
UARTS					
XR-16C450	Asynchronous Receiver and Transmitter	Pin and Functional Compatible to INS8250 Includes Modem Control Signals Programmable Character Length (5,6,7,8) Odd, Even or No Parity Generation Independent Receive and Transmit Control TTL Compatible Input and Outputs	CMOS	+5V ±5%	40 Pin Plastic PLCC
XR-88C681 XR-68C681	Dual Asynchronous Receiver and Transmitter	Fully Independent Operation Buffered Receiver and Transmitter Programmable Stop Bits (1/16 Increments) Internal Bit Rate Generator Bit Rate Selection (Receiver or Transmitter Max Bit Rate (1XCLK=1MBPS, 16XCLK=125KBPS) Normal, Autoecho, Local and Remote Loopback Multifunction 16 Bit Counter/Timer Eight Maskable Interrupt Conditions Interrupt Vector Output on Acknowledge Programmable Interrupt Daisy Chain 15 I/O Pins Depending on Package Multidrop Mode (8051 Nine Bit Mode) Stand By Mode for Reduced Power	CMOS	+5V±5%	28 & 40 Pin Ceramic CLCC Plastic
XR-82C684	Quad Asynchronous Receiver and Transmitter	Quadruple Receive and Transmit Buffer Programmable Stop Bits in 1/16 Increments Pin Selectable 88 or 68 Mode Four Bit Rate Generators (33Baud Rates) External Clock Capability Normal, Autoecho, Local and Remote Loopbacks Two Multifunction 16 Bit Counter/Timer Interrupt Vector Output on Acknowledgement Programmable Interrupt Daisy Chain 16 I/O Pins Depending on Package Multidrop Mode Depending on Package Stand By Mode for Reduced Power Debounced Reset Input (20NS) Operates with 3.68 or 7.38MHZ Crystals	CMOS	+5V ±5%	44 Pin PLCC 68 Pin PLCC
FIFOs					
XR-T7201/2/3	Line Bit FIFO Memories	Organization: 512, 1024, 2048 x 9 Ultra High Speed Timing Cycle (Typ 45ns) Asynchronous and Simultaneous Read and Write Expandable by Word Width and Length Empty and Full Warning Flags Auto Retransmit Capability Pin Compatible to IDT 7201 and MK4501	CMOS	+5V ±5%	28 Pin Plastic LCC

V.32 High Speed Modem

GENERAL DESCRIPTION

The XR-3200 chip set is designed to provide the CCITT V.32, V.22bis, and V.22, as well as Bell 212A and 103 modem standard. This will provide 3200 BPS full duplex communication on the Public Switched Telephone Network (PSTN) as well as 2400, 1200 and 300 BPS. The Chip set is defined as the XR- 3201 Digital Signal Processor (DSP), the XR-3202 Analog Front End (AFE) and the XR-3203 Echo Canceller and Viterbi Algorithm DSP.

The XR-3201 will provide the digital demodulation and modulation for the CCITT V.32, including the Trellis encoding, and decoding V.22bis and Bell 212A The XR-3201 will also include the Adaptive Equalizer and Automatic Gain control for compensation of the various telephone lines to be found in the PSTN.

The XR-3202 Analog Front End (AFE) will provide both the transmit and receive analog interface for the DSPs. The XR-3202 will include a compromise band limiting filter, a DTMF guard tone generator,the analog to digital converter for the receive signal path and a Digital to analog converter for the transmit filter path as well as a Programmable gain amplifier to complete the AGC. The XR-3202 will support Call Progress Monitoring for providing the status of originating calls. The XR-3202 will provide the interface between the DPS's of the XR-3200 Chip set and any controller or processor desired.

The XR-3203 DSP will interface with the XR-3201 to provide the near and far end echo cancellation which will remove the local transmitted signal from the received signal as well as any reflections received from the far end time delayed. The carrier frequency offset correction function is performed in the XR-3203. The Viterbi Algorithm for Forward Error Correction (FEC) will be included as well.

FEATURES

3200 BPS (32 carrier states with Trellis Encoding/Decoding), 2400 BPS (QAM), 1200 BPS (PSK) and 300 BPS (FSK)
V.32 (If Trellis Encoded), V.22bis, V.22, Bell 212A, and Bell 103 Compatible
Microprocessor/Microcontroller Interface
No tuning required: (Utilizes Digital Signal Processors)
DTMF Dialing

Consult Factory for Pinout.

Low Power CMOS: 1.2 W Total for all 3 devices
Full Duplex Operation
Adaptive Equalization
Near and Far End Echo Cancellation
Carrier Frequency Offset Correction
Asynchronous or Synchronous Operation
Call Progress Monitoring Feature
Trellis Encoding and Decoding
Forward Error Correction

APPLICATIONS

Personal Workstations
Graphics Terminal
Database Computer
Home Offices
Inter-Division Data Links

SYSTEM DESCRIPTION

The XR-3200 chip set is optimized to interface with any microcontroller or Microprocessor. Since no limitation exists as to what processor or controller is used with the 3 chip set, an established proprietary compression technique or error detection technique can be included along with an established command set.

The pinout of the XR-3202 will be optimized so that the analog interface pins are grouped allowing for proper PC board layout techniques to be used. With the CPM capability of the XR-3202, the system can be quite complete in its screen update, providing information as to a dialtone, busy signal, the far end ringing or if voice is detected. This will help in qualifying the system in various countries.

For interface with a parallel bus system such as a personal computer, a UART would be added to the controller, such as the XR-16C450, or use a controller which includes a UART.

For Serial Interface the XR-3200 with a microcontroller and RS-232 interface adaptor will provide a stand alone modem.

XR-2900 Fax/Data Modem Chip Set

GENERAL DESCRIPTION

The XR-2900 is a two chip set that provides the modem data pump function for 9600 BPS half duplex / 2400 BPS full duplex applications. The XR-2900 supplies all the functions for implementing a modem for facsimile or V.29 applications. Also included is a complete V.22 bis/DATA modem.

The XR-2901 is a digital signal processor-based chip supporting primarily the modulation/demodulation function. The XR-2902 is a combination analog and digital chip. Its analog portions support the transmit and receive filters, A/D and D/A functions, transmit level attenuator, and programmable gain amplifier.

The digital portion of the XR-2902 supports the transmit clock, and async/sync converter, interface circuit between XR-2901 and host controller, and a receive clock digital phase locked loop.

Both chips utilize CMOS technology for low power operation. The XR-2901 and XR-2902 are available in 40 and 48 pin dip and 44 and 52 pin PLCC packages respectively. Power required is a single +5 volt for the XR-2901 and ±5 volts for the XR-2902.

FEATURES

V.29 / V.27ter / V.21 Ch. 2 Fax Modes
V.22bis / V.22 / 212A / 103 Data Modes
Standard Microcontroller Interface
Analog, Remote and Local Digital Test Facilities
DTMF Generator
9600 / 7200 / 4800 / 2400 / 300 BPS Half Duplex Operation
2400 / 1200 / 300 BPS Full Duplex DATA Mode
CMOS Technology
Automatic Adaptive Equalization
Guard Tone Generators
Call Progress Monitor Mode

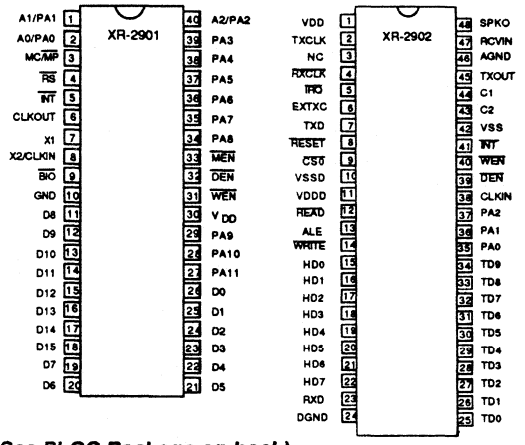
APPLICATIONS

V.29 Modems
Fax Machine Modem
PC Fax/Data Modem
Hayes Compatible Modems

ABSOLUTE MAXIMUM RATINGS

V_{DD}	-0.3 to 7V
V_{SS}	0.3 to -7V

PIN ASSIGNMENT



(See PLCC Package on back)

Input Voltage	V_{SS} -0.7V to V_{DD} +0.3V
DC Input Current	±10mA
Power Dissipation **(package limitation)**	
Plastic	1 watt
Derate above +25°C	5 mw/°C
Storage Temperature Range	-65°C to 150°C

ORDERING INFORMATION

Part No.	Package	Operating Temp.
XR-2901CP	Plastic DIP	0°C to 70°C
XR-2901CJ	PLCC	0°C to 70°C
XR-2902CP	Plastic DIP	0°C to 70°C
XR-2902CJ	PLCC	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2901/2902 chip set provides the complete data pump function for both G3 9600 BPS fax, as well as V.22bis data modes of operation. A complete micro-controller interface for popular devices such as 8031 types, is also included.

For fax modes of operation, fallback from 9600 BPS to 7200 BPS, 4800 BPS, or 2400 BPS is provided for poor line quality conditions. Data mode operation provides high compatibility with 2400 BPS, as well as 1200 BPS and 300 BPS modems.

ELECTRICAL CHARACTERISTICS: XR-2901

Test Conditions: V_{DD} =5VDC, ±5%. GND = 0VDC, T_A = 25°C, CLKIN = 20.2752MHz±0.01%, unless otherwise specified.

DC CHARACTERISTICS						
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
I_{DD}	Positive Supply Current		45	70	mA	
V_{IL}	Input Logic Low Voltage			0.8	V	All inputs except MC/$\overline{MP}$
				0.6	V	MC/$\overline{MP}$ input
V_{IH}	Input Logic High Voltage	2.0			V	All inputs except X2/CLKIN
		3.0			V	X2/CLKIN
I_I	Input Current			±20	µA	All inputs except X2/CLKIN
				±50	µA	X2/CLKIN
V_{OH}	Output Logic High Voltage	2.4	3.0		V	I_{OH} = 300 µA
V_{OL}	Output Logic Low Voltage		0.3	0.5	V	I_{OL} = 2 mA
I_{OH}	Logic High Output Current			-300	µA	
I_{OL}	Logic Low Output Current			2	mA	

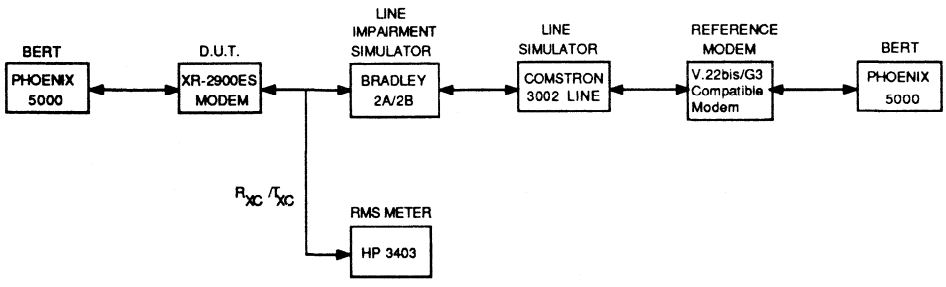
ELECTRICAL CHARACTERISTICS: XR-2902

Test Conditions: V_{DD} = 5 VDC ± 5%. V_{SS} = -5VDC ± 5%, T_A = 25°C, CLKIN = 5.0688MHz ±0.01% unless otherwise specified.

DC CHARACTERISTICS						
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
I_{DD}	Positive Supply Current		25		mA	
	PWRD Mode			5	mA	
I_{SS}	Negative Supply Current		-25		mA	
	PWRD Mode			-5	mA	
V_{IL}	Input Logic Low Voltage			0.6	V	
V_{IH}	Input Logic High Voltage	2.0			V	
I_I	Input Current			10	µA	
V_{OH}	Output Logic High Voltage	3.0			V	I_{OH} = 300µA
V_{OL}	Output Logic Low Voltage			0.4	V	I_{OL} = 2mA
I_{OH}	Logic High Output Current			-300	µA	
I_{OL}	Logic Low Output Current	1.6	2		mA	

AC CHARACTERISTICS Refer to Figure 1, (ADD = Address)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
T_{ALE}	Address Latch Enable Pulse Width	100			nS	
T_{LCM}	Minimum Latch to $\overline{READ}/\overline{WRITE}$ Control	60			nS	
T_{READ}	Read Pulse	0		160	nS	
T_{RWL}	$\overline{READ}/\overline{WRITE}$ Control to Latch	20			nS	
T_{WRITE}	Write Pulse Width	140		25000	nS	
T_{AL}	ADD/$\overline{CS}$ Set-up Before ALE	40			nS	
T_{LAH}	ADD/$\overline{CS}$ Hold After Latch	40			nS	
T_{DRD}	Valid Data From $\overline{Read}$	0		140	nS	
T_{DAR}	Data Held After $\overline{Read}$	0		200	nS	
T_{WS}	Write Data Set-up After $\overline{WRITE}$	150			nS	
T_{DHAW}	Data Hold After $\overline{WRITE}$	40			nS	
TRANSMITTER POWER LEVELS						
TX_{CAR}	Transmit Carrier Power				dBM	QAM, DPSK, FSK Modulation
$TX_{CAR\ 500}$	550 Hz Guard Tone Power	-10		-8	dBM	GTE=1, GTS=0
$TX_{CAR1800}$	1800Hz Guard Tone Power	-13		-11	dBM	GTE=1, GTS=1
SYSTEMS SPECIFICATIONS See Performance Test Set-Up						
DYNMC	Dynamic Range Min Limits	-43			dBM	
S/N V.22bis	Signal-to-Noise Ratio for V.22bis		17		dB	2400BPS operation BER ≤ 1/10 -5
S/N V.29	Signal-to-Noise Ratio for V.29 (9600BPS)		23		dB	9600BPS operation BER ≤ 1/10 -5
PCD	Carrier Detect Level		-43		dBM	
CDHYT	Carrier Detect Hysteresis		3		dB	



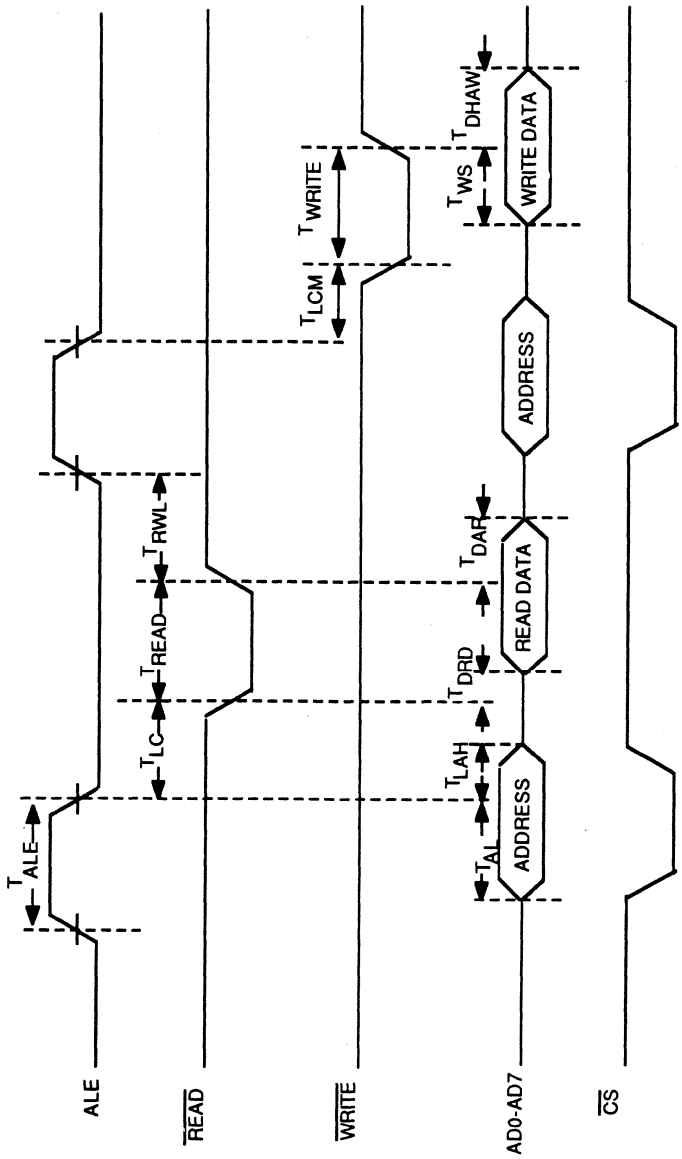
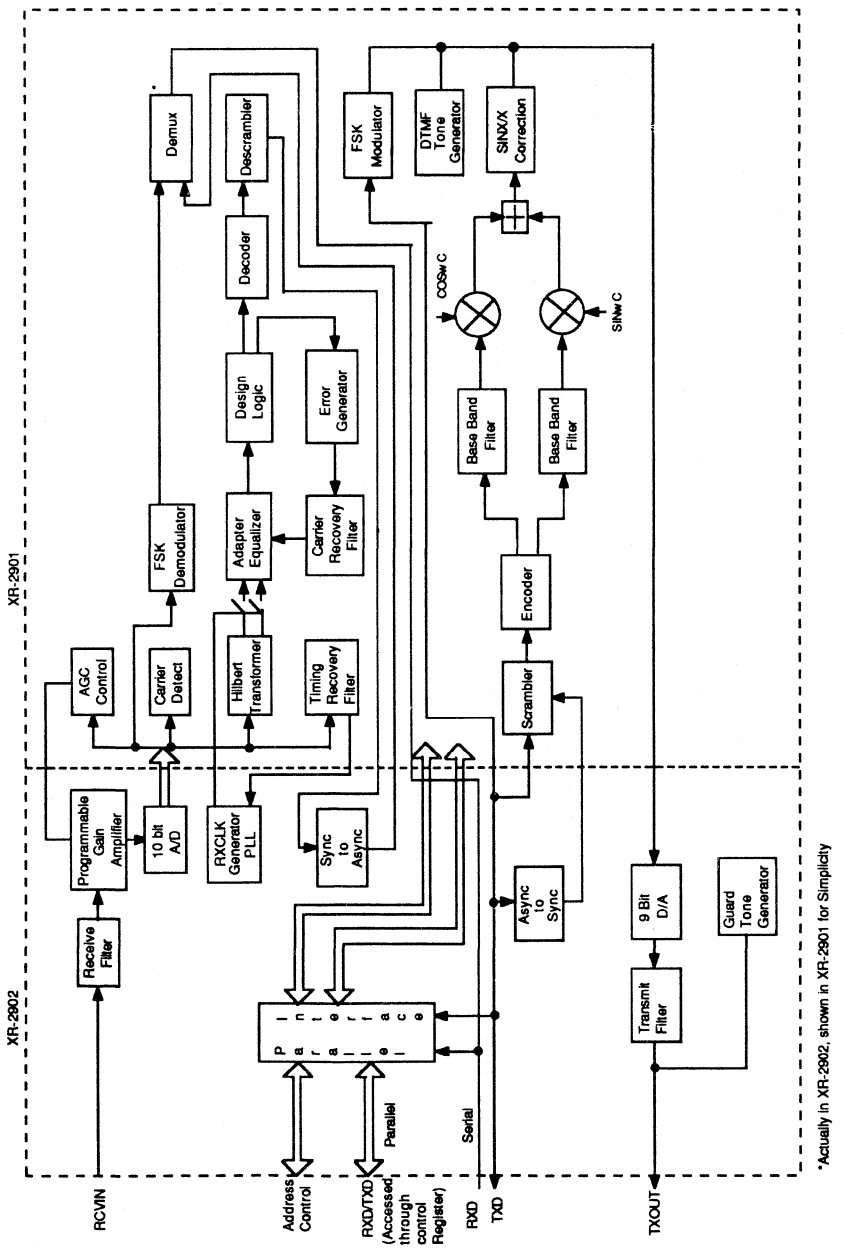


Figure 1. AC Timing Diagrams



*Actually in XR-2902, shown in XR-2901 for Simplicity

Figure 2. Equivalent Block Diagram

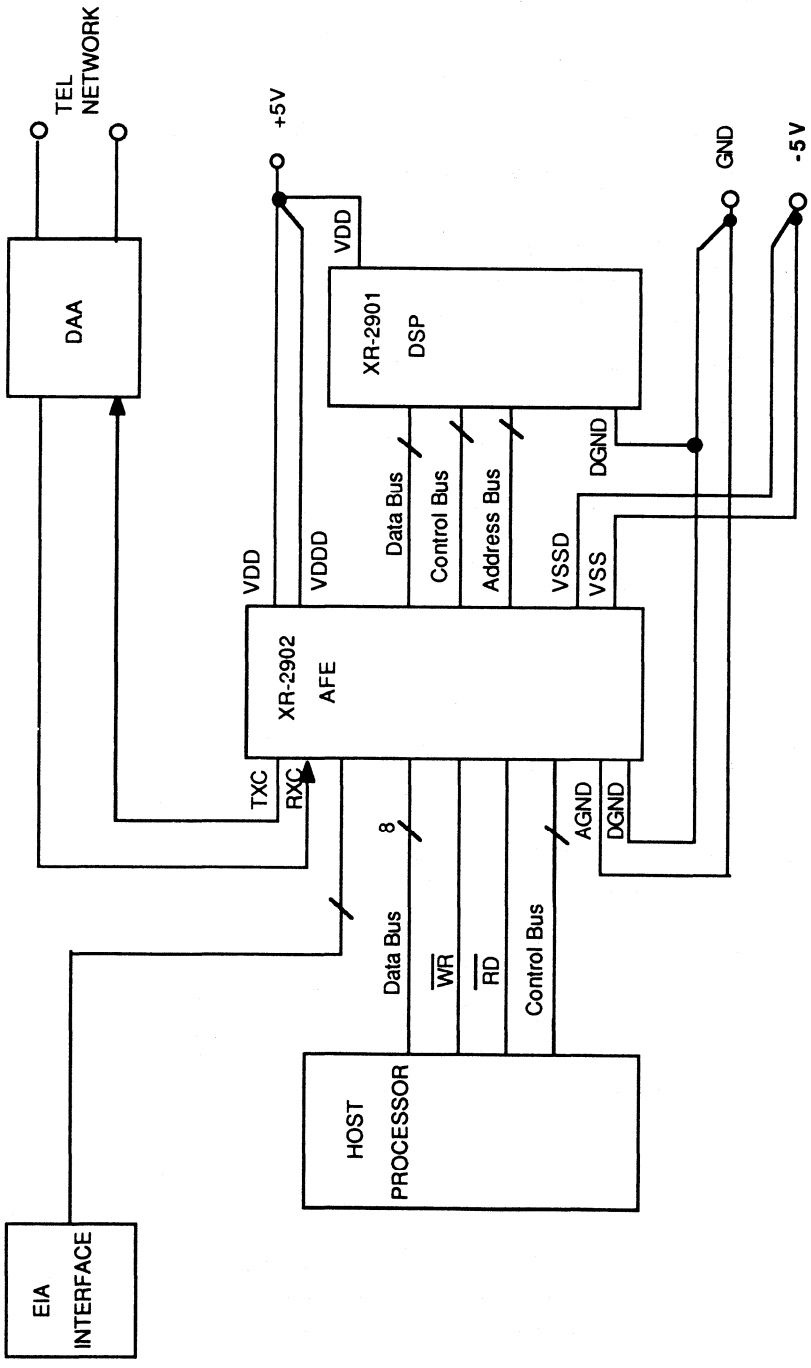


Figure 3. XR-2900 Generalized System Connection

PIN DESCRIPTIONS: XR-2901
(DIP Package Pin Numbers)

Pin #	Mnemonic	I/O	Description
1,2,40	A0/PA0-A2/PA2	I/O	Input/Output Port Address
3	MC/MP	I	Micro-controller/Micro-processor control input
4	$\overline{RS}$	I	$\overline{RESET}$, used to initialize the device.
5	$\overline{INT}$	I	External Interrupt Input
6	CLKOUT	O	Clock Output equal to 1/4 of master 20.2752MHz clock (5.0688MHz)
7	X1	O	Crystal Oscillator Output
8	X2/CLKIN	I	Crystal Oscillator Input/ External Clock Input
9	$\overline{BIO}$	I	Polling Input
10	GND	I	Ground
11-18	D8-D15	I/O	Data Lines 8-15
19-26	D7-D0	I/O	Data Lines 7-0
27-29	A11-A9	O	Address Lines 11-9
30	VDD	I	Positive Power Supply Input (+5 Volt)
31	$\overline{WEN}$	O	$\overline{Write\ Enable}$ Output
32	$\overline{DEN}$	O	$\overline{Data\ Enable}$ Output
33	$\overline{MEN}$	O	Memory Enable Output
34-39	A8-A3	O	Address Lines 8-3

PIN DESCRIPTIONS: XR-2902
(DIP Package Pin Numbers)

Pin #	Mnemonic	I/O	Description
1	VDD	I	Positive Analog Power Supply Input (+5 Volt)
2	TXCLK	O	Transmit Clock Output
3	$\overline{NC}$		
4	$\overline{RXCLK}$	O	Receive Clock Output
5	$\overline{IRQ}$	O	Interrupt Request. Open collector type output
6	EXTXC	I	External Transmit Clock Input
7	$\overline{TXD}$	I	$\overline{Serial}$ Transmit Data Input
8	$\overline{RESET}$	I	$\overline{Reset\ Input}$
9	$\overline{CS0}$	I	Chip Select Input
10	VSSD	I	Negative Digital Power Supply Input (-5 Volt)
11	VDDD	I	Positive Digital Power $\overline{Supply\ Input}$ (+5 Volt)
12	$\overline{READ}$	I	Read Enable Input
13	ALE	I	Address Latch Enable $\overline{Input}$
14	$\overline{WRITE}$	I	$\overline{Write\ Enable}$ Input
15-22	HD0-HD7	I/O	Address/Data Bus Input/Output
23	RXD	O	Serial Receive Data Output, Open Collector
24	DGND	I	Digital Ground
25-34	TD0-TD9	I/O	DSP Data Bus
35-37	PA0-PA2	I/O	Port Address Input/ Output
38	CLKIN	I	Master Clock Input. 5.0688MHz
39	$\overline{DEN}$	I	$\overline{Data\ Enable}$ Input
40	$\overline{WEN}$	I	$\overline{Write\ Enable}$ Input
41	$\overline{INT}$	O	Interrupt Output
42	VSS	I	Negative Analog Power Supply Input (-5 Volt)
43	C2	I	AGC Input
44	C1	O	AGC Output
45	TXOUT	O	Transmit Carrier Output
46	AGND	I	Analog (Signal) Ground
47	RCVIN	I	Receive Carrier Input
48	SPKO	O	Speaker Output

MODES OF OPERATION

The XR-2900 supports various modes of operation for both fax and data standards, as shown in figure 4.

FAX (Half Duplex)		DATA (Full Duplex)	
Standard	Data Rate BPS	Standard	Data Rate BPS
V.29	9600	V.22bis	2400
	7200	V.22	1200
	4800	*212A	1200
V.27ter	4800	*103	300
	2400		
**V.21 Ch.2	300		

*Bell Standard, all others are CCITT.
**Used only for signalling, not a data mode.

Figure 4. XR-2900 Fax/Data Modes

To support the various standards and speeds, as shown in Figure 5, three different modulation schemes are utilized:

- FSK Frequency Shift Keying
  -Two discrete frequencies are used to represent binary data.
- PSK Phase Shift Keying
  -Phase changes in a constant frequency carrier represent data to be transmitted.
- QAM Quadrature Amplitude Modulation
  -Both phase and amplitude modulation of a constant frequency carrier are used to represent data to be transmitted.

These different modulation schemes are necessary due to phone line bandwidth limitations. As data rates increase, each discrete change (frequency/phase/amplitude) is used to represent groups of data. The changes are known as baud, the rate of change being the modems baud rate. Figure 5 shows the relationship between the actual data transfer rate in bits per second (BPS) and baud rate. The data encoding indicates how many bits of data are represented by each baud change.

Mode	Data Rate (BPS)	Baud Rate	Data Encoding	Modulation Scheme	Carrier Frequency (Hz)	*Transmit Carrier Shaping
V.29	9600	2400	Quadbit	QAM	1700	20%
V.29	7200	2400	Tribit	QAM	1700	20%
V.29	4800	2400	Dibit	QAM	1700	20%
V.27ter	4800	1600	Tribit	PSK	1800	50%
V.27ter	2400	1200	Dibit	PSK	1800	90%
V.22bis	2400	600	Quadbit	QAM	1200/2400	75%
V.22	1200	600	Dibit	PSK	1200/2400	75%
212A	1200	600	Dibit	PSK	1200/2400	75%
103	300	300	-	FSK	1070/1270 2025/2225	-
V.21	300	300	-	FSK	1650/1850 980/1180	-

*Square root raised cosine shaping

Figure 5. Data/Baud Rate Relationships

A modems baud changes may be shown as a signal constellation, illustrating possible combinations. Figure 6 illustrates the constellations for various modes of operation.

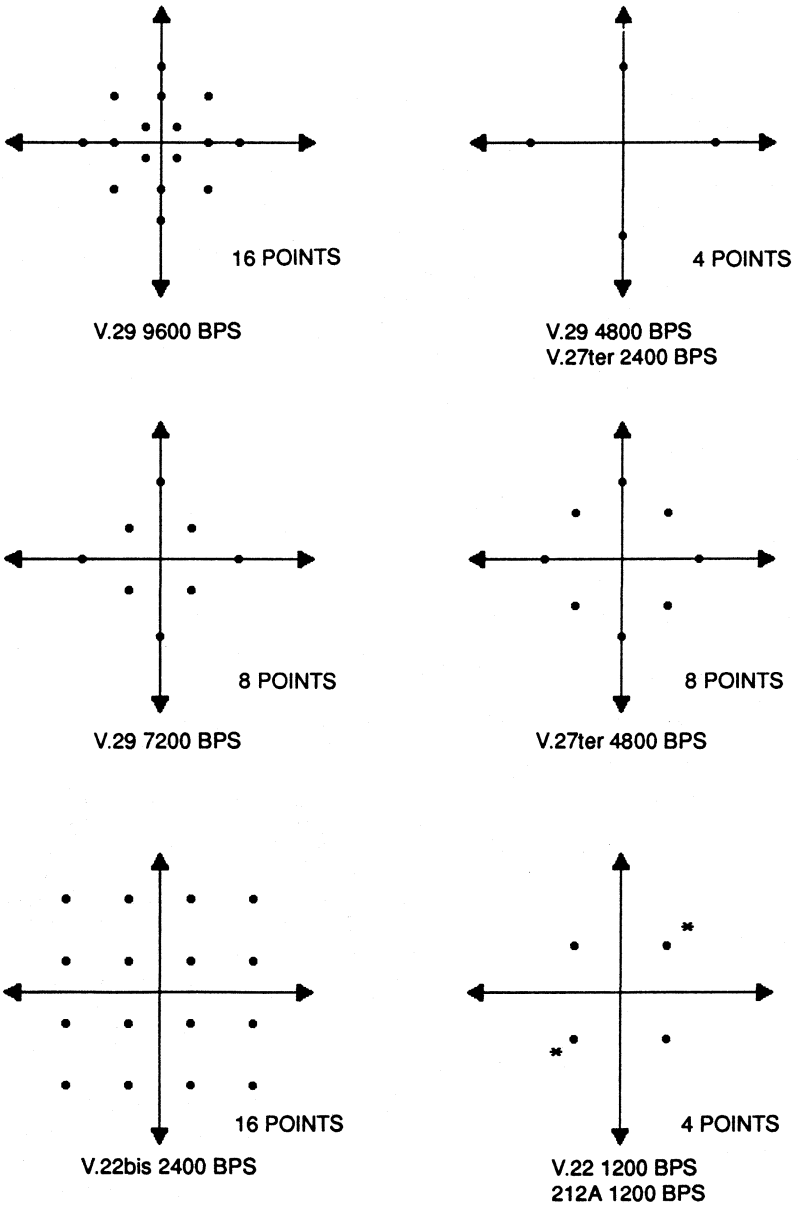


Figure 6. Constellations

(* FSK constellation will be two point)

The XR-2900 must generate several different tones to provide the necessary handshaking, guard tones, and other functions. Figure 7 lists these tones and related accuracy.

TONE (Hz)	FUNCTION	ACCURACY (%)
462	Procedure Interrupt	0.01
550/1800	Guard Tones	0.1
1100	Line Conditioning Signal/Calling Tone	0.01
2100	Answer Tone	0.1

Figure 7. Tone Generator Frequencies/Accuracy

REGISTER DESCRIPTION

The XR-2900 utilizes a set of 32, 8 bit, registers for controlling fax or data functions. A register plane is selected and than various modes/functions within that plane are programmed for fax or data operation. The MCFN bit is used for programming fax or data mode. A reset input will automatically default to the fax plane.

REGISTERS FOR FAX OPERATION - INTERFACE MEMORY (Refer to Figure 9)

REGISTER	BIT(S)	MNEMONIC	R/W	DESCRIPTION
0:0	0-7	TXRXD	R/W	**TRANSCEIVER DATA:** Provides input for transmit data or output for receive data.
0:1	0-7	RESERVED		
0:2	0-7	FREQL	R/W	**RAM DATA/FREQUENCY SELECT LOW ORDER BYTE:** Low order byte of tone generator select.
0:3	0-7	FREQM	R/W	**RAM DATA/FREQUENCY SELECT HIGH ORDER BYTE:** High order byte of tone generator select. To enable the tone transmit mode, register 4, modem configuration must be set to Hex 80. The tone generator is controlled by a 16 bit, two byte, word written to the FREQL and FREQM registers from the host processor. The control word, N, represents the desired frequency by the relationship: $N = \frac{\text{Frequency}}{0.14686}$

Below commonly used tones and the Hexadecimal numbers which are written to the FREQL/FREQM registers are listed.

Frequency (Hz)	FREQM	FREQL
462	0C	52
1100	1D	55
1650	2C	00
1850	31	55
2100	38	00

DTMF tone generation mode is selected by setting the modem configuration register to Hex 81. Tone pairs are then controlled by bits 0-3 of register 2, as shown below:

Dial Digit	Register Value D3	D2	D1	D0	Tone Pairs fLow(Hz)	fHigh(Hz)
0	0	1	1	1	941	1336
1	0	0	0	0	697	1209
2	0	1	0	0	697	1336
3	1	0	0	0	697	1477
4	0	0	0	1	770	1209
5	0	1	0	1	770	1336
6	1	0	0	1	852	1477
7	0	0	1	0	852	1209
8	0	1	1	0	852	1336
9	1	0	1	0	852	1477
*	0	0	1	1	941	1209
#	1	0	1	1	941	1477
A	1	1	0	0	697	1633
B	1	1	0	1	770	1633
C	1	1	1	0	852	1633
D	1	1	1	1	941	1633

0:4 0-7 MCFN R/W **MODEM CONFIGURATION:** This register provides mode control. This value, when the set up bit is set, controls the XR-2900 mode of operation. Figure 8 shows the mode/ register value relationship.

MCFN, Register 4, Bits 7	6	5	4	3	2	1	0	Hex	Mode
0	0	0	1	0	1	0	0	14	V.29 9600 BPS
0	0	0	1	0	0	1	0	12	V.29 7200 BPS
0	0	0	1	0	0	0	0	11	V.29 4800 BPS
0	0	0	0	1	0	1	1	0A	V.27ter 4800 BPS
0	0	0	0	1	0	0	1	09	V.27ter 2400 BPS
0	0	1	0	0	0	0	0	20	V.21 300 BPS
1	0	0	0	0	0	0	0	80	Tone Transmit
1	0	0	0	0	0	0	1	81	DTMF Tones Transmit
0	1	1	0	0	0	0	1	61	Bell 103 300 BPS
0	1	1	0	0	0	1	0	62	V.22bis/Bell 212A

Figure 8. Mode Programming

0:5 0-1 RESERVED

2 SQEXT R/W **SQUELCH EXTEND:** When set, receive carriers are gated out for 130mS after the transmitter is turned off.

3 EPT R/W **ECHO PROTECTION TONE:** When set, an unmodulated carrier (frequency determined by modem configuration register) is transmitted for 185mS, followed by 20mS of quiet, and then the normal training sequence.

	4	RESERVED		
	5	RAMW	R/W	**RAM WRITE:** This bit is set when a write routine to the diagnostic RAM is needed. This bit will be reset when a diagnostic read routine is executed.
	6	TDIS	R/W	**TRAINING DISABLED:** When set, the modem goes directly to receive mode, bypassing the training sequence. If the modem is transmitting the training sequence will not occur at the start of transmission.
	7	RTS	R/W	**REQUEST TO SEND:** When set, the transmit sequence is initiated.
0:6	0-7	RESERVED		
0:7	0-3	RESERVED		
	4	RCVG	R/W	**RECEIVE FILTER GAIN CONTROL:** An additional 10dB of receive path gain (16dB total) can be selected by resetting this bit. When set, 6dB of gain is selected for high receive level applications, such as leased line. Receive levels up to 0dBM are possible by selecting 3dB of receive path gain.
	5-7	RESERVED		
0:8	0-5	RESERVED		
	6	$\overline{\text{CTS}}$	R	**CLEAR TO SEND:** When low, indicates the XR-2900 is ready to send (transmit) data.
	7	RESERVED		
0:9	0-7	RESERVED		
0:A	0-3	RESERVED		
	4	SPC	R/W	**SPEAKER CONTROL:** When set, the speaker output is enabled.
	5	VOL 1	R/W	**VOLUME CONTROL 1:** See Volume Control 2 for description.
	6	VOL 2	R/W	**VOLUME CONTROL 2:** These two bits, Vol 1/Vol 2, control the signal amplitude at the speaker output, as shown below:

Vol 1	Vol 2	Relative Level
0	0	Low
0	1	Low
1	0	Medium
1	1	Maximum

0:B	0-7	RESERVED		
0:C	0-7	RESERVED		
0:D	0-3	TXL 1-4	R/W	**TRANSMIT LEVEL CONTROL:** These four bits control the transmit carrier level, as shown below. The values listed are attenuations from nominal transmitter output.

TXL4	TXL3	TXL2	TXL1	TXOUT Attenuation (dB)
0	0	0	0	-15
0	0	0	1	-14
0	0	1	0	-13
0	0	1	1	-12
0	1	0	0	-11
0	1	0	1	-10
0	1	1	0	-9

				0	1	1	1	-8
				1	0	0	0	-7
				1	0	0	1	-6
				1	0	1	0	-5
				1	0	1	1	-4
				1	1	0	0	-3
				1	1	0	1	-2
				1	1	1	0	-1
				1	1	1	1	-0

	4	RDEQ	R/W	**RECEIVER DELAY EQUALIZER ENABLE:** When set, a delay equalizer is enabled for compensating the telephone line characteristics.
	5	CAB 1	R/W	**CABLE EQUALIZER CONTROL 1:** See CAB 2.
	6	CAB 2	R/W	**CABLE EQUALIZER CONTROL 2:** CAB 1/CAB 2 control the cable equalizer amplitude compensation, as shown below

CAB 1	CAB2	Length
0	0	0.0 Meters
0	1	1.8 Km
1	0	3.6 Km
1	1	7.2 Km

	7	RESERVED		
0:E	0	MDAO	R	**MODEM DATA AVAILABLE:** When high, data is ready for host processor to read or write data to register 0, during parallel data mode.
	1	RESERVED		
	2	IEO	R/W	**INTERRUPT ENABLE:** When set, the IRQ output will be set low, assuming MDA0 bit is set to a high.
	3	SETUP	R/W	**SETUP:** This bit must be set whenever a change is made to register 4. After configuration change is complete, this bit will be reset automatically.
	4-6	RESERVED		
	7	IAO	R	**INTERRUPT ACTIVE:** This bit will be set when IRQ is active
0:F	0-6	RMAA	W	**RAM ACCESS ARRANGEMENT:** This register is used to read various diagnostic functions from the XR-2901. The process of reading the functions is described in data plane, register 0:F (Bits 0-6).
	7	PDM	R/W	**PARALLEL DATA MODE:** When set, the modem is put in parallel data mode and the diagnostic RAM cannot be read.
1:0	0-7	RESERVED		
1:1	0-7	RESERVED		
1:2	0-7	RESERVED		
1:3	0-7	RESERVED		
1:4	0-1	RESERVED		
	2	P2DET	R	**P2 DETECTION:** This bit, when low, indicates that the P2 pattern has been received.
	3-7	RESERVED		
1:5	0-5	RESERVED		
	6	FED		
	7	RESERVED		
1:6	0-7	RESERVED		

1:7	0	$\overline{\text{CDET}}$	R	**CARRIER DETECT:** When low, indicates the presence of a received signal within the passband of the received filters. $\overline{\text{CDET}}$ will remain high during a training sequence. $\overline{\text{CDET}}$ will go low at the start of data state and return to a one at the end of the receive signal.
	1-5	RESERVED		
	6	$\overline{\text{PNDET}}$	R	**PN DETECT:** When low, the PN sequence has been detected during the training sequence.
	7	RESERVED		
1:8	0-7	RESERVED		
1:9	0-7	RESERVED		
1:A	0-7	RESERVED		
1:B	0-4	RESERVED		
	5	FR1	R	**FREQUENCY 1 DETECT:** When high, a 2100 Hz tone has been detected. This register is only active if V.21 mode has been set.
	6	FR2	R	**FREQUENCY 2 DETECT:** When high, a 1100 Hz tone has been detected.
	7	FR3	R	**FREQUENCY 3 DETECT:** When high, a 462 Hz tone has been detected.
1:C	0	RESERVED		
	1	$\overline{\text{FRT}}$	R/W	**FREEZE TAPWEIGHTS:** This bit, when reset, freezes the last positions of the tapweights of the adaptive equalizer. This bit can be used to compensate for a momentary loss of receive carrier in fax reception.
	2-7	RESERVED		
1:D	0-7	RESERVED		
1:E	0-7	RESERVED		
1:F	0-7	RESERVED		

REGISTERS FOR DATA MODE OPERATION - Modem Register Plane. Refer to Figure 10. NOTE 1: See fax register for description.

REGISTER	BIT(S)	MNEMONIC	R/W	DESCRIPTION
0:0	0-7	PRXD	R	**PARALLEL RECEIVER DATA:** In parallel mode, the received data is read from this register, when PDM bit (register 0F, Bit 7) is set.
0:1	0-7	PTXD	W	**PARALLEL TRANSMIT DATA:** Data to be transmitted, in parallel mode is written to this register, when PDM bit (register0 F, Bit 7) is set.
0:1	0	STXD	W	**SERIAL TRANSMIT DATA:** When the PDM bit is set and the SPDM bit is set, this bit can be used to send data in serial/parallel mode. This serial/parallel mode is data input into a parallel register, but bit by bit (one bit at a time).
0:2	0-7	FREQL	R/W	NOTE 1
0:3	0-7	FREQM	R/W	NOTE 1
0:4	0-7	MCFN	R/W	NOTE 1
0:5	0	REQ	R/W	**RESET EQUALIZER:** The setting of this bit resets the adaptive equalizer of the XR-2901.
	1	UNDEFINED		

	2	SCR	R/W	**SCRAMBLER ENABLE:** When this bit is set, the scrambler for the transmitter and descrambler for the receiver are enabled.
	3	RXSP	R/W	**RECEIVER SPEED SELECT:** This bit, when set, selects 2400 BPS and when low, 1200 BPS modes of operation.
	4	TXSP	R/W	**TRANSMITTER SPEED SELECT:** This bit, when set selects 2400 BPS and when low, 1200 BPS modes of operation.
	5	UNDEFINED		
	6	UNDEFINED		
	7	RTS	R/W	**REQUEST TO SEND:** This bit controls the XR-2900 transmitter. When set, the transmitter is on. A low level stops the transmitter carrier.
0:6	0-7	UNDEFINED		
0:7	0	UNDEFINED		
	1	MOD	W	**MODE SELECT:** When set, answer mode and when reset, originate modes of operation are selected.
	2	GTE	R/W	**GUARD TONE ENABLE:** This bit, when set, enables either a 550 Hz or 1800 Hz tone to be transmitted.
	3	GTS	R/W	**GUARD TONE SELECT:** This bit, when set, selects an 1800 Hz tone, and when reset, a 550 Hz tone.
	4	RCVG	R/W	**RECEIVE FILTER GAIN CONTROL:** When set, 16 dB of receive gain is selected. Resetting this bit lowers the gain to 6 dB.
	5	PWRD	R/W	**POWER DOWN:** Setting this bit puts the XR-2902 into a low power mode. (See Electrical Characteristics for supply current values.)
	6	CPM	R/W	**CALL PROGRESS MONITORING:** When set, call progress mode of operation will be selected.
	7	ALB	R/W	**ANALOG LOOP BACK:** This bit, when set, enables the analog loop back mode of the XR-2900. The transmitted signal bypasses the receive filter and is applied to the demodulator input. Originate/Answer modes are selected by the Mode bit.
0:8	0	RXD	R	**RECEIVE DATA OUTPUT:** This bit represents the receive data in a serial format. The data at this point has not yet passed through the data buffer (sync-to-async converter.)
	1	URXD	R	**UNSCRAMBLED RECEIVE DATA OUTPUT:** The data available at this location is directly from the demodulator output, prior to the demodulator. This signal is used during handshaking and DLB initiation.
	2	CD	R	**CARRIER DETECT:** This bit is the output of the energy detect circuit, and is the logical inversion of $\overline{FED}$.
	3	SGQ	R	**SIGNAL QUALITY:** When high, this bit indicates a degradation of signal quality and increased chance for errors. Less severe signal degradations will cause this output to 'chatter', and an averaging may be necessary.
	4	S1D	R	**S1 SIGNAL DETECT:** This bit, when high, indicates the detection of an S1 pattern.
	5	DOT	R	**DOTTING PATTERN DETECTORS:** A high at this bit indicates the reception of a dotting pattern, as used in a request for remote digital loopback.

	6	UNDEFINED		
	7	UNDEFINED		
0:9	0	CRXD	R/W	**CLAMP RECEIVE DATA:** When set, the receive data output will be clamped to a high level.
	1	SPDM	R/W	**SERIAL DATA MODE SELECT:** When set, the serial/parallel data mode is selected. See STXD (Register 1, Bit 0) for mode description.
	2	SLAVE	R/W	**SLAVE MODE:** When this bit is set, the transmit clock is internally connected to the receive clock.
	3	ETE	R/W	**EXTERNAL TRANSMIT CLOCK ENABLE:** This bit, when set, allows an external transmit clock to be applied to pin 6 of the XR-2902.
	4	DLB	R/W	**DIGITAL LOOP BACK:** When enabled, set to a high, the transmit clock will track the receive clock, and transmit data will be tied to the receive data. This bit is used to enable remote digital loopback after a receive signal dotting pattern is detected.
	5	NTD	R/W	**NORMAL TRANSMIT DATA:** When this bit is set, the transmit path is from the STXD, transmit byte register, or TXD pin. When reset, the special transmit pattern bits control the data to be transmitted.
	6	STC1	R/W	**SPECIAL TRANSMIT PATTERN CONTROL 1:** See STC2
	7	STC2	R/W	**SPECIAL TRANSMIT PATTERN CONTROL 2:** STC1/STC2 control the generation of special transmit patterns, as described below:

STC2	STC1	PATTERN
0	0	Space
1	0	Mark
1	1	Dotting
1	0	300Hz for S1 Pattern

0:A	0	DBEN	R/W	**DATA BUFFER ENABLE:** This bit, when set, enables the async-to-sync and sync-to-async converters.
	1	DSPD	R/W	**DATA BUFFER OVERSPEED SELECT:** This bit, when set, extends the allowable asynchronous data rate from its normal +1% / -2.5% to +2.3% / -2.5%.
	2-3	BC1/BC2	R/W	**BIT PER CHARACTER SELECTION:** The asynchronous character lengths are controlled according to the following table:

BC2	BC1	Character Length (1 start+data+1 stop)
0	0	8 Bits
0	1	9 Bits
1	0	10 Bits
1	1	11 Bits

	4	SPC	R/W	**SPEAKER CONTROL:** This bit, when set, enables the speaker output.
	5,6	VOL1, VOL2	R/W	**VOLUME CONTROL 1/2:** NOTE 1
	7	RESERVED	R/W	**SPECIAL EXAR TEST BIT.** This bit must be set to low for normal operation.
0:B	0-7	RESERVED		
0:C	0-7	RESERVED		
0:D	0-3	TXL1-4	R/W	**TRANSMIT LEVEL CONTROLS:** NOTE 1
	4-7	RESERVED		
0:E	0	MDA0	R	**MODEM DATA AVAILABLE:** NOTE 1
	1	MDAT	R	**TRANSMIT MODEM DATA AVAILABLE:** This bit, when set indicates transmit data can be applied to the transmit register.
	2	IEO	R/W	**RECEIVE INTERRUPT ENABLE:** This bit will go low when the receive data buffer is full.
	3	SETUP	R/W	**SETUP:** This bit must be set whenever a change is made to register 4. When the change is complete, the bit will be reset.
	4	IET	R/W	**INTERRUPT ENABLE:** This bit will be high when the transmit buffer is empty.
	5-6	RESERVED	R/W	
	7	IAO	R	**INTERRUPT ACTIVE:** This output indicates when the XR-2902 has requested an interrupt.
0:F	0-6	RMAA	R/W	**RAM ACCESS ADDRESS:** These bits select the RAM address for the XR-2901 for diagnostic purposes. Figure 10 contains the function information. The process of reading these locations is as follows: •Load desired RAM location into location 0F, Bits 0-6. •Read Register 0; this resets register 0E, Bit 0. •When Register 0E, Bit 0, returns to a Logic 1, data is present at Register 0:3 as described in Figure 10.
	7	PDM	R/W	**PARALLEL MODE:** This bit, when set, allows TXD/RXD to go through parallel bus.
1:0-1:4	0-7	RESERVED		
1:5	0-5	RESERVED		
	6	$\overline{\text{FED}}$	R	**FAST ENERGY DETECT:** NOTE 1
	7	RESERVED		
1:6-1:A	0-7	RESERVED		
1:B	0-4	RESERVED		
	5, 6, 7	FR1, FR2, FR3	R	**FREQUENCY 1, 2, 3 DETECT:** NOTE 1
1:C	0-7	RESERVED		
1:D	0	RESERVED		
	1	$\overline{\text{FRT}}$	R/W	**FREEZE EQUALIZER TAPS:** When set, the equalizer taps are fixed at their last value. This is used to compensate for a momentary loss of receive carrier.
	2-7	RESERVED		
1:E-1:F	0-7	RESERVED		

Location Bit	7	6	5	4	3	2	1	0
1 F								
1 E								
1 D							$\overline{\text{FRT}}$	
1 C								
1 B	FR3	FR2	FR1					
1 A								
1 9								
1 8								
1 7		$\overline{\text{PNDET}}$						$\overline{\text{CDET}}$
1 6								
1 5		$\overline{\text{FED}}$						
1 4						$\overline{\text{P2DET}}$		
1 3								
1 2								
1 1								
1 0								
0 F	PDM		RAM Access Address					
0 E	IA0				SETUP	IE0		MDA0
0 D		CAB2	CAB1	RDEQ	TXL4	TXL3	TXL2	TXL1
0 C								
0 B								
0 A		VOL2	VOL1	SPC				
0 9								
0 8		$\overline{\text{CTS}}$						
0 7				RCVG				
0 6								
0 5	RTS	TDIS	RAMW		EPT	SQEXT		
0 4			Modem Configuration					
0 3			RAM Data XSM; FREQM					
0 2			RAM Data XSL; FREQL					
0 1								
0 0			Transceiver PTXRXD					

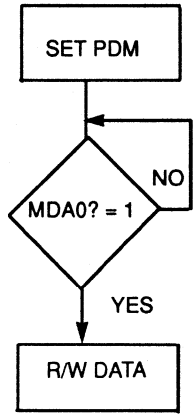
Figure 9. XR-2900 Control Register Plane for Fax Operation

Location Bit	7	6	5	4	3	2	1	0
1 F								
1 E								
1 D							$\overline{\text{FRT}}$	
1 C								
1 B	FR3	FR2	FR1					
1 A								
1 9								
1 8								
1 7								
1 6								
1 5		$\overline{\text{FED}}$						
1 4								
1 3								
1 2								
1 1								
1 0								
0 F	PDM		RAM Access Address					
0 E	IA0			IET	SETUP	IE0	MDAT	MDA0
0 D	GTF				TXL4	TXL3	TXL2	TXL1
0 C								
0 B								
0 A	TEST	VOL2	VOL1	SPC	BC2	BC1	DSPD	DBEN
0 9	STC2	STC1	NTD	DLB	ETE	SLAVE	SPDM	CRXD
0 8			DOT	S1D	SGQ	CD	URXD	RXD
0 7	ALB	CPM	PWRD	RCVG	GTS	GTE	MOD	- -
0 6								
0 5	RTS			TXSP	RXSP	SCR		REQ
0 4			Modem Configuration					
0 3			RAM Data XSM; FREQM					
0 2			RAM Data XSL; FREQL					
0 1			Parallel Transmit Data PTXD					STXD
0 0			Parallel Receiving Data PRXD					

Figure 10. XR-2900 Control Register Plane for Data Mode

Read / Write Parallel Data Transfer to the XR-2900 -Transferring data to and from the XR-2900 is done differently, depending whether polling or interrupt driven.

POLLING



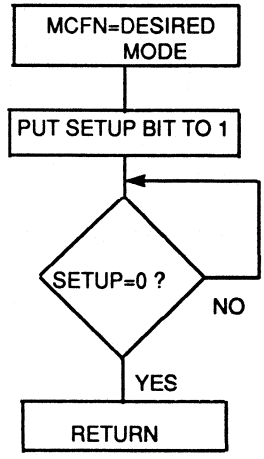
REG O:F (HEX15) BIT 7

INTERRUPT

FULL DUPLEX
1. Set PDM
2. Set IE0 IET to Enable Interrupt
3. Depending on Transmit or Receive Data
   MDA0 - For RXD
   MDAT - For TXD
   Reset INT to low
4. When Data is ready the interrupt will go low

HALF DUPLEX
1. Set PDM Mode
2. Set IEQ to Enable Interrupt
3. When Data is ready, the interrupt will go low

XR-2900 Mode Setting - The following flow diagram describes the XR-2900 mode setting procedure.



REG 0:E (HEX 14) BIT 3

POWER ON RESET

The XR-2900 contains an automatic internal hardware power-on reset/initialization routine. On power up the chip set is configured for V.29/9600 BPS fax operation. The following lists the functions within the fax mode set by the reset routine, with respective registers/values.

Mode/Function	(FAX Plane) Control Register	Register Value (HEX)
•V.29 / 9600 BPS	04	14
•Serial Data Transfer		
•Training Enabled		
•Echo Protector Tone Enabled	05	08
•No Extended Squelch		
•High Receive Gain Selected (16 dB)	07	00
•Unused Register	09	00
•Speaker Output is Disabled	0A	00
•Set Transmit Carrier Amplitude and Disable Receiver Cable Equalizer	0D	00

Call Progress Mode Operation

Call Progress Mode (CPM) is a mode of operation (Data Mode) which allows the modem to detect various telephone signals. These signals are:

- Busy Tone
- Dial Tone
- Ring Back
- Answer Tone (Modem)

As the telephone signals fall in a different frequency band than the modem carriers, filtering requirements must change. To achieve this, the receive filter is changed for moniroting the various tones, as shown in table 1. In each case the carrier detect (CD) bit, bit2/Register 0:8 in data plane, is monitored. Sensing not only high or low, but also the duration and repetition rate of the CD active state is required.

CPM	MOD	CD
1	0	Receive High Band Monitor Answer Tone
1	1	Receive Low Band: Monitor Dial Tone, Busy Tone and Ring Back Signal.
0	0	Normal High Band Energy Detect
0	1	Normal Low Band Energy Detect

CPM: REG 0:7, Bit 6
MOD: REG 0:7, Bit 1
CD: REG 0:8, Bit 2

Table 1. CD Frequency Band Assignments

APPLICATIONS INFORMATION

The XR-2900 Fax/Data chip set provides the complete data pump function for implementing a modem supporting 9600 BPS G3 facsimile operation, as well as full duplex data capability at 2400 BPS, 1200 BPS, and 300 BPS. The generalized system connection, figure 3, illustrates the remaining functions supporting the XR-2900 to complete the modem, also described here:

- •Data Pump - XR-2900/XR-2901 chip set
  - Modulation/demodulation for Fax/ Data Modes
  - Signals for Handshaking/Establishing Connections/Telephone Signals (call progress, dialing)
  - Test Modes
  - Interface for Host Controller
- •Telephone Line Interface (DAA)
  - Line Interface Functions Required by FCC
    - DC Isolation
    - High Voltage Protection
    - Out of Band Frequency Suppression
  - Hybrid Function for Separating Transmit and Receive Signals
- •DTE (Data Terminal Equipment) Interface
  - Serial (Stand-alone type modem)
    - EIA Level Translation (RS-232C)
  - Parallel (Internal Type Modem)
    - UART (Serial to Parallel Conversion)
- •Host Controller
  - Timing/Control for Handshaking
  - Command (Hayes®, MNP®, Fax Control) Interpretation
  - ROM (EPROM) for Commands
  - RAM (MNP, Data Mode)

Figure 12, illustrates a practical example of a stand-alone Fax/Data modem. For this example a 8031 type microprocessor provides the XR-2901/XR-2902 chip set its need control. An external EPROM contains the control commands, such as Hayes commands for data mode. Exar will also offer a masked ROM controller, supporting MNP 5 operation during data mode (pin-to-pin replacement for generic 8031 controller).

LAYOUT CONSIDERATIONS

The XR-2900 provides the heart of the modem system, which processes signals from very low level analog to logic level digital. This mix of sensitive analog with noise causing digital signals calls for some special care in system layout.

Referring to figure 3, the generalized connection, the most critical signals path is that of the transmit (TXC) and receive (RXC) signals. They are passed from the telephone network through the line interface circuit (DAA) and on to the XR-2902 AFE. This path should be kept as short as possible and away from the digital circuitry, microcontroller and its memory components, and XR-2901 DSP. Figure 11 illustrates this concept.

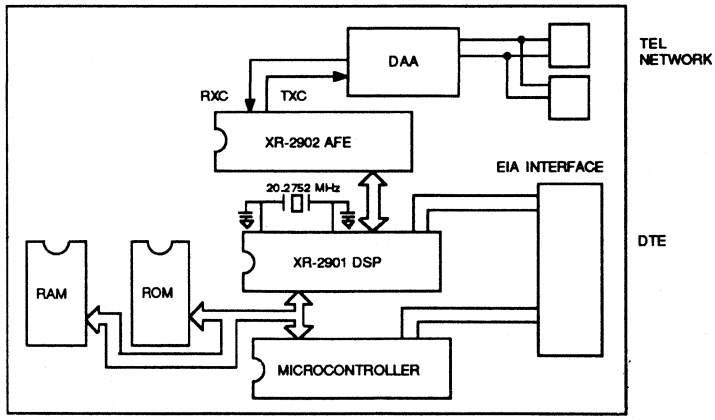


Figure 11. XR-2900 System Layout

CRYSTAL OSCILLATOR

The XR-2900 master clock, typically generated from a 20.2752 MHz crystal is another area requiring special attention. As with the analog and digital signal considerations, the crystal should be kept away from the TXC/RXC signal paths.

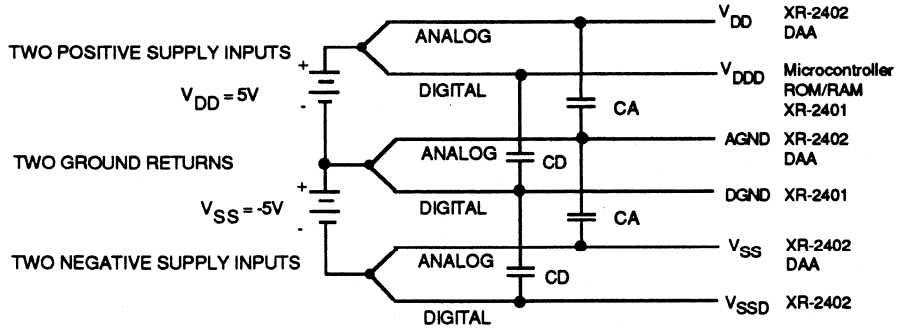
The accuracy and stability of the clock circuit are also extremely important. Per system specifications, it must have an accuracy of less than ±0.01 percent from nominal. The type of oscillator circuitry within the XR-2901 requires a parallel resonant type crystal. Typical external load capacitance (which can vary for different crystals) is 17pF. The capacitors should be returned to digital ground. The lines from the crystal to the XR-2901 should be kept short to minimize stray capacitance.

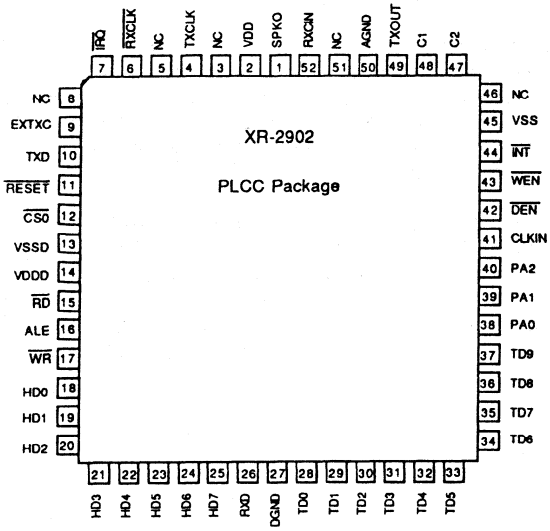
POWER / GROUND PRECAUTIONS

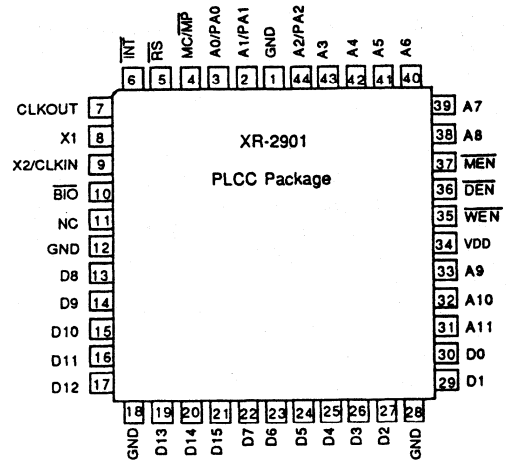
To help keep analog and digital circuitry separated, the system should incorporate independent paths for the power and signal supplies and gounds. As illustrated below, the digital and analog lines should be kept separated up to the power supply where they are single point connected.

Supply bypassing is important with both VDD (VDDD) and VSS (VSSD), each having several bypassing capacitors distributed around the board. The VSS line near the XR-2902 is particularly critical and should have bypassing near it. Capacitors on analog supplies are returned to analog ground, and likewise digital to digital.

Capacitor valves around the board of 0.01µF are usually adequate, with a larger value, 4.7µF, at the power supply.




XR-2902
PLCC Package
1 RD
2 RXCLK
3 NC
4 TXCLK
5 NC
6 VDD
7 SPKO
8 RXCIN
9 NC
10 AGND
11 TXOUT
12 C1
13 C2
14 NC
15 EXTXC
16 TXD
17 RESET
18 CS0
19 VSSD
20 VDDD
21 RD
22 ALE
23 WR
24 HD0
25 HD1
26 HD2
27 HD3
28 HD4
29 HD5
30 HD6
31 HD7
32 RXD
33 DGND
34 TD0
35 TD1
36 TD2
37 TD3
38 TD4
39 TD5
40 TD6
41 TD7
42 TD8
43 TD9
44 PA0
45 PA1
46 PA2
47 CLKIN
48 DEN
49 WEN
50 INT
51 VSS
52 NC


XR-2901
PLCC Package
1 INT
2 RS
3 MC/MP
4 A0/PA0
5 A1/PA1
6 GND
7 A2/PA2
8 A3
9 A4
10 A5
11 A6
12 A7
13 A8
14 MEN
15 DEN
16 WEN
17 VDD
18 A9
19 A10
20 A11
21 D0
22 D1
23 GND
24 D13
25 D14
26 D15
27 D7
28 D6
29 D5
30 D4
31 D3
32 D2
33 GND
34 D8
35 D9
36 D10
37 D11
38 D12
39 CLKOUT
40 X1
41 X2/CLKIN
42 BIO
43 NC
44 GND

V.22 bis Modem

GENERAL DESCRIPTION

The XR-2400 Chip Set is designed to provide the complete modem function for V.22 bis (2400 BPS) type modems. The chip set consists of the XR-2401 DSP Modem Signal Processor and the XR-2402 Analog Front End (AFE) with microcontroller interface. The XR-2400 set also supports Bell 212A (1200/300 BPS) and CCITT V.22 (1200 BPS) modes for a Bell/CCITT compatible system.

The XR-2401 is the heart of the system. It is a digital signal processor (DSP) based chip providing 300 BPS FSK, 1200 BPS,DPSK, and 2400 QAM modulation and demodulation for the system. Other functions included are scrambler/descrambler, adaptive equalizer, carrier detection, DTMF tone generator, and AGC control.

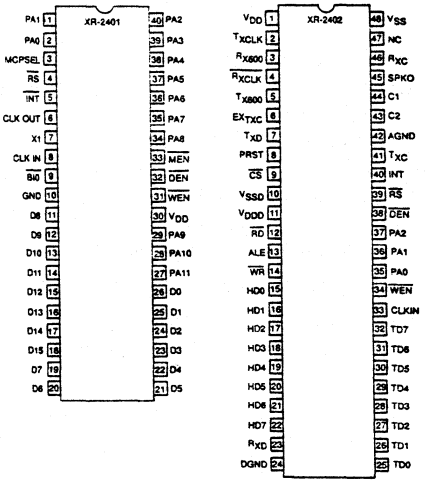
The XR-2402 provides the interface functions for the XR-2401, such as A/D and D/A converters for accessing the DSP chip inputs and outputs. Also provided are band splitting filters (SCF type), a programmable gain amplifier (PGA), asynchronous to synchronous and synchronous to asynchronous conversion, guard tone generation for CCITT applications, and a timing recovery.

Both the XR-2401 and XR-2402 are constructed with the Si-gate CMOS technology for low power operation. The XR-2401 is available in a 40 pin and the XR-2402 in a 48 pin package. The XR-2401 operates from a single +5 volt and XR-2402 from ±5 volt power supply.

FEATURES

2400 BPS (QAM), 1200 BPS (DPSK), 300 BPS (FSK) Operation
V.22 bis, V.22, 212A, 103 Compatible
DSP Based (XR-2401)
Bus Structured Control
No Adjustments
DTMF Dialing
Low Power CMOS (450 mw max.)
Adaptive Equalization
Asynchronous/Synchronous Operation
550 Hz/1800 Hz Guard Generation
Automatic Call Progress Monitoring
Low Chip Count Modems With XR-2404 Dedicated 'AT' microcontroller
Upgradeable to MNP® 5 Operation With the XR-2403B MNP 5 microcontroller or V.42bis with the XR-2442

PIN ASSIGNMENT



(See PLCC Package on back page)

APPLICATIONS

Stand Alone Modems
Internal Modems
Smart Modems
Laptop Applications

ABSOLUTE MAXIMUM RATINGS

Power Supply	
XR-2401	-0.3 to +7 V
XR-2402	-7 to +7 V
Input Voltage	-0.7 to VDD + 0.3 V
DC Input Current (Any Input)	± 10mA
Power Dissipation (package limitation)	1 Watt
Storage Temperature Range	-65°C to +125°C

ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-2401CP	Plastic	0°C to 70°C
XR-2402CP	Plastic	0°C to 70°C
*XR-2401CJ	PLCC	0°C to 70°C
*XR-2402CJ	PLCC	0°C to 70°C

*See Back Page for Pinout.

SYSTEM DESCRIPTION

The XR-2401 / XR-2402 Modem Chip Set is designed to interface directly to popular microcontrollers, such as 8031 or Z - 8 types. The microcontroller provides such functions as handshake control, smart functions such as "AT" commands, and dialing control. Exar provides a complete "AT" command set which can be used as is or modified.

The only other circuitry necessary is a line interface circuit (DAA) and RS-232 interface.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
XR-2401 $f_{CLKIN} = 19.6608$ MHz ± 0.01%						
I_{DD}	Positive Supply Current		33	50	mA	
V_{DD}	Positive Supply Voltage	4.5	5.0	5.5	V	
V_{IH}	High Level Input Voltage	2.0			V	Except CLKIN
V_{IHC}	CLK High Level Input Voltage	0.56 V_{DD}			V	
V_{IL}	Low Level Input Voltage			0.8	V	
I_{OH}	High Level Output Current			20	µA	$V_{OH} = V_{DD} - .4V$
				300	µA	$V_{OH} = 2.4V$
I_{OL}	Low Level Output Current			2	mA	
V_{OH}	High Level Output Voltage	$V_{DD} - .4$			V	$I_{OH} = 20$ µA
		2.4			V	$I_{OH} = 300$ µA
I_I	Input Current			50	µA	$V_I = 0$ to V_{DD}
XR-2402 $f_{CLKIN} = 4.9152$ MHz ± 0.01%						
V_{DD}	Positive Supply Voltage	4.5	5.0	5.5	V	
VSS	Negative Supply Voltage	-5.5	-5.0	-4.5	V	
I_{DD}	Positive Supply Current		15	20	mA	
I_{DDS}	Positive Supply Current, Standby Mode		3	5	mA	
I_{SS}	Negative Supply Current		15	20	mA	
I_{SSS}	Negative Supply Current, Standby Mode		3	5	mA	
V_{IH}	High Level Input Voltage	2.0			V	
V_{IL}	Low Level Input Voltage			0.8	V	
I_{OH}	High Level Output Current			300	µA	$V_{OH} = 2.4V$
I_{OL}	Low Level Output Current			2	mA	
V_{OH}	High level Output Voltage	2.4			V	$I_{OH} = 700$ µA
I_I	Input Current			50	µA	$V_I = 0$ to V_{DD}
R_{XC}	Receive Carrier Range	-6		-45	dBM	(Using 6/16 dB RCVG feature)

TRANSMITTER SPECIFICATIONS

All values are measured at TXC (Pin 41) of the XR-2402 with Bit 0-2 = 1 of CNTRL 0.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
TRANSMITTER POWER						
T_{XC} QAM	QAM/PSK Transmitter Power	-.6		+3.4	dBm	
T_{XC}550	CCITT Guard Tone Power	-1.7		-.4	dBm	T_{XC} = 2 dBm
T_{XC}1800		-5.2		-3.4	dBm	T_{XC} = 2 dBm
T_{XC} QAM/PSK 550	QAM/PSK Transmitter Power With Guard Tone	1.9		*	dBm	
T_{XC} QAM/PSK 1800		*		*	dBm	
T_{XC} FSK	FSK Transmitter Power	-.16		+2.5	dBm	
T_{XC} AT	Answer Tone Power	1.6		2.9	dBm	
T_{XC} DTMF C	DTMF Tone Power Column	-4.9		-3.1	dBm	
T_{XC} DTMF R	DTMF Tone Power Row	-6.2		-4.4	dBm	
ΔT_{XC} DTMF	DTMF Amplitude Difference	-2		+2	dB	

* Not currently measured in final test program, limits to be determined. 10/31/89 for value to be determined.

SYSTEM PERFORMANCE

V_{RXD} = -40dBm, Originate Mode, 3002 Line Conditions, T_{XC} = -10dBm.

SYSTEM	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
S/N	Signal-to-Noise Ratio		16		dB	2400 BPS
			9		dB	1200 BPS
			12		dB	300 BPS
F_{OFF}	Frequency Offset		±10		Hz	2400/1200 BPS

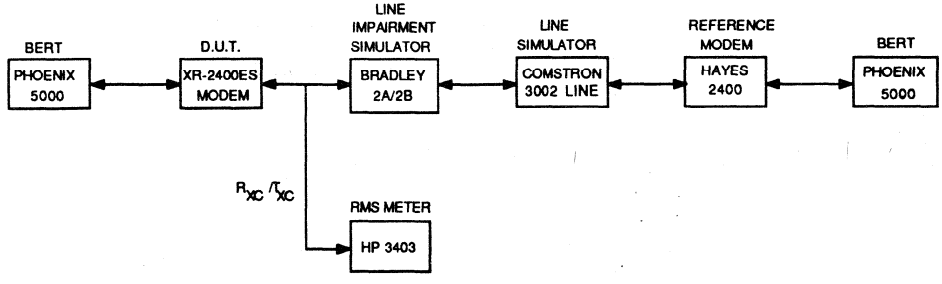
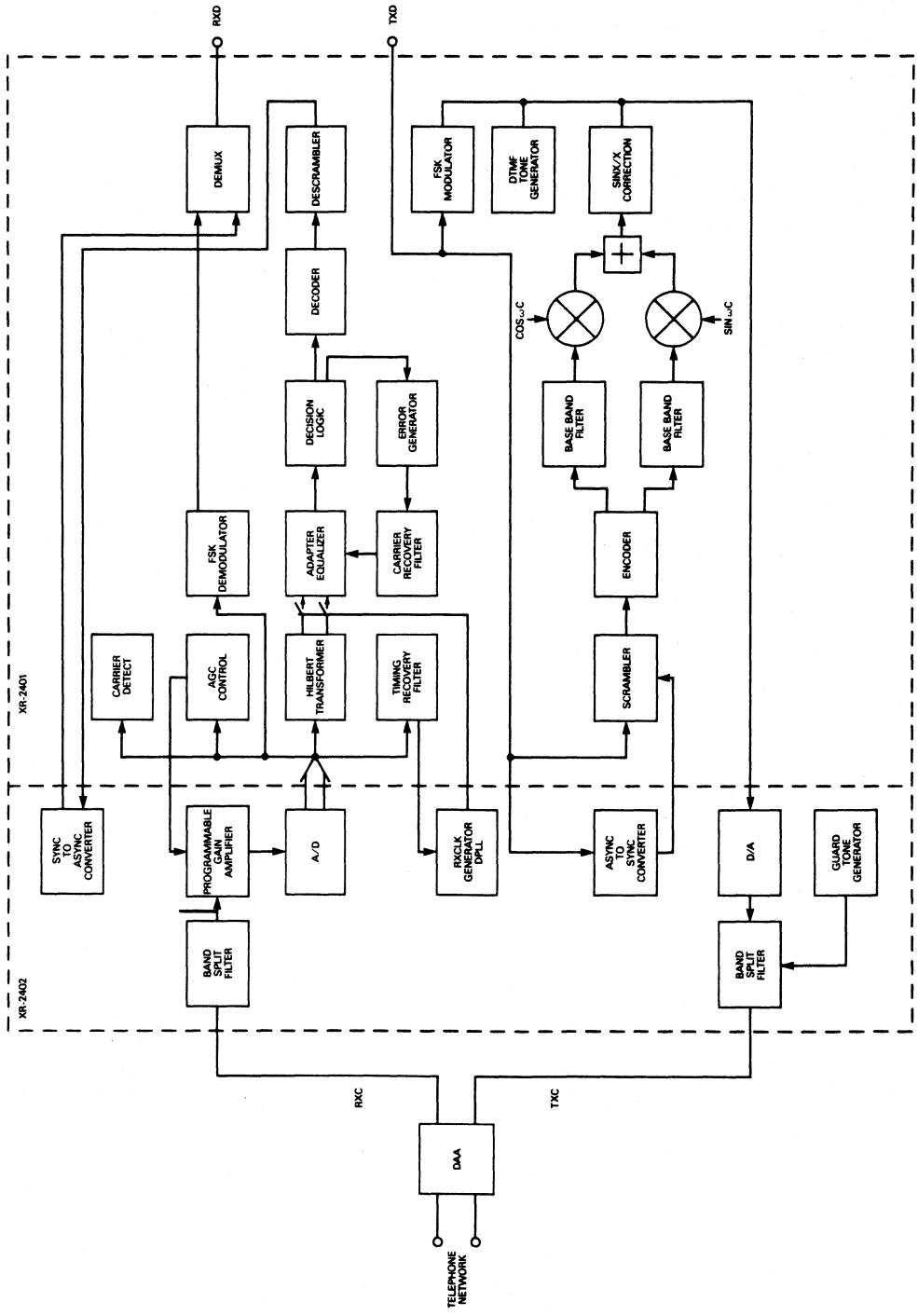
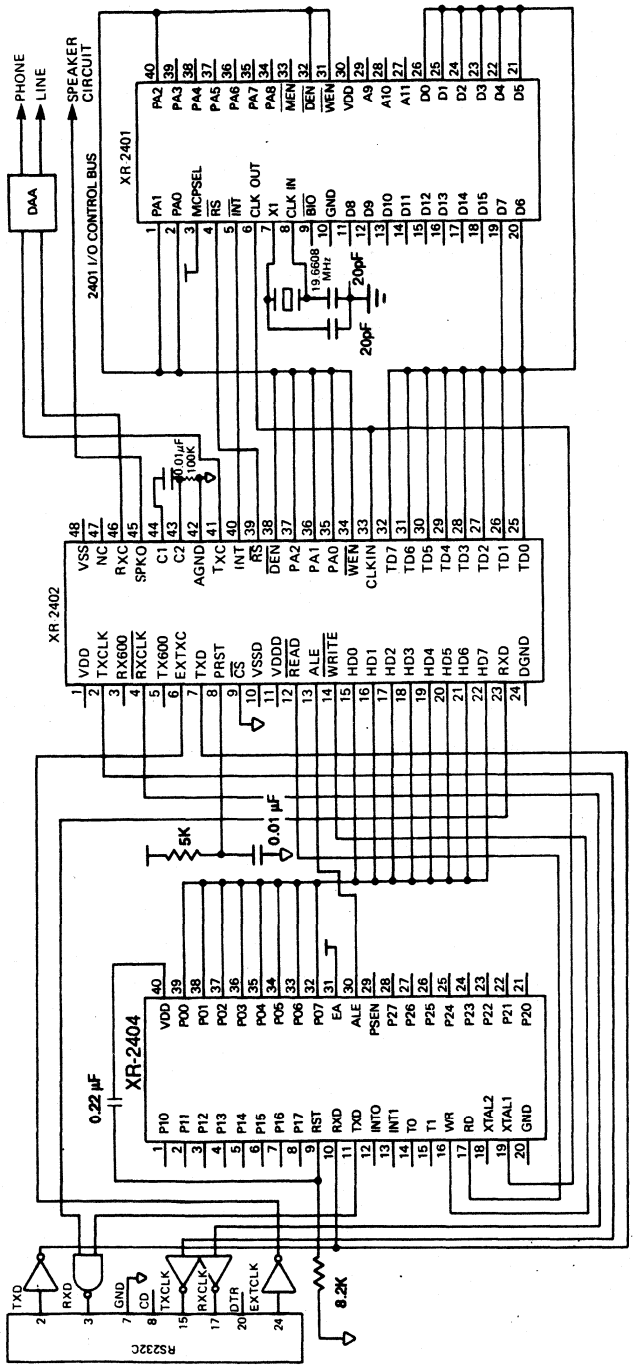


Figure 1. Performance Test Set-Up



XR-2400 Functional Block Diagram



XR-2400 V. 22 bis MODEM

PIN DESCRIPTIONS/FUNCTIONS

The XR-2401 and XR-2402 provide the heart of a V.22 bis modem system and when connected to a microcontroller such as the 8031 type, a complete system is formed. The XR-2402 provides the analog front end (AFE) function as well as the bridge, or interface, between the XR-2401 digital signal processor (DSP) and microcontroller.

The pin functions of the XR-2401 are as follows:

Name	I/O	Pin	Description
V_{DD}	I	30	Positive supply Voltage +5V ±5%
GND	I	10	Ground connection - digital
$\overline{RS}$	I	4	Reset to initialize chip
X1	I	7	Crystal input 19.6608 MHz ±0.01%
CLK IN	I	8	Crystal input or external clock
CLK OUT	O	6	1/4 crystal/CLK IN frequency
PA0-PA11	OUT	1,2 27,29, 34-40	External address bus. I/O port address multiplexed over PA0-PA2
$\overline{BIO}$	I	9	External polling input for bit test and jump operations.
D0-D15	I/O	11-26	16 bit data bus
$\overline{DEN}$	O	32	Data enable indicates the XR-2401 accepting input data on D0-D15.
$\overline{INT}$	I	5	Interrupt input
MCPSEL	I	3	Mode select. 1 = microcomputer mode, 0 = microprocessor mode.
$\overline{MEN}$	O	33	Memory enable indicates that D0-D15 will accept memory instruction.
$\overline{WEN}$	O	31	Write enable indicates valid data on D0-D15.

The pin functions of the XR-2402 are as follows:

Name	I/O	Pin	Description
VDD	I	1	Positive analog supply +5V ±5%
VSS	I	48	Negative analog supply -5V ±5%
VDDD	I	11	Logic positive supply +5V ±5%
VSSD	I	10	Logic negative supply -5V ±5%
DGND	I	24	Logic ground
AGND	I	42	Analog ground
PRST	I	8	Power on reset input

Microprocessor Interface

Name	I/O	Pin	Description
ALE	I	13	Address latch enable
HD0	I/O	15	Address/data bus bit 0
HD1	I/O	16	Address/data bus bit 1
HD2	I/O	17	Address/data bus bit 2
HD3	I/O	18	Address/data bus bit 3
HD4	I/O	19	Address/data bus bit 4
HD5	I/O	20	Address/data bus bit 5
HD6	I/O	21	Address/data bus bit 6
HD7	I/O	22	Address/data bus bit 7
$\overline{CS}$	I	9	Chip select
$\overline{WR}$	I	14	Write strobe
$\overline{RD}$	I	12	Read strobe

XR-2401 Interface

Name	I/O	Pin	Description
CLK IN	I	33	4.9152MHz input from XR-2401
$\overline{INT}$	O	40	Interrupt flag for XR-2401
$\overline{RSB}$	O	39	Reset output for XR-2401
PA0	I	35	I/O port address bus bit 0
PA1	I	36	I/O port address bus bit 1
PA2	I	37	I/O port address bus bit 2
$\overline{DENB}$	I	38	Read enable strobe
$\overline{WEN}$	I	34	Write enable strobe
TD0	I/O	25	Data bus bit 0
TD1	I/O	26	Data bus bit 1
TD2	I/O	27	Data bus bit 2
TD3	I/O	28	Data bus bit 3
TD4	I/O	29	Data bus bit 4
TD5	I/O	30	Data bus bit 5
TD6	I/O	31	Data bus bit 6
TD7	I/O	32	Data bus bit 7

RS232C Interface

Name	I/O	Pin	Description
EXTXC	I	6	External transmit clock
TXCLK	O	2	Transmit clock output
TXD	I	7	Transmit data input
$\overline{RXCLK}$	O	4	Receive clock output
RXD	O	23	Receive data output, with pull-up resistor

Special Functions

Name	I/O	Pin	Description
TX600	O	5	Transmit 600 Hz output
RX600	O	3	Receive 600 Hz output
SPKO	O	45	Audio output to speaker

Analog Interface

Name	I/O	Pin	Description
TXC	O	41	Transmit carrier output
RXC	I	46	Receive carrier input
C1	O	44	Programmable gain stage output
C2	I	43	A/D input

SYSTEM OPERATION

The XR-2400 (XR-2401/2402) is designed to interface with a host controller by both hardware and software. The XR-2400 looks like a memory mapped peripheral to the host controller. The XR-2402 acts as a bridge or interface between the XR-2401 DSP and host controller and thus, all control/status information will pass through it. Figure 2 shows the general data/address bus connection of the XR-2400 to the host controller.

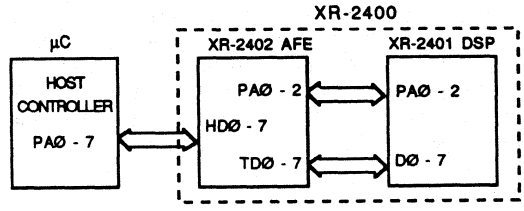


Figure 2. General Data/Address Bus Connection

The XR-2401 DSP performs all of the modem signal processing functions. While, the controller functions are left to the host microcontroller for system flexibility.

There are two kinds of control/status registers for the host microcontroller to access; one in the XR-2402 and one in the XR-2401 via the XR-2402 interface buffer. To the µc, the XR-2402 register looks just like an external data memory. The XR-2401 data memory must be accessed through the XR-2402. The handshake procedure to access the memory map is shown in Table I.

Read	Write	XR-2402
	0	Address register (8 bit latch)
	1	Write data register (8 bit latch)
2		Read data register (8 bit latch)
3		Status register in XR-2402
	3	Control register in XR-2402

Table 1. Memory Map for Host

GENERAL MODE SETTING READING INFORMATION FROM XR-2400

A handshake procedure is necessary for communication between the host microcontroller and XR-2400. All data (address, write data, read data) passes through a register in the XR-2402 with the procedure for controlling this register as follows:

Read Cycle

First, the host microcontroller will write a target address to the XR-2402 address register. Simultaneously, the XR-2402 will generate an interrupt for the XR-2401, which will branch to interrupt service routine and send data out to the XR-2402 reading register. This procedure takes 3 microseconds, thus, the host microcontroller needs to ensure it waits at least 3 microseconds from target address and reading data. (Refer to Figure 12)

Write Cycle

The write cycle is used for the host microcontroller to write to the XR-2400. Data is written first to the XR-2402 then the target address to the address register. It will generate interrupt for the XR-2401 and after a 6 microseconds delay, the XR-2401 will take the data from the write register. (Refer to Figure 12)

Read/Write Data Directly From the XR-2402

There are two data memory locations which the host microcontroller can access immediately.

1. Status Register - Address 3

   Bit 3 - Bit 0 are copied from Control Register 7 in the XR-2401. Bit 6 - bit 4 are generated in the XR-2402.

Bit 0	R_{XDATA}
Bit 1	Unscrambled R_{XDATA}
Bit 2	Energy Detect
Bit 3	Signal Quality Indicator
Bit 4	S1 Signal Detector. With and S1 pattern coming in, Bit 4 will be continuously high allowing the user to access the coming S1 signal information.
Bit 5	Dotting Pattern Detect Indicator. With an incoming dotting pattern (alternating etc.), this indicator will be high allowing the user to detect digital loopback.
Bit 6	R_{XD} after Buffer. The user may access parallel R_{XD} through the data bus.

   The following is an instruction example for the status register:

   ```
   MOV   RO,#3  ;   Put #03 in RO
   MOVX  A, @ RO;   Move external memory #03 to ACC.
   ```

2. Control Register

Bit 0	Parallel TXD Input - This allows the user to input TXD through the parallel data bus.
Bit 1	Software Reset for XR-2401 - Reset = "0" ; Normal Operation = "1". For proper reset operation, a low must be present for at least 2 µs.

   The following is an example of writing to the control register:

   ```
   MOV     RO, #3  ;   Put #03 in RO
   MOVX @ RO, A    ;   Move data from ACC
                       to external memory.
   ```

Modem Mode Selection Control

The XR-2401 data memory location #69 is used for mode selection as follows:

0	Idle Mode
1	FSK Mode
2	PSK Mode
3	DTMF Mode

Handshake Sequences

The XR-2400 chip set provides operating modes of 2400 BPS, 1200 BPS and 300 BPS to cover CCITT standards of V.22 bis and V.22 as well as Bell 212A and 103. The following figures illustrated the handshake sequences for automatic rate speed selection. Figure 3 shows the sequence for 2400 BPS (V.22 bis) with V.25 automatic answering. The following figures, 4 through 7, show the remaining handshake sequences needed to support other CCITT/Bell operating modes.

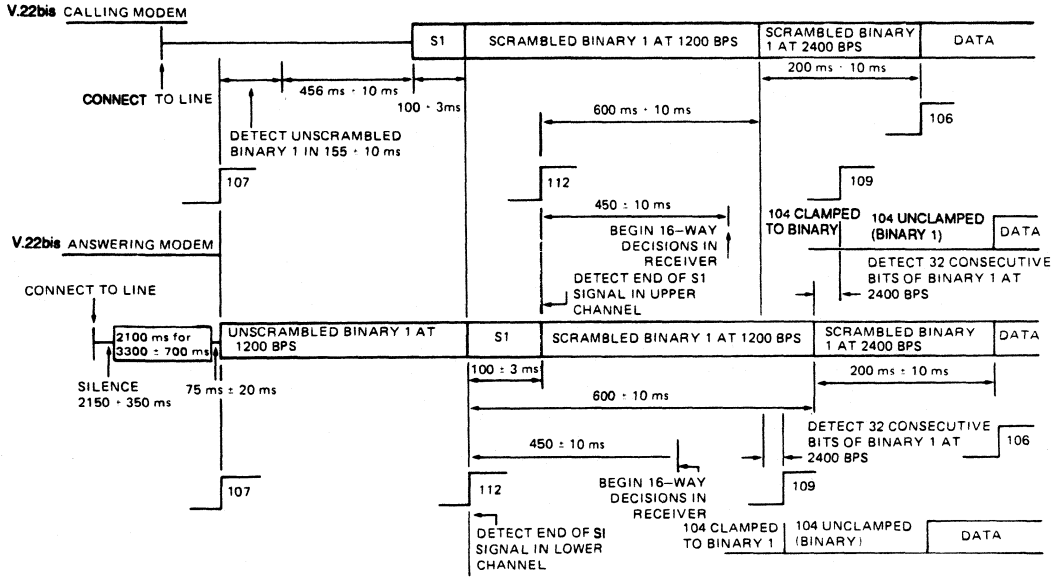


Figure 3. V.22 bis Handshake Sequence at 2400 BPS (with V.25 Auto Ans.)

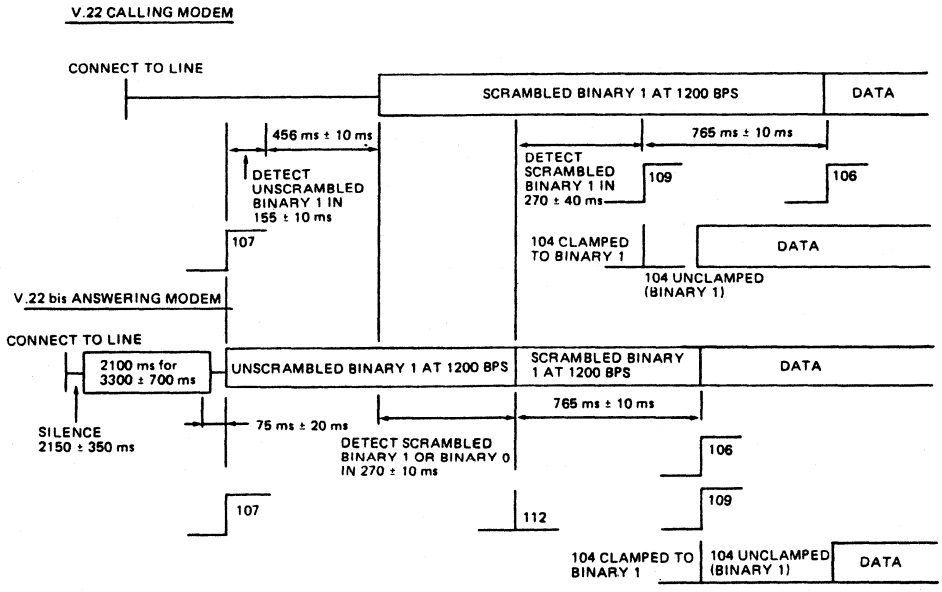


Figure 4. V.22 bis Handshake Sequence at 1200 BPS with V.22 Calling Modem (with V.25 Auto Ans.)

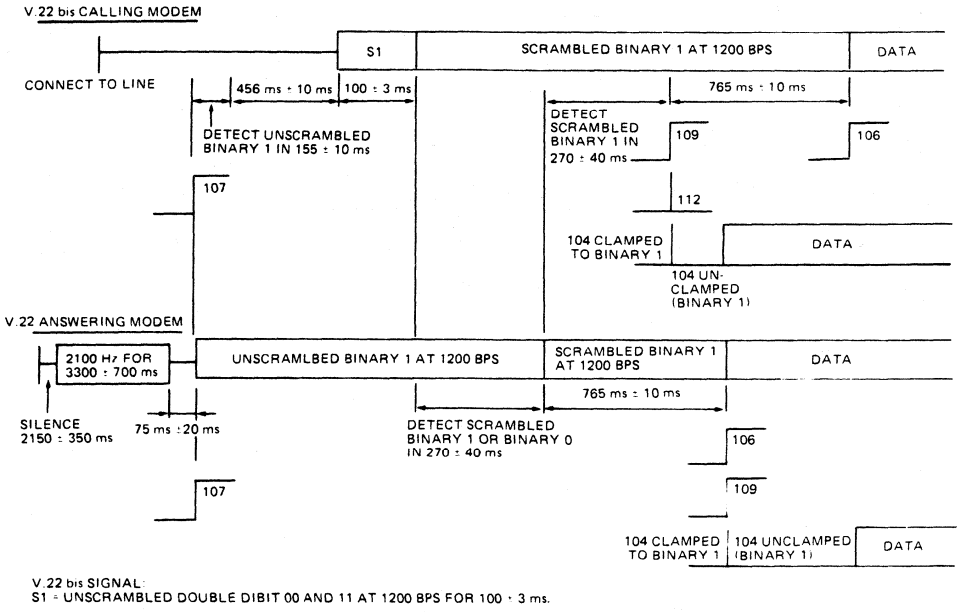


Figure 5. V.22 bis Handshake Sequence at 1200 BPS with V.22 Answering Modem (with V.25 Auto Ans.)

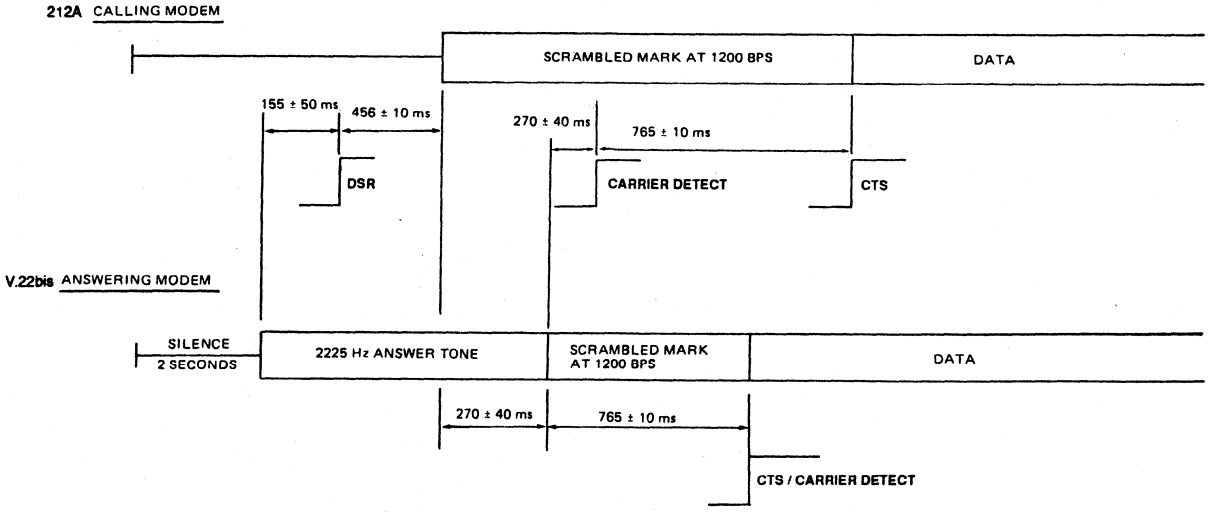


Figure 6. 212A Handshake Sequence at 1200 BPS with 212A Modem

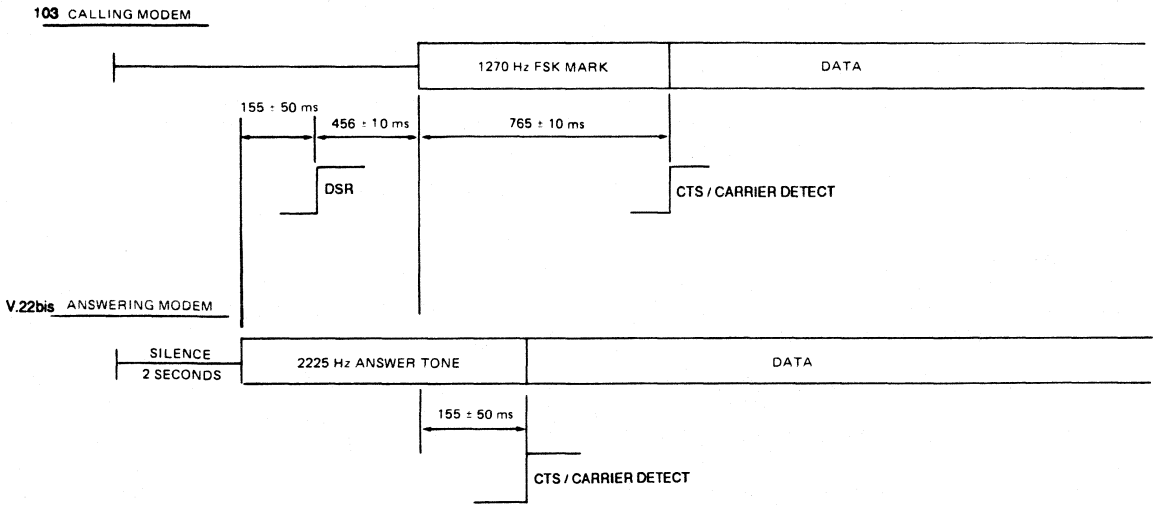


Figure 7. 103 Handshake Sequence at 300 BPS with 103 Modem

DTMF Generation

The XR-2400 provides an onboard DTMF generator which is controlled by the host microcontroller. The flow chart in Figure 8 illustrates the procedure for DTMF tone generation.

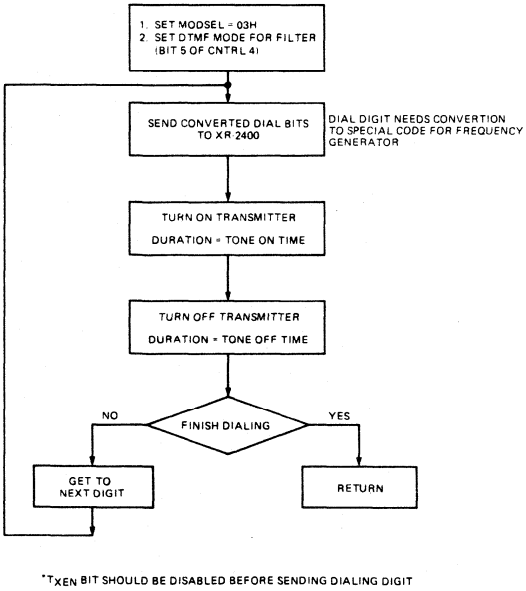


Figure 8. DTMF Generation Flow

Table 2 shows the digit/tone pairs for the DTMF generator.

Dial Digit	Encode D4	D3	D2	D1	Tone Pairs (Hz) Tone 1	Tone 2
0	0	1	1	1	941	1336
1	0	0	0	0	697	1209
2	0	1	0	0	697	1336
3	1	0	0	0	697	1477
4	0	0	0	1	770	1209
5	0	1	0	1	770	1336
6	1	0	0	1	770	1477
7	0	0	1	0	852	1209
8	0	1	1	0	852	1336
9	1	0	1	0	852	1477
*	0	0	1	1	941	1209
#	1	0	1	1	941	1477
(B)	1	1	0	0	697	1633
(C)	1	1	0	1	770	1633
(D)	1	1	1	0	852	1633
(F)	1	1	1	1	941	1633

Table 2. DTMF Tone Pairs / Dial Digits

Call Progress Tone Monitor Operation

The host microcontroller uses the XR-2402 as a filter for call progress detection mode. When CPM = HIGH (enabled), the XR-2402 low band will be scaled down by a factor of 2.5 or 300-660 Hz. The ALB control bit provides the input for band connection to the carrier detect as shown in Table 3.

CPM = 1

ALB	Carrier Detect (CD) Connected to
0	High Band (2400 Hz)
1	Low Band (Scaled low band 300-660 Hz)

Table 3. CPM Frequency Band Assignments

The output of the CD circuit is monitored by the host microcontroller for duration and repetition rate to determine line status. The CD information is available by reading Bit 2 of CNTRL 7. The CD status is as follows:

CD = Energy Detect (direct access locations)

1 = Energy Detected

0 = No Energy

The MODSEL is set to FSK mode. After CPM mode, the microcontroller needs to send a reset signal to the XR-2401.

Table 4 indicates the various CD selections.

CPM	ALB	A/O	CD
1	0	0	Received high band; monitor answer tone.
1	1	0	Received low band filter scaled down by 2.5; monitoring dial tone, busy tone, and ring back tone.
0	0	0	Normal high band energy detect.
0	0	1	Normal low band energy detect.

Table 4. CD Frequency Band Assignments

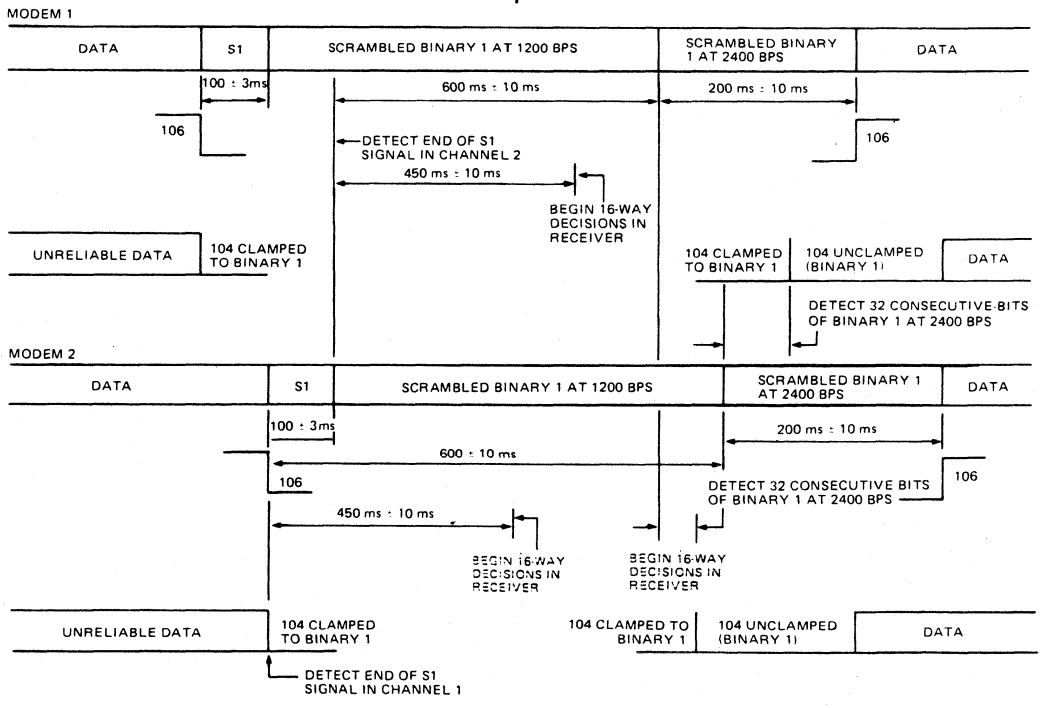


Figure 9. 2400 BPS Retrain Sequence

Signal Quality Indicator

The XR-2400 provides a signal quality indicator, SGQ, to indicate the quality of the received demodulated data. The state of this output is as follows:

SGQ Output:	
0	Good Signal
1	Bad Signal

The XR-2401 signal quality detector utilizes least mean square error method for error detection.

The XR-2400 provides the SGQ indicator for the host microcontroller. A counter is set up in the microcontroller, and if the value in it exceeds a preset value in a predetermined time, a request for retrain requirement will be given. The retrain sequence is shown in Figure 9.

Test Modes

ALB, Analog Loopback, is a test mode which is used for complete testing of the local modem. Figure 10 illustrates the basic signal flow.

The transmit carrier is looped back to the demodulator input, bypassing the receive filter. The demodulator is set to the transmit carrier frequency. Table 5 illustrates ALB selection for answer and originate.

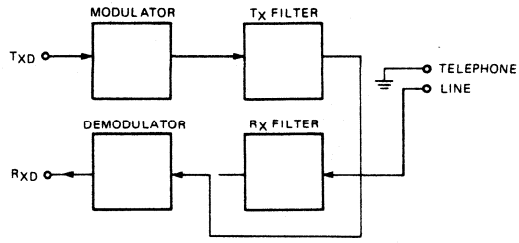


Figure 10. ALB Signal Flow

ALB = 1

MODE	T_X	R_X
ANS	Low Band	Low Band
ORIG	High Band	High Band

Table 5. ALB Frequency Assignments with ALB = 1

RDLT, Remote Digital Loopback, is used to test the far-end or remote modem. The start of this type of loopback is automatically initiated by sending an unscrambled mark pattern, as seen in Figure 11. Also shown in Figure 11 is the carrier pattern for termination of RDLB.

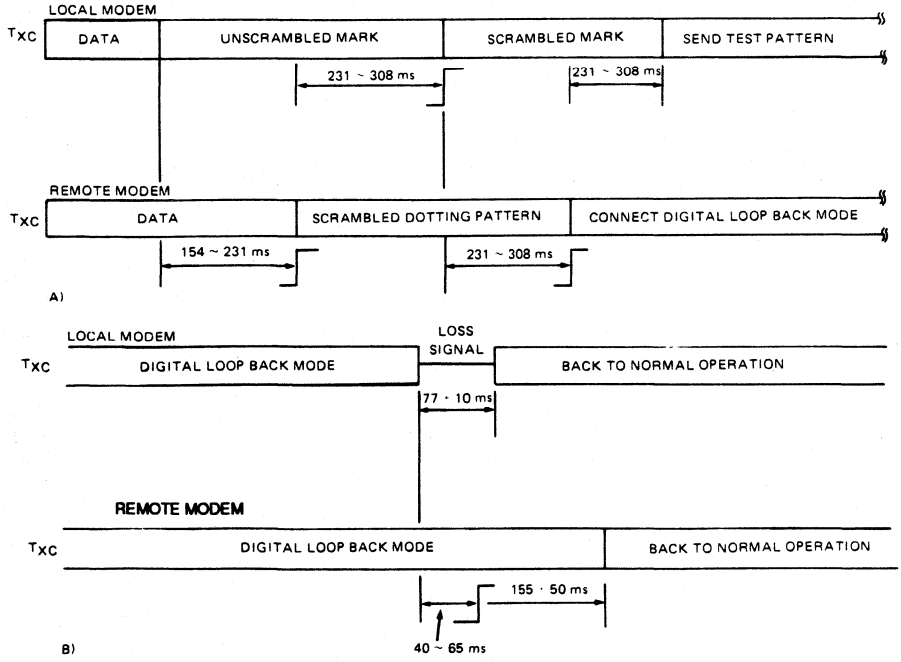


Figure 11. RDLB Initiation (A) and Termination (B)

XR-2400 / MICROCONTROLLER INTERFACING

The XR-2400 looks as a memory peripheral to a host microcontroller. The following indicates the address locations with bit functions of XR-2401 registers.

Location 60H - CNTRL 0

Bit	Description
0	TXL1
1	TXL2
2	TXL3
3	SPC
4	TST1 (EXAR SPECIAL TEST MODE)
5	TST2 (EXAR SPECIAL TEST MODE)
6	TST3 (EXAR SPECIAL TEST MODE)
7	-

Bits 4, 5, 6 need to be set to 0 for normal operation.

Location 61H - CNTRL 1

0	OPTD
1	SP1
2	SP2
3	ETE
4	DLB
5	BC1
6	BC2
7	ASY

Bit 2	Bit 1	Bit 0	Transmit Level (±1 dB)
0	0	0	-10.5 dB
0	0	1	-9.0 dB
0	1	0	-7.5 dB
0	1	1	-6.0 dB
1	0	0	-4.5 dB
1	0	1	-3.0 dB
1	1	0	-1.5 dB
1	1	1	0

Bit 3	Speaker
0	OFF
1	ON

Bit 0	Async Data Rate
0	+1% to -2.5%
1	+2.3% to -2.5%

Bit 2	Bit 1	Receiver Speed
1	1	2400 BPS
0	1	1200 BPS
1	0	300 BPS

Bit 3	Transmit Clock
0	Internal
1	External

Bit 4	Bit Status	
0	Normal Data Mode	
1	Digital Loopback	TXCLK connect to RXCLK TXDATA connect to TXDATA

Bit 6	Bit 5	ASY Character Length
0	0	8 bit
1	0	9 bit
0	1	10 bit
1	1	11 bit

Bit 7	Mode
0	Synchronous
1	Asynchronous

Location 62H - CNTRL 2

0	TEN	Transmitter Enable (EN = 1)
1	SCR	Scrambler Enable (EN = 1)
2	64B	64 Bit Mark Sensor (EN = 1)
3	EQO	Adaptive Equalizer ON/OFF Control (ON @ 1)
4	EQT	Adaptive Equalizer T or T/2 Select (T/2 = 1)
5	VBS	Transmitter Shaping Select 1 = CCITT 75% square root raised cosine 0 = Bell shaping
6	ANT	Answer Tone Selection (0=2225 Hz / 1 = 2100 Hz)
7	REQ	Equalizer Reset Control (RS = 0)

Location 63H - CNTRL 3

0	FL	Fast Locking Control (FL = 1). At the beginning of communication FL is set to 1 for fast DPLL response to the incoming signal.
1	CRD	RXD Clamp Control (RXD = 1 when CRD = 1)
2	TSP	Transmit Clock Select (2400 BPS = 1 / 1200 BPS = 0)
3	TST4	EXAR SPECIAL TEST MODE, set to 0 for normal operation.
4	PTD	Parallel TXD Input Selection (Parallel = 1). TXD will be taken from the µc data bus.
5	NTD	Normal Data Mode TXD from RS232 when (NTD = 1). 0: TXDATA will be taken from the selection of TC1, TC2.
6	TC1	
7	TC2	

Bit 7	Bit 6	TXC (NTD = 0)
1	1	Dotting Pattern used for DLB/Self Test
0	1	300 Hz, used to Generate S1 Pattern
1	0	Mark (ones)
0	0	Space (zeros)

Location 64H - CNTRL 4

0	PDM	Power Down Mode (PD=1). During power down mode, only the analog portion of the XR-2402 is disabled. The digital portion will still be active waiting for a control signal from the µc.
1	MOD	Answer/Originate Mode (Ans=1)
2	GTE	Guard Tone Enable (GT=1)
3	GTS	Guard Tone Selection (1800 Hz=1 / 550 Hz = 0)
4	RCVG	Receive Filter Gain (6dB=1, 16 dB =0)
5	DMFM	DTMF Mode Control (DTMF=1)
6	CPD	Call Progress Tone Detect Mode (CPT = 1)
7	ALB	Analog Loopback Enable (ALB = 1)

Location 65H - CNTRL 5

0	D1	Dial Digit 1
1	D2	Dial Digit 2
2	D3	Dial Digit 3
3	D4	Dial Digit 4
4	-	
5	-	
6	-	
7	-	

Location 66H - CNTRL 6 AGC Word

0	AG0	7 bits AGC control, each step is 0.375 dB
1	AG1	
2	AG2	
3	AG3	
4	AG4	
5	AG5	
6	AG6	
7	-	

Location 67H - CNTRL 7 Status Word

0	RXD	Receive Data
1	USD	Unscrambled Received Data
2	CD	Energy Detect
3	SGQ	Signal Quality Indicator

Location 69H - MODSEL

0	IDLE MODE
1	FSK MODE
2	PSK MODE
3	DTMF TONE MODE

A summary of control locations is given below in Table 6.

CNTRL	BIT 7	BIT 6	BIT5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CNTRL 0	-	TST3	TST2	TST1	SPC	TXL3	TLX2	TLX1
CNTRL 1	ASY	BC2	BC1	DLB	ETE	SP2	SP1	OPTD
CNTRL 2	REQ	ANT	VBS	EQT	EQO	64B	SCR	TEN
CNTRL 3	TC2	TC1	NTD	PTD	TST4	TSP	CRD	FL
CNTRL 4	ALB	CPDQ	DMFM	RCVG	GTS	GTE	MOD	PDM
CNTRL 5	-	-	-	-	DIAL DIGIT	DIAL DIGIT	DIAL DIGIT	DIAL DIGIT
CNTRL 6	-	AGC6	AGC5	AGC4	AGC3	AGC2	AGC1	AGC0
CNTRL 7	-	-	-	-	SGQ	CD	URXD	RXD

Table 6. Control / Status Locations

The following describes the read/write ports of the XR-2401 which is selected by PA0 ~PA2

Write Ports (WEN)

Port 0	Write to XR-2402 DAC D0-D7
Port 3	Write RXD to XR-2402 D0-RXD D1 - Underscrambled RXD D2 - CD D3 - Equalizer Crash Indicator
Port 4	Write AGC Gain to XR-2402/ Reset RX600 FLAG 6 D0 - D6
Port 5	Write PLL Information to XR-2402 D0 -Late/Early (L/E) Information
Port 6	Write Eye Pattern Information D0 - D15
Port 7	Write Data to XR-2402 D0 - D7

Read Ports (DEN)

Port 0	Read Status from XR-2401 and XR-2402 D0 - RX9600 Hz Ready D1 - TX9600 Hz Ready D2 - RX600 Hz Ready D3 - TXD Ready D4 - RXD Ready D5 - TX600 Hz Ready D6 - D7 - Write Register Ready
Port 1	Read Serial TXD from XR-2402
Port 3	Read Converted Signal from A/D on XR-2402 D0 - D7
Port 4	Read Address Information from XR-2402 D0 - D7
Port 5	Read "Write Register" Data from XR-2402 D0 - D7
Port 6	Output Dummy to Reset TX600 Flag

The following illustrates the 8031 type microcontroller read/write of the XR-2401.

1. Read Target Address #60H in XR-2401:

```
MOV  A,#60H  ; Set up target address for XR-24011
MOV RO,#00   ; Set up RO for external memory
                 read
MOVX@RO,A ;  Move target address to address
                 register
             ;  After this instruction will poll the
             ;  interrupt for XR-2401
NOP          ; These NOP ensure there is 3 µs
NOP          ;  for data setting
MOV RO,#02   ; Put #02 in RO
MOVX A,@RO ; Move data read data register
```

2. Write Data #AA to target Address #60H in XR-2401:

```
MOV A,#AA    ;  Put desired data in accumulator
MOV RO,#01   ;  Put #01 in RO
MOVX @RO,A ;  Move #AA to write data register
MOV A,#60H   ;  Move target address #60 to
                accumulator
MOV RO,#00   ;  Put #00 in RO
MOVX @RO,A ;  Move target address to address
                register
```

After 6 microseconds, the XR-2401 will take data from the XR-2402 to finish the write cycle.

Note: In order to maintain proper operation, there are some limitations on read/write access for the XR-2401. In normal operation (excluding idle mode), more than one access within 100 microseconds is not allowed.

Figure 12 illustrates the read/write data timing to the XR-2400.

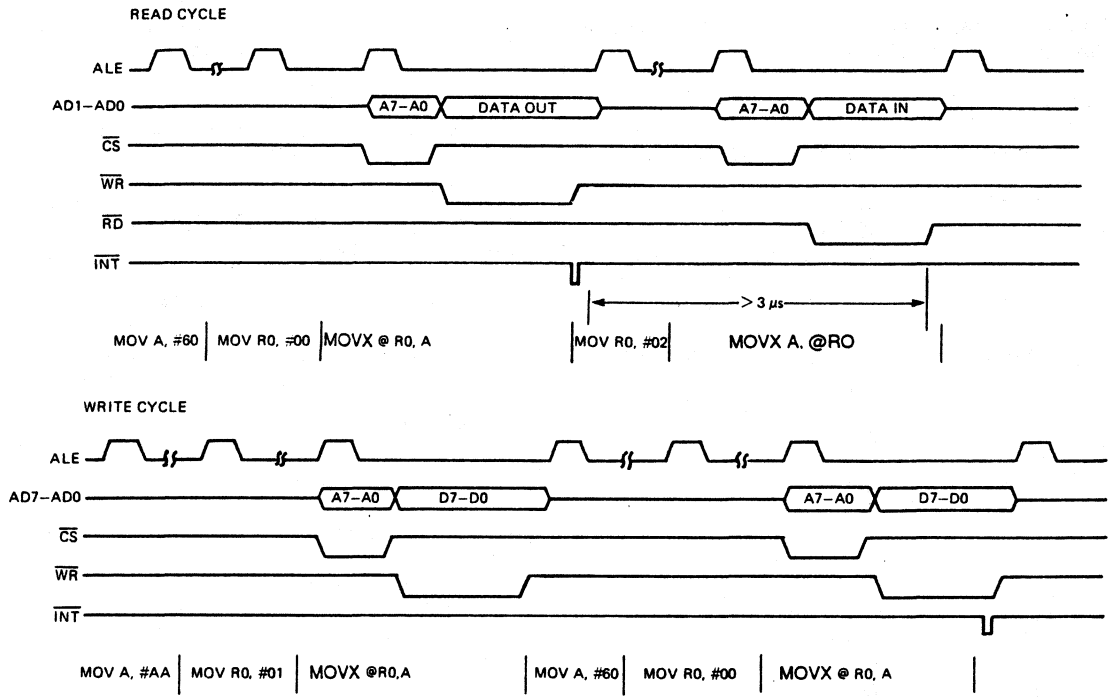


Figure 12. Timing for XR-2400 Read/Write Data

APPLICATIONS INFORMATION

Figure 17 shows the XR-2401/XR-2402 in a complete stand alone V.22 bis modem. In this system, an 8031 type µC is used for providing the handshake and command set control. The 2764 EPROM would hold the command set, with the 373 necessary to interface the 8031 to the 2764.

Special attention should be followed in system grounding. The analog and digital grounds should be single point connected at the power supply.

Figure 18 shows XR-2401/XR-2402 in a complete internal V.22bis modem.

Signal Constellation Monitor Circuit

For system testing and evaluation, it is often instructive to evaluate the signal constellation of the modem. During design and testing, the constellation provides useful information on demodulation quality. The circuit in Figure 13 provides an output which can be displayed on an oscilliscope. The general characteristics of the signal constellation is illustrated in Figure 14.

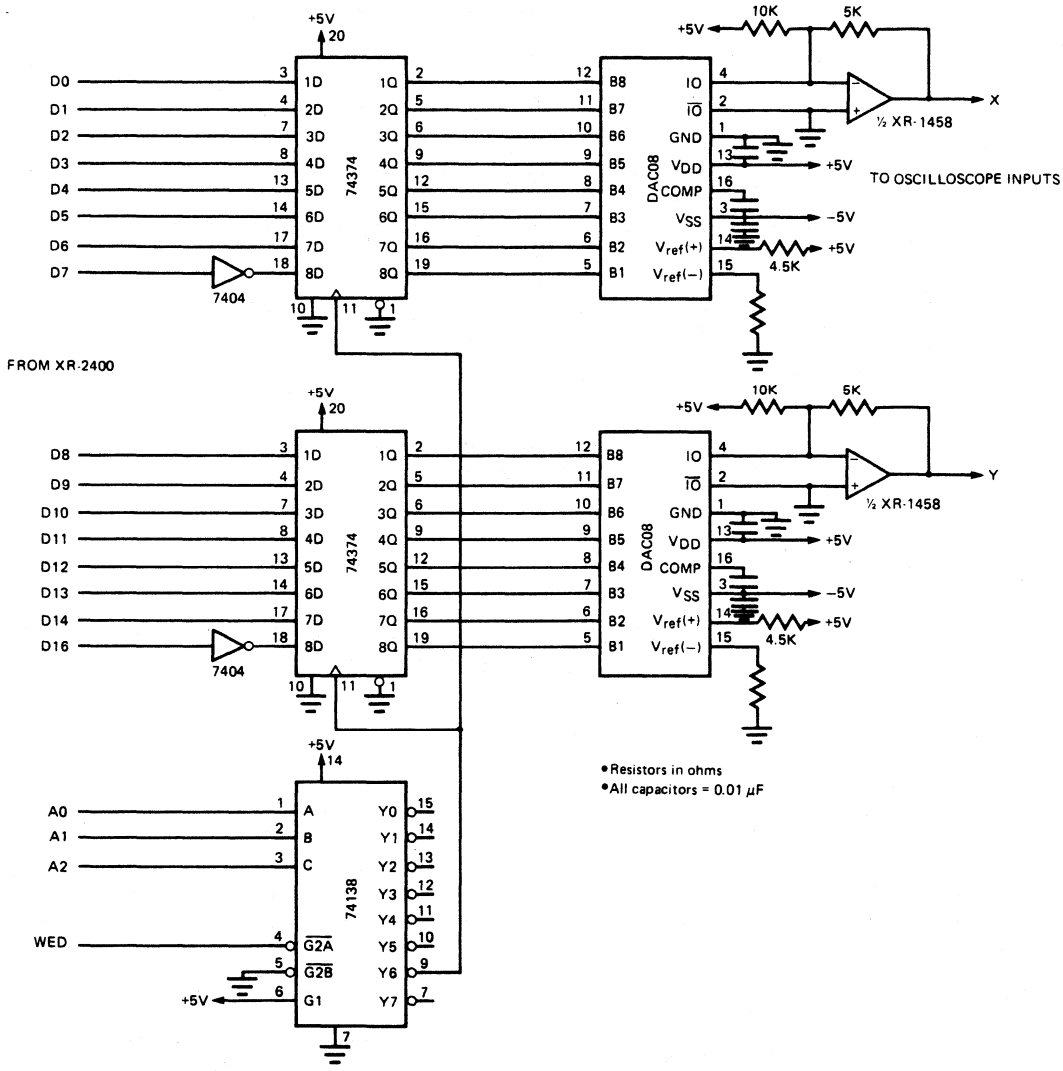


Figure 13. Signal Constellation Monitor

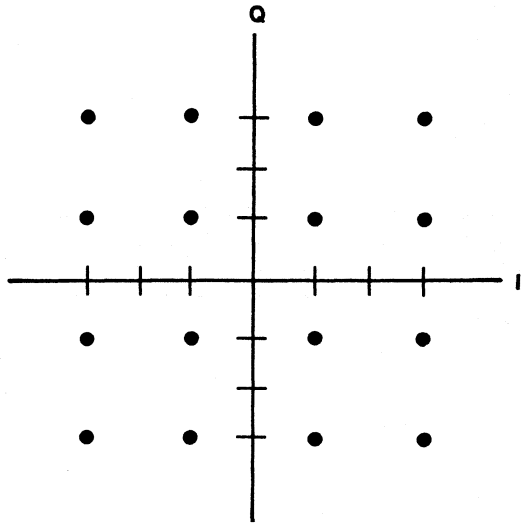


Figure 14. General Characteristics of 16 Point Constellation at 2400 BPS Q I

SYSTEM PERFORMANCE

Test set-up conditions shown on page 3, Figure 1.

Data quality is illustrated in figures 15 and 16 for 2400 BPS and 1200 BPS operation.

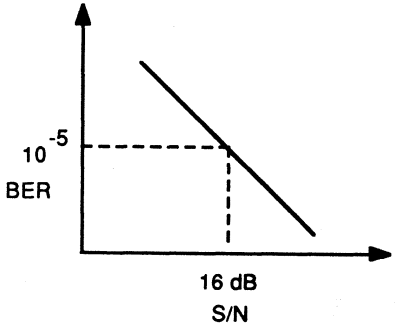


Figure 15. 2400 BPS BER vs. S/N

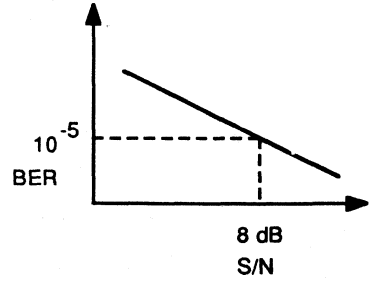
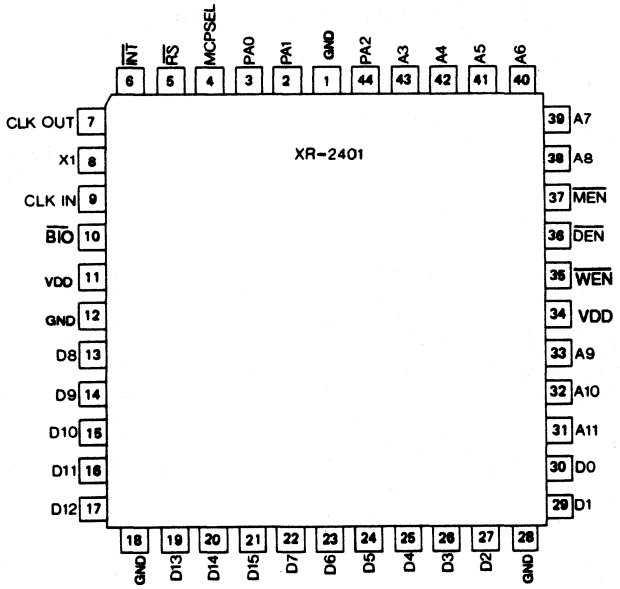
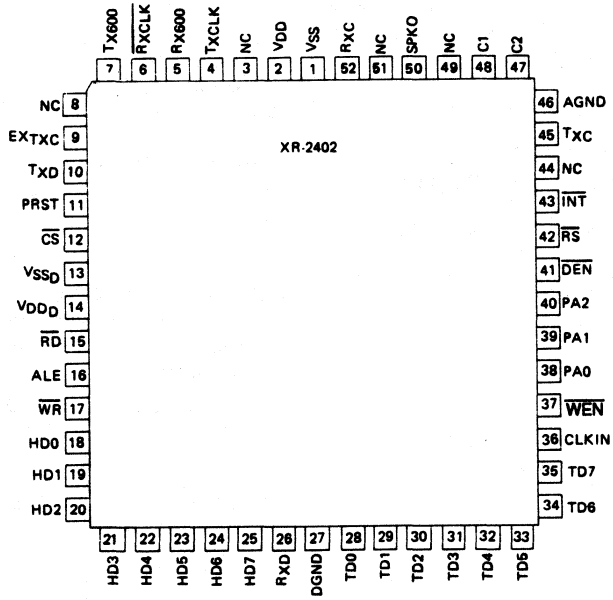


Figure 16. 1200 BPS BER vs. S/N


XR-2401
INT 6
RS 5
MCPSEL 4
PA0 3
PA1 2
GND 1
PA2 44
A3 43
A4 42
A5 41
A6 40
CLK OUT 7
X1 8
CLK IN 9
BIO 10
VDD 11
GND 12
D8 13
D9 14
D10 15
D11 16
D12 17
39 A7
38 A8
37 MEN
36 DEN
35 WEN
34 VDD
33 A9
32 A10
31 A11
30 D0
29 D1
18 GND
19 D13
20 D14
21 D15
22 D7
23 D6
24 D5
25 D4
26 D3
27 D2
28 GND


XR-2402
TX600 7
RXCLK 6
RX600 5
TXCLK 4
NC 3
VDD 2
VSS 1
RXC 52
NC 51
SPKO 50
NC 49
C1 48
C2 47
NC 8
EXTXC 9
TXD 10
PRST 11
CS 12
VSSD 13
VDDD 14
RD 15
ALE 16
WR 17
HD0 18
HD1 19
HD2 20
46 AGND
45 TXC
44 NC
43 INT
42 RS
41 DEN
40 PA2
39 PA1
38 PA0
37 WEN
36 CLKIN
35 TD7
34 TD6
21 HD3
22 HD4
23 HD5
24 HD6
25 HD7
26 RXD
27 DGND
28 TD0
29 TD1
30 TD2
31 TD3
32 TD4
33 TD5

V.22bis High Performance AFE

GENERAL DESCRIPTION

The XR-2402A High Performance AFE (Analog Front End) is designed to directly interface to the XR-2401 DSP Modem Signal Processor to provide the complete V.22bis 2400 BPS modem function. The XR-2401 is described in detail on the XR-2400 datasheet.

The XR-2402A is a redesigned, enhanced version of the XR-2402. While maintaining pin-to-pin compatibility with the XR-2402, the XR-2402A offers improved low signal level performance. Circuitry has also been added for speaker volume (during CPM) control under 'AT' command set control (ATL 0,1,2,3).

The XR-2402A provides analog interface functions to support the XR-2401 DSP such as, 8 bit D/A and A/D converters allow analog signals to get into and out of the digital XR-2401 DSP chip. Also included are band splitting filters (SCF type), a programmable gain amplifier (PGA), synchronous to asynchronous and asynchronous to synchronous conversion, guard tone generation (CCITT Operation), and timing recovery circuitry.

The XR-2402A is constructed with Si-Gate CMOS technology for low power operation. The XR-2402A is available in a 48 pin DIP or 52 pin PLCC package, and operates from ±5 Volt power supplies.

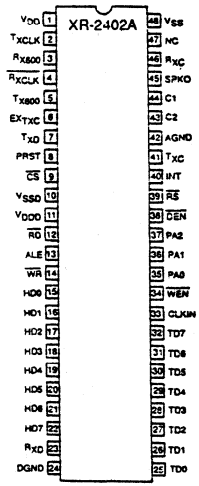
FEATURES

(When used with the XR-2401 DSP)
Pin-to-Pin Compatible with XR-2402
Improved Low Level Performance (Compared to XR-2402)
2400 BPS (QAM), 1200 BPS (PSK), 300 BPS (FSK) Operation
V.22bis, V.22, 212A, 103 Compatible
Bus Structure Control
DTMF Control
Low Power CMOS (110 mw typ)
Power - Down Mode
Asynchronous / Synchronous Operation
Speaker Volume Control Via Control Register
MNP 5 Operation with XR-2403A/B
V.42bis Upgradable with XR-2442

APPLICATIONS

Stand-alone Modems
Internal Modems
Laptop Applications
Low Power Applications

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Power Supply	
VDD	-0.3 to +7V
VSS	+0.3 to -7V
Input Voltage	VSS -0.3V to VDD +0.3V
DC Input Current (Any Input)	±10 mA
Power Dissipation (Package Limitation)	1 Watt
Storage Temperature Range	-65°C to +125°C

ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-2402ACP	Plastic Dip	0°C to 70°C
XR-2402ACJ	Plastic PLCC	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2402A offers additional features and performance enhancements over the original XR-2402, such as;

	XR-2402A	XR-2402
Speaker Volume Control	Internal	External Latch and 2 transistors
Minimum Receive Level for Error-Free Operation	-45dBm	-43dBm
Typical Power Consumption	110 mw	160 mw

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{DD} = 5V ±5%, V_{SS} = -5V ±5%, f_{CLKIN} = 4.9152 MHz ±0.01%, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{DD}	Positive Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Negative Supply Voltage	-5.5	-5.0	-4.5	V	
I_{DD}	Positive Supply Current		11	20	mA	
I_{DDS}	Positive Supply Current Standby mode		3	5	mA	
I_{SS}	Negative Supply Current		11	20	mA	
I_{SSS}	Negative Supply Current		3	5	mA	
V_{IH}	High Level Input Voltage	2.0			V	
V_{IL}	Low Level Input Voltage			0.8	V	
I_{OH}	High Level Output Current			300	µA	V_{OH} = 2.4V
I_{OL}	Low Level Output Current			2	mA	
V_{OH}	High Level Output Voltage	2.4			V	I_{OL} = 700 µA
I_I	Input Current			50	µA	V_I = 0 to V_{DD}
R_{XC}	Receive Carrier Range	-45		-6	dBM	Using 6/16 dB RCVG feature. (Pin 46 is 3 dB higher than tip and ring)

TRANSMITTER SPECIFICATIONS

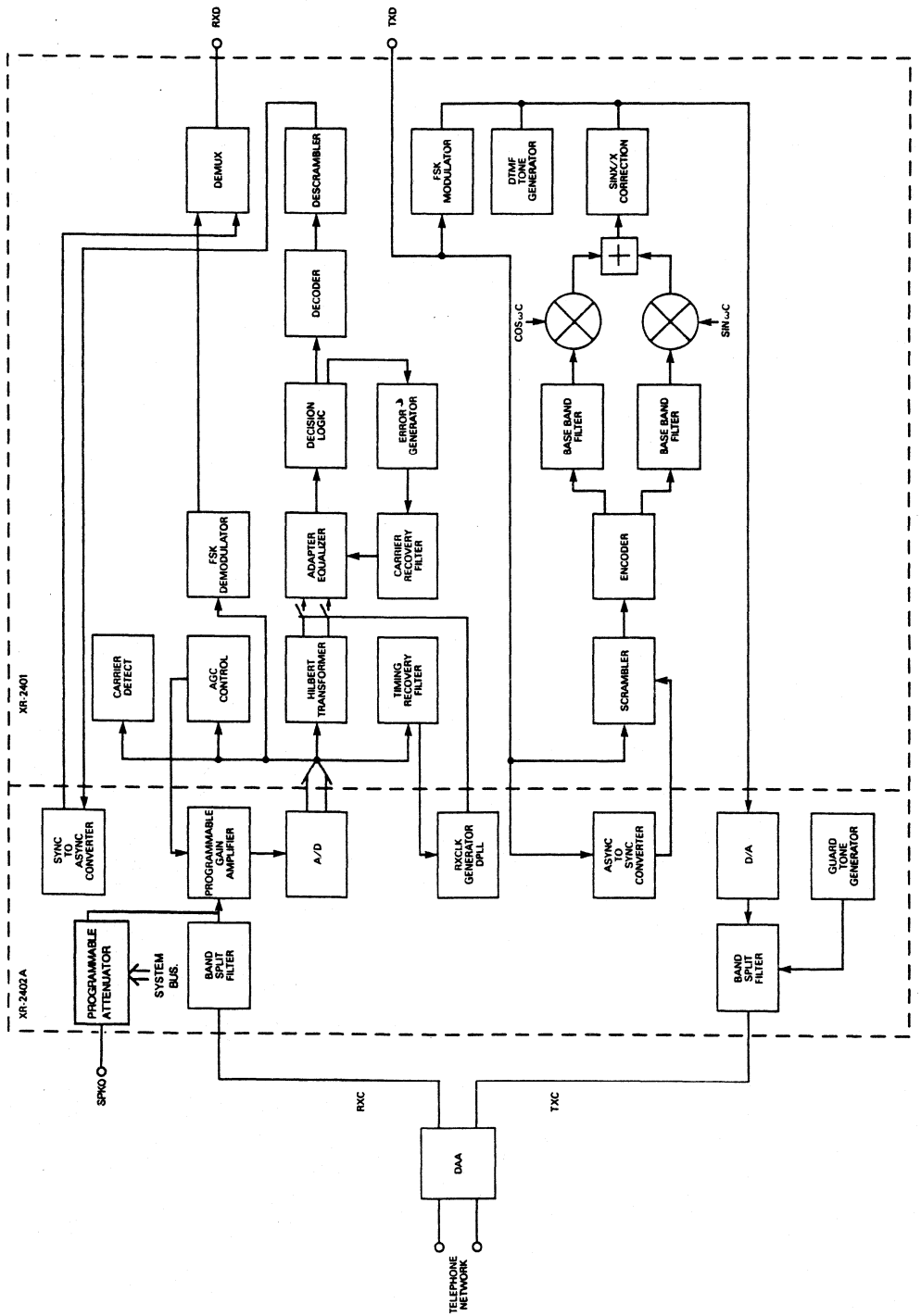
All values are measured at T_{XC} (Pin 41) of the XR-2402A with Bit 0-2 = 1 of CNTRL 0.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
TRANSMITTER POWER						
T_{XC} QAM/PSK	QAM/PSK Transmitter Power		+2		dBm	
T_{XC} 550	CCITT Guard Tone Power	-2		0	dBm	T_{XC} = 2dBM
T_{XC} 1800		-5		-7	dBm	T_{XC} = 2dBM
T_{XC} QAM/PSK 550	QAM/PSK Transmitter Power With Guard Tone		+3.5		dBm	
T_{XC} QAM/PSK 1800			+3		dBm	
T_{XC} FSK	FSK Transmitter Power		+1		dBm	
T_{XC} AT	Answer Tone Power		+1		dBm	
T_{XC} DTMF C	DTMF Tone Power Column		-5		dBm	
T_{XC} DTMF R	DTMF Tone Power Row		-4		dBm	
T_{XC} DTMF T	DTMF Tone Power Twist		-1.5		dBm	

SYSTEM PERFORMANCES (Performance Test Set-up Shown in Figure 1)

VRXD = -40 dBM, Originate Mode, C2, 3002, or B/B Line Conditions, T_{XC} = -10 dBm.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
S/N	Signal-to-Noise Ratio		16		dB	2400 BPS
			9		dB	1200 BPS
			12		dB	300 BPS
FOFF	Frequency Offset		±10		Hz	2400/1200 BPS
R_{XC} Min	Minimum Receive Carrier Carrier Level For Error Free Operation		-45		dBm	2400 BPS


RXD
TXD
DEMUX
DESCRAMBLER
FSK MODULATOR
DTMF TONE GENERATOR
SIN(X)/X CORRECTION
DECODER
COS ωC
SIN ωC
DECISION LOGIC
ERROR GENERATOR
BASE BAND FILTER
BASE BAND FILTER
FSK DEMODULATOR
ADAPTER EQUALIZER
CARRIER RECOVERY FILTER
ENCODER
CARRIER DETECT
AGC CONTROL
HILBERT TRANSFORMER
TIMING RECOVERY FILTER
SCRAMBLER
XR-2401
SYNC TO ASYNC CONVERTER
PROGRAMMABLE GAIN AMPLIFIER
A/D
RXCLK GENERATOR DPLL
ASYNC TO SYNC CONVERTER
D/A
GUARD TONE GENERATOR
PROGRAMMABLE ATTENUATOR
SYSTEM BUS
BAND SPLIT FILTER
BAND SPLIT FILTER
XR-2402A
SPKO
RXC
TXC
DAA
TELEPHONE NETWORK

MICROCONTROLLER OPTIONS

The XR-2402A, when used with the XR-2401 modem DSP (See XR-2400 Datasheet for details) forms the complete V.22bis modem data pump function.

The XR-2402A/2401 pair, XR-2400A, requires a modem controller for supporting intelligent functions such as Hayes 'AT' command control or MNP (Microcom Networking Protocol) control.

The XR-2400A has been designed with a very flexible interface to accommodate various common microcontrollers. Exar provides a number of different options and programs to minimize the design cycle. In each case, production worthy, commented source code is provided for use as is or for user customization to individualize each particular design.

The following is a list of current standard controller options available. Refer to Figure 2 for general connection.

CONTROLLER	FUNCTION	EXTERNAL EPROM	ADVANTAGES
1) 8031	Non-MNP	8K - 2764 (V2.00 E)	External EPROM allows easy modifications and enhancements to controller program. Utilizes inexpensive off-the-shelf µC.
2) XR-2404 (V2.00I)	Non-MNP Masked Controller		Masked controller offers a minimum component count design. Ideal for designs such as laptops or pocket type modems. Refer to XR-2404 datasheet.
Non-MNP, Polling Auto-Band*			
MNP/Non-MNP, interrupt Auto-Band*			
3) 8031	Non-MNP, chip upgradeable to MNP 5	8K-2764 (V3.00)	As with option number 1, an easily enhanced architecture is realized. This option also allows upgradeability to MNP 5 by simply changing chips (See Option 4).
4) XR-2403 A/B masked µC with MNP 5 function	MNP 5 same hardware as as option 3, but controller and EPROM are changed	8K-2764, XR-2403A 16K-27128, XR-2403B (V5.00) MNP 'AT'	This function was realized with the exact same hardware as option 3, but the following chip changes were made: 8031 → XR-2403 A/B; 2764 ('AT') → 27128 ('AT' / MNP); 8K SRAM. Refer to XR-2403B datasheet.
5) XR-2442 Masked µc with V.42bis/ MNP5 function	V.42bis/MNP5 same hardware as options 3 and 4 controller EPROM, and SRAM are changed	32K - 27256 (V 7.00) MNP/ V.42bis/ 'AT'	This function was realized with the exact same hardware as option 3, but with the following chip changes: XR-2403A/B → XR-2442; 27128('AT'/MNP) → 27256 ('AT'/MNP/ V.42bis); 8K SRAM → 32K SRAM

* The importance of these are that µC's from polling auto-baud cannot be substituted into interrupt type or the reverse.

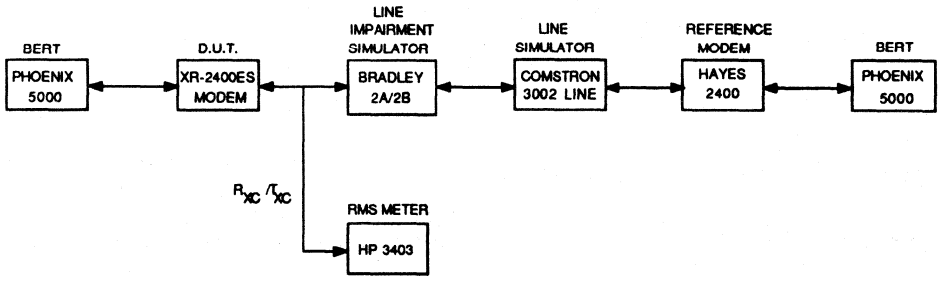


Figure 1. Performance Test Set-Up

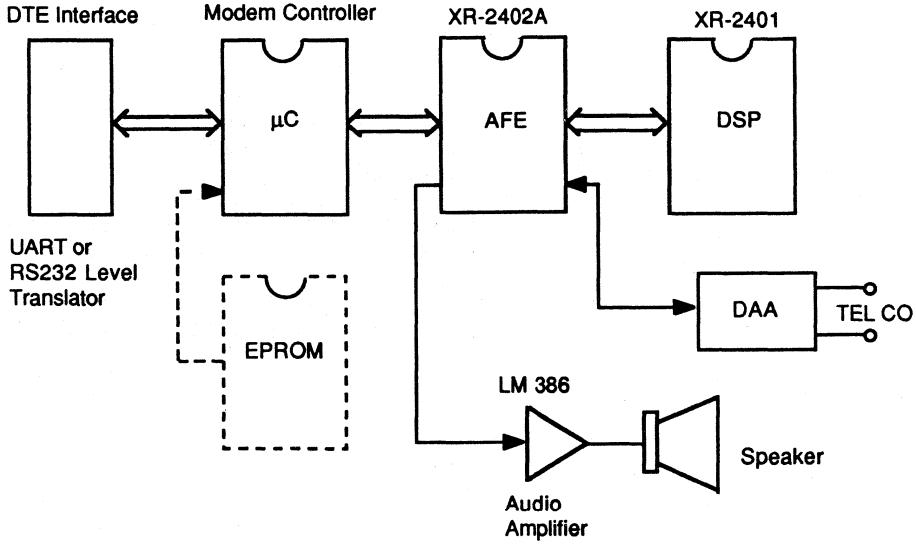


Figure 2. Typical System Connection

APPLICATIONS INFORMATION

Detailed descriptions and operation of the XR-2402A may be found on the XR-2400 datasheet which describes the pin-to-pin and functionally equivalent XR-2402. The information provided here is additional.

Speaker Volume Control

The XR-2402A provides a complete digitally controlled, three level, speaker driver. The control for the driver is located in:

Location 60H - CNTRL 0

Bit	Description
0 TXL1	
1 TXL2	
2 TXL3	
3 SPKR	On/Off (O = Off)
4 TST1	(Exar Special Test Mode)
5 TST 2	(Exar Special Test Mode)
6 SPKR 1	Speaker Control LSB
7 SPKR 2	Speaker Control MSB

The output levels relative to command/logic levels are:

Gain From RXCAR (P46) to SPK0	Bit 7	Bit 6
6 dB	0	0
-3 dB	0	1
-3 dB	1	0
-12 dB	1	1

DESIGN CONSIDERATIONS

A complete external or stand-alone type V.22bis modem is shown in Figure 3. This modem uses option 1, the non-MNP, ROMLESS, µC.

Several design considerations must be followed in order to ensure optimum system performance, as follows:

1. System Grounding - The XR-2402A provides both analog and digital grounds. These grounds should be separate up to the actual power supply ground, and single point connected there.

2. Power Supplies - Power supply bypassing should be provided at several points throughout the PCB. At the power input both a high frequency capacitor (0.1µF) and larger type (4.7 µF) for current transients. Particular should be taken to provide bypassing for the XR-2403A, located near the chip.

3. Receive Carrier Input R_{XC} - Care must be taken to route the RXC trace such that it is not near any crystals or logic IC's. in order to keep a clean layout the XR-2402A should be placed on the printed circuit layout near the telephone interface (DAA).

PERFORMANCE

One of the main parameters used as the yardstick to compare modems is the probability of producing errors while subjected to noise, commonly known as bit error rate verses signal-to-noise ratio (BER vs. S/N). The data supplied here was measured by an independent modem test house, Telequality Ass. in Colorado.

The curve in Figure 4 was generated from the modem in Figure 3. This test is purely a measure of the data pump, XR-2402A/XR-2401.

TELEQUALITY BER VS S/N TEST RESULTS

SNR MAP

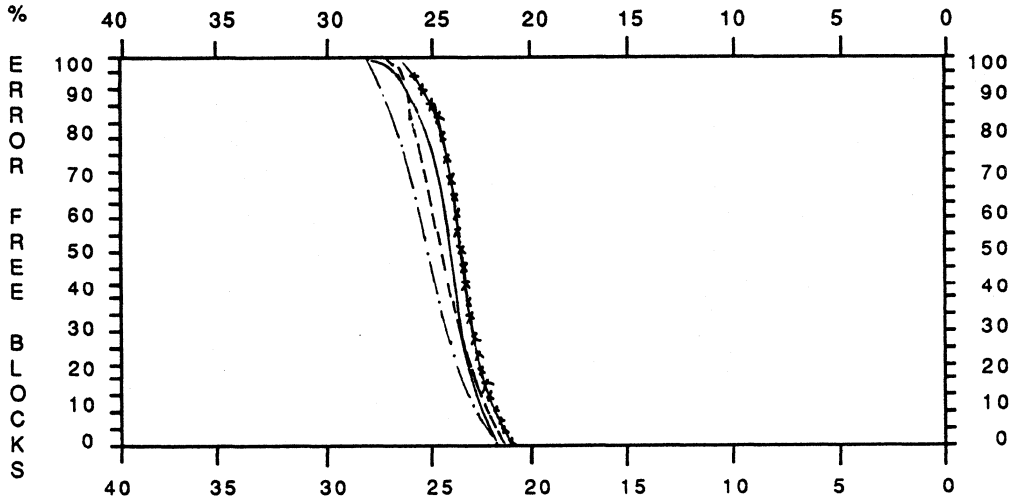
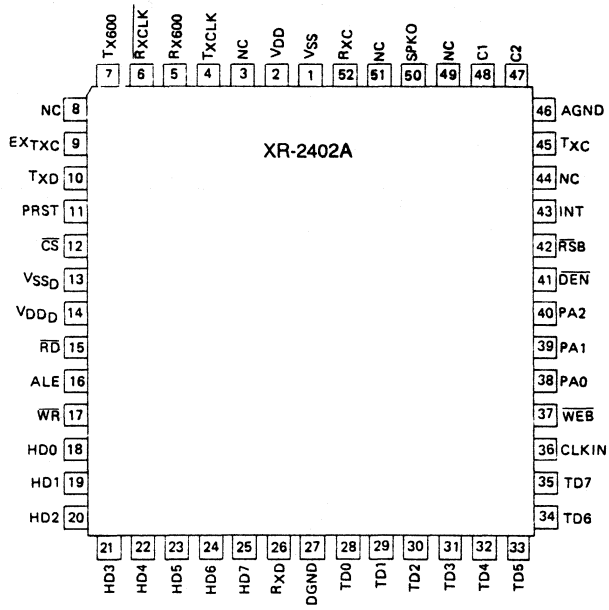


Figure 4. BER vs. S/N

EXAR 2400ES
IN ORIGINATE MODE
RECEIVING FROM CONCORD 224
AT 2400 BPS OVER
3002 LINE SIMULATOR

SIGNAL LEVEL (1004 Hz)
-12 dBm
-26 dBm
-32 dBm
-35 dBm


XR-2402A
TX600 7
RXCLK 6
RX600 5
TXCLK 4
NC 3
VDD 2
VSS 1
RXC 52
NC 51
SPKO 50
NC 49
C1 48
C2 47
NC 8
EXTXC 9
TXD 10
PRST 11
CS 12
VSSD 13
VDDD 14
RD 15
ALE 16
WR 17
HD0 18
HD1 19
HD2 20
46 AGND
45 TXC
44 NC
43 INT
42 RSB
41 DEN
40 PA2
39 PA1
38 PA0
37 WEB
36 CLKIN
35 TD7
34 TD6
21 HD3
22 HD4
23 HD5
24 HD6
25 HD7
26 RXD
27 DGND
28 TD0
29 TD1
30 TD2
31 TD3
32 TD4
33 TD5

MNP® 5 MICROCONTROLLER

GENERAL DESCRIPTION

The XR-2403B is a dedicated microcontroller programmed to provide 'AT' and MNP command control for the XR-2400 V.22bis modem chip set. Coupled with the XR-2400 a modem supporting MNP (Microcom Networking Protocol) class 2-5 operation is easily implemented. The lower classes of MNP (2-4) ensure error free operation, while class 5 adds data compression which basically doubles (4800 BPS) data throughput.

The 8031 based XR-2403B also provides 'AT' command control with the actual command set supported in an external EPROM (16K Bytes) for maximum flexibility. Either use the complete command set supplied by Exar or modify it to meet your specific requirements.

The XR-2403B operates from a single +5 V power supply and offers low power operation with CMOS technology.

FEATURES

100% Reliable Data Transfer with MNP 2-4
Increased Data Throughput by MNP 5 Data Compression (~200%)
Industry Compatible Commands
Easily Modified/Enhanced Command Set
Offers Minor Chip Change Solution for MNP/Non-MNP Conversion (Same PC Board)
Optimal System Partitioning Provides High Data Throughput for Both Half and Full Duplex Operations
CCITT V.42 Compatible
Future V.42bis Chip Upgrade

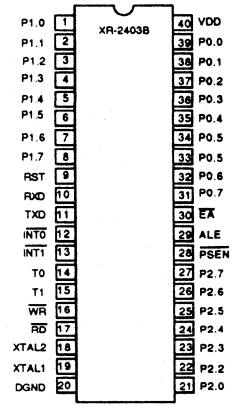
APPLICATIONS

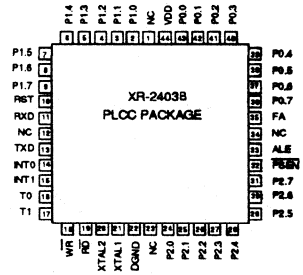
Modem Requiring Highly Reliable Data Transfer
Enhanced Throughput Applications - up to 200% (4800 BPS)
Low Power Designs Such as Laptop Applications

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.3V to + 7.0V
Input Voltage	-0.7V to (VDD +0.3) V
DC Input Current (any input)	± 10 mA
Power Dissipation (Pkg. Limitation)	1 watt
Storage Temperature Range	-65°C to + 125°C

PIN ASSIGNMENT





ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-2403BCP	Plastic	0°C to 70°C
XR-2403BCJ	PLCC	0°C to 70°C

SYSTEM DESCRIPTION

When coupled with the XR-2400 V.22bis chip set the XR-2403B allows the implementation of an error free, enhanced throughput V.22bis modem.

An Exar supplied 'AT' command set provides:
- Hayes® 'AT' Compatibility
- Microcom "\" Commands
- Optional Customized Code by Changing External EPROM Code

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 5V \pm 5\%$, $f_{CKLIN} = 11.0592\ MHz \pm 0.05\%$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	
I_{DD}	Power Supply Current		18	22.0	mA	$V_{DD} = 5.5V$
V_{IH}	Input High Voltage Except XTAL 1 and RST	1.8			V	
V_{IH}	Input High Voltage	3.5			V	XTAL 1 and RST
V_{IL}	Input Low Voltage			1.0	V	
V_{OH}	Output High Voltage Ports 1, 2, 3	2.4			V	$I_{OH} = -60\mu A$
V_{OH}	Output High Voltage Port 0 in Ext Bus Mode, ALE, $\overline{PSEN}$	2.4			V	$I_{OH} = -400\mu A$
V_{OL}	Output Low Voltage Ports 1, 2, 3			0.45	V	$I_{OL} = 1.6$ MA
V_{OL}	Output Low Voltage Port 0, ALE, $\overline{PSEN}$			0.45	V	$I_{OL} = 3.2$ MA
I_{IH}	Input High Current (Leakage)			±10	µA	$0.45 < Vin < V_{DD}$
I_{IL}	Input Low Current			50	µA	Vin = 0.45V

SYSTEM OPERATION

Figure 1 shows the interconnection of the XR-2403B and XR-2400 V.22bis chip set.

The XR-2400 provides the complete modem data pump function for 2400/1200/300 BPS modes. Command control is provided by the XR-2403B, both for MNP and 'AT' functions.

The 'AT' MNP commands reside in the 27128 (16K Byte) EPROM. Exar supplies this set to be used as is or modified to provide individuality to the modem. To allow customer modification, the source code is provided for the 'AT' / MNP commands. Also the entry points to the XR-2403B are provided to allow user modification (last section on datasheet).

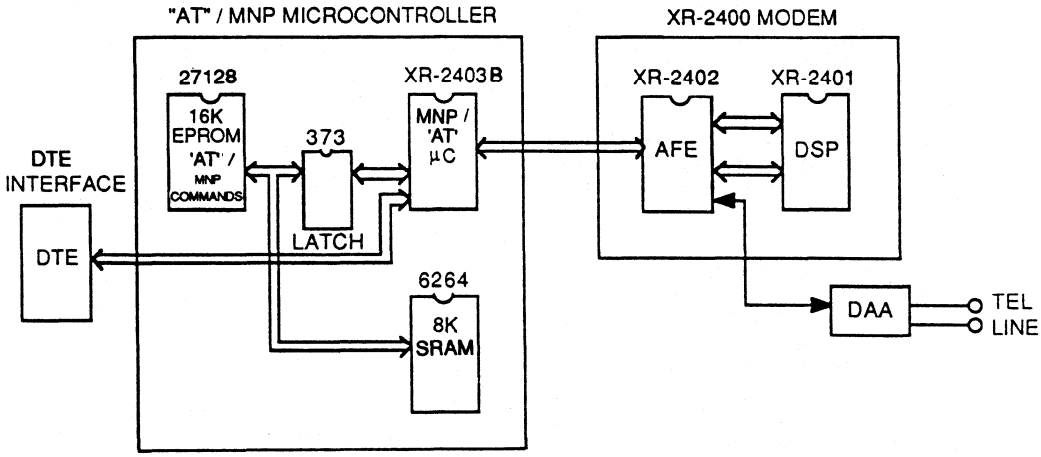


Figure 1. XR-2403B / XR-2400 System Configuration.

MNP OPERATION

To gain a better understanding of the XR-2403B operation and uses, the various modes, flow controls and other aspects of MNP must be understood. The following is provided to help with this understanding and its relation to the XR-2403B.

MNP, an acronym for Microcom Networking Protocol, was developed by Microcom, Inc., a modem manufacturer. Various classes of operation have emerged with class 1-5 operation most popular and being implemented on many 2400 BPS modems.

MNP Classes (Throughput data is based on 2400 BPS line speed).

Class 1 Is a half duplex protocol and not included in many new designs. Throughput was about 70% or 1690 BPS.

Class 2 Asynchronous operation with byte oriented data formatting. Throughput is roughly 84% of nominal or about 2000 BPS.

Class 3 Conversion to synchronous, bit oriented data handling is transmitted in blocks consisting of 1 to 64 characters. Throughput is about 108% or 2600 BPS. Class 3 was the "industry standard" in 1987.

Class 4 Basic characters are the same as class 3 but block size is dynamic (flexible size is based on data transmission quality). Throughput is 120% or 2900 BPS.

Class 5 Includes class 3 and 4 with data compression techniques added. The compression effectiveness is dependent on the type of data, but typical throughput enhancements are up to 200% or 4800 BPS.

ERROR CORRECTION

Error correction is added to modems to ensure 100% perfect data transfer. Software schemes have been most popular until recently, such as X modem and Kermit for async file transfer or SDLC and HDLC Async schemes for mainframe environments. The throughput for these software schemes vary but all reduce data transfer below its nominal rate or typically 91%, which equates to about 2200 BPS for 2400 BPS.

Hardware based MNP converts asynchronous data to be transmitted to a synchronous format (strips start and stop bits) for a bit oriented protocol. Typical throughput is about 108% or 2600 BPS.

Actual error correction is accomplished by first attaching a known data pattern to each block of data to be transmitted. Then the receiving side will check each block for the added data pattern and if found to be incorrect, will request the block to be retransmitted.

The data added to each block is based on a 16 bit CRC (Cyclic Redundancy Check) calculation of block of data to be transmitted. The receiving side then calculates each block's CRC value to determine if any errors existed and if retransmission is necessary.

The higher MNP classes 3-5, provide flexible block sizes to decrease the number of retransmitted blocks in poor environments such as noisy line conditions.

DATA COMPRESSION

MNP Class 5 offers data compression techniques to substantially increase a modem's data throughput over its basic line rate. MNP 5 utilizes a scheme which dynamically tabulates redundant characters. These characters are then transmitted in an abbreviated form to increase throughput as much as100% or 4800 BPS for a 2400 BPS modem.

To provide data transmission enhancement the DTE (Data Terminal Equipment) speed must be greater than the line speed. In order to accomplish this a data buffer is included at the transmit data input. The buffer acts as a reservoir to ensure data is not lost when DTE speeds exceed line speed.

The data buffer has a finite size and provision must be supplied to ensure it does not overflow and cause data loss. The method for controlling this condition is known as flow control.

FLOW CONTROL

As previously outlined, a method for regulating the flow of data to be transmitted is necessary when DTE data rates exceed line rates. Figure 2 illustrates a basic modem connection and helps illustrate where flow controls fit in.

Flow control can be under hardware or software control.

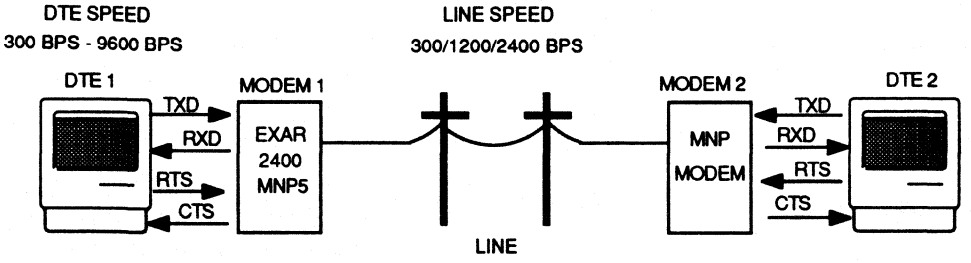


Figure 2. Basic Modem Configuration

HARDWARE FLOW CONTROL

Hardware Flow Control allows the modem to lower or raise its CTS (Clear to Send) line to the DTE. This provides an on/off control of data flow from DTE to modem. If the modem data buffer becomes full it lowers the CTS line to stop transmit data flow to allow the modem to "catch-up".

SOFTWARE FLOW CONTROL

An alternative to hardware flow control is controlled by software, known as Xon/Xoff.This is accomplished by special characters inserted into the data stream to start and stop data flow. Control Q (^Q) is used to start or restart data flow and control S (^S) to stop data flow.

Three different variations of Xon/Xoff control modes are:

- Send Only
- Normal
- Passthrough

For a detailed description of both the hardware and software flow control operation, refer to AN-37, Understanding Modem Flow Control.

XR-2403B MNP FUNCTIONS AND COMMANDS

The XR-2403B with external EPROM (16K x 8) provides control for the following major functions:

FUNCTION	DESCRIPTION
• 'AT' Command Control	Provides 'AT' Command Set Control
• MNP Level 2-4	Provides error correction for 100% perfect data transfer.
• MNP Level 5	Allows roughly a 100% increase (4800BPS for V.22bis mode) in data throughput, through data compression techniques.
• Speed Conversion	Maintain up to 9600 BPS DTE (terminal speed for 300 BPS to 2400 BPS line speeds, both for MNP and non-MNP connections.

A complete list of MNP functions and responsive commands are as follows:
Note: Default values are indicated by *

COMMAND	DESCRIPTION/RANGE - SIZE	FUNCTION
AT \ N0	Normal	Operating Mode
AT & E0 or \N1	Direct	
AT & E1 or \N2	Reliable	
AT & E2 or \N3*	Auto Reliable	
AT \ A0	64 Characters	Transmit Block Size
AT \ A1	128 Characters	
AT \ A2	192 Characters	
AT \ A3*	256 Characters	
AT%An	n = 0-127 ASCII	Auto-Reliable Fallback Character
AT \ L0*	Stream Link	Block MNP Link
AT \ L1	Block Link \L1 = \L0	(Stream Mode)
AT \ O	Initiate Reliable Link After Escape Command Independent of Modem Initial mode (ANS or ORG)	Originate Reliable Link
AT \ U	Accept Reliable Link after Escape Command request from Initiator of LInk	Accept Reliable Link
AT \ Y	Establish Reliable Link after Connecting in Normal Mode	Switch to Reliable Mode
AT \ Z	Switch to Normal Mode After Establishing a Reliable Link	Switch to Normal Mode
AT & E1 or % C0	MNP 5 Disabled	Compression On/Off Control
AT & E2 or % C1*	MNP 5 Enabled	

Note: AT & E1 $\triangleq$ AT \ N2 % CO
AT & E2 $\triangleq$ AT \ N2 % C1

COMMAND	DESCRIPTION / RANGE - SIZE	FUNCTION
AT \ V0*	Standard Non-MNP Result Codes	Result Code Form
AT \ V1	Modified MNP Result Codes (As Listed Below)	
AT \ Bn	N = 0 - 9 (100ms Increments) Disable Transmitter Break Default = 0	Transmit Break for Normal Data Mode
AT \ C	Not Functional	Set Auto-Reliable Buffer
AT \ K1	Empty Data Buffers And Immediately Send a Break to the Remote Mode	Break Control for Reliable Data Mode
AT \ K3	Immediately Send a Break to the Remote Terminal or Computer	
AT \ K5	Send a Break to the Remote Modem in Sequence With Any Data Received from the Serial Port	
AT \ K0,2,4	Not Supported (Will be equal to AT \ K5 if selected)	
AT \ Tn	N = 0-90 min N* = 0 (disable)	Inactivity Timer
AT \ I	Not Functional	Interface Protocol
AT \ J0	BPS Rate Adjust Disabled	Speed Conversion Control
AT \ J1*	BPS Rate Adjust Enabled	
AT \ S	Status Display	Read On-Line Status
AT \ G0*	Disables Modem Port Flow Control	Set Modem Port
AT \ G1	Sets Modem Port Flow Control to Xon / Xoff	Flow Control
AT \ X0*	Does Not Pass Xon / Xoff to Remote Modem	Xon / Xoff Pass Through Control
AT \ X1 or E7	Passes Xon / Xoff to Remote Modem	
AT \ Q0	Disable Flow Control	Serial Port Flow Control
AT \ Q1 or &E4	Bidirectional Xon / Xoff Enabled	
AT \ Q2*or &E6	Unidirectional Hardware Control by CTS	
AT \ Q3 or &E9	Bidirectional Hardware Control by RTS / CTS	
AT \ Q4 or &E8	UnidirectionalXon /Xoff Send Only	
AT % U	Not Functional	Clear Serial Port Speed Serial Port
AT - P0*	Ignores Parity for Special Characters	Check Parity
AT - P1	Processes Special Characters Only if they have Correct Parity	

See Command AT \ V1 Above

STANDARD RESULT CODES		MODIFIED RESULT CODES	
Verbose	Numerical	Verbose	Numerical
Connect	1	Connect 300	20
Connect 1200	5	Connect 1200 / REL 4 or 5	22
Connect 2400	10	Connect 2400 / REL 4 or 5	23

APPLICATIONS INFORMATION

Figure 7 illustrates a complete stand-alone version of a V.22 bis modem incorporating MNP 5 operation.

SYSTEM PERFORMANCE

Performance was measured on a 2400 BPS modem supporting MNP class 2-5 as shown in Figure 3.

Beyond error correction, giving 100% reliable data, data compression operation (class 5) is often the parameter used for comparison purposes.

When measuring data throughput several conditions must be considered. First the speed of data transfer may vary depending on full or half duplex data transfer. This condition will occur if the MNP implementation is processor speed limited. Exar's implementation yields identical throughput for both half or full duplex.

A second consideration is the type of data to be transferred. The efficiency of the MNP 5 data compression is a function of data redundancy. For example a data pattern of "...abab..." would yield an extremely high throughput, roughly 240% of nominal. On the other hand, the standard "quick brown fox" pattern with little redundancy yields a throughput in the 175% area.

Figure 3 shows the effective data throughput for the XR-2400 MNP chip set for various data patterns. The test set-up used is shown in Figure 4.

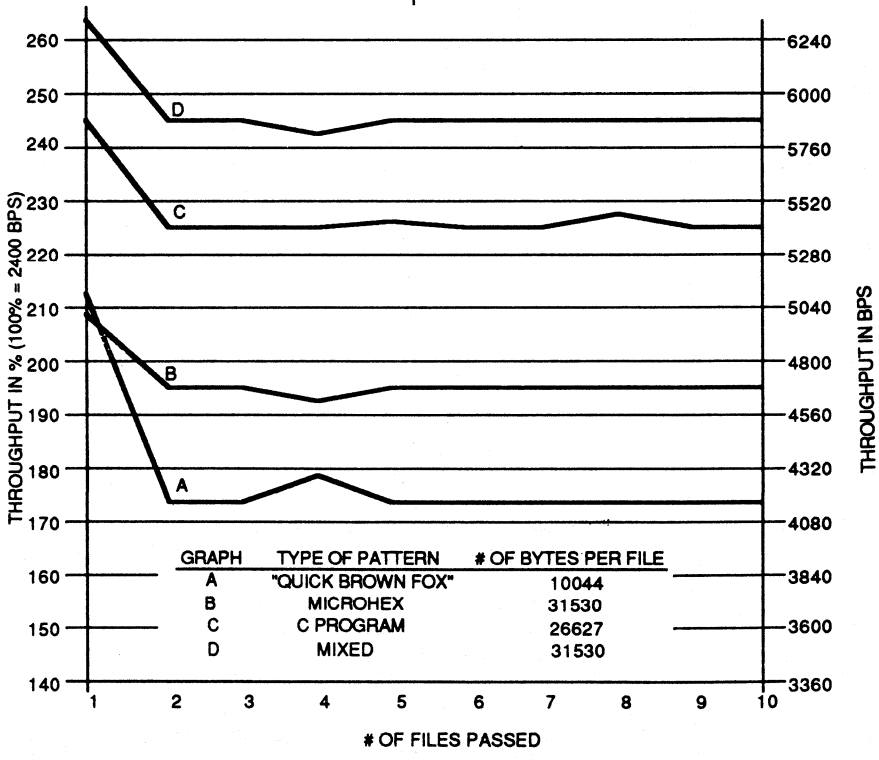
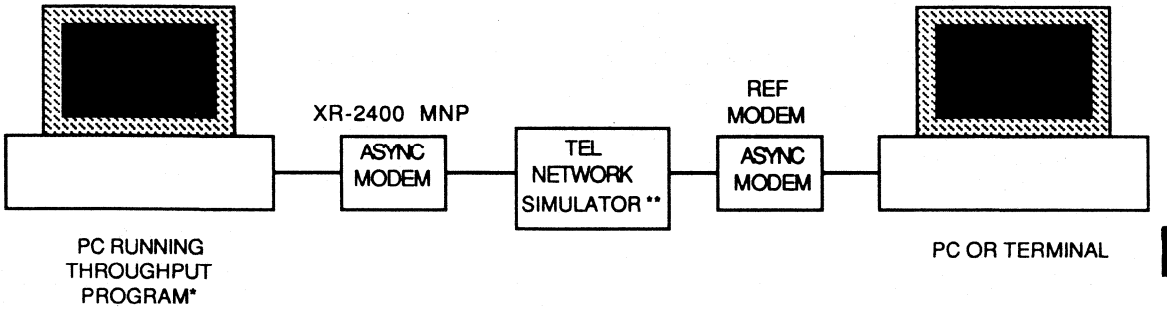


Figure 3. Effective Data Throughput

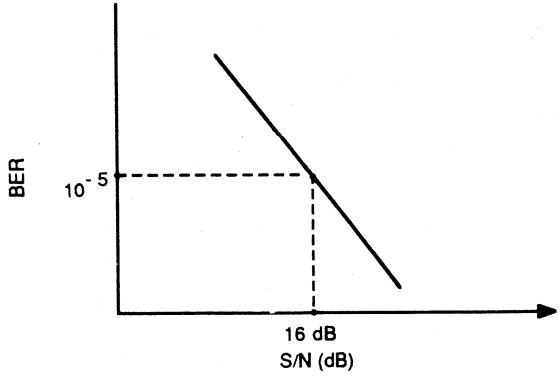


* APT (Asynchronous Performance Tester), also contains data or files to be used during measurement.
** Simulates line impairment and attenuation conditions.

Figure 4. MNP Throughput Measurement Test Set-up.

SYSTEM PERFORMANCE

The modem of Figure 7 was tested for data non-MNP mode. The curve in Figure 5 shows the probability of errors (BER) as a function of input signal-to-noise (S/N) ration. This curve was generated with the set-up as shown in Figure 6. The conditions of the set-up are indicated in Figure 5.



Conditions:
- 2400 BPS
- Originate Mode
- RXCAR = -40dBM
- 5KHz Noise Bandwidth

Figure 5. 2400 BPS BER vs S/N (Non-MNP Mode)

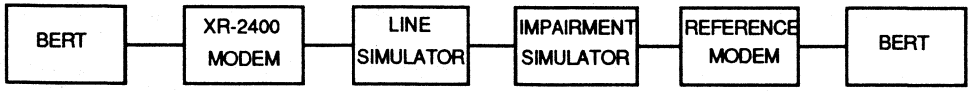


Figure 6. Data Quality Test Set-Up

ENTRY POINTS AND MEMORY MAPPING

The XR-2403B MNP 5 Microcontroller when used with the XR-2400 V.22bis chip set, provides a highly compatible MNP 5 / 'AT' 2400 BPS modem function, the architecture as seen in Figure 1, is open with regard to command set modification. This is accomplished by having both MNP and 'AT' commands residing in external EPROM.

To aid in customer modification of 'AT' or MNP commands, the following information is provided.

Entry Point Information

The XR-2403B is a masked 8031 type microcontroller with 8K of internal program memory. The internal program provides control for MNP and 'AT' functions. The MNP portion of the program is Exar proprietary. information and not accessible externally. However, to facilitate modification or enhancement of 'AT' or MNP commands, entry points to the MNP program are provided.

Status / Mode Setting Memory Locations

Status	Location	Description
PASS_B	9D14H	Escape Code Checking Byte in Speed Conversion Mode.
SPEED	9D15H	Speed Indicator For All Modes. 0 - 9600 BPS 1 - 4800 BPS 2 - 2400 BPS 3 - 1200 BPS 4 - 300 BPS
Z_BUF	9D16H	Auto Reliable Fallback Character.
MRCVP2	803BH	Disconnect to Check Auto-Reliable Fallback Mode.
SPD_FLG	20 H.7	Speed Conversion Enable Flag.
MNP_5	9E22H	Reliable Link Indicator
BACK-RAM	9D1AH	Starting Address for Command Buffer Back-up.
BK_PRE	51 H	Break Prescaler Timer
BK_TMR	52 H	Break Timer
OPT_P	9D50H	Output Port Selection Option (F0FF H to 40 FFH). This Parameter is Initialized Immediately After Power On and constantly monitored by MNP Module.

Function Call Locations - MNP Program Entry Points

Function	Location	Description
EC_MAIN	0080H	Calling Main MNP Program. This is the only location which will initiate the MNP program.
MNP_IN	0066H	MNP Program Immediate Re-Entry Point for modifying MNP Program.
MSG_CPY	0063H	Exar Copyright Calling Subroutine.
MSG_CP	0030H	Exar Copyright Message.
P_ECRAM_1	0060H	After Escape MNP Re-Entry Point.
SPD_INM	0069H	Speed Conversion Program Jump-In Point.
INI_SPDM	006CH	Speed Conversion Initialization Routine.
SCTINT_1	0006H	Interrupt 0 Jump-In Point.
SCRINT_1	0016H	Interrupt 1 Jump-In Point.
SPINT_1	0026H	Serial Port Interrupt Jump-In Point.
V21_IN_1	006FH	300 BPS Speed Conversion Timer Set-Up.

XR-2403B Re-Entry Points

Function	Location	Description
PWR_ONS	C000H	Power On
OUT_SCT	C003H	Interrupt 0
OUT_T0	C006H	Timer 0
OUT_SCR	C009H	Interrupt 1
OUT_T1	C00CH	Timer 1
OUT_SP	C00FH	Serial Port Interrupt
OUT_T2	C0012H	Timer 2
MNP_OUT	C0015H	MNP Program Intermedia Point
CHK0705	C01BH	MNP 'ESC' Jump Out Point
DISCONNECT	SC01EH	MNP Disconnect
ON_LOOPS	C021H	Auto-Reliable Fallback Point.
SPD-OUTS	C024H	Speed Conversion Jump Out Point.
V21_INS	C027H	Call Speed Conversion ASM for 300 BPS.
SPD_TXD	C02AH	Put TXDATA to Modem Chip.
SPD_RXD	C02DH	Get RXDATA From Modem Chip.

RAM Locations

The stack in the 'AT' program starts from 0C0H on page 1 and occupies 64 bytes of space. Internal RAM on page 0 has 23 bytes and page 1 64 bytes of free space.

The external RAM data memory is as follows:

1) Error Control	8000H-8FFFH
2) Data Compression Buffer	9000H-93FFH
3) Break Buffer	9A00H-9AFFH
4) DTE TX Buffer	9B00H-9BFFH
5) DTE RX Buffer	9C00H-9CFFH
6) Misc. Registers	9D00H-9DFFH
7) MNP Program RAM Backup Buffer	9E00H-9EFFH
8) 'AT' Program RAM Backup Buffer	9F00H-9FFFH

Note: For program control, the XR-2403B backs up the entire 256 bytes of internal RAM into external RAM before jumping into or out of the MNP program. The 'AT' program RAM is 9F00H and MNP program RAM is 9E00H-9EFFH.

9) Customer Register	9H00H-99FFH

Interrupt Vectors

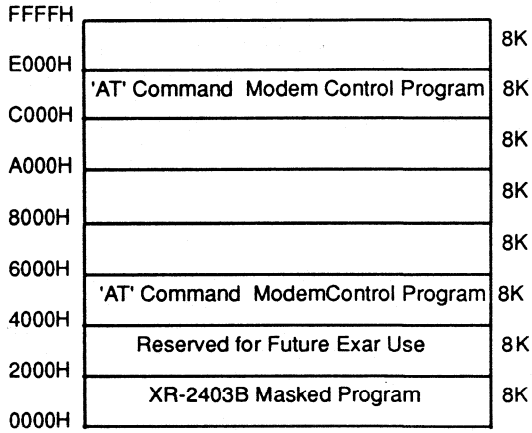
The XR-2403B brings out all interrupt vectors to the external program. This allows easy customer modification of service routines to suit a particular application. The interrupt vectors of the XR-2403B are as follows:

```
        ORG     0
        LJMP    PWR_ONS; Jump to Power
                         On Set Up Routine
        ORG     3H
EXT_INTO:                ; Interrupt 0 for SCT
        LJMP    OUT_SCT
SCTINT1:
        LJMP    SCTINT
        ORG     OBH
T_INTO:                  ;Timer 0 Interrupt
        LJMP    OUT_TO
        ORG     13H
EXT_INT1:                ;Interrupt 1 for SCR
        LJMP    OUT_SCR
SCRINT_1:
        LJMP    SCRINT
        ORG     1BH
T_INT1:                  ;Timer 1 Interrupt
        LJMP    OUT_T1
        ORG     23H
INT_SER:                 ;Serial Port Interrupt
        LJMP    OUT_SP
SPINT_1:
        LJMP    SPINT
        ORG     2BH
T_INT2:                  ;Timer 2 Interrupt
        LJMP    OUT_T2
```

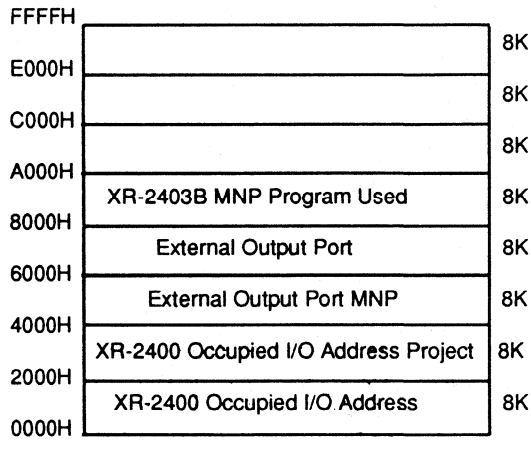
XR-2403B Program Memory Map

The following is a memory map for both external memory and external I/O.

External Program Memory Map



External Data Memory Map (OPT_P=1)



3

'AT' Command Set Modem Controller

GENERAL DESCRIPTION

The XR-2405 dedicated modem controller provides the "AT" command set for easier interfacing with the XR-2401 and XR-2402A V.22bis modem chip set. The XR-2405 eliminates the use of external EPROM is most applications and allows for a turn key solution in applications where the modem functions will be limited to that provided by most modems. However if MNP® is desired the XR-2403B,with EPROM SRAM and latch can be substituted on a board for the XR-2405.

The XR-2405 is pin for pin compatible with the XR-2403B. A single board (either 1/2 card,lap top computer or standalone can be designed that allows a simplification for Production Control: If the XR-2405 is used, the board is for the non-MNP market. If MNP® is desired, then the XR-2403B would be stuffed into the board. The XR-2405 cannot be used with the XR-2402, because of register conflicts. The XR-2405 is designed for use with the XR-2402A High Performance Analog Front End.

The XR-2405 is fabricated in CMOS for low power (100 mW typical) and is available in a 40 pin Dual-In-line Pin package or in a 44 pin PLCC (plastic leaded chip carrier). The XR-2405 operates with a single supply +5VDC and operates over the commercial temperature range (0°C to 70°C).

FEATURES

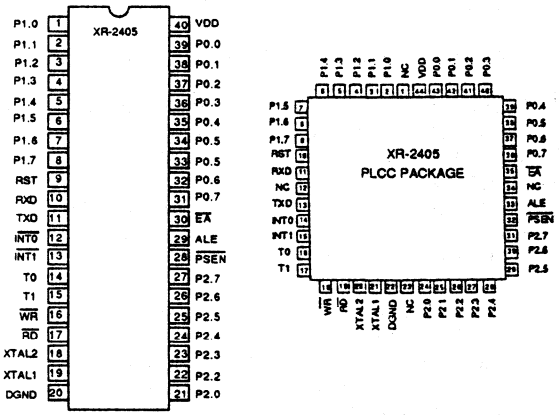
Complete "AT" Command set
- •leased line mode
- •synchronous data mode
- •Volume Control

Reduce modem parts count
Reduces Board Inventory: One board for MNP® and Non-MNP®
Uses Common 11.0592 MHz Crystal
Provides UART Clock (with 74HC194)
Low Power CMOS

APPLICATIONS

1/2 Cards modems for PC Using XR-2401 and XR-2402A
Stand alone modems using XR-2401 and XR-2402A
Lap Top Computer Modem Cards and Modules
Dedicated System Modems (for System updates over the phone)

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Voltage on VDD 6.5VDC
Voltage on any Pin -0.5 V to VDD +0.5V
Storage Temperature -65°C to +150°C
Power Dissipation (Package Limitation)
- 40 Pin Plastic
- 44 Pin PLCC

Derate above 25°C

ORDERING INFORMATION

Part #	Package	Operating Temp
XR-2405CP	40 Pin Plastic DIP	0°C to 70°C
XR-2405CJ	44 Pin PLCC	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2405 with its address/data lines interfaces with the XR-2401 and XR-2402A. With the addition of a OCTAL latch interface to the relay and hardware flow control signals is provided. The XR-2405 provides the advantage of reducing the number of PC boards that must be designed. Also, to add MNP® no jumpers would be needed on the board. Only the removal of the XR-2405, replacing it with the XR-2403B, 8kBytes of SRAM, a 16kByte EPROM and an address/data latch. If jumpers are added then the board could be upgraded to V.42bis and retain MNP® classes 2-5, by replacing the XR-2405 with the XR-2442 and using a larger EPROM.

V.42 / MNP®5 Microcontroller

GENERAL DESCRIPTION

The XR-2442 is a dedicated microcontroller that provides command control for the XR-2400 V.22bis modem chip set. The XR-2442 provides control for CCITT recommended V.42 error correction, including LAPM and MNP 2-4 protocols , with MNP class 5 data compression is included for greater compatibility. Also supported are the standard 'AT' commands.

The system architecture of the XR-2442/XR-2400 allows the actual command sets for the 'AT', MNP, and V.42 to reside external to the XR-2442, allowing ease of customization. Exar provides these command sets to use as is or modify to the requirements of your design.

The XR-2442 operates from a single +5 volt power supply, offering low power consumption through CMOS technology.

FEATURES *

Error Free Data Transfer
- LAPM
- MNP 2-4

Increased Data Throughput by MNP 5 Data Compression
- 4800 BPS Throughput

'AT' Command Control
Industry Standard Commands
- Easily Modified

Future Chip Upgrade to V.42bis (XR-2442B)
*(Apply when used with XR-2400 V.22bis modem chip set)

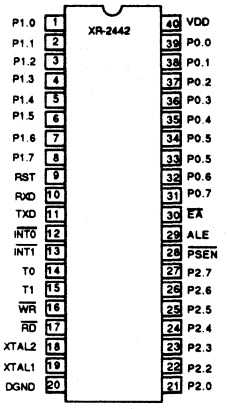
APPLICATIONS

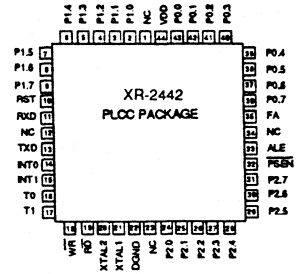
Error Free Modem Applications
Stand-Alone Modems
Smart Modems
Laptop Modems

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.3V to + 7V
Input Voltage	-0.7V to (VDD +0.3V)
DC Input Current (any input)	±10mA
Power Dissipation **(Package Limitation)**	1W
Storage Temperature Range	-65°C to +125°C

PIN ASSIGNMENT





ORDERING INFORMATION

Part #	Package	Operating Temp
XR-2442CP	40 Pin Plastic Dip	0°C to 70°C
XR-2442CJ	44 PIN PLCC	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2442, when coupled to the XR-2400 V.22bis modem chip set, allows the implementation of an error-free, increased throughput V.22bis modem.

The XR-2442 is just one in the family of controller options for the XR-2400 V.22bis modem chip set, including:

FUNCTION	CONTROLLER
'AT'	8031
'AT'/MNP 5	XR-2403B
'AT'/V.42/MNP 5	XR-2442
'AT'/V.42bis/MNP 5	XR-2442B*

* Future Product

V.23/V.21 Single Chip Modem

GENERAL DESCRIPTION

The XR-2321 is a single-chip asynchronous continuous phase FSK (Frequency Shift Keying) mode modem. Half or full duplex operation is possible over general switched network or leased line conditions. Modem functions and modes are selected through micro-controller bus structured interfaces. It is compatible with the CCITT recommended standards for V.21 and V.23 type modems.

The XR-2321 can be used with other higher speed Exar modem chips, such as the XR-2400 chip set in a V.22 bis/V.22/212A multi-modem application.

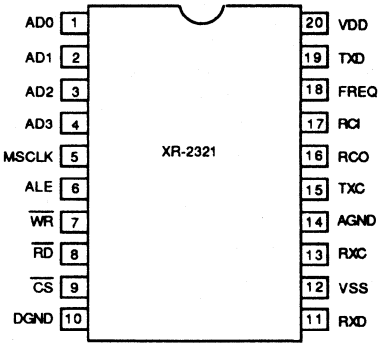
Switched capacitor techniques and CMOS technology are employed in the XR-2321 to perform all major filtering functions and modulation/demodulation respectively. The 75 BPS back channel is also provided when it is selected in V.23 mode.

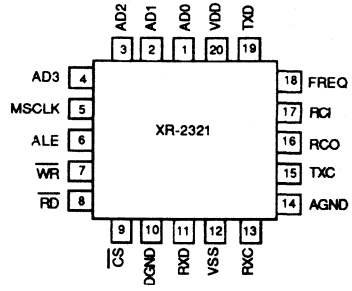
The XR-2321 is available in a 20 pin DIP or PLCC package. All the digital input and output signals are TTL compatible. Power supply requirements are +/-5 volts.

FEATURES

Dual FSK Modem Chip in a 20-Pin Package
CCITT V.21 (300 BPS Full Duplex) Compatible
CCITT V.23 (1200 BPS Half Duplex Mode 2)
Compatible, also with 75 BPS FSK Back Channel
No External Filtering Required
Analog Loop Back Test Mode
2 Wire Full Duplex for 300 BPS
2 Wire Half Duplex for 1200 BPS
Universal Microcontroller Interface
Low Power CMOS
Generator & Detector for Answer & Calling Tones
Power Down Mode
Line Equalizer Enable or Disable (Selectable)
XR-2100 Pin-to-Pin Compatible

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS

Power Supply	
VDD	-0.3 to 7V
VSS	0.3 to -7V
Input Voltage	VSS -0.3V to VDD +0.3V
DC Input Current	±10mA
Power Dissipation (Package Limitation)	
Plastic Dip	1W
Derate Above 25°C	
Plastic Dip	5mW/°C
Storage Temperature Range	-65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-2321 CP	Plastic	0°C to 70°C
XR-2321 CJ	PLCC	0°C to 70°C

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$, MSCLK = 11.0592 MHz ± 0.05%, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_{DD}	Positive Supply Current		11		mA	
	Power Down Mode		5		mA	
I_{SS}	Negative Supply Current		12		mA	
	Power Down Mode		5		mA	
V_{IH}	High Level Input Voltage	2.0			V	
V_{IL}	Low Level Input Voltage			0.8	V	
I_{OH}	High Level Output Current			300	µA	$V_{OH} = 2.4$ V
I_{OL}	Low Level Output Current			2	mA	
I_I	Input Current			50	µA	$V I = 0$ to V_{DD}
TXC	Transmit Carrier Output	-2	0	+2	dBM	FSK Carrier
RXC	Receiver Dynamic Range	-43		-10	dBM	ANS, ORIG mode.
CD off	Carrier Detect Off Level		-48		dBM	FSK
			-43		dBM	1300 Hz
			-37		dBM	2100 Hz
CD on	Carrier Detect On Level		-43		dBM	FSK
			-36		dBM	1300 Hz
			-30		dBM	2100 Hz
CD_{HYS}	Carrier Detect Hystersis	2	6		dB	FSK, 1300 Hz, 2100 Hz

SYSTEM PERFORMANCE Transmit Level = -10dBm*, Receive Level = -40dBM*
Conditions: Noise BW = 5KHz, C2, 3002, B/B Line Conditions, 511 PRBP

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V.21 MODE						
S/N	Signal-to-Noise Ratio		7		dB	BER < 10^{-5}
BIAS DIST	Bias Distortion		6 6		% %	ORIG Mode ANS Mode
V.23 MODE						
S/N	Signal-to-Noise Ratio		15		dB	BER <10^{-6} Primary Channel Receive Reverse Channel Transmit.
BIAS DIST	Bias Distortion		 7 7		 % %	Primary Channel ORIG Mode ANS Mode
S/N	Signal-to-Noise Ratio		7		dB	BER <10^{-5} Reverse Channel Receive Primary Channel Transmit
BIAS DIST	Bias Distortion		 5 5		 % %	Reverse Channel ORIG Mode ANS Mode

FREQUENCY PARAMETERS

Mode	Baud Rate (BPS)	Duplex	Transmit Frequency		Receive Frequency		FREQ Accuracy (Hz)
			Space (Hz)	Mark (Hz)	Space (Hz)	Mark (Hz)	
CCITT V.21 ORIG.	300	FULL	1180	980	1850	1650	+/-2
CCITT V.21 ANS	300	FULL	1850	1650	1180	980	+/-2
CCITT V.23 Primary	1200	HALF	2100	1300	2100	1300	+/-6
CCITT V.23 Reverse	75	HALF	450	390	450	390	+/-2

Answer Tone Frequency: 2100 Hz +/- 6Hz
* The level is measured at Tip and Ring with 600Ω load.

PIN DESCRIPTIONS

Name	Pin #	I/O	Description
ADO - AD3	1,2,3,4	I/O	Address/Data bus for microcontroller.
MSCLK	5	I	External master clock input of 11.0592MHz +/- .01%.
ALE	6	I	Address latch enable from microcontroller.
$\overline{WR}$	7	I	Write Enable for microcontroller. Active Low.
$\overline{RD}$	8	I	Read Enable for microcontroller. Active Low.
$\overline{CS}$	9	I	Chip select. This enables the 4-bit parallel bus on the XR-2321.
DGND	10	I	Digital Ground. This pin should be routed separately from the AGND trace to the power supply.
RXD	11	O	Demodulated receive data output for V.21, V.23 main or reverse channel.
VSS	12	I	Negative power supply -5V +/- 5%. A 0.1µF ceramic bypass capacitor should be placed near the device.
RXC	13	O	Analog receive carrier input for V.21, V.23 or backward channel signal.
AGND	14	I	Analog Ground. This pin should be routed separately to the DGND to the power supply.
TXC	15	O	Analog transmit carrier output for V.21, V.23 or backward channel signal.
RCO, RCI	16,17	I/O	Receive filter output and demodulator input require 0.1µF +/- 10% ceramic capacitor connected between them.
FREQ	18	O	This provides a TTL compatible limited output of the signal received.
TXD	19	I	Transmit data input for V.21, V.23 main or reverse channel.
VDD	20	I	Positive power supply, +5V. A 0.1 µF ceramic bypass capacitor should be placed near the device.

FUNCTIONAL DESCRIPTION

As outlined in Figure 1, the XR-2321 consists of three main sections which perform the functions of transmitter, receiver and logic control.

Transmitter

The transmitter section consists of a Frequency Shift Keying (FSK) modulator, a Digital-to-Analog (D/A) converter, transmit filter, and an output gain stage. Its primary function is to convert binary digital data into a corresponding analog signal suitable for transmission on the telephone line system.

The binary data appears at the input of the FSK modulator at the TRANSMIT DATA (TXD) pin. The modulator creates a digitally synthesized sine wave at a given frequency depending on whether a logic 1 or logic 0 is present at the TXD pin. Following a digital filtering stage in the FSK modulator, this digital representation is converted into an analog signal by the DAC. The signal is then filtered by the transmit filter which is implemented using switched capacitor techniques. The resulting signal is finally smoothed using a continuous time low-pass filter and amplified by a programmable gain stage. The FSK-modulated carrier is then brought to the output TRANSMIT CARRIER (TXC) pin, and normally applied to the phone line through a Data Access Arrangement (DAA) interface or an acoustic coupler.

Receiver

The receiver consists of an anti-aliasing filter, a receive filter, a tone conditioner, a slicer, a FSK demodulator, a carrier detector, and a post-detection filter. Its function is to recover the binary digital information from the received analog signal.

The FSK-modulated carrier is received through a DAA or acoustic coupler and fed to the RECEIVE CARRIER (RXC) input pin. The signal is first presented to a simple low-pass anti-aliasing filter and then routed to both the receive band-pass filter and the tone conditioning section. This latter section provides a TTL compatible limited output of the received analog signal at the FREQUENCY OUTPUT (FREQ) output pin. Along the other route, the receive filter band limits the signal and passes it to the slicer section which creates a digital bit stream. This bit stream is processed by the FSK demodulator and passed through a post-detection filter. The resulting signal is squared off by the output comparator section whose output now represents the recovered data pattern. This is made available at the RECEIVE DATA (RXD) output.

A CARRIER DETECT (CD) signal is also generated from the received line carrier after the receive filter. The CD signal, which is used to indicate the presence of valid data, is read via the data bus by addressing the READ register of the XR-2321. Control programming information is discussed in the following section.

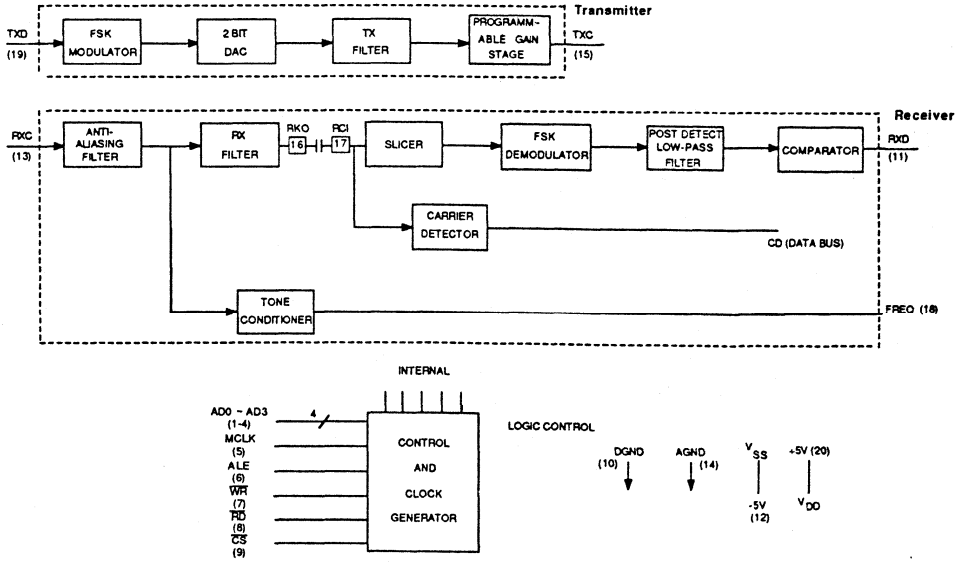


Figure 1. Functional Block Diagram

CONTROL PROGRAMMING INFORMATION

Operation of the XR-2321 is programmed via the read and write registers which are accessed by the AD0-AD3 pins. Control and mode configuration is achieved by writing control words into the appropriate write register, while status and data information can be read from the read register. Read/write register address locations are given in Table 1.

Register bit formats are shown in Table 2. By following the READ/WRITE cycle procedure outlined in Figure 2, the individual bits can be accessed. Figure 2 outlines the timing applicable to interfacing the XR-2321 with the 8031 or alike modem controllers.

Write Register Bit Description

ALB - Analog Loop Back

This bit will activate analog loop-back mode for diagnostic testing purposes.

RXDMK - Receive Data Mark

By setting this bit high, the user can force the RXD output pin high continuously. This is useful when performing functions such as handshaking protocol and/or CD is off.

A/O - Answer/Originate Mode

In the low state, this bit will configure the modem in originate mode and conversely, when set high, the modem will be in answer mode.

TONE/FSK - Transmit Tone or Transmit FSK Modulated Carrier

This bit controls the TXC output pin to transmit the 2100 Hz answer/ 1300 Hz calling tone when the bit is set high. When low, TXC will be the standard FSK-modulated carrier. (Note: TONE/DTMF = 1 for tone operation.)

TXD - Transmit Data

This bit is the data bit to be transmitted and is loaded via the data bus.

PDN - Power Down Mode

When selected, all sections of the device are powered off except for the control section. This mode allows for reduced power consumption when the modem is not receiving or transmitting.

TXEN - Transmitter Enable

When set low the transmitter output is disabled.

CPM - Call Progress Mode

This bit is set high when the modem is attempting call establishment in originate mode by monitoring dial tone, ring back tone or busy tone.

TONE/DTMF

With this bit set high, the transmitter will operate at tone frequencies corresponding to the given configuration. When set low, the transmitter is set to DTMF mode and follows the configuration programmed in the DTMF Bit Select register.

V.23/V.21

This configuration bit is to set the modem in V.23 or V.21 communications mode. V.23 is selected with this bit high, while V.21 is set with this bit low.

PTXD - Parallel Transmit Data

This bit allows the user to select whether data to be transmitted is loaded from the parallel data bus, or if it is to be loaded serially from the TXD pin. With PTXD set low, data is taken from pin 19 (TXD).

DTH3 - DTH2/DTL1 - DTL0 - DTMF Bit Select

These bits are used to set the DTMF frequencies to be transmitted. The bits are programmed according to Table 4 - DTMF Bit Selectable Table.

TX3 - TX0 - Transmit Gain Bit Select. Refer to Table 5 for gain selection.

Read Register Bit Descriptions

FREQ - Frequency Output

Reading from this bit is equivalent to pin 18 FREQ output. It provides a TTL version of the received analog signal.

CD - Carrier Detect

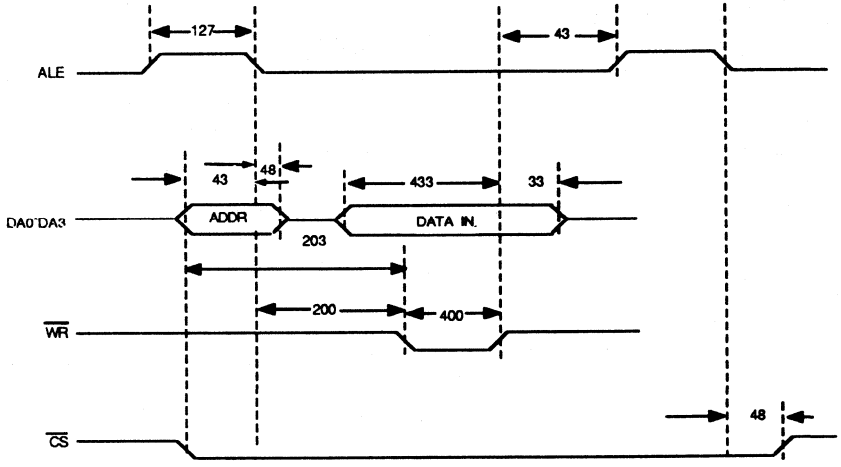
If this bit is high, it indicates the presence of a valid signal in the receive band.

RXD - Receive Data

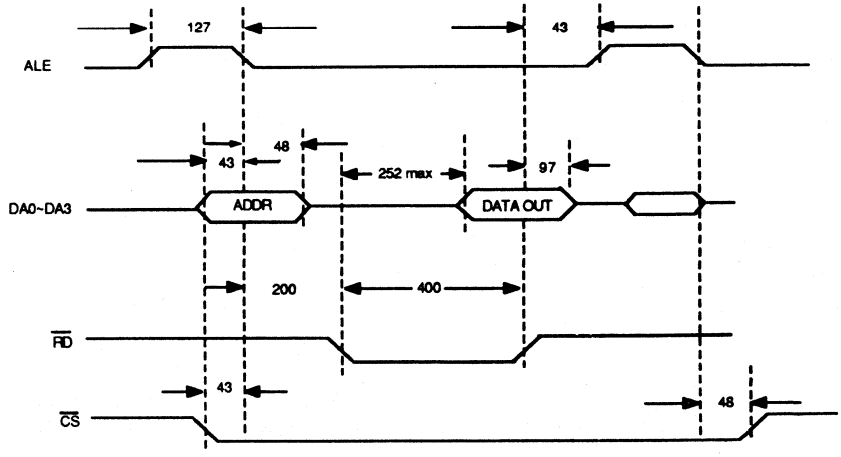
Demodulated digital data is read from this bit. When data is read from this register, the RXD pin can be ignored.

Mode Configuration Programming

Tables 3 to 5 detail the necessary bit register programming steps for each configuration mode, DTMF select and transmit carrier gain select levels respectively.



Read Cycle



Write Cycle

Note: 12 MHz Oscillator
All units in nanoseconds (minimum), unless otherwise specified.

Figure 2. Read/Write Timing Waveforms (12MHz Clock)

CONTROL REGISTERS FOR XR-2321

	ADDRESS BITS				
	AD3	AD2	AD1	AD0	HEX
$\overline{WR}$=0	1	0	0	0	(8)
	1	0	0	1	(9)
	1	0	1	0	(A)
	1	0	1	1	(B)
	1	1	0	0	(C)
$\overline{RD}$=0	1	0	0	0	

Table 1. Read/Write Register Address Locations

	DATA BITS			
	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{WR}$=0	ALB	RXDMK	A/O	TONE/FSK
	V.23 EQ	TXD	PDN	TXEN
	CPM	TONE/DTMF	V23/V21	PTXD
	DTH3	DTH2	DTL1	DTL0
	TX3	TX2	TX1	TX0
$\overline{RD}$=0	***	FREQ	CD	RXD

Table 2. Read/Write Register Bit Assignments

CONFIGURATION MODE BIT PROGRAMMING

D = Databit

FUNCTION	WRITE ADDRESS (HEX)	DATA BITS BIT 3	BIT 2	BIT 1	BIT 0
V.21 ORG mode, Transmit low and and receive high band.	8	0	0	0	0
	9	X	D	0	1
	A	0	X	0	0/1
V.21 ANS mode, Transmit high band and receive low band.	8	0	0	1	0
	9	X	D	0	1
	A	0	X	0	0/1
V.23 mode, Primary channel transmit and reverse channel receive.	8	0	0	0	0
	9	0	D	0	1
	A	0	X	1	0/1
V.23 mode, Reverse channel transmit and primary channel receive.	8	0	0	1	0
	9	0	D	0	1
	A	0	X	1	0/1
Transmit calling tone and prepare to detect calling tone energy.	8	0	X	0	1
	9	X	X	0	1
	A	0	1	X	X
Transmit answer tone and prepare to detect calling tone energy.	8	0	X	1	1
	9	X	X	0	1
	A	0	1	X	X
Transmit calling tone and receive CPM.	8	0	X	0	1
	9	1	X	0	1
	A	1	1	X	X
V.21 Analog loop back in originate mode.	8	1	0	0	0
	9	X	D	0	1
	A	0	X	0	0/1
V.21 Analog loop back in answer mode.	8	1	0	1	0
	9	0	D	0	1
	A	0	X	0	0/1
V.23 Primary channel analog loop back.	8	1	0	0	0
	9	0	D	0	1
	A	0	X	1	0/1

Table 3. Configuration Mode Programming

V.23 Reverse channel analog loop back.	8	1	0	1	0
	9	X	D	0	1
	A	0	X	1	0/1
Read register. Pin 11 is clamped to "Mark" in V.21 mode.	8	X	1	X	X
	9	X	X	0	X
	A	0	X	0	X
Read register. Pin 11 is clamped to "Mark" in V.23 mode.	8	X	1	X	X
	9	X	X	0	X
	A	0	X	1	X
Power down mode.	8	X	X	X	X
	9	X	X	1	X
	A	X	X	X	X
V.21 high band filer check.	8	1	X	0	0
	9	X	D	0	1
	A	1	X	0	0/1
V.21 low band filter check.	8	1	X	1	0
	9	X	D	0	1
	A	1	X	0	0/1
V.23 back channel check.	8	1	X	0	0
	9	X	D	0	1
	A	1	X	1	0/1
V.23 main channel check.	8	1	X	1	1
	9	X	D	0	1
	A	0	X	1	0/1
Busy tone filter check.	8	1	X	1	0
	9	X	D	0	1
	A	1	X	1	0/1

Table 3 (Cont'd) - Configuration Mode Programming

DTMF BIT PROGRAMMING

WRITE ADDRESS	DATA BITS				TONE FREQUENCY		
	BIT3	BIT 2	BIT 1	BIT0	LOW	HIGH	
8 9 A	0 1 0	0 X 0	0 0 X	1 1 X			
B	0	1	1	1	941	1336	(0)
B	0	0	0	0	697	1209	(1)
B	0	1	0	0	697	1336	(2)
B	1	0	0	0	697	1477	(3)
B	0	0	0	1	770	1209	(4)
B	0	1	0	1	770	1336	(5)
B	1	0	0	1	770	1477	(6)
B	0	0	1	0	852	1209	(7)
B	0	1	1	0	852	1336	(8)
B	1	0	1	0	852	1477	(9)
B	0	0	1	1	941	1209	(*)
B	1	0	1	1	941	1477	(#)
B	1	1	0	0	697	1633	(A)
B	1	1	0	1	770	1633	(B)
B	1	1	1	0	852	1633	(C)
B	1	1	1	1	941	1633	(D)

Table 4. DTMF Programming

TRANSMIT GAIN BIT PROGRAMMING

WRITE ADDRESS	DATA BITS BIT 3	BIT 2	BIT1	BIT 0	OUTPUT TRANSMIT LEVEL (dBm)
C	0	0	0	0	-18.0
C	0	0	0	1	-16.8
C	0	0	1	0	-15.6
C	0	0	1	1	-14.4
C	0	1	0	0	-13.2
C	0	1	0	1	-12.0
C	0	1	1	0	-10.8
C	0	1	1	1	-9.6
C	1	0	0	0	-8.4
C	1	0	0	1	-7.2
C	1	0	1	0	-6.0
C	1	0	1	1	-4.8
C	1	1	0	0	-3.6
C	1	1	0	1	-2.4
C	1	1	1	0	-1.2
C	1	1	1	1	0

Table 5. Transmit Gain Programming

APPLICATIONS INFORMATION

Figures 3 and 4 illustrate various application circuits using the XR-2321. In each example, a few precautions should be followed to ensure optimum performance.

1) Analog (AGND) and digital (DGND) grounds should be routed separately to the power supply. They should be single-point connected at the supply in order to minimize higher digital currents from interfering with the more sensitive analog sections.

2) Power supply pins should bypass as close as possible to the IC with a 0.1 µF ceramic capacitor.

Figure 3 shows an XR-2321 based V.23/V.21 modem with the 8031 microcontroller for status and control programming. In Figure 4, the XR-2321 is shown integrated into a V.22bis/V.22 modem with the XR-2400 chip set. The XR-2321 provides the V.23 and V.21 functions resulting in a quad modem solution. If the user is upgrading from a XR-2100 (V.21 single-chip modem) design, the circuit can be retrofitted with the pin-for-pin compatible XR-2321 by replacing the XR-2100 and removing the jumper on pin 18 (FREQ out).

For more information on quad modem applications refer to Application Note AN-38 "An Exar Quattro Modem Solution."

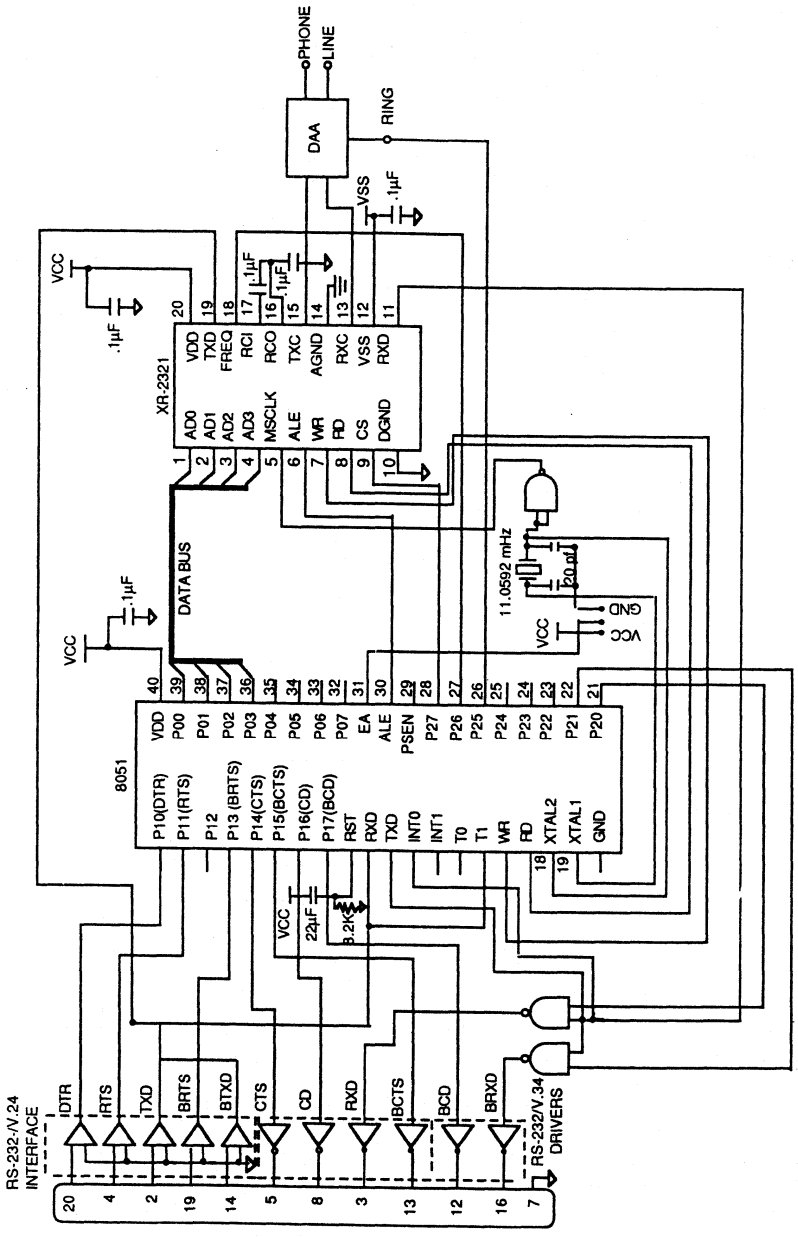
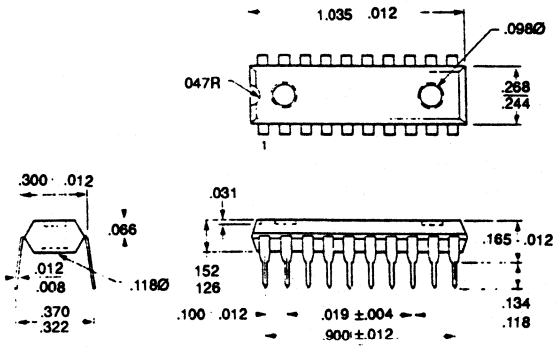


Figure 3. XR-2321 V.23/V.21 Modem

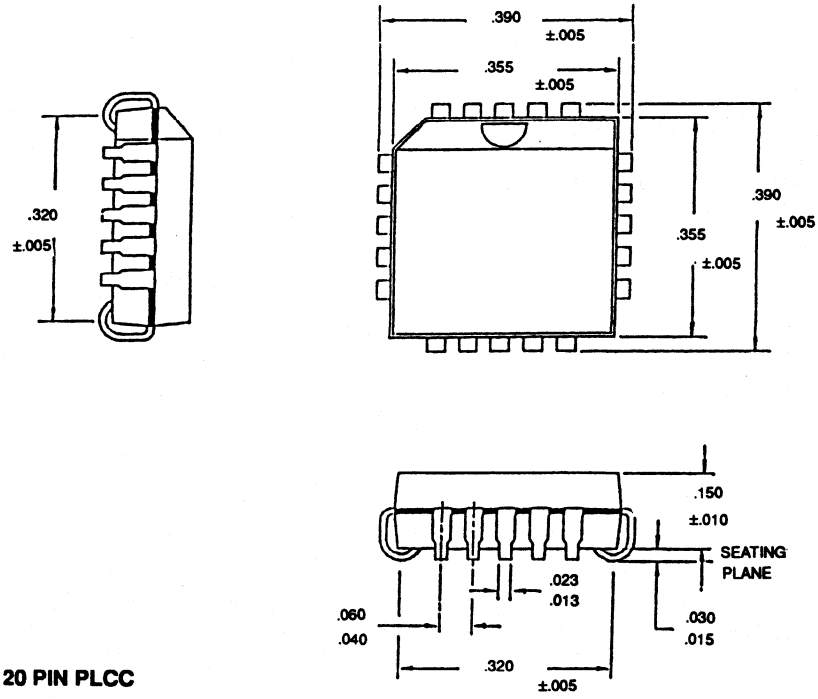
XR-2321 - PHYSICAL DIMENSIONS

CP Suffix
Plastic
Package



20 PIN MOLDED PLASTIC DIP

C J Suffix
PLCC
Package



20 PIN PLCC

V.21 MODEM

GENERAL DESCRIPTION

The XR-2100 is designed to provide the CCITT V.21 modem function. Complete circuitry is included for this 300 BPS FSK full duplex operation.

The XR-2100 can be used as a stand-alone modem under control of a standard microcontroller such as the 8031. Bus structured control interfaces have been implemented for direct microcontroller connection. The XR-2100 may also be programmed for serial control.

The XR-2100 can also be used to provide V.21 operation for other higher speed Exar modem chips such as the XR-2400 chip set for V.22 bis/V.22/212A applications. The XR-2100 ties directly to the same control bus and line interface circuitry as the XR-2400 chip set.

The XR-2100 is constructed in silicon gate CMOS technology for low power operation. Available in a 20 pin dip (0.3" width) and PLCC package, the XR-2100 operates from ±5 volt power supplies.

FEATURES

CCITT V.21 operation
300 BPS FSK, full duplex
Universal microcontroller or serial interface
Direct connection to:
XR-2400 V.22 bis/V.22/212A modem
Low power CMOS(100 mW TYP)
Analog loopback
Generator and detector for answer and calling tones
Power down mode

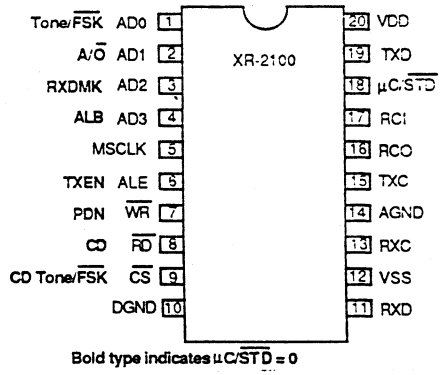
APPLICATIONS

Stand-alone V.21 Modem
V.21 Mode for 1200/2400 BPS Systems
Internal Type Modem

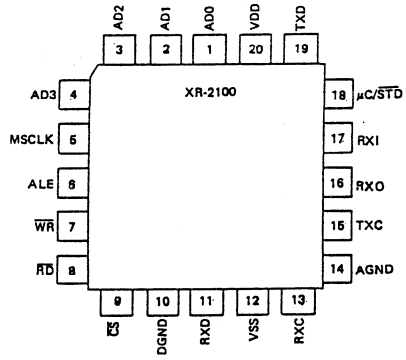
ABSOLUTE MAXIMUM RATINGS

Power Supply	
VDD	-0.3 to 7V
VSS	0.3 to -7V
Voltage	VSS -0.3V to VDD +0.3V
DC Input Current	+10mA
Power Dissipation (Package Limitation)	
Plastic Dip	1W
Plastc Dip	5mW/°C
Storage Temperature Range	-65°C to +150°C

PIN ASSIGNMENT



Bold type indicates µC/STD = 0



ORDERING INFORMATION

Part No.	Package	Operating Temperature
XR-2100 CP	Plastic	0°C to 70°C
XR-2100 CJ	PLCC	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2100, when connected to a microcontroller and line interface circuit, forms a complete CCITT V.21 300 BPS modem. Utilizing a universal bus interface, the XR-2100 can be used as a stand-alone modem or for providing the V.21 to existing modem ship sets such as the XR-2400 V.22bis modem.

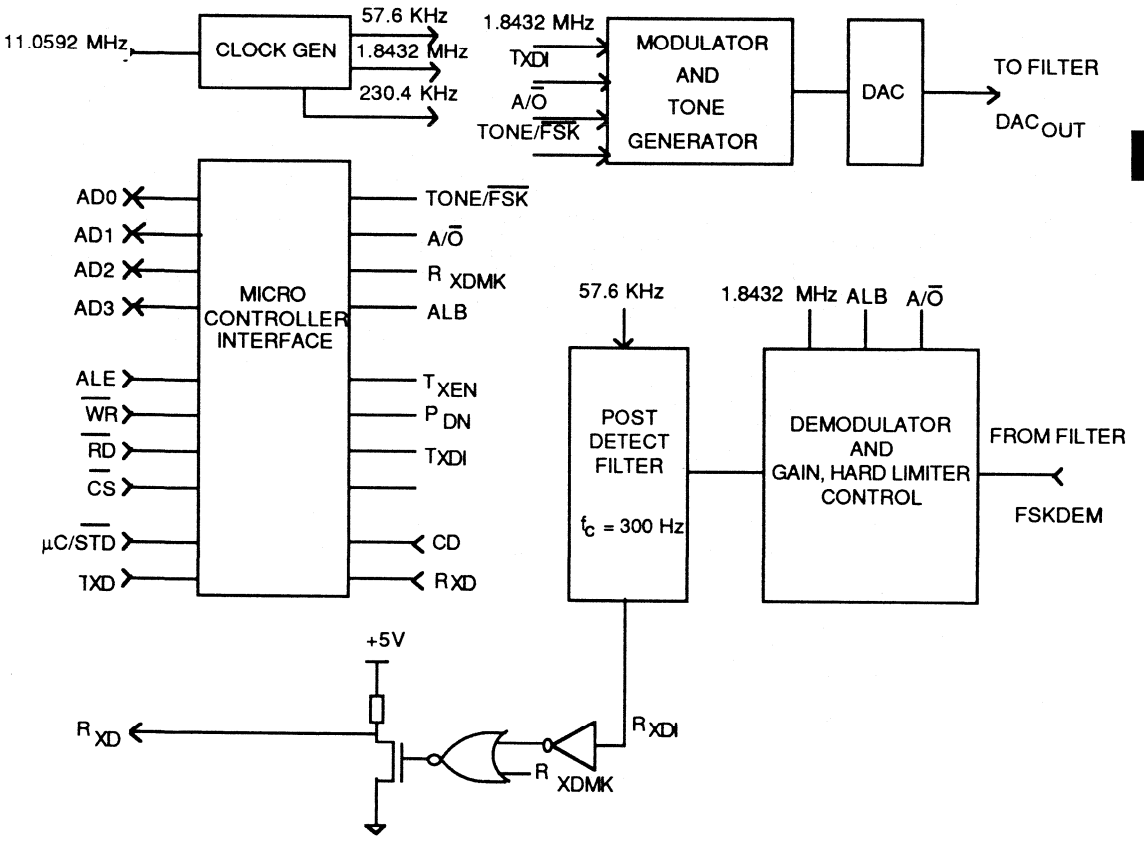


Figure 1. Digital Section Block Diagram For XR-2100

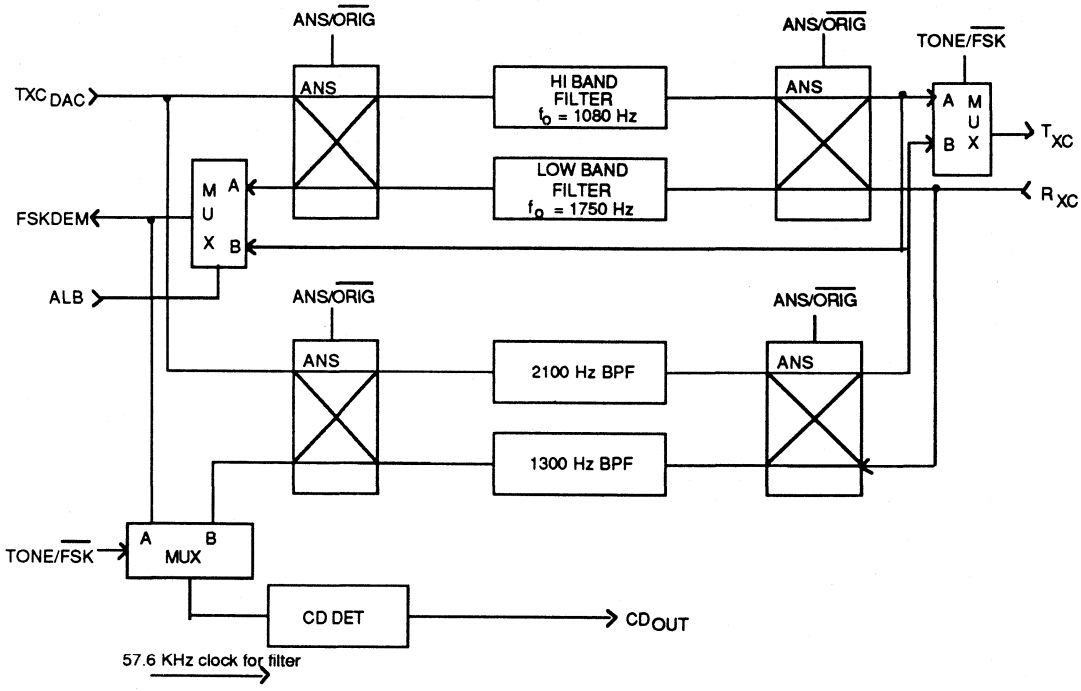


Figure 2. Block Diagram of XR-2100 Filter Section

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25^oC$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$, $MS_{CLK} = 11.0592$ MHz ± 0.05% unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_{DD}	Positive Supply Current		11	28	mA	
	Power Down Mode		7	10	mA	
I_{SS}	Negative Supply Current		11	28	mA	
	Power Down Mode		7	10	mA	
V_{IH}	High Level Input Voltage	2.0			V	
V_{IL}	Low Level Input Voltage			0.8	V	
I_{OH}	High Level Output Current			300	µA	$V_{OH} = 2.4$ V
I_{OL}	Low Level Output Current			2	mA	
I_I	Input Current			50	µA	V1 = 0 to V_{DD}
VO_{CAR}	Transmit Carrier Output	6.5	7.3	8.2	dBM	FSK Carrier calling or ANS Tone.
$V_{CAR\ RNG}$	Input Carrier Range	-43		+10	dBM	ANS, ORIG mode.
CD off	Carrier Detect Off Level		-48		dBM	FSK
			-43		dBM	1300 Hz
			-37		dBM	2100 Hz
CD on	Carrier Detect On Level		-42		dBM	FSK
			-36		dBM	1300 Hz
			-30		dBM	2100 Hz
CD_{HYS}	Carrier Detect Hystersis	2	6		dB	FSK, 1300 Hz, 2100 Hz
S/N	Signal-to-noise Ratio		7		dB	ANS/ORIG R_{XC} = -40 dBM T_{XC} = -10 dBM C0, C2, or B/B line conditions BER≤1/10-5
BIAS DIST	Bias Distortion		4		%	ORIG mode
			5		%	ANS mode

Carrier Frequencies fMSCLK - 11.0592 MHz

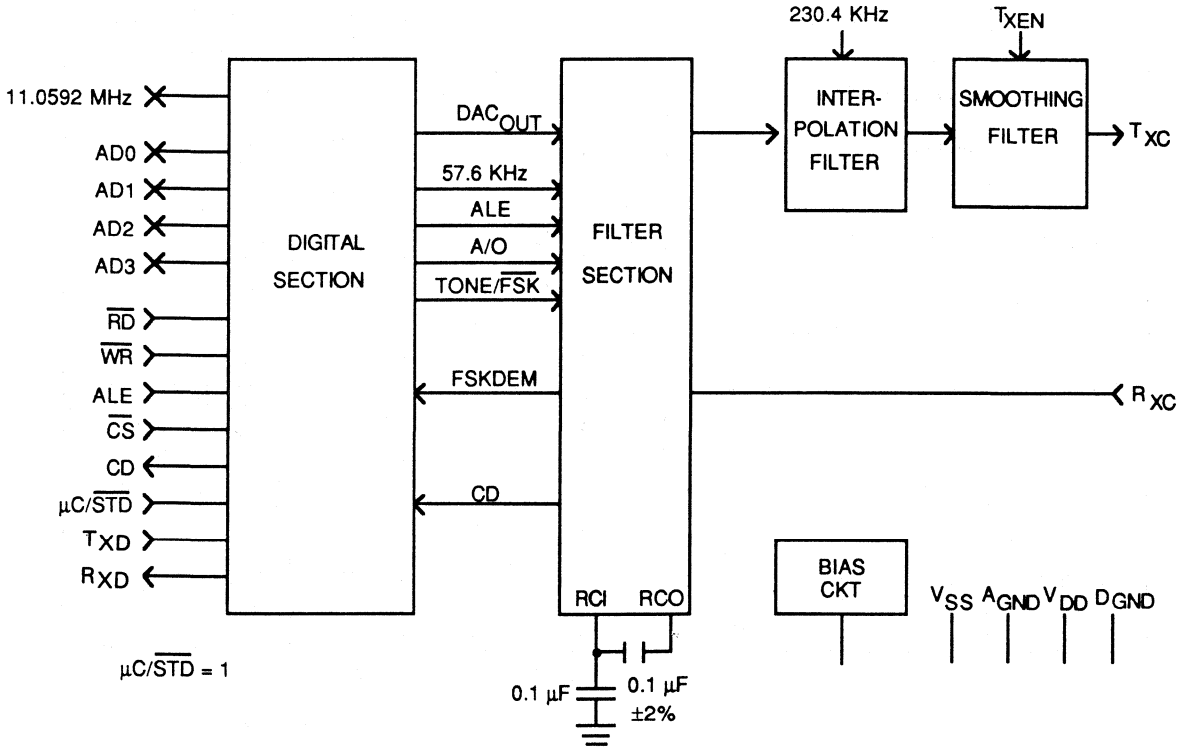
Desired (Hz)	Actual (Hz)	Error (Hz)
980	978.34	-1.66
1180	1181.54	+1.54
1650	1651.61	+1.61
1850	1850.60	+0.60
1300	1301.69	+1.69
2100	2104.11	+4.11

Table 1. Frequency Accuracy

Mode	Transmit Frequency (Hz)		Receive Frequency (Hz)	
	Mark	Space	Mark	Space
Originate	980	1180	1650	1850
Answer	1650	1850	980	1180

Table 2. CCITT V.21 Frequency Parameters

CCITT V.25 Answer
Tone: 2100 Hz



SYSTEM BLOCK DIAGRAM FOR XR-2100

PIN DESCRIPTIONS

Name	Pin#	I/O	Description
AD0 (Tone/$\overline{FSK}$)	1	I/O	Address/data bus bit 0 for µC. Select tone or FSK mode for stand-alone (Tone = 1, FSK = 0).
AD1 (A/$\overline{O}$)	2	I/O	Address/data bus bit 1 for µC. Mode select for stand-alone (ANS = 1, Orig = 0).
AD2 (RX_{DMK})	3	I/O	Address/data bus bit 2 for µC. R_{XD} control for stand-alone (R_{XD} clamped to mark = 1, R_{XD} from DEMOD = 0).
AD3 (ALB)	4	I/O	Address/data bus bit 3 for ALB control for stand-alone (ALB = 1, normal receive = 0).
MSCLK	5	I	Master clock input of 11.0592 MHz.
ALE (T_{XEN})	6	I	Address latch enable for µC. Transmit carrier control for stand-alone (1 = enable, 0 = disable).
$\overline{WR}$ (P_{DN})	7	I	Write enable 'not' for µC. Power down control for stand-alone (1 = power down, 0 = normal operation).
$\overline{RD}$ (CD)	8	I/O	Read enable 'not' for µC. Carrier detect status for stand-alone.
$\overline{CS}$ (CD Tone/$\overline{FSK}$)	9	I	Chip select 'not' for µC. Energy output control stand-alone. (1 = Tone Energy, 0 = FSK Energy)
DGND	10	I	Digital ground. This pin should be routed separate to the AGND to the power supply.
R_{XD}	11	O	Receive data output from the demodulator output (1 = mark, 0 = space).
V_{SS}	12	I	Negative power supply, -5V ±5%. A 0.1uF ceramic bypass capacitor should be placed near the device.
R_{XC}	13	I	Analog recieve carrier input.
AGND	14	I	Analog ground. This pin should be routed separate to the DGND to the power supply.
T_{XC}	15	O	Analog transmit carrier output.
R_{CO}	16	O	Receive filter output. Connected to the R_{CI} through a 0.1 µF capacitor.
R_{CI}	17	I	Demod input. Connected to R_{CO} through a 0.1 µF capacitor
µC/$\overline{STD}$	18	I	Control input for selecting µC or stand-alone interface. (1 = µC, 0 = stand-alone).
T_{XD}	19	I	Transmit data input (1 = mark, 0 = space).
V_{DD}	20	I	Positive power supply voltage, +5V±5%. A 0.1 µF bypass capacitor should be placed near this pin.

CONTROL REGISTERS
With µC/$\overline{STD}$ = 1 (µC interface selected)

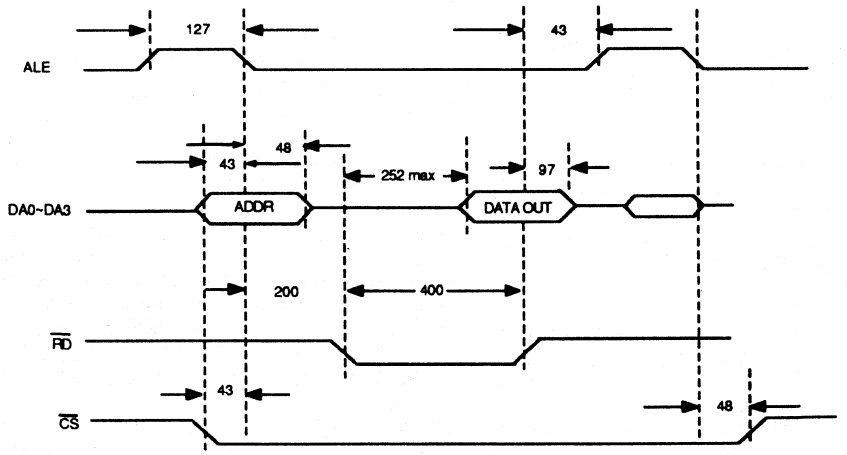
ADDRESS BITS				DATA BITS			
AD3	AD2	AD1	AD0	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{WR}$ =0							
1	0	0	0	ALB	RXDMK	A/$\overline{O}$	Tone/$\overline{FSK}$
1	0	0	1	CD Tone/$\overline{FSK}$	-	PDN	TXEN
$\overline{RD}$ = 0							
1	0	0	0	-	-	CD	RXD

Table 3. µC Control Bit Assignments

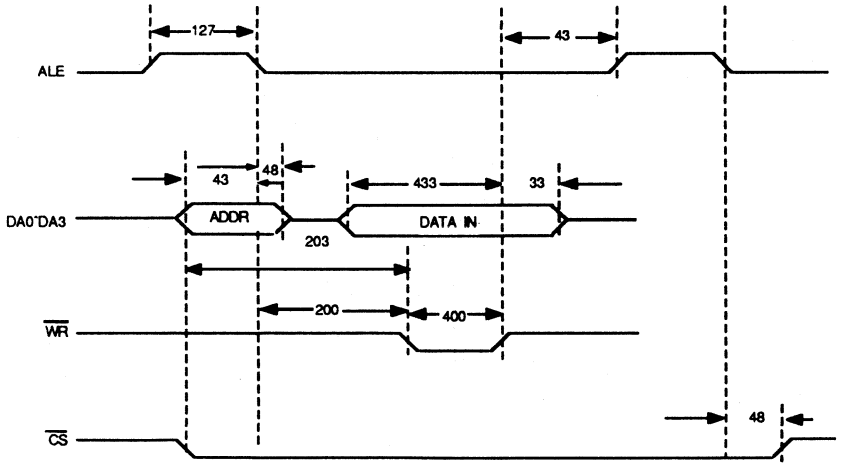
STAND-ALONE MODE SELECTIONS
With µC/$\overline{STD}$ = 0 (Stand-alone mode selected).

Mode	I/O State	Mode Descriptions
Tone/$\overline{FSK}$	1	Answer or calling tone, 2100 Hz for A/$\overline{O}$ = 1 and 1300 Hz for A/$\overline{O}$ = 0.
	0	FSK mode, 980 Hz/ 1180 HZ for mark/space in ORIG and 1650 Hz/ 1850 Hz for mark/space
A/$\overline{O}$	1	Answer mode.
	0	Originate mode.
RXDMK	1	R_{XD} is clamped to mark.
	0	R_{XD} is demod output.
ALB	1	ALB
	0	Normal mode.

Mode	I/O State	Mode Descriptions
T_{XEN}	1	T_{XC} is enabled.
	0	T_{XC} is disabled.
P_{DN}	1	Power down mode
	0	Normal operation.
CD	1	CD is on.
	0	CD is off.
		CD depends on the mode selected, it can be: . Normal receive HI band: FSK Orig. . Normal receive LO band: FSK Ans. . Ans Tone Detect: Tone Orig. . Calling Tone Detect: Tone Ans.



Read Cycle



Write Cycle

Note: 12 MHz Oscillator
All units in nanoseconds (minimum), unless otherwise specified.

Figure 3. Read/Write Timing Waveforms for XR-2100 Using 8031/51 Controller

APPLICATIONS INFORMATION

Figures 4 and 5 illustrate the XR-2100 used in various applications. In each, several precautions should be followed in order to ensure optimum performance.

1.) Analog (AGND) and digital (DGND) grounds should be routed separately to the power supply. They should be single point connected at the supply. This will minimize higher digital currents from interfering with more sensitive analog sections.

2.) The power supply pins should be bypassed with 0.1 µF ceramic capacitors close to the IC.

Figure 4 shows the XR-2100 used in a stand-alone configuration as selected by µC/$\overline{STD}$ = 0. The various modes of operation are selected by switches S1-S7.

The XR-2100 is shown in figure 5 to provide the V.21 operation for a V.22 bis (2400BPS) modem. Here the XR-2401/XR-2402 chips support V.22 bis, V.22 and Bell 212A modes. The control for both the XR-2100 and XR-2401/XR-2402 come from the XR-2403A microcontroller. User-specified firmware can be added to drive the XR-2100.

Should your future application require combined V.21 and V.23 communications, the design shown in Figure 5 can be easily retrofitted with the pin-compatible XR-2321. By a simple drop-in replacement and one jumper modification, the resulting solution will support all four CCITT Standards (V.22bis, V.22, V.23 and V.21) providing "Quad" modem capabilities.

For more information on quad modem applications refer to Application Note AN-38 "An Exar Quattro Modem Solution."

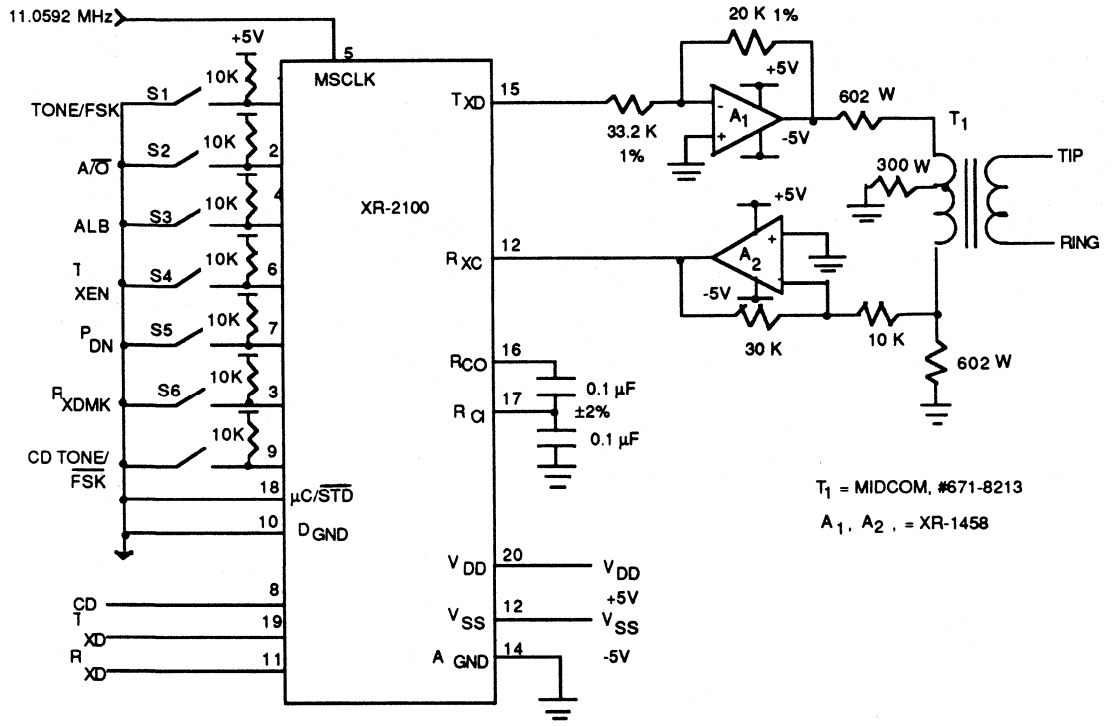


Figure 4. Stand-Alone V.21 Modem With Serial Control

PSK Modulator/Demodulator

GENERAL DESCRIPTION

Each of these devices provide the modulator and demodulator for phase-shifted keyed modulated signals. The devices have an on-chip digital-to-analog converter, allowing digital external programming of Bell 212A, CCITT V.22 or V.26 functions.

The XR-2123 provides the modulator and demodulator functions. It is adequate for Bell 212A (1200 BPS only) and Bell 201 standards. The XR-2123 requires a synchronous-to-asynchronous converter and scrambler-descrambler for the digital portion of the modem for 212A applications. Level shifters and filtering is required for the analog portion.

The XR-2123A provides the ±7 Hz carrier capture range needed for V.22 and V.26. It is externally identical to the XR-2123.

The XR-2123 and XR-2123A utilize CMOS technology for power operation while providing single 5 volt operation. Both devices come in a 28 pin DIL pin package in either plastic or ceramic.

FEATURES

Single +5 Volt Operation
Low Power Consumption (typ. 10 mw)
1200 BPS Full Duplex
2400 BPS Half Duplex
Programmable for US or European Standards (CCITT)
Dibit PSK (DPSK) Operation
Cyrstal Controlled
Synthesized Sine Wave Modulator Output
Adjustable Modulator Output Amplitude
Input Protection

APPLICATIONS

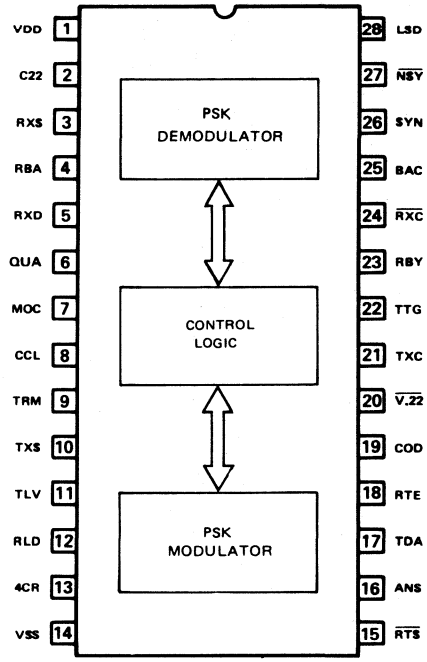
Bell Standard 201 or 212A Modems
CCITT Standard V.22 or V.26 Modems

ABSOLUTE MAXIMUM RATINGS

Power Supply	5.5 V
Power Dissipation	1.0 W
Derate Above 25°C	5 mW/°C
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C
All Input Voltage	-0.5 V to (V_{DD} + 0.5 V)
DC Current Into Any Input*	±1 mA

*Please note that with polysilicon gate inputs, the maximum voltage rating at any pin may be reached before the absolute maximum current of the input is reached. Caution should be used.

FUNCTIONAL BLOCK DIAGRAMS



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2123CN	Ceramic	0°C to +70°C
XR-2123CP	Plastic	0°C to +70°C
XR-2123ACN	Ceramic	0°C to +70°C
XR-2123ACP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2123 and XR-2123A provide the complete modulation and demodulation of DPSK modem systems. The modulator transmits a sampled sine wave in dibit phase-shifted keyed format (DPSK). The phase shifts and carrier frequencies are controlled with logic inputs. With these controls, a Bell 212A/CCITT V.22 or a Bell 201/CCITT V.26 can be created.

The XR-2123 and XR-2123A require a separate scrambler/descrambler and synchronous-to-asynchronous converter.

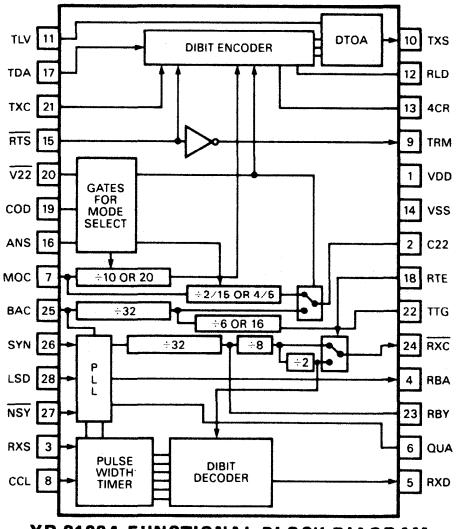
ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = +5V, V_{SS} = 0V, T_j = 0°C to 70°C

Digital Inputs: RXS, MOC, CCL, $\overline{RTS}$, ANS, TDA, RTE, COD $\overline{V22}$, TXC, BAC, SYN, $\overline{NSY}$, LSD

Digital Outputs: C22, RBA, RXD, QUA, TBA, 4CR, TTG, RBY, $\overline{RXC}$

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{OL}	Output Low Voltage			0.5	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	4.4			V	I_{OH} = 1.0 mA
V_{IL}	Input Low Voltage	-0.5		1.1	V	
V_{IH}	Input High Voltage	3.5		5	V	
I_{IL}	Input Leakage Current		1μA		pA	
I_{DD}	Power Supply Current		2.5	4	mA	
C_I	Input Capacitance					
t_R	Low to High Logic Transition Time		20		ns	C_L = 10 pF
t_F	High to Low Logic Transition Time		20		ns	C_L = 10 pF
V_{TXS}	Transmitted Carrier Signal Level		-9		dBm	$V_{PIN\ 11}$ = 1 V



XR-2123A FUNCTIONAL BLOCK DIAGRAM

THEORY OF OPERATION

A system using a XR-2123 or XR-2123A would require both additional analog and digital circuitry. The digital circuitry required for the XR-2123, XR-2123A is a scrambler/descrambler which is a pseudo-random pattern generator. Figure 1 showns a hardware approach of doing the scrambler/descrambler. If the modem is intended to be operated asynchronously, a synchronous-to-asynchronous converter is needed. With the XR-2123 or XR-2123A the XR-2125 can be used. If additional features are desired, a microprocessor can be used to implement both the scrambler/descrambler and the synchronous-to-asynchronous converter.

A counter circuit is needed to provide the baud clock (BAC), which needs to be synchronized with the 4.608 MHz master clock (MOC).

The analog portion of the modem circuit consists of two parts, the bit carrier recovery and the baud carrier recovery. The bit carrier occurs at either 1200 or 2400 Hz. A modem filter, such as the XR-2120, can be used to remove out-of-band signals. The signal is passed through an automatic gain control (AGC), and then through a level shifter. The signal from the level shifter is applied to Pin 3 of the XR-2123 or XR-2123A (RXS).

The baud carrier recovery is similar. After the AGC, the signal is applied to a precision full wave rectifier. The baud rate is always 600 Hz for Bell 212A (1200 BPS) or V.22.

By rectifying the signal, the 600 Hz carrier appears as an amplitude modulation. After the rectifier, the signal is applied to a 600 Hz bandpass filter with an approximate Q of 20. The phase shift through this portion is very important. It must be -180° of phase shift from input to output. This is to place the baud clock in the correct reference with the recovered bit carrier. This signal is then level-shifted and applied to Pin 26, SYN. Figure 2 shows the signals after the XR-2120 after the full wave precision rectifier, after the 600 Hz bandpass filter, and after the level-shifter. Figure 11 shows a typical application. The 8048 microprocessor performs the scrambler/descrambler function as well as the synchronous-to-asynchronous function. A copy of the software used to implement this function is available from EXAR.

Bell 201/CCITT standard V.26 implementation with the XR-2123A requires an additonal filter and a mixer stage in the analog portion. V.26/201 is a synchronous data transmission and does not require a synchronous-to-asynchronous converter. A scrambler/descrambler is also not required, making the digital portion of the modem circuit very simple. A counter circuit to divide down the 4.608 MHz clock (MOC) for the baud clock (BAC) is the only digital circuit needed.

The receive portion of the analog circuit will be discussed first. The received signal is filtered through an 1800 Hz bandpass filter with -3 dB points at 760 and 2860 Hz. This can be constructed with discrete components or with a pro-

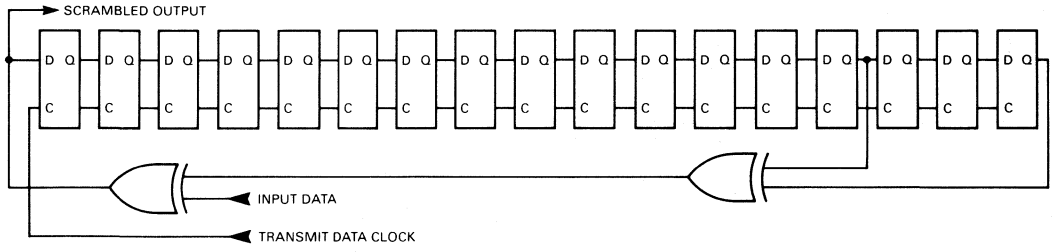


Figure 1A. Scrambler

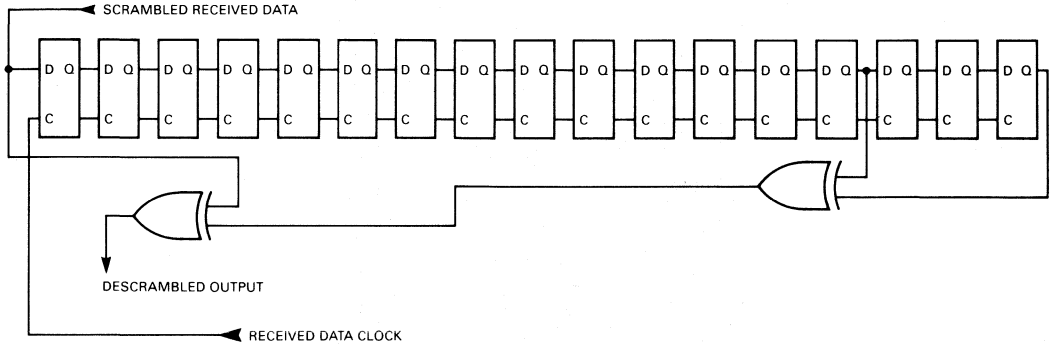


Figure 1B. Descrambler

grammable filter. After the filter, the signal is passed through an automatic gain control (AGC), A mixer is then used to bring the 1800 Hz received signal up to 9 kHz. This signal is filered through a 9 kHz bandpass filter. This filter should have a Q of approximately 9. The signal is limited and applied to Pin 3, RXS.

The baud carrier can be seen as a amplitude modulation on the 9 kHz signal. This is filtered off using a 1200 Hz bandpass filter. The Q of this filter should be approximately 2. The phase shift through this filter is very important. At 1200 Hz, the phase of the output referenced to the input should be -90°. After the 1200 Hz bandpass filter, the signal is applied to a level shifter and applied to Pin 26, SYN.

It should be noted that variation in delay of the 9 kHz filter can affect the point at which the 1200 Hz filter should be tuned. If the delay of the 1200 Hz Amplitude Modulation Envelope occurs as shown in Figure 5, then a different amount of phase shift for the 1200 Hz would be needed. The most important point is that the phase shift by -180° after passing through both the 9 kHz and the 1200 Hz bandpass filters.

The transmit output, Pin 10, of the XR-2123 or XR-2123A requires a low pass filter with a -3 dB point of 3500 Hz. Either the XR-1015 low pass filter or a discrete component filter can be used.

Figure 3 shows the signal after the mixer, after the 9000 Hz filter and after the 1200 Hz filter. Figure 4 shows one method of utilizing the XR-2123A for a V.26/ 201 modem. To create the optional 75 baud reverse direction, the XR-2206 and XR-2211 can be used.

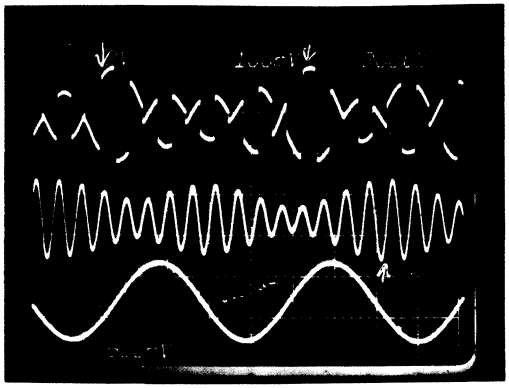


Figure 4. The above photograph shows the output of the mixer with a 01 pattern being received. The center trace shows the shift of the envelope after passing through the 9 kHz bandpass filter. Please note that the phase of the envelope has been shifted by approximately -270°. The lower trace shows the output of the 1200 Hz bandpass filter tuned to obtain the +90° phase shift for a total sum of -180°.

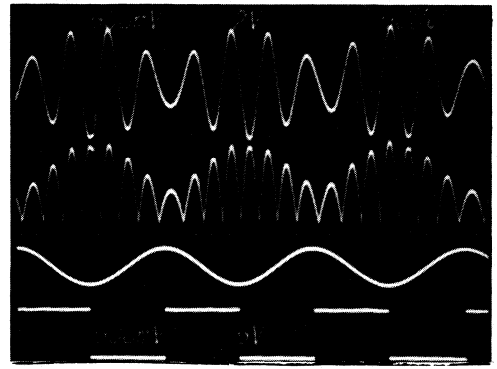


Figure 2. Showing received signal after the XR-2120, after full wave precision recitifier, after the 600 Hz bandpass filter, and after the level shifter.

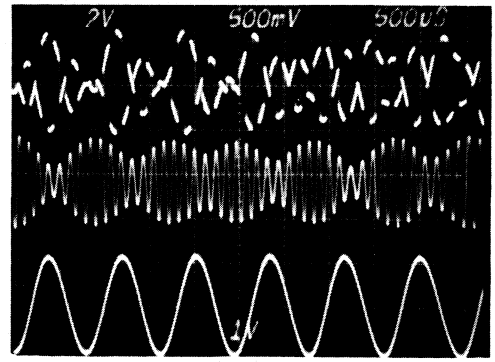


Figure 3. Showing the output of the mixer, the output of the 9000 Hz filter, and the output of the 1200 Hz bandpass filter (baud clock recovery).

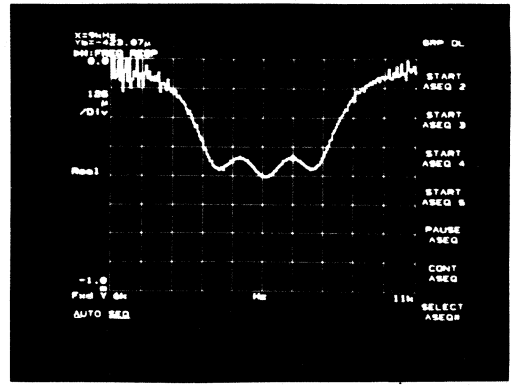


Figure 5. This photograph shows the typical group delay variation in the passband of the 9 kHz filter.

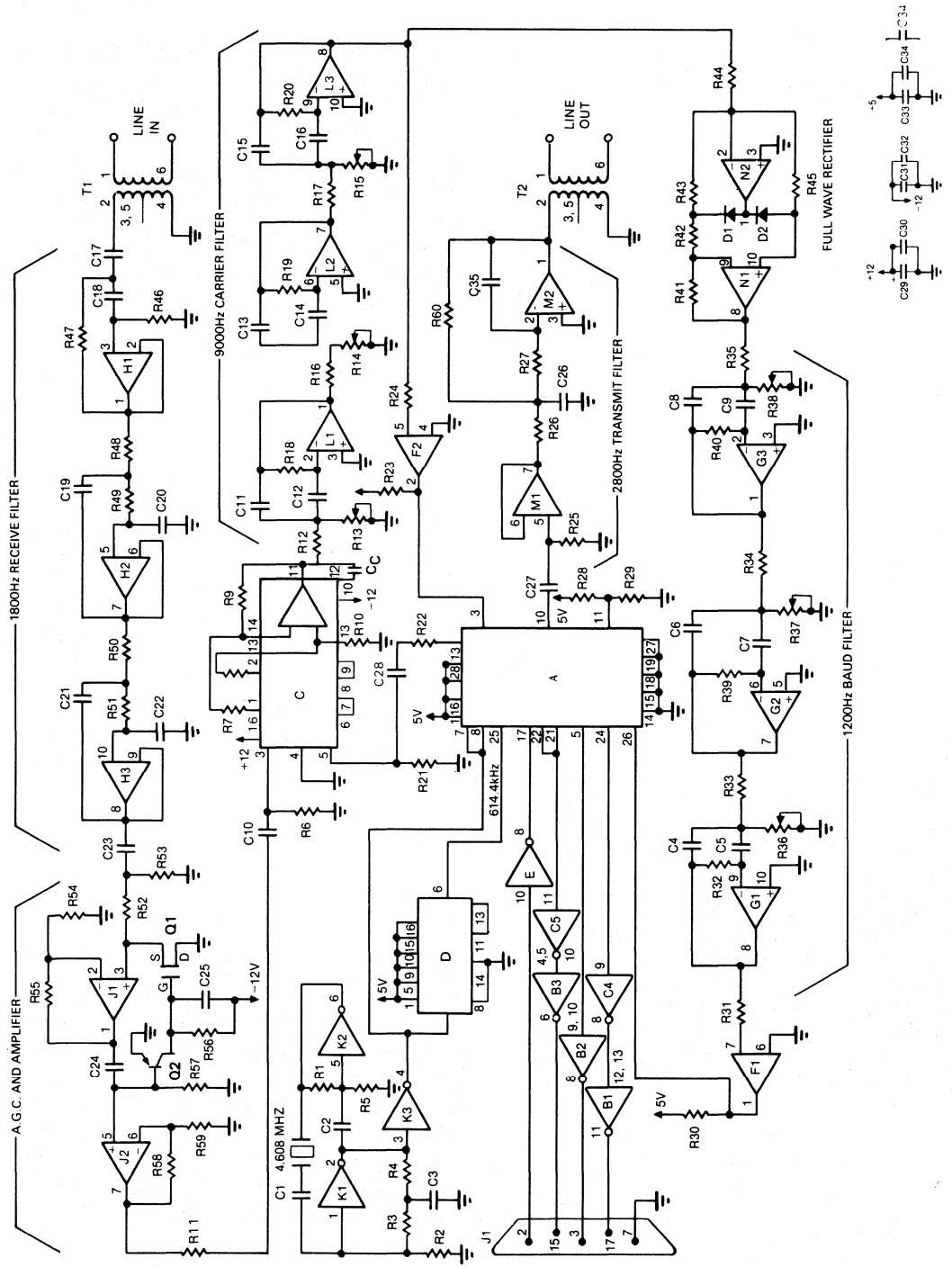


Figure 6. CCITT V.26 2400 BPS Modem Application Schematic

INTEGRATED CIRCUITS

A	XR-2123/A	EXAR
B	XR-1488	EXAR
C	XR-2208	EXAR
D	DM-74193	National
E	XR-1489	EXAR
F	LM-339-N	Texas Instruments
G	XR-4741	EXAR
H	XR-4741	EXAR
J	XR-1458	EXAR
K	F-7404	Fairchild
L	XR-4741	EXAR
M	XR-1458	EXAR
N	XR-4741	EXAR

CAPACITORS

C1	82 pf	C19	.01 μf
C2	.0022 μf	C20	.001 μf
C3	.033 μf	C21	.01 μf
C4	.033 μf	C22	100 pf
C5	.033 μf	C23	2.2 μf
C6	.033 μf	C24	2 μf
C7	.033 μf	C25	10 μf
C8	.033 μf	C26	.033 μf
C9	.033 μf	C27	1 μf
C10	.1 μf	C28	.1 μ
C11	.0033 μf	C29	4.7 μf
C12	.0033 μf	C30	.1 μf
C13	.0033 μf	C31	4.7 μf
C14	.0033 μf	C32	.1 μf
C15	.0033 μf	C33	4.7 μf
C16	.0033 μf	C34	.1 μf
C17	.1 μf	C35	.0068 μf
C18	.1 μf		

RESISTORS

R1	1.2K	R21	2K	R41	10K
R2	2.2K	R22	100K	R42	10K
R3	2.2K	R23	10K	R43	10K
R4	2.2K	R24	10K	R44	10K
R5	2.2K	R25	1M	R45	10K
R6	2K	R26	3.32K	R46	5.76K
R7	24K	R27	2.2K	R47	2.74K
R8	24K	R28	1K	R48	2.61K
R9	50K	R29	1K	R49	75K
R10	50K	R30	10K	R50	7.87K
R11	200K	R31	10K	R51	249K
R12	43.2K	R32	82.2K	R52	120K
R13	1K POT	R33	29.1K	R53	10K
R14	1K POT	R34	29.1K	R54	1K
R15	1K POT	R35	29.1K	R55	68K
R16	43.2K	R36	500Ω POT	R56	1M
R17	43.2K	R37	500Ω POT	R57	10K
R18	109K	R38	500Ω POT	R58	4.7K
R19	109K	R39	82.2K	R59	1K
R20	109K	R40	82.2K	R60	6.8K

TRANSISTORS

Q1	2N4861	Q2	2N4403

TRANSFORMERS

T1	T2220
T2	T2220

DIODES

D1	IN914
D2	IN914

CONNECTOR

J1	RS232

Figure 6A. V.26 2400 BPS Modem System Components List

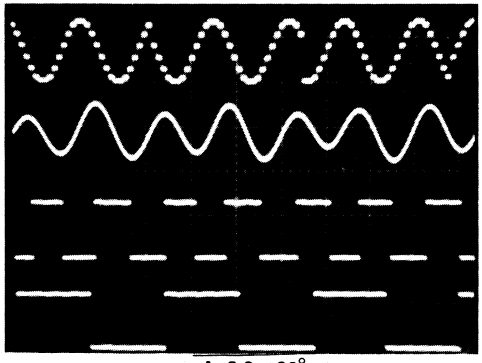
Modulation

The data to be modulated is applied to Pin 17, TDA. This must be synchronized to the transmitter bit timing clock, Pin 22, TTG. This internally creates a dibit signal which then selects the amount of phase shift needed to be encoded properly. This is coherent phase modulation which means the only phase reference is the phase of the signal before the transition.

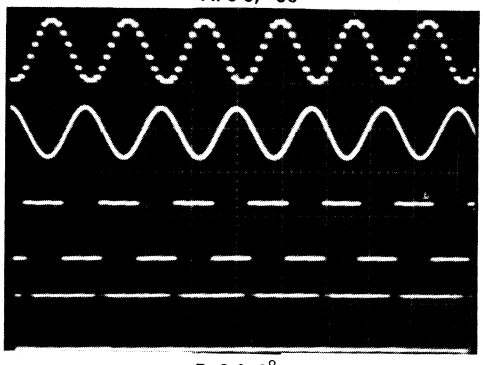
To encode the data, a counter, which accesses the digital-to-analog converter, is preset to a particular point depending on the phase change needed. Figure 7 shows four possible phase shifts with the four bit patterns (00, 01, 10, 11) and the ouput of the XR-2120 filter. It should be noted that the baud rate stays at 600 Hz whether in originate (2400 Hz carrier) or in answer mode (1200 Hz data carrier).

The amplitude of the transmitted signal is controlled by the TLV, transmitter level, Pin 11. This is a DC input, typically set for 0.8 VDC. The input draws approximately 15 μA, and can be controlled with a resistor divider or a digital-to-analog converter for adapting to poor lines. Figure 8 shows the relationship between V_{TLV} and V_{TXS}.

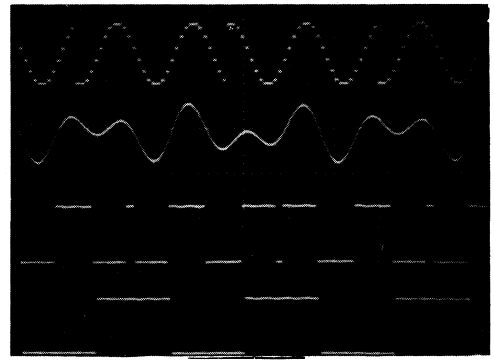
Figure 7. TXS, Transmit Output — Output of 2120, Output of Limiter Receovered Baud Clock



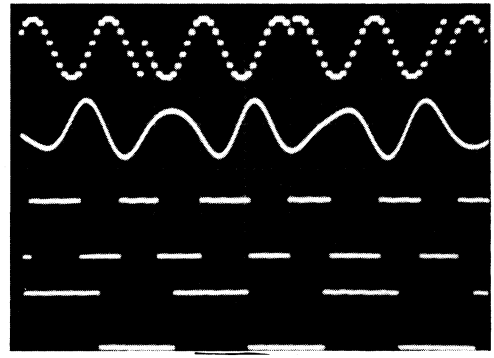
A. 0 0; +90°



B. 0 1; 0°



C. 1 0; 180°



D. 1 1; 270°

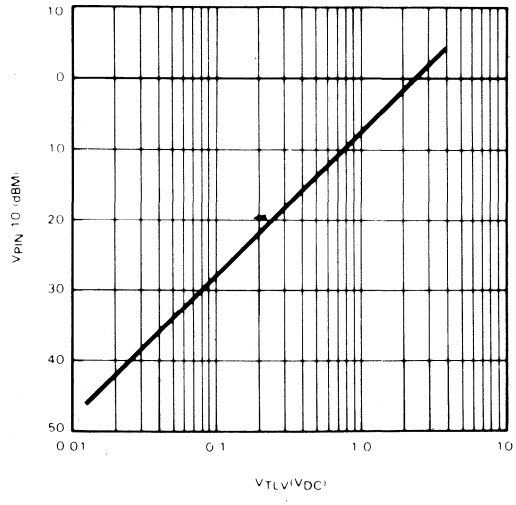


Figure 8. TXS vs. VTLV

Demodulation

The demodulator uses a pulse width measuring technique which compares the pattern received on RXS within the window set by the baud clock, applied to the synchronizer pin, SYN This is a coherent demodulation technique, so no reference phase is needed. The carrier clock, CCL, is used to time the widths of the received pulses. As it was shown in Figure 5, the phase changes produce a distinctive pulse pattern. The clock frequency applied to the carrier clock pin, CCL, is changed for each carrier frequency used. The greater the carrier frequency, the greater the carrier clock frequency.

The V.26 demodulation is the same internally. With a 1800 Hz bit carrier and a 1200 Hz phase carrier, only 1½ cycles of the 1800 Hz carrier exist within the window created by the baud clock. This does not provide enough pulses to provide an accurate measurement. Also, the baud clock is not easily recovered with the received waveform. When the received signal is mixed up to 9000 Hz, the phase carrier appears as an amplitude modulation. This can be easily detected with the full wave precision rectifier and a 1200 Hz bandpass filter. Figure 4 shows the typical signals seen at various points.

The quality pin, Pin 6, on the XR-2123A is error jitter of the phase-lock loop. It is latched so that it remains high a minimum of approximately 1 ms. This can be used as an indication of the quality of the line in use. If the quality pin is high often, the possibility of errors is greater.

The received bit timing clock is used to synchronize the data at Pin 5, RXD. This clock is found on Pin 24, RXC. Figure 9 shows the relationship between $\overline{RXC}$ and RXD. If the XR-2125 was used, $\overline{RXC}$ is tied to Pin 9, RXC IN, and RXD is tied to RXD IN, Pin 10.

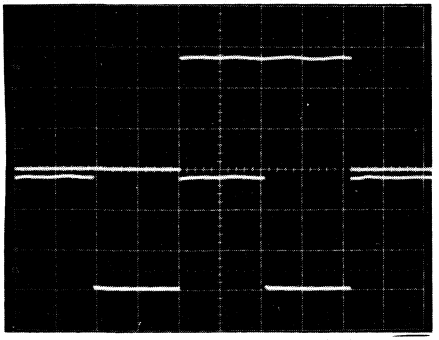


Figure 9. Top Trace RXD, Bottom Trace $\overline{RXC}$

PIN DESCRIPTIONS

Pin	Name	Description
1	VDD	+5 V_{DC} ±0.25 V
2	C22	Carrier clock for Bell 212/V.22. This output clock is used by the demodulator for timing the pulse widths of the received signal. When in the originate mode, the frequency of the pin is 614.4 kHz. When the XR-2123 or XR-2123A is set in the answer mode, the frequency at this pin is 1.2288. This allows the counter circuit in the demodulator to arrive at the same total count for a given baud rate. This pin is controlled by V.22, ANS, and COD pins on the device as shown.

	V.22	ANS	COD	C.22
1200 Hz	0	1	1	1.2288 MHz
2400 Hz	0	1	0	0.6144 MHz
See Select Mode	1	X	X	9600 Hz Mode

When V.22 is high, C.22 produces a 9600 Hz clock. This clock is not normally used for V.26 and is NOT applied to Pin 8, CCL.

3	TXS	Received signal input. This is the received signal input after level shifting (0-5 V). This signal carries the bit data.
4	RBA	Received baud timing. This output provides a clock at the baud rate chosen. For V.22 and Bell 212, it is at 600 Hz. For V.26, it is at 1200 Hz. It is derived from BAC and also phase locked to the signal applied to Pin 26, SYN.
5	RXD	Received data. This output is the demodulated data from the signals applied to pins 3 and 26 (RXS and SYN respectively).

6	QUA	The quality of demodulation. This pin shows the amount of error in the timing relationship between SYN and RBA. If the recovered baud carrier has too much noise, this pin will be high for a minimum of approximtely 1 ms. Please read the demodulation section of this data sheet for more detail.
7	MOC	Modulator clock input. This is the master clock. For V.22, Bell 212A and V.26, this clock is 4.608 MHz.
8	CCL	Carrier clock. This input is for the clock which measures the time that RXS, Pin 3, is high within one window. This input is always 512 times the received bit carrier. For example if f_{RXS} = 1200 Hz f_{CCL} = 614.4 kHz f_{RXS} = 2400 Hz f_{CCL} = 1.228 MHz f_{RXS} = 9000 Hz f_{CCL} = 4.608 MHz For V.22 and Bell 212 applications, CCL is applied from the output C.22, Pin 2, of the device. When V.26 is needed, CCL is tied to the master clock, Pin 7. The received frequency of 9000 Hz for V.26 is explained in the demodulation section.
9	TRM	Transmit mode. This output indicates the state of the modulator. When high, the device is transmitting. When low, carrier output is clamped. It is controlled by Pin 15, $\overline{RTS}$. When $\overline{RTS}$ is low, TRM is high. When $\overline{RTS}$ is high, TRM is low.
10	TXS	Transmitted signal. This is the output of the internal digital-to-analog converter. The modulated 8-level sine wave can be seen at this pin. This output is usually applied to the XR-2120 modem filter.
11	TLV	Transmitter level. This input controls the amplitude of the transmitter output, Pin 10. It typically draws approximately 15 µA and can be adjusted using a resistor divider circuit. Although not critical, this input should be relatively free of any AC component since it will cause an amplitude modulation of the TXS output.
12	RLD	Received data. This tells the terminal that the data to be transmitted has been received by the modem. It is at the baud rate of the mode the device is set in. It is counted down from BAC, Pin 25. When RLD goes high, this marks the end of the dibit set.

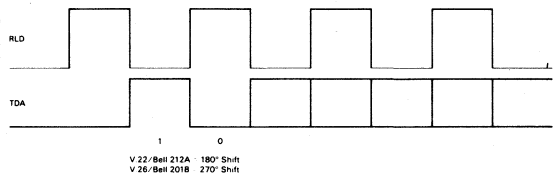


Figure 10. RLD Timing

13	4CR	Four times the carrier frequency. This output is used for the V.26 mixer in the demodulator circuit. For V.22 and Bell 212A it is not used.
14	V_{SS}	Ground.
15	$\overline{RTS}$	Request to send. This input controls the transmitter output and the TRM, transmit mode output. The following chart describes the possibilities:

RTS	TRM	TXS
0	1	carrier
1	0	clamped to DC level

16	ANS	Answer tone. This input controls the frequency of the transmitter output. It is used along with $\overline{V.22}$ and COD. The details about using this pin is found under those two pins.
17	TDA	Transmitted data. This input is where data to be transmitted is applied. It should be synchronized to the transmit clock, Pin 22, TTG. By comparing the data applied to this pin and Pin 12, RLD, the various phase shifts can be predicted for troubleshooting purposes.

18 RTE — Rate. Control $\overline{RXC}$, Pin 24, and Pin 22, TTG. When set at a logic 1 level, the frequency at the two outputs is ½ what is normally seen there. The block diagram shows the dividers controlled by RTE.

19 COD
20 $\overline{V22}$ V.22 mode
ANS answer tone — Code. These three inputs determine the mode of the modulator and demodulator of the device. Also, with these pins the 2100 Hz tone for handshaking can be created. The following truth table applies to these pins:

$\overline{V.22}$	ANS	COD	APPLICATION
0	0	0	Transmit and receive at 2400 Hz (high ch.) This is for analog loop back.
0	0	1	Transmit and receive at 1200 Hz (low ch.) This is for analog loop back.
0	1	0	Transmit at 2400 Hz (high ch.) Receive at 1200 Hz (low ch.)
0	1	1	Transmit at 1200 Hz (low ch.) Receive at 2400 Hz (high ch.)
1	0	0	Answer Tone at
1	0	1	2100 Hz.
1	1	0	V.26 mode Phase shifts have an initial 90° skew.
1	1	1	V.26 mode Phase shifts have an initial 45° skew.

21 TXC — Transmitter bit timing. This input is usually tied to Pin 22, TTG, timing for transmitter. For V.22/Bell 212A (1200 BPS), the frequency at Pin 21 is 1200 Hz. For V.26, the frequency is 2400 Hz. Note: this assumes that Pin 18, RTE, is low in both cases.

22 TTG — Timing for transmitter. This output is applied to pin 21 for all standard uses (V.22, Bell 212A, Bell 201, and V.26). It is counted down from BAC clock input. Please read the descriptions for TXC and RTE for details.

23 RBY — Received byte timing. This output is a square wave at a frequency 16 times the received baud timing. It is not normally used.

24 $\overline{RXC}$ — Received bit timing. This output is synchronized to the recovered baud carrier. It is usually used to perform the asynchronous-to-synchronous conversion.

25 BAC — Baud clock. This input is used to create the modulation and demodulation baud clock. Internal countdown circuitry sets the baud rate at either 600 Hz or 1200 Hz. For V.22/Bell 212A operation, a 307.2 kHz clock is applied to BAC. For V.26 operation, a 614.4 kHz clock is applied.

26 SYN — Synchronization. This input is where the recovered baud carrier is applied. This clock is internally applied to a phase lock loop which has BAC as the local oscillator. The error voltage is shown as the difference between $\overline{RXC}$ and RBA. This error output can be found on the quality pin, QUA, Pin 6.

27 $\overline{NSY}$ — New synchronization. This input will force the received data output to a high state. The synchronization takes place when the $\overline{NSY}$ pin is changed from high to low.

28 LSD — Line signal detector. When high, the receiver is operating normally. When this input is low, the receiver is clamped. This can be tied through an inverter to the signal applied to the $\overline{NSY}$ input.

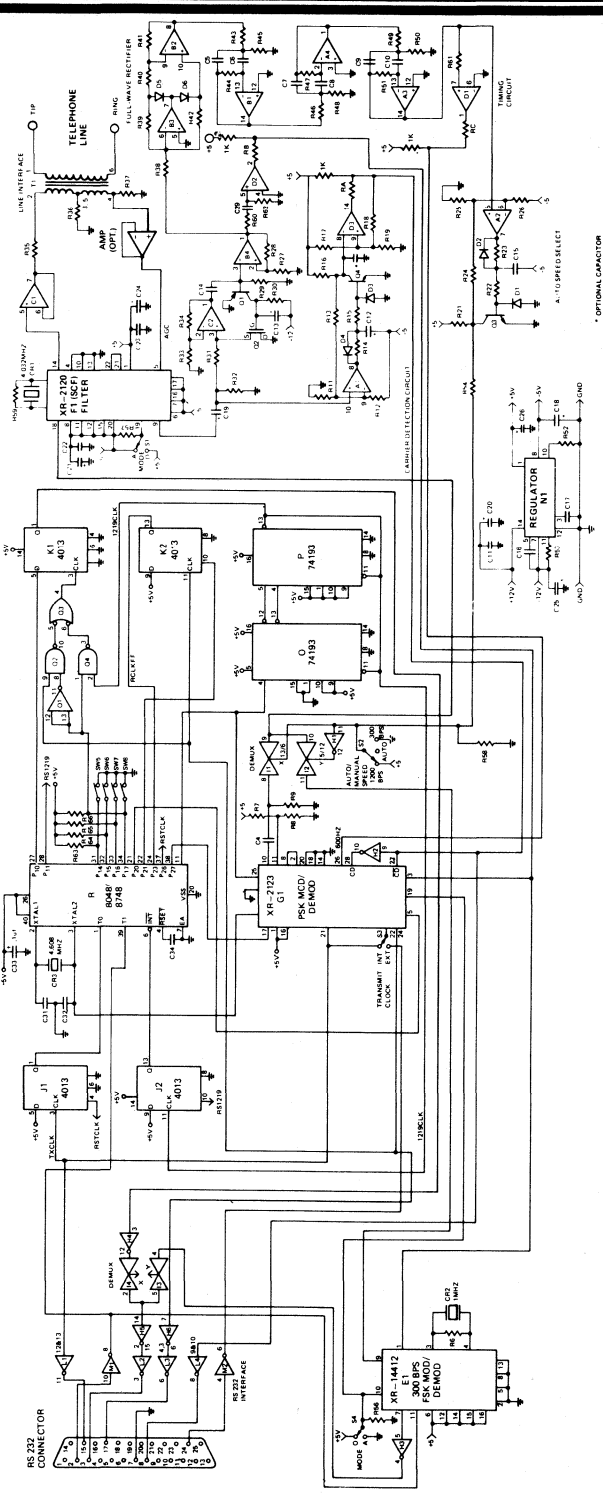


Figure 11. Bell 212A Modem Application Schematic

A	XR-4741	Quad Op Amp
B	XR-4741	Quad Op Amp
C	XR-1458	Dual Op Amp
D	LM-339	Quad Comparator
E	XR-14412	FSK Mod/Demod 300 BPS
F	XR-2120	Filter-Switched Cap
G	XR-2123	PSK Mod/Demod 1200 BPS
H	CD-4049	Hex Inverter
I	CD-4016	Quad B1 - Lateral Switch
J	CD-4013	Dual D Flip-Flop
K	CD-4013	Dual D Flip-Flop
L	XR-1488	Quad Line Driver
M	XR-1489	Quad Line Receiver
N	XR-4194	Dual Tracking Regulator
O	74C193	Synchronous Up/Down Counter
P	74C193	Synchronous Up/Down Counter
Q	CD4011	Quad 2 Input Nand Gate
R	8048/8748	Microprocessor

C1	82 pF	C17	0.001μF
C2	0.033μF	C18	4.7μF
C3	0.022μF	C19	2.2μF
C4	0.1μF	C20	4.7μF
C5	0.033μF	C21	4.7μF
C6	0.033μF	C22	0.1μF
C7	0.033μF	C23	0.1μF
C8	0.033μF	C24	4.7μF
C9	0.033μF	C25	4.7μF
C10	0.033μF	C26	4.7μF
C11	0.1μF	C27	0.1μF
C12	0.22μF	C28	0.1μF
C13	4.7μF	C29	.22μF
C14	1 μF	C31	20 pF
C15	0.1μF	C32	20 pF
C16	0.001μF	C33	0.1μF
		C34	1μF

R1	2.2K	R2	2.2K	R3	2.2K
R4	2.2K	R5	1.2K	R6	1M
R7	10K	R8	1.6K	R9	1M
R10	1K	R11	1K	R12	62K
R13	100K	R14	47K	R15	62K
R16	10K	R17	100K	R18	470K
R19	100K	R20	1K	R21	10K
R22	62K	R23	47K	R24	100K
R25	18K	R26	62K	R27	1K
R28	4.7K	R29	10K	R30	1M
R31	120K	R32	10K	R33	1K
R34	68K	R35	600	R36	300
R37	600	R38	10K	R39	10K
R40	10K	R41	10K	R42	10K
R43	39K*	R44	180K*	R45	300**
R46	39K*	R47	180K*	R48	300**
R49	39K*	R50	300**	R51	180K
R52	13K	R53	71.5K	R54	10K
R55	1K	R56	10K	R57	10K
R58	10K	R59	1M	R60	10K
R61	10K	R62	220K	R63	20K
R64	20K	R65	29K	R66	20K
RA	1K	RB	1K	RC	1K

All resistor values are in ohms
* 1% Tolerance
** May Need Fine Tune

CRYSTALS

XTAL1 - 4.032 MHz M-TRON
XTAL2 - 1.000 MHz FOX
XTAL3 - 4.608 MHz X-TRON

TRANSFORMER

T1 - T2220 MICROTRAN

TRANSISTORS

Q1 - 2N4403 Q3 - 2N4401 Q4 - 2N4401

FETs

Q2 - 2N4861

DIODES

D1 - D6 1N914

EXAR Bell 212A Parts List

XR-2135A CCITT Data Buffer

GENERAL DESCRIPTION

The XR-2135A is a digital circuit designed to perform the function of data buffering for various serial data systems, including modems. Both the asynchronous-to-synchronous conversion and the synchronous-to-asynchronous conversion are performed at data rates up to 19.2 kBPS. The XR-2135A is selectable for character lengths of 8, 9, 10 and 11 bits. A combined enable/disable input is supplied for the synchronous-to-synchronous and asynchronous-to-synchronous converter sections. This input allows the same data lines to be used for synchronous or asynchronous modes of operation.

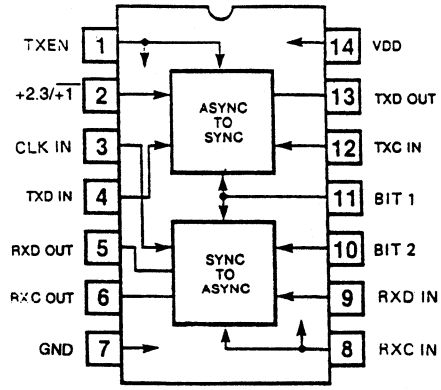
The receive data buffer section (synchronous-to-asynchronous) accepts input synchronous data along with a receive clock and converts this to an asynchronous format. The transmit data buffer (asynchronous-to-synchronous) accepts on the input asynchronous data and will synchronize the data to a transmit clock. The transmit data input can accept data from -2.5% underspeed up to +2.3% overspeed in 8, 9,10 bit and 11 bit word modes. The +2.,3/+1* pin selects the overspeed capability. Automatic break extension is included in case of a break being received.

The XR-2135A is constructed using polysilicon gate CMOS technology for low power and high speed operation. The master clock (CLK IN) can be clocked at speed up to 4.9152 MHz (19.2 kBPS data rate). The XR-2135A, available in a 14 pin package, is designed to operate with a single 5V supply.

FEATURES

Data Rates up to 19.2 kBPS
Asynchronous-to-Synchronous Conversion
Synchronous-to-Asynchronous Conversion
Independent Disable Inputs for Receiver and Transmitter Sections
Single 5 Volt Supply Operation
Underspeed and Overspeed capability of -2.5% to +1%or +2.5% to +2.3%
Missing Stop bit detector
Break extended for transmitted data
Programmable Character Lengths of 8, 9, 10 or 11 bits

PIN ASSIGNMENT



APPLICATIONS

Modem Data Buffers
Terminals
Data Communication Test Equipment

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.3 to +7.0 V
Input Voltage	-0.3 to VDD+0.3V
DC Input Current (any input)	±10 mA
Power Dissipation (Package Limitation)	250 mW
Storage Temperature Range	-65°C to +125C

ORDERING INFORMATION

Part Number	Package	Operating Temp
XR-2135ACN	Ceramic	0°C to 70°C
XR-2135ACP	Plastic	0°C to 70°C

ELECTRICAL CHARACTERISTICS

Test Conditions: VDD = 5VDC ±5%, TA = 25°C, CLK IN = 307.2 KHz ±0.01%, Data Rate = 1200 BPS $f_{TXC\ IN}$ = 1200 Hz $f_{RXC\ IN}$ = 1200 Hz ±0.01%, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DC CHARACTERISTICS						
V_{OL}	Output Low Voltage			0.05	V	I_{OL} = 20 uA
V_{OH}	Output High Voltage	4.8	5.0		V	I_{OH} = -20uA
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
I_{OL}	Output Low Current	2	7		mA	
I_{OH}	Output High Current		-9	-400	uA	
I_{IN}	Input Leakage Current	-10	0	10	uA	
I_{DD}	Supply Current Quiescent		100	250	uA	CLK IN, TXCIN, RXC IN At 5 VDC
AC CHARACTERISTICS						
t_{wstr}	Start Bit Width	819	821		uS	B1 = 1 B2 = 0 (10 bit)
BPS RANGE	Receiver Transmit Data Rate Capability	1170	1200	1212	BPS	8, 9, and 10 Bit Mode
f_{RXCO}	RXC OUT frequency Multiplier	1.5			Hz/Hz	RXC OUT = 1219 Hz

SYSTEM DESCRIPTION

The XR-2135A provides the complete interface between synchronous and character asynchronous formatted data systems. The synchronous side consists of two data lines TXD IN and RXD IN each with their respective clocks, TXC and RXC. Received data should change on the falling edge of RXC and be stable on the rising edge of RXC. The asynchronous-to-synchronous conversion handles data that is formatted so that the data bits or data and parity bits are bracketed by start and stop bits. Acceptable character lengths are 8, 9, 10 and 11 bits. The word length is pin selectable.

The XR-2135A is optimized for applications where a single clock is the source for the master clock (CLK IN), the TXDIN IN and RXC IN. The master clock (CLK IN) is 256 times the data rate. In modem applications, the RXC IN should be in lock with the received data, and jitter should be less than ±30 ns. The asynchronous transmit data being clock in by an asynchronous clock at the data rate (CLK IN/256). The asynchronous-to-synchronous converter when receiving overspeed data will shave on the stop bit. The break signal extended will detect a missing stop bit and extend this an additional character length and 3 bits.

PRINCIPLES OF OPERATION

The XR-2135A data buffer can be separated into three blocks: the asynchronous-to-synchronous converter for the transmitted data, the synchronous-to-asynchronous converter for the received data and the master clock divider.

The asynchronous-to-synchronous converter uses a two bit shift register to allow resetting of the stop bit to compensate for underspeed conditions.

A counter circuit, synchronized to the location of the stop start bit occurrence is used to control when the stop bit needs to be adjusted. An 11 bit shift register is used to monitor the data for the occurrence of a break signal.

The break extended is activated by the continuous reception of a series of logic 0s for one entire word's time (8, 9, 10 or 11 bits depending upon the setting of BIT 2 and BIT 1). When this occurs, the synchronized register is reset, and 2 words + 3 bits of logic 0s are shifted out and appear at TXD OUT.

If 1% overspeed data is received, and the modem is selected for 8, 9, 10 or 11 bit word operation, the stop bit in the word will be increased in width. In the case of underspeed, the stop bit will be truncated, when the one bit shift register is reset. When the +2.3% mode is selected the operation remains the same, only a different timer is used to determine the location of the stop bit.

The enable pin, Pin 1, controls the bypassing of the asynchronous-to-synchronous converter and the synchronous-to-asynchronous converter. The bypass mode is buffered and the delay through the buffer is less than 30 ns.

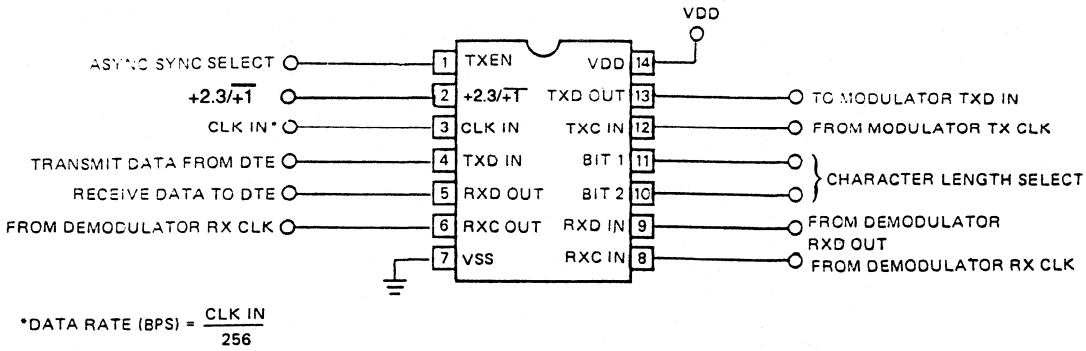
The synchronous to asynchronous converter contains a 21 bit synchronous shift register and a 8,9, 10 or 11 bit programmable parallel loading asynchronous shift register also uses a stop-start bit detector. The difference is that a missing stop bit detector is needed for synchronous data that is received without a stop bit. When this occurs, the last stage of the asynchronous shift register is set, and a stop bit re-inserted. The asynchronous shift register is clocked at a rate that is 1.5 times the nominal data rate. For 1200 BPS, this is 1219. For 9600 BPS, the rate would be 9744 BPS.

The master clock divider takes the CLK IN and divides by 256 to provide the internal data clocks as well as producing various reset pulses to perform the functions described above.

PIN DESCRIPTIONS

Pin#	Name	Description
1	TXDIN	Enable Input: This input when tied to a logic high permits the TXD IN to be clocked through the asynchronous-to-synchronous converter. When this input is tied to a logic low, the shift registers of the asynchronous-to-synchronous converter and synchronous-to-asynchronous converters are bypassed and both TXD IN and RXD IN are buffered and connected.
2	+2.3/+1%	Overspeed Enable Input: This input when tied to a logic high enables the asynchronous-to-synchronous converter to accept data at a rate from -2.5% to +2.3%. When dis-

		abled, the transmit data rate range acceptable is from -2.5% to +2.3%.
3	CLK IN	Master Clock Input: This clock provides the asynchronous clocks and reset pulses used by the XR-2135 to perform the asynchronous-to-synchronous conversion as well as the synchronous to asynchronous conversion. The formula to use for determining the data rate is CLK IN / 256 = data rate in BPS.
4	TXD IN	Transmit Data Input: The serial data should be applied to this pin. When 8, 9, or 10 bits are selected, the range for the data rate is -2.5% to +1%. This input has a high input impedance.
5	RXD OUT	Received Data Output: This is the asynchronous received data output (when RXEN is tied high). The data rate of this output is 1.5 times the synchronous data rate.
6	RXC OUT	Received Clock Output: This clock is synchronized with the RXD OUT. It should be noted that when stop bits are being inserted or deleted, the clock will produce a pulse at the time of the stop bit.being shifted out at R XD OUT.
7	GND	This pin should be tied to the digital ground of the system using the XR-2135.
8	RXC IN	Receive Clock Input: The received clock synchronous with the received data should be tied to this pin. The acceptable jitter is only ±30ns relative to the data. The data should be stable on the rising edge of this clock and change on the falling edge. If the received data is bit asynchronous (no clock relative to the data) this pin does not have to be clock for the data to appear at RXD OUT if RXEN is at a logic low.
9	RXD IN	Received Data input: The synchronous data is applied to this pin.
10 11	BIT 2 BIT 1	Character Length Select: These two digital inputs control the length of the word that will be applied to the XR-2135. Refer to Table 2 for the truth table of the function.
12	TXC IN	Transmit Clock Input: The system clock that the transmit data is to be synchronized to be tied to this pin. Note that this clock must be locked to the master clock CLK IN. Acceptable variation is+0.01%. In many modem applications this is not a problem.
13	TXDOUT	Transmit Data Output: This output provides the serial data synchronous to the clock applied to TXCIN if TXEN is at a logic high. In an underspeed situation, all bits will be shortened. In an overspeed situation, all bits will be widened. If TXEN is at a logic low this output will provide a buffered version the data at TXD IN. The amount of delay is 30 ns.
14	V_{DD}	Positive Supply: This input should be tied to 5 V ± 5%. A 0.1 µF decoupling capacitor should be adequate for decoupling any system noise to ground.

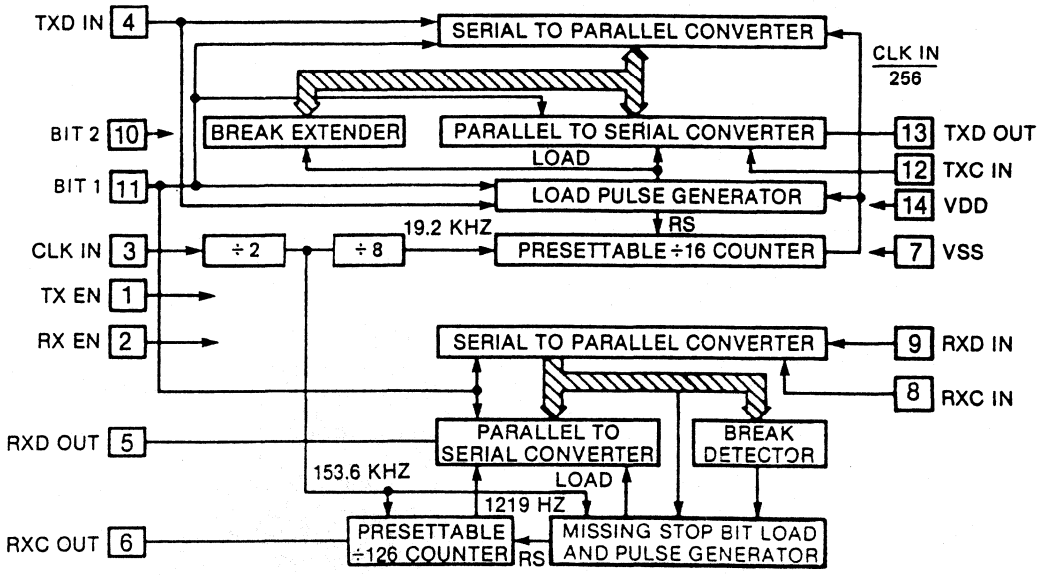


*DATA RATE (BPS) = $\frac{\text{CLK IN}}{256}$

Figure 1. Test Circuit

BIT 1 (11)	BIT 2 (10)	CHARACTER LENGTH
0	0	8 Bit
0	1	9 Bit
1	0	10 Bit
1	1	11 Bit

Table 2. Character Length Selection



FREQUENCIES SHOWN ARE FOR 1200 BPS OPERATION,
CLK IN EQUALS 307.2 KHZ

Figure 2. Equivalent Schematic Diagram

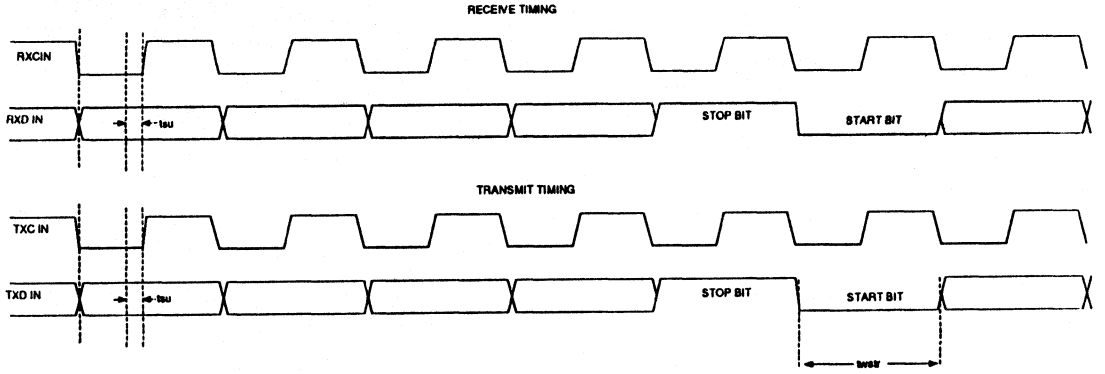


Figure 3. Transmit Receive Timing Characteristics

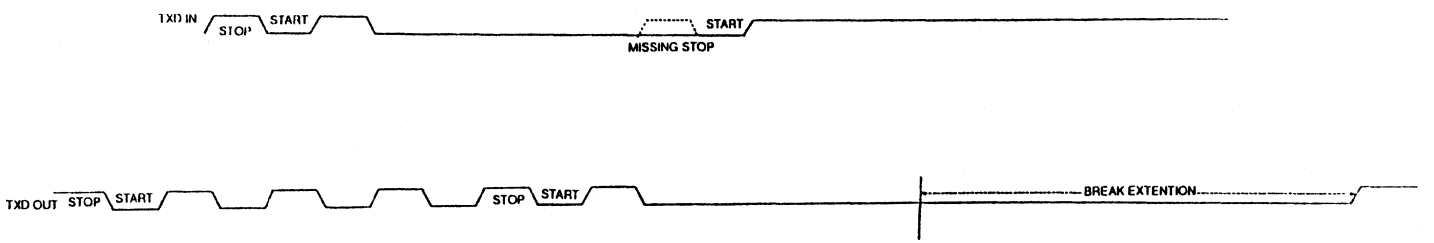


Figure 4. Break Extention and Data Delay Example At 8 Bit Word Length

FSK Modem System

GENERAL DESCRIPTION

The XR-14412 contains all the necessary circuitry to construct a complete FSK modulator/demodulator (MODEM) system. Included is circuitry for pin-programmable frequency bands, either U.S. or foreign (CCITT) standards for low-speed MODEMS. The XR-14412 provides T^2L-compatible inputs and outputs. Included in the XR-14412 are features for self-testing and an echo suppression tone generator. The XR-14412 utilizes complementary MOS technology for low-power operation.

FEATURES

Simplex, Half-Duplex, and Full-Duplex Operation
Crystal Controlled
Answer or Originate Modes
Single Supply Operation
Self-test Mode
Selectable Data Rates—300, or 600 bps
T^2L- or CMOS-Compatible Inputs and Outputs
Echo Suppressor Disable Tone Generator
U.S. or Foreign (CCITT) Compatible

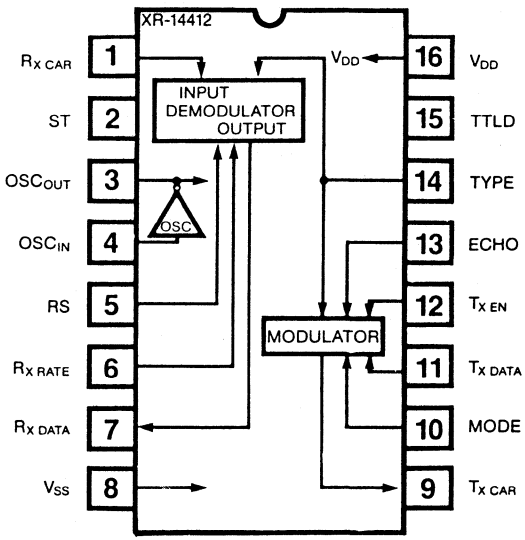
APPLICATIONS

Stand-Alone MODEMS
Remote Terminals
Acoustical Couplers
Built-in MODEMS

ABSOLUTE MAXIMUM RATINGS

Power Supply	
XR-14412V	6V
Any Input Voltage	V_{DD} + .5V to V_{SS} − .5V
Output Current from any Pin (Except Pins 7 or 8)	10 mA
Output Current from Pin 7 or 8	35 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	
Ceramic Package	1000 mW
Derate Above T_A = +25°C	8.0 mW/°C
Plastic Package	625 mW
Derate Above T_A = +25°C	5.0 mW/°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Voltage Range
XR-14412VP	Plastic	4.75V to 6V
XR-14412VN	Ceramic	4.75V to 6V

SYSTEM DESCRIPTION

The XR-14412 is basically comprised of two main components; the FSK modulator and demodulator. The modulator serves to convert or encode incoming binary data into two discrete frequencies. The pair of frequencies generated are determined by which standard (US or CCITT), and mode (answer or originate), are selected. These frequencies are within a range suitable for transmission over the telephone lines. The demodulator performs the opposite function by decoding the received pairs of frequencies into binary data. It also responds to those frequencies selected by the standard and mode selected. All functions within the XR-14412 are digital and controlled by a master clock. This clock is generated by an external crystal connected between the OSC_{IN} and OSC_{OUT} pins. As well as being used internally by the 14412, the clock may be used to clock other circuitry by using the OSC_{OUT} pin.

XR-14412

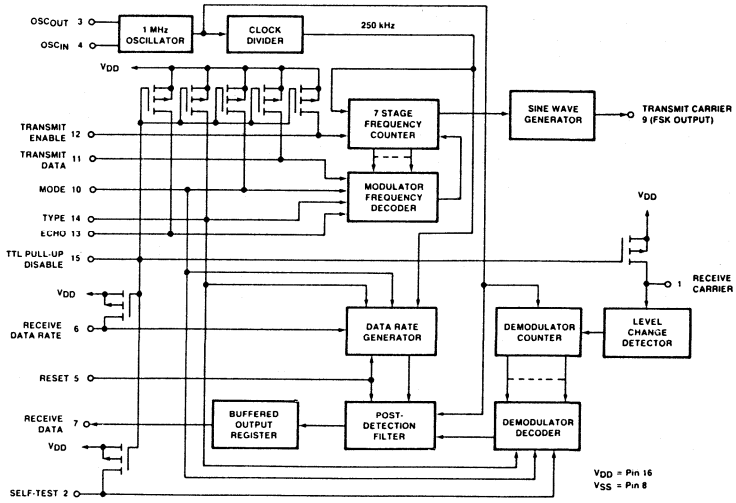
ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	V_{DD} Vdc	−40°C **		+25°C			+85°C **		UNIT
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{OL}	Output Voltage "0" Level $V_{IN} = V_{DD}$ or 0	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
V_{OH}	"1" Level $V_{IN} = 0$ or V_{DD}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
V_{IL}	Input Voltage* "0" Level ($V_O = 4.5$ or 0.5 Vdc)	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
V_{IH}	"1" Level ($V_O = 0.5$ or 4.5 Vdc)	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
	Pins 12, 15	5	0.75	—	0.8	2.0	—	0.85	—	
I_{OH}	Output Drive Current ($V_{OH} = 2.5$) (Pin 7)	5	−0.62	—	−0.5	−1.5	—	−0.35	—	mAdc
I_{OL}	($V_{OL} = 0.4$)	4.75	2.3	—	2.0	4.0	—	1.6	—	mAdc
I_{IN}	Input Current (Pin 15 = V_{DD})	—	—	—	—	±0.00001	±0.1	—	—	μAdc
I_P	Input Pull-up Resistor Source Current (Pin 15 = V_{SS}, $V_{IN} = 2.4$ Vdc) Pin 1,2,5,6,10,11,12,13,14	5	285	—	250	460	—	205	—	μAdc
C_{IN}	Input Capacitance	—	—	—	—	5.0	—	—	—	pF
I_T	Total Supply Current (Pin 15 = V_{DD})	5	—	4.5	—	1.1	4.0	—	3.5	mAdc
ACC	Modulator/Demodulator Frequency Accuracy (Excluding Crystal)	5	—	—	—	0.5	—	—	—	%
V_{2H}	Transmit Carrier Output 2nd Harmonic	5	—	—	−20	−26	—	—	—	dB
V_{OUT}	Transmit Carrier Output Voltage ($R_L = 100$ kΩ) (Pin 9)	5	—	—	0.2	0.30	—	—	—	V_{RMS}
		10	—	—	0.5	0.85	—	—	—	
		15	—	—	1.0	1.5	—	—	—	
t_{TLH}, t_{THL}	Receive Carrier Rise and Fall Times (Pin 1)	5	—	15	—	—	15	—	15	ns

*DC Noise Immunity (V_{IL},V_{IH}) is defined as the maximum voltage change from an ideal "0" or "1" input level, that the circuit will withstand before accepting an erroneous input.

**Note: -40°C and +85°C minimum and maximum, are guaranteed, but not tested in production.

EQUIVALENT SCHEMATIC DIAGRAM



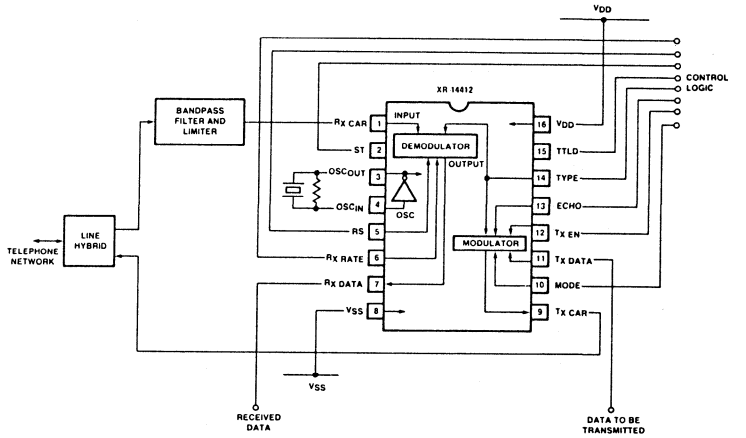


Figure 1. Typical Connection of the XR-14412 in a Complete Modem System

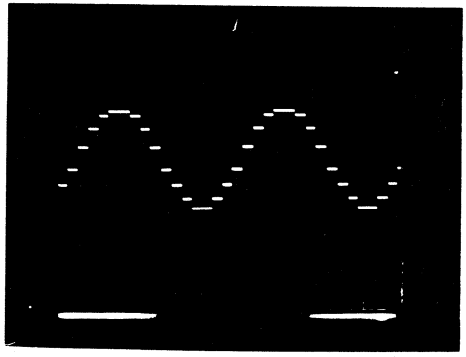


Figure 2. Transmit Carrier Sine Wave

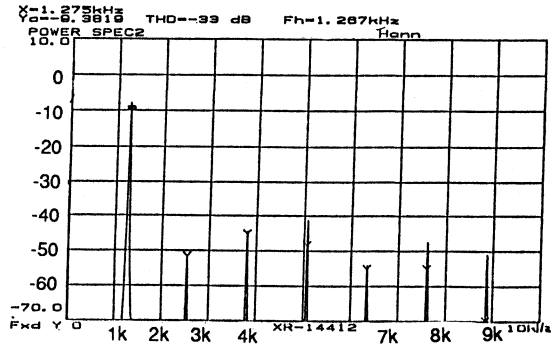


Figure 3. Typical Transmit Carrier Frequency Spectrum

PRINCIPLES OF OPERATION

Figure 1 shows the typical connection for the XR-14412 as a modem system. The system has four main component blocks. They are FSK modulator and demodulator, which are contained in the XR-14412, the bandpass filter, and the line hybrid. The function of each block is as follows:

Line Hybrid: This block acts to direct received FSK information to the bandpass filter and demodulator, while the FSK modulated carrier is directed to the telephone network.

Bandpass Filter and Limiter: Received FSK information is filtered by this block to remove extraneous signals received from the telephone network. The local transmitter carrier is also filtered out. The limiter stage is used to provide the XR-14412 with a TTL- or CMOS-compatible signal.

Modulator: This block, contained in the XR-14412, converts serial binary data into an FSK-encoded carrier signal. The carrier frequency is controlled by the mode and type inputs. Input data must be TTL- or CMOS-compatible. The output of the modulator is a digitally synthesized sine wave (see Fig. 2), with its harmonic content shown in Fig. 3.

Demodulator: This is used to convert an FSK-encoded carrier signal into serial data. The rate at which data can be received and decoded is controlled by the R_X rate and type control inputs.

Description of Control Inputs—Refer to Figure 1 and Table 1.

Type (Pin 14): This input is used to select either U.S. or CCITT operating frequencies.

Transmit Data (T_X DATA, Pin 11): This is the input for binary serial data.

Transmit Carrier (T_X CAR, Pin 9): This output provides a digitally synthesized sine wave derived from a 1 MHz crystal oscillator. The carrier frequency is controlled by the type and mode inputs.

Transmit Enable (T_X ENABLE, Pin 12): This pin is used to enable and disable the modulator, or T_X CAR, output.

Mode (Pin 10): In conjunction with the type input, the carrier frequencies are selected with this input.

Echo (Pin 13): This input is used to program the modulator to produce a 2100-Hz tone for disabling line echo suppressors.

Receive Data (R_X DATA, Pin 7): This is the binary data output resulting from demodulating the FSK-encoded receive carrier.

Receive Carrier (R_X CAR, Pin 1): The FSK-encoded receive carrier is fed into this input. The input signal must have either TTL or CMOS logic levels with a duty cycle of 50% ± 4%.

Receive Data Rate (R_X RATE, Pin 6): This input is used to adjust the demodulator for the incoming data rate.

Self-Test (ST, Pin 2): When a high level (ST = "1") is placed on this input, the demodulator is switched to the modulator frequency and demodulates the transmitted FSK signal.

Reset (R_S, Pin 5): This input can be used to disable the demodulator. With reset at logic "1", the demodulator output is forced high, logic "1". For normal operation, reset is tied low, logic "0".

Crystal (OSC_{IN}, OSC_{OUT}, Pin 4, Pin 3, respectively): A 1.0 MHz crystal is connected between these two pins for utilizing the on-chip oscillator. An external oscillator can also be used by feeding it into the OSC_{IN}, Pin 4, input. In the crystal mode, external parasitic capacitance, including crystal shunt capacitance, must be less than 9 picofarads at Pin 4.

TTL Pull-Up Disable (TTLD, Pin 15): All of the inputs to the XR-14412 have on-chip pull-up resistors. These pull-up resistors may be disabled when interfacing to CMOS logic by taking the TTLD input to a logic "1". For TTL logic interfacing, TTLD is tied to a logic "0".

APPLICATIONS

Figure 4 shows the XR-14412 connected as a 300-baud FSK modem. Amplifiers A_1 – A_3 are connected as bandpass filters to remove extraneous signals picked up from the phone line as well as local oscillator isolation. A_4 is connected as a comparator to provide limiting to the received carrier and provide the necessary square wave for Pin 1, R_X CAR, input. A_5 acts as a line hybrid. It provides amplification to the received carrier while attenuating the local oscillator, trying to go toward the bandpass filter. A_6 is simply used to buffer the T_X CAR, Pin 9, output of the XR-14412.

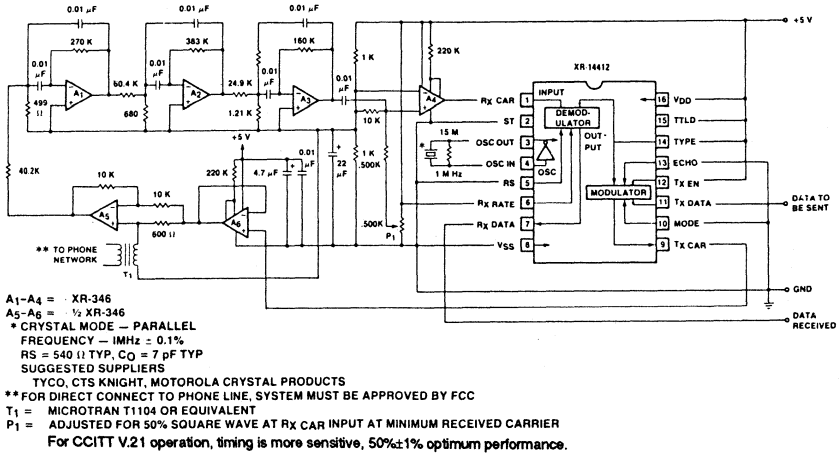
The configuration as shown is for answer mode, as the mode pin is at a logic "0". This circuit will work over a received carrier range of –10 dBm to –40 dBm.

Figure 5 shows a connection using the two spare amplifiers from the XR-346 to provide a carrier detect output. Here A_7 acts to amplify and peak detect the received carrier from the output of the bandpass filter. This voltage is then fed to A_8, connected as a comparator, to provide a logic output for carrier detect indication.

Table 1. Input/Output Controls

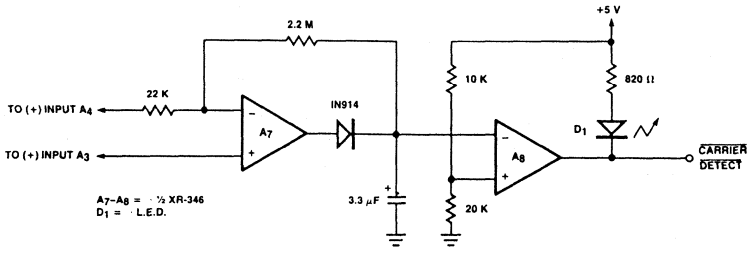
INPUTS					OUTPUTS				
T_X ENABLE (12)	R_X RATE (6)	MODE (10)	TYPE (14)	ECHO (13)	STANDARD	MODE	T_X DATA	T_X CARRIER	BAUD RATE
1	0	1	1	0	US	ORIGINATE	MARK 1	1270 Hz	600 bps
1	0	1	1	0	US	ORIGINATE	SPACE 0	1070 Hz	600 bps
1	0	0	1	0	US	ANSWER	MARK 1	2225 Hz	600 bps
1	0	0	1	0	US	ANSWER	SPACE 0	2025 Hz	600 bps
1	1	1	1	0	US	ORIGINATE	MARK 1	1270 Hz	300 bps
1	1	1	1	0	US	ORIGINATE	SPACE 0	1070 Hz	300 bps
1	1	0	1	0	US	ANSWER	MARK 1	2225 Hz	300 bps
1	1	0	1	0	US	ANSWER	SPACE 0	2025 Hz	300 bps
1	1	1	0	0	CCITT	CHANNEL 1	MARK 1	980 Hz	300 bps
1	1	1	0	0	CCITT	CHANNEL 1	SPACE 0	1180 Hz	300 bps
1	1	0	0	0	CCITT	CHANNEL 2	MARK 1	1650 Hz	300 bps
1	1	0	0	0	CCITT	CHANNEL 2	SPACE 0	1850 Hz	300 bps
1	X	0	0	1	CCITT	CHANNEL 2	— 1	2100 Hz	—
0	X	X	X	X	—	—	— —	NO OUTPUT	—

1 — Input or output is at a digital high, refer to Electrical Characteristics for exact value.
0 — Input or output is at a digital low, refer to Electrical Characteristics for exact value.
X — Can be either a 1 or a 0.



A_1–A_4 = ½ XR-346
A_5–A_6 = ½ XR-346
* CRYSTAL MODE — PARALLEL
FREQUENCY — 1MHz ± 0.1%
RS = 540 Ω TYP, C_O = 7 pF TYP
SUGGESTED SUPPLIERS
TYCO, CTS KNIGHT, MOTOROLA CRYSTAL PRODUCTS
** FOR DIRECT CONNECT TO PHONE LINE, SYSTEM MUST BE APPROVED BY FCC
T_1 = MICROTRAN T1104 OR EQUIVALENT
P_1 = ADJUSTED FOR 50% SQUARE WAVE AT R_X CAR INPUT AT MINIMUM RECEIVED CARRIER
For CCITT V.21 operation, timing is more sensitive, 50%±1% optimum performance.

Figure 4. Complete 300 Baud, Answer Mode, FSK Modem



A_7–A_8 = ½ XR-346
D_1 = L.E.D.

Figure 5. Carrier Detect Circuit

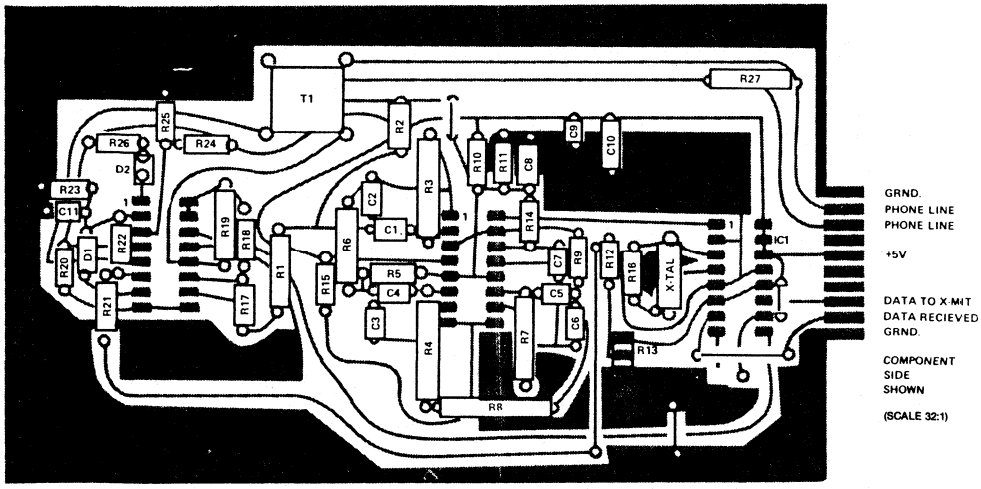


Figure 6. Complete FSK Modem Printed Circuit Board Layout (Circuit Shown in Figure 4)

3

Table 2. Parts List for 300 Baud MODEM.

*1% tolerance; all other resistors are 1/4W, 10%; all capacitors are 10%. Resistors are in ohms and capacitors are in μF.

	ANSWER	ORIGINATE		ANSWER	ORIGINATE
*R1	40.2K	47.5K	R24	20K	20K
*R2	499	191	R26	500	500
*R3	270K	357K	*R27	600	600
*R4	383K	270K			
*R5	680	160	C1–C6	.01	.01
*R6	60.4K	39.4K	C7	.1	.1
*R7	160K	160K	C8	22	22
*R8	24.9K	20K	C9	.01	.01
*R9	1.21K	360	C10	4.7	4.7
R10–R11	1K	1K	C11	3.3	3.3
R12	500K	500K			
R13	500K Pot	500K Pot	D1	IN914	IN914
R14	10K	10K	D2	LED	LED
R15	220K	220K			
R16	15M	15M	T1	Microtran T1104	Microtran T1104
R17–R18	10K	10K			
*R19	600	600			
R20	220K	220K	CRYSTAL	1 MHz ± .1%	1 MHz ± .1%
R21	22K	22K			
R22	2.2M	2.2M	A1–A8	XR-346	XR-346
R23	3.0K	3.0K			
R24	20K	20K	MODEM IC_1	XR-14412VP	XR-14412VP
R25	30K	30K			

FSK Modem Filter

GENERAL DESCRIPTION

The XR-2103 is a Monolithic Switched-Capacitor Filter designed to perform the complete filtering function necessary for a Bell 103 Compatible Modem. The XR-2103 is specifically intended for use with the XR-14412 Modulator/Demodulator to form a complete stand alone two-chip modem. In addition to complete high and low bandpass filters, the XR-2103 contains internal mode switching, auto-zeroing limiter and dedicated duplexer op amp. An on board carrier detect circuit is also included to complete the overall system. Designed for crystal-controlled operation, the XR-2103 operates from a 1.0 MHz crystal or external clock. Buffered clock output is provided for the XR-14412. A self-test circuit is included.

An input amplifier with programmable gain is provided for the receive signals. The XR-2103 contains an internal clock oscillator which accepts either a crystal or an external oscillator of 1 MHz.

The XR-2103, available in a 20 pin package, utilizes CMOS technology for low power operation with a supply voltage range from 4.75V to 6V.

FEATURES

Single 5 Volt Operation
Complete On Board Output Active Filters
Low Supply Current
Internal Answer/Originate Mode Switching
Programmable Input Receive Gain
Carrier Detect Output
Active Duplexer

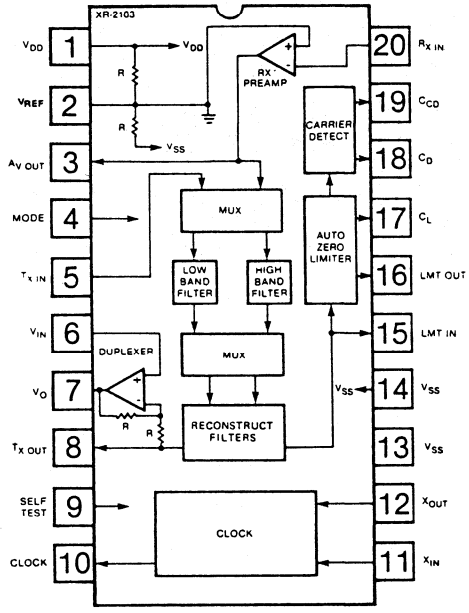
APPLICATIONS

Bell 103 Transmit/Receive Filtering
Complement to XR-14412 or Other Modulators/Demodulators

ABSOLUTE MAXIMUM RATINGS

Power Supply	16V
Power Dissipation Plastic Package	650 mW
Derate Above 25°C	5.0 mW/°C
Power Dissipation Ceramic Package	1.0 W
Derate Above 25°C	8.0 mW/°C
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C
Any Input Voltage	(V_{DD} + 0.5V) to (V_{SS} -0.5V)

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2103CP	Plastic	0°C to 70°C
XR-2103CN	Ceramic	0°C to 70°C
XR-2103ACP	Plastic	0°C to 70°C
XR-2103ACN	Ceramic	0°C to 70°C
XR-2103P	**Plastic**	**-20°C to +85°C**

SYSTEM DESCRIPTION

The XR-2103 internally consists of four main signal blocks. They are: input and output multiplexers to route the transmit and receive signals to the proper filter and output, according to the mode input; high and low band filters, 6 poles each, to perform precise bandpass filtering; output RC active filters to perform output reconstruction and filtering; carrier detection circuit for system interfacing.

The XR-2103 can also be interfaced with many microcontrollers for combining a FSK modem with a control or monitoring function.

The XR-2103ACP features tighter output limiter symmetry for easier interfacing with the XR-14412 modulator/demodulator.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5V, V_{SS} = 0V, X_{IN} = 1.0 MHz, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
V_{DD}	Power Supply Voltage Range	4.75		6.0	V	V_{SS} = 0
I_{DD}	Power Supply Current		7	10	mA	V_{DD} = 5V
ANALOG SECTION						
RECEIVE AMPLIFIER						
V_{OS}	Offset Voltage	-150		150	mV	
A_{OL}	Open Loop Gain		80		dB	R_L = 100Ω
I_B	Input Bias Current		1		mA	
SR	Slew Rate		2		V/μs	
	Output Swing	3	4.5		Vp-p	R_L = 100kΩ to V_{REF} (Pin 2)
DUPLEXER						
	Isolation		44		dB	R_2 = Line Resistance = 600Ω
	Output Swing	3	4.5		Vp-p	
V_{OS}	Offset Voltage	-150		150	mV	
LIMITER						
	Output Symetery	-1.5	±1	+1.5	%	XR-2103AC } C_C = 0.1μF from
		-3	±1.5	+3	%	XR-2103C } 50% Duty Cycle
	Output Swing		4		Vp-p	R_L = 1MΩ
	Output Current		100		μA	R_L = 1kΩ
CARRIER DETECT						
V_{th}	Threshold Voltage		-48		dBm	Receive Amplifier Gain =24 dB
	Hysteresis	2	4	6	dBm	
t_{on}	Turn On Time		⩾100		msec	C_{cd} = 0.1μf, V_{in} = 48dBm, Gain = 24dB
t_{off}	Turn Off Time		⩽100		msec	
LOW BAND FILTER						
f_o	Center Frequency	1160	1170	1180	Hz	
BW	Bandwidth			500	Hz	
V_{fs}	Full Scale Input		2.5		Vp-p	
A_r	Pass Band Gain	3	4	5	dB	
DR	Dynamic Range		50		dB	
PSRR	Power Supply Rejection		15		dB	f = 2 kHz
	Pass Band Ripple			2	dB	p-p 1070 Hz-1270 Hz
	High Band Rejection	40			dB	2025 Hz-2225 Hz
GD	Differential (Group) Delay		200	500	μs	1070 Hz-1270 Hz
	Clock Feedthrough		-60		dBV	**62.5 kHz w/1nF capacitor at pin 8**

HIGH BAND FILTER						
f_o	Center Frequency	2105	2125	2145	Hz	
BW	Bandwidth		500		Hz	
V_{fs}	Full Scale Input		2.5		Vp-p	
A_r	Pass Band Gain	3	4	5	dB	
DR	Dynamic Range		50		dB	
PSRR	Power Supply Rej.		18		dB	f = 1 kHz
	Pass Band Ripple			2	dB	p-p 2025 Hz - 2225 Hz
	Low Band Rejection	40			dB	1070 Hz - 1270 Hz
GD	Differential (Group) Delay		200	500	μs	2025 Hz - 2225 Hz
	Clock Feedthrough		-60		dBV	62.5 kHz
TRANSMIT						
V_{OS}	DC Offset Voltage	-150		+150	mV	
	Output Swing	2.2			Vp-p	R_2 = Line Resistance = 600Ω
	Output Current		1.2		mA	
DIGITAL CMOS LOGIC LEVELS (V_{DD} = 5V, V_{SS} = 0 V)						
V_{ih}	Input Voltage		2.75	3.5	V	'1' Level
V_{il}	Input Voltage	1.5	2.25		V	'0' Level
I_{oh}	Output Current	0.5	1.5		mA	'1' Level CLK OUT
I_{ol}	Output Current	1.0	5.0		mA	'0' Level CLK OUT
I_{oh}	Output Current	0.1	1.5		mA	'1' Level X OUT
I_{ol}	Output Current	0.2	0.9		mA	'0' Level X OUT

OPERATING PRINCIPLES

The XR-2103 contains all the filtering and multiplexing functions necessary for a Bell 103 type (300 baud) FSK modem. A complete modem requires only the XR-2103, the XR-14412, and telephone line interfacing hardware. A description of the main functional blocks follows.

Bandpass Filtering: Two six pole, 500 Hz bandwidth switched capacitor filters, designed for Bell 103 standard center frequencies of 1170 Hz (low band) and 2125 Hz (high band), constitute the main portion of the device. Both filters feature +4 dB passband gain, 50 dB dynamic range, and more than 40 dB opposite band rejection. Filter response curves are depicted in Figure 3. On board multiplexing allows using these filters for both transmitting and receiving. Active low pass filters reconstruct the time sampled output signals, characteristic of switched capacitor filters, and attenuate the unwanted energy above 15 kHz.

Duplexer: An operational amplifier is employed as an active two to four wire converter (duplexer). The two phone wires are "split" into transmit and receive components for proper processing; the transmit output from Pin 8 is applied to the lines through a resistor and the received signal is drawn from the line and routed into a preamplifier. Transmit energy appears as a common mode signal, hence does not appear on the duplexer output. The received signal, meanwhile, is amplified by two. Isolation is maximized when the transmit injection resistor (between Pins 6 and 8) is equal in magnitude to the phone line impedance (600 Ω nominal). Transmit signal levels are typically -9 dBm.

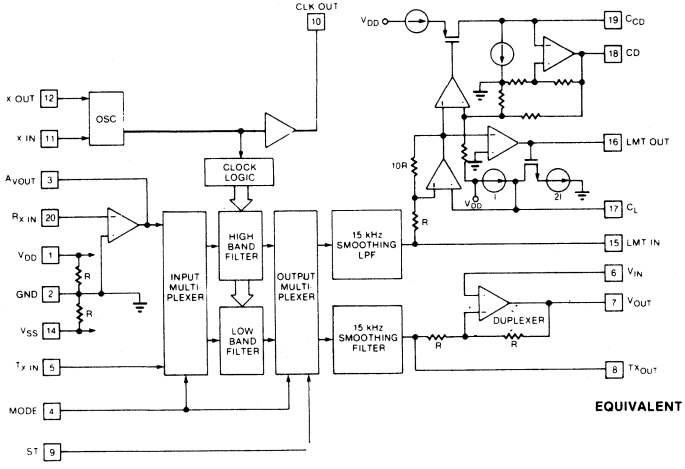
Received Carrier Amplifier: An operational amplifier, with its inverting input on Pin 20 and output on Pin 3, serves as a received carrier amplifier. Duplexer output (Pin 7) is routed to Pin 20 through a 100 kΩ or larger resistor. Gain, typically 5 (14 dB), equals the ratio of the feedback resistor (Pin 3 to Pin 20) to the input resistor (Pin 7 to Pin 20). The non-inverting input is internally biased to one half supply. The amplifier features open loop gain of 80 dB, output swings of 4.5 Vp-p, and a slew rate of 2V/μs. This pin-out allows flexible signal processing capabilities: for example, an input low pass filter for eliminating aliasing is easily achieved.

Auto-Zeroing Limiter: An automatic offset zeroing comparator (limiter) compensates for errors caused by system offset voltages and currents, and converts the received carrier into an accurate 50% duty cycle waveform. The resultant square wave on Pin 16 is at digital logic levels and can interface directly with the modulator/demodulator circuit.

Carrier Detector: An on board carrier detection circuit simplifies total system interfacing. Carrier detect output (Pin 18) pulls low when a suitable signal is received. With 14 dB of gain in the receiver preamplifier, the threshold level is -38 dBM and has 4 dB of hysteresis. Turn on/off delay time is externally programmable by a capacitor from Pin 19 to ground. A 0.1 μF unit yields 100 ms; delay is directly proportional to capacitance.

Clocking: Filter frequency accuracy is directly related to the clock frequency. The device operates within specifications with a 1 MHz clock, provided by either a 1 MHz crystal or by sharing the 1 MHz clock signal from the XR-14412. The device will operate at other clock frequencies, but the filter center frequencies will differ. The crystal and a parallel 10 MΩ resistor are attached between Pins 11 and 12. The crystal should be series resonant with a shunt capacitance less than 9 pF. Pin 10 is the buffered clock output for interconnection with other devices.

Self Test: An on board self test diagnostic activates an analog loop-back mode: the transmit carrier is routed through the proper filter and back through the receive limiter, allowing performance verification of all systems. T_X OUT and R_X IN are disabled when self test is high.



EQUIVALENT SCHEMATIC DIAGRAM

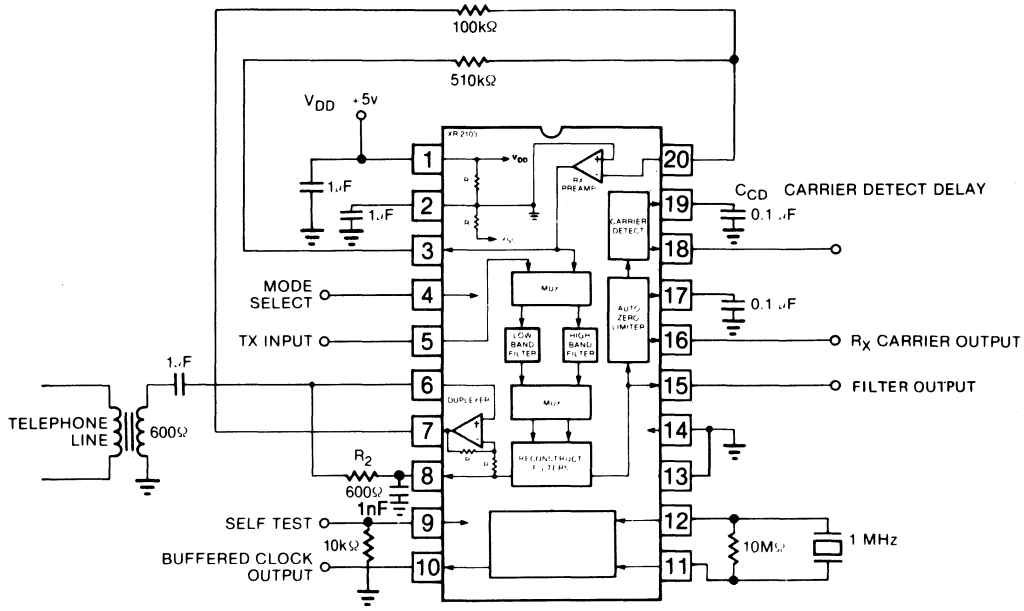


Figure 1. Basic Applications Circuit

Carrier detect threshold is -38dBm in this configuration.

STATE / LOGIC INPUT	0	1
MODE	ANSWER	ORIGINATE
ST	NORMAL OPERATION	SELF TEST MODE

Figure 2. Control Inputs

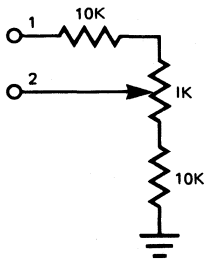


Figure 3. Reference Voltage Trimming for Performance Optimization

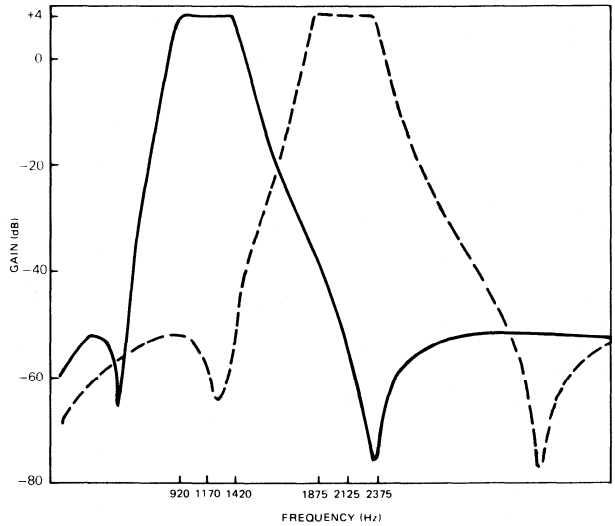


Figure 4. Filter Characteristics

APPLICATIONS

The Bell 103 compatible modem of Figure 5 consists of the XR-2103 FSK modem filter and the XR-14412 FSK modulator/demodulator. Designed for full duplex 300 baud operation, the circuit requires only telephone line and computer interfacing. The entire system uses a single 5V supply, and performs both answer and originate functions. Answer/Originate selection is controlled by the mode input; low input selects answer, high selects originate.

The telephone line is connected via an isolation transformer to the duplexer input (Pin 6) of the XR-2103. A resistor, equal to the line resistance, attaches from Pin 6 to the transmit output (Pin 8) and couples the transmit signal to the line. The received signal is removed from the line via the duplexer (also called a "two to four wire converter" or "hybrid"). Duplexer output is coupled through the receive carrier preamplifier into the multiplexer, where the proper band pass filter is selected. Transmit energy is seen as a common mode signal and does not appear on the duplexer output.

If the system is in the originate mode (mode pin pulled high), the received signal passes through the high band filter. Then, the sampled signal is reconstructed by an on board RC active low pass filter and is fed into the limiter and carrier detect circuit. Carrier detect output (Pin 18) pulls low after a 100 ms delay, controlled by the 0.1 μF capacitor on the C_{CD} pin (Pin 19). The limiter circuit compensates for circuit imperfections (offset voltages, etc.), and outputs a 50% duty cycle waveform to the demodulator input (Pin 1) of the XR-14412. The demodulated data appears on Pin 7 of the XR-14412.

Transmit data is applied to the modulator input (Pin 11) of the XR-14412. Depending on mode, answer or originate, the data modulates either the high or low band. The modulated signal exits Pin 9 and is applied to the transmit multiplexer input (Pin 5) of the XR-2103; is filtered, reconstructed, and sent into the duplexer and the phone line.

One shared time base is employed: here, the oscillator of the XR-2103 serves both devices. Buffered output is routed from Pin 10 of the XR-2103 into Pin 4 of the XR-14412.

With suitable telephone line coupling and data system interfacing, this modem realizes its goals of high performance and reliability at low cost.

With the 500 Hz filter bandwidth datarates can be achieved up to 450 BPS using the XR-2103 and XR-14412. For 600 BPS applications, the XR-1010 filter is recommended along with an external limiter.

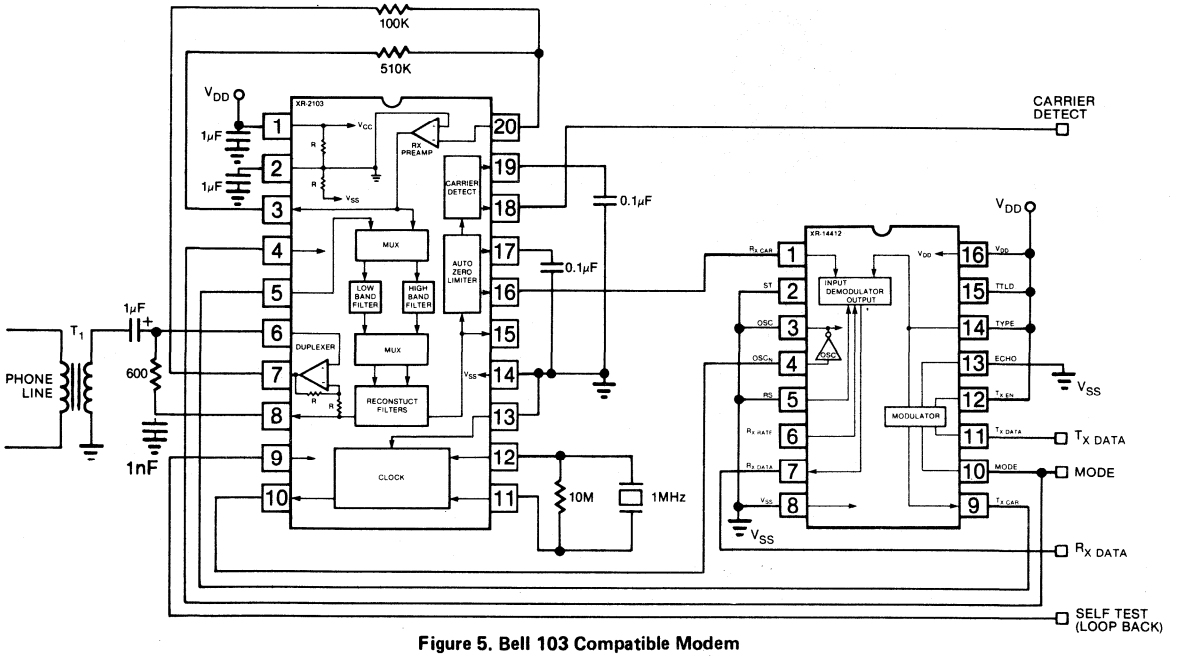


Figure 5. Bell 103 Compatible Modem

PSK Modem Filter

GENERAL DESCRIPTION

The XR-2120 is a self-contained bandpass filter set designed for realization of Bell 212A compatible 1200 bits/sec PSK modems. The XR-2120 utilizes CMOS technology and switched capacitor circuit techniques to minimize external components to a single crystal or frequency source. Contained in the device are two complete bandpass filters centered around the Bell standard 1200 Hz and 2400 Hz send **and receive frequencies. This filter also provides compromise line equalization. Additional features included are digitally programmable transmit and receive gains as sell as input anti-aliasing and complete output smoothing filters. Separate V_{SS} pins for transmit, receive, and digital sections are provided to minimize crosstalk.**

XR-2120C group delay specified within ±150µS. The device is available in a 22 pin (0.4 inch wide) plastic or ceramic package, and operate over a wide range of supply voltages.

FEATURES

On-board Crystal Oscillator With Buffered Output
Internal Anti-aliasing Filters
Complete On-board Output Active Filters
Digitally Programmable Transmit and Receive Gains
MODE Input Internally Switches Filters
for Answer/Originate
Single or Split Supply Operation
Center Frequencies Movable with Input Clock
High-Impedance Inputs (100 kΩ min)
1% Center Frequency Accuracy
Separate CLK IN and CLK OUT Pins

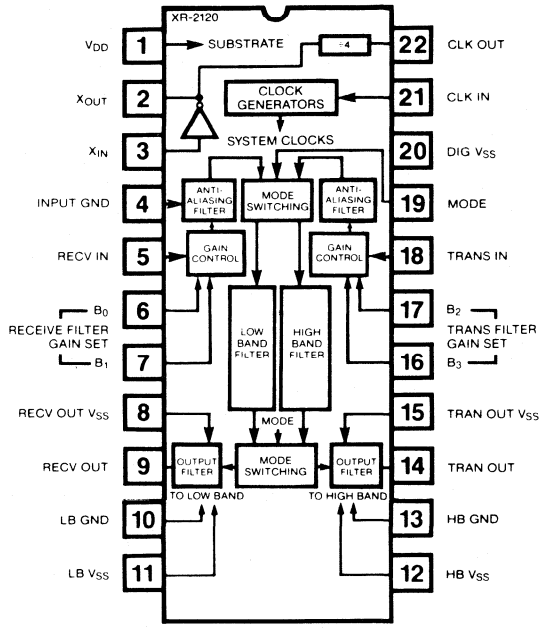
APPLICATIONS

Bell 212A Transmit/Receive Filtering
Answer Back Signal Filtering

ABSOLUTE MAXIMUM RATINGS

Power Supply	16V
Power Dissipation, Plastic	1.0W
Derate Above 25°C	5 mW/°C
Power Dissipation, Ceramic	1.3W
Derate Above 25°C	7 mW/°C
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C
Any Input Voltage	(V_{DD} + 0.5V) to (V_{SS} - 0.5V)

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2120CN	Ceramic	0°C to 70°C
XR-2120CP	Plastic	0°C to 70°C
XR-2120CQ	Plastic Quad Flat Pack	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2120 is comprised of four main signal blocks: The digitally programmable gain amplifier, an input anti-aliasing switched capacitor filter, switched capacitor bandpass filters at 1200 Hz and 2400 Hz, and output RC active filters. These sections serve to: (1) amplify and condition incoming signals, (2) remove noise which can cause aliasing problems in the bandpass filters, (3) provide very precise bandpass filtering and phase compensation, and (4) perform output reconstruction and filtering. To perform these necessary filtering and phase compensation functions, a total of 48 poles are used in the XR-2120.

The programmable gain stages provide 4 selectable gains for transmit or receive. Separate clock output and input pins are provided for flexibility.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5 V, V_{SS} = −5 V, X_{IN} = 4.032 MHz (CLK IN = 1.008 MHz), T_A = 25°C, unless otherwise specified. Input gain = 0 dB **(B1/B3 = B0/B2 = -5V_{DC})**.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
DIGITAL SECTION						
CLK OUT	CLK OUT Drive Capability			50	pF	
I_I	Digital Input Current	−1.0		1.0	μA dc	
V_{IL}	Digital Input Voltage	V_{SS}		V_{SS}+2	V	For "0" Level
V_{IH}		V_{DD}-2		V_{DD}	V	For "1" Level
ANALOG SECTION						
f_{OL}	Filter Center	1190	1200	1210	Hz	Low Band
f_{OH}	Frequencies	2380	2400	2420	Hz	High Band
BW	3 dB Bandwidth	900	950		Hz	**Both Bands**
R_i	Input Impedance	100k			Ohms	
C_i	Input Capacitance			10	pF	
f_{SI}	Anti-Aliasing Filter Sampling Frequency		504		kHz	**CLKIN/2**
f_{SB}	High/Low Band Sampling Frequency		126		kHz	**CLKIN/4**
	Tran/Recv Output Drive Capability	10k		50	Ohms pF	
	Output Clock Feedthrough			2	mV rms	at 126 kHz
$e_{o}100$	Output Noise		160		μV rms	In Passbands (100 Hz BW)
$e_{o}1000$	Output Noise		700		μVrms	In Passbands (1kHz BW)
ei_{range}	Dynamic Range of Filters		70		dB	Note 1
Vo_{sw}	Output Voltage Swing	6.0	6.8		V pp	Note 2
2ndHarm	2nd Harmonic Content		-60		dB	f_{IN} = 1200 Hz Referenced to Fundamental
T_{SW}	Mode Switching		10		ms	
I_{DD}	Supply Current		9	27	mA	
V_{SUP}	Supply Voltage Range	±4.75 9.5	±5 10	±7.5 15.0	V V	Dual Supplies V_{DD} Reference to V_{SS}
A_V	Passband Gain					Input Gain = 0 dB
	Low Band	3.2	4.2	5.2	dB	1200 Hz
		−1.4	0	1.4	dB	900 - 1500 Hz (Note 3)
	High Band	2.8	3.8	4.8	dB	2400 Hz
		−1.7	0	1.7	dB	2100 - 2500 Hz (Note 3)
		0	1.2	2.2	dB	2500 - 2800 Hz (Note 3)

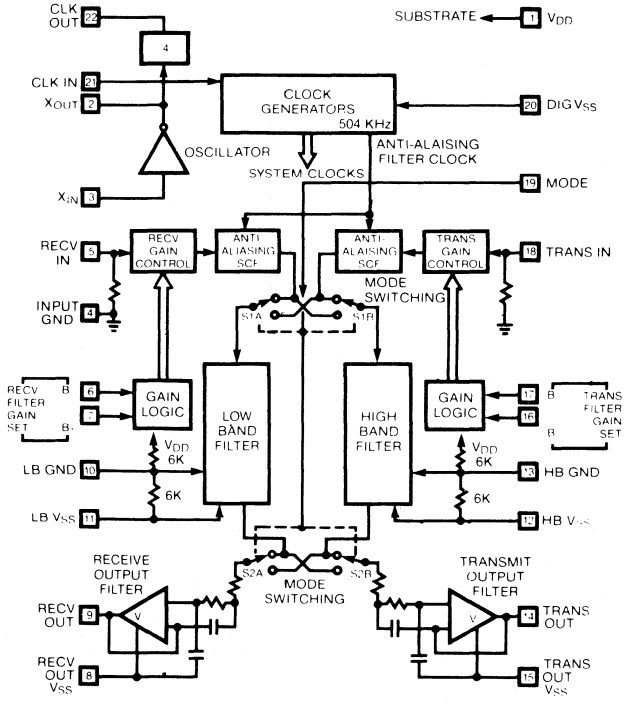
Note 1 Dynamic range is defined as ei_{range} = 20 Log (Vo_{sw}/e_o).
Note 2 Vo_{sw} is the maximum output swing before output clipping occurs.
Note 3 Gain measurements are relative to passband center frequency gain normalized to 0 dB.

ELECTRICAL CHARACTERISTICS Continued

FILTER RESPONSE

SYMBOL	PARAMETER	XR-2120C MIN	XR-2120C TYP	XR-2120C MAX	UNIT	CONDITIONS
GD	Group Delay Low Band Filter	5010	5160	5310	µs	900 Hz (See Figure 7)
		5050	5200	5350	µs	1kHz
		5110	5260	5410	µs	1.1kHz
		5150	5300	5450	µs	1.2kHz
		5165	5315	5465	µs	1.3kHz
		5205	5355	5505	µs	1.4kHz
		5210	5360	5510	µs	1.5kHz
	High Band Filter	5220	5370	5520	µs	2.1kHz (See Figure 8)
		4990	5140	5290	µs	2.2kHz
		5090	5240	5390	µs	2.3kHz
		4965	5115	5265	µs	2.4kHz
		4950	5100	5250	µs	2.5kHz
		4870	5020	5170	µs	2.6kHz
		4750	4900	5050	µs	2.7kHz

EQUIVALENT SCHEMATIC DIAGRAM



PRINCIPLES OF OPERATION

Figure 1 shows the typical connection for the XR-2120 in a split supply configuration. In this mode, Pins 4, 10, and 13, are simply tied to ground. For single supply operation, Pins 10 and 13 internally bias to half supply and should be externally bypassed with 2.2 μF capacitors. Pin 4 does not **contain an internally dc bias circuit, however, Pin 10 or 13 can provide it with a half supply bias point. In this connection, a 10kΩ resistor should be used between Pin 4, and Pin 10 or 13, with Pin 4 bypassed with a 2.2 μF capacitor.**

Signal flow is illustrated as shown in Figure 2. The transmit or receive signal will follow a path through four internal blocks. First it passes through a digitally programmable gain stage. The gain, as a function of a 2-Bit digital input, is shown in Figure 3. Next, the signal passes through a two-pole anti-aliasing low-pass filter at 12 kHz. This is used to remove noise around the main filter switching frequency of 126 kHz. The anti-aliasing filter is also a sampled-data filter, but is switched at a much higher rate of 504 kHz. It is necessary, therefore, to ensure that wideband noise above 252 kHz is not present at the inputs. In noisy environments a single noise pole RC filter at 30 kHz is usually sufficient for filtering input noise. The third signal block is the main bandpass filtering section at 1200 Hz or 2400 Hz, depending on the mode selected. The last section is the output smoothing filter; a two-pole RC active filter used to reconstruct the signal from its sampled data form.

The mode input pin is used to direct the transmit and receive signals to the appropriate filter section. Figure 4 shows mode selection logic convention.

The XR-2120 is designed to be operated with a 4.032 MHz crystal between the X_{IN} and X_{OUT} pins. The 4.032 MHz is divided by four and output on the CLK OUT pin, Pin 22. For normal operation, the CLK OUT is tied to the CLK IN pin, Pin 21; however, the bandpass center frequencies can be decreased by providing a divider between these two pins. An external CLK can be used by inputing a 1.008 MHz clock into the CLK IN pin, or a 4.032 MHz clock into the X_{IN} pin.

Figure 5 shows circuitry suitable for translating TTL signals to the CMOS levels required by all XR-2120 digital inputs. The amplitude and group delay characteristics of the XR-2120 are shown in Figures 6 through 8.

The XR-2120 may also be used in CCITT V.22 applications by adding guard tone notch filters as shown in Figure 9 or 10. This type of filter, when used with the XR-2120, will produce at least 60 dB of attenuation to either 550 Hz or 1800 Hz signals.

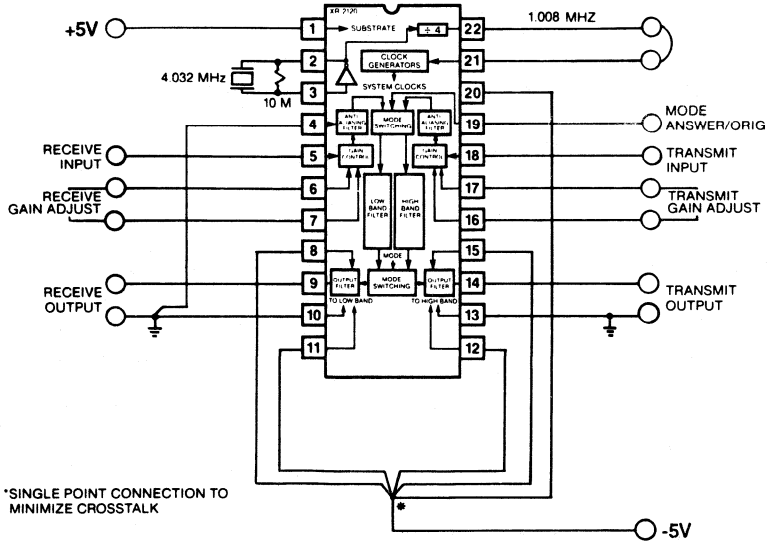


Figure 1: Typical Split Supply Connection.

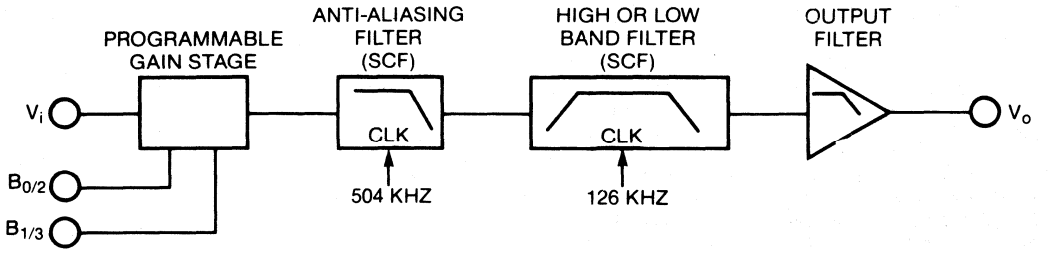


Figure 2: Signal Path

B1 / B3	B0 / B2	INPUT GAIN (dB)	
0	0	0	
0	1	6	
1	0	10	1 = Logic High (V_{DD})
1	1	14	0 = Logic Low (V_{SS})

Figure 3: Gain Programming (Nominal Gain Shown in Fig. 6)

MODE PIN	TRANSMIT	RECEIVE	TERMINOLOGY
1	Low Band	High Band	Originate
0	High Band	Low Band	Answer

Figure 4: Mode Selection Logic

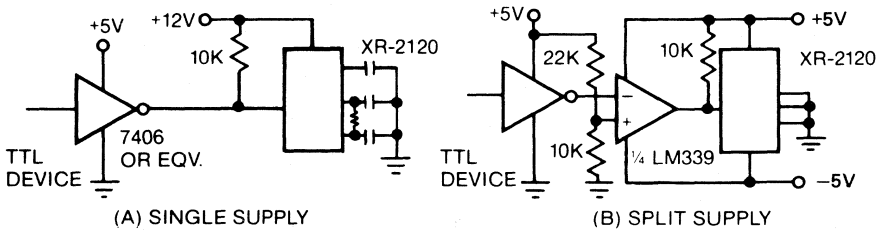


Figure 5: TTL Interfacing of Digital Inputs.

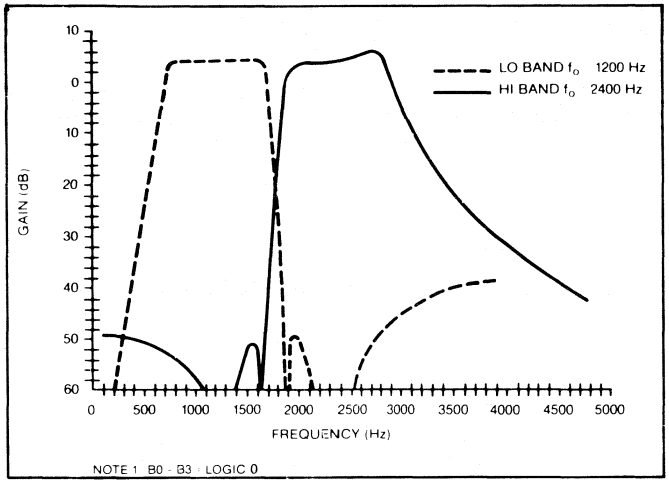


Figure 6: High and Low Band Amplitude Response.

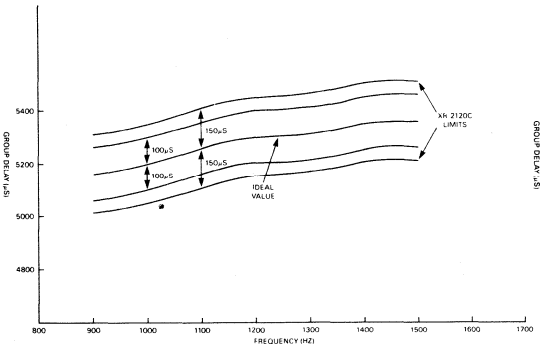


Figure 7: Low Band Group Delay Characteristics

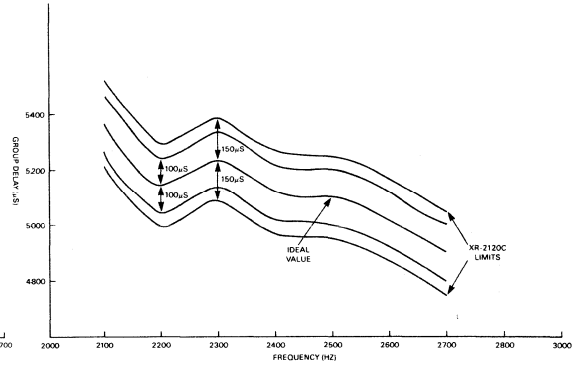


Figure 8: High Band Group Delay Characteristics

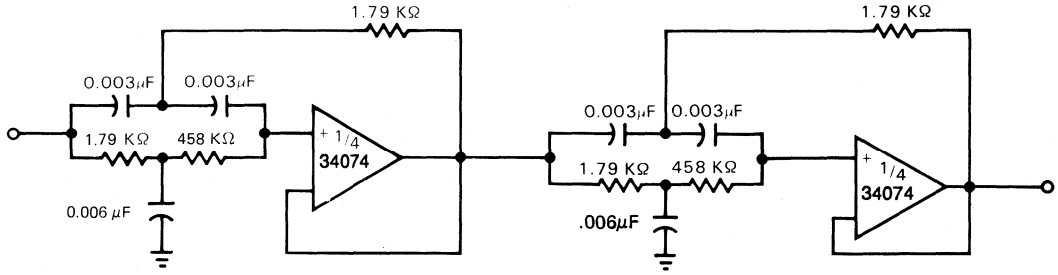


Figure 9. V.22 1800 Hz Notch Filter

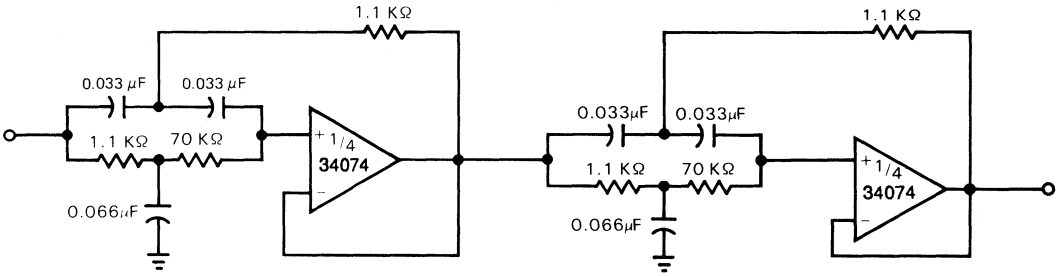


Figure 10. V.22 550 Hz Notch Filter

Asynchronous Receiver and Transmitter (UART)

GENERAL DESCRIPTION

The XR-16C450 is an universal asynchronous receiver and transmitter with modem control signals. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 56KHz. The XR-16C450 is fabricated in an advanced 2μ CMOS process to achieve low power, and high speed requirements.

FEATURES

Pin to pin and functionally compatible to INS8250, NS16C450
Modem control signals (CTS~,RTS~, DSR~, DTR~, RI~, DCD~)
Programmable character lengths (5, 6, 7, 8)
Even, odd, or no parity bit generation and detection
Status report register
Independent transmit and receive control
TTL compatible inputs, outputs

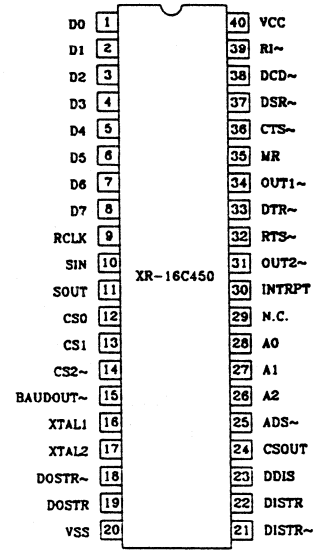
APPLICATIONS

RS232 receiver or transmitter
Serial to parallel / parallel to serial converter
Modem hand-shaking

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	7V
Voltage at any Pin	V_{SS} -0.3V to V_{CC} +0.3V
Storage Temperature	-55°C to +150°C
Power Dissipation	80 mW

PIN ASSIGNMENT



*** For 44 pin PLCC please refer to page 16**

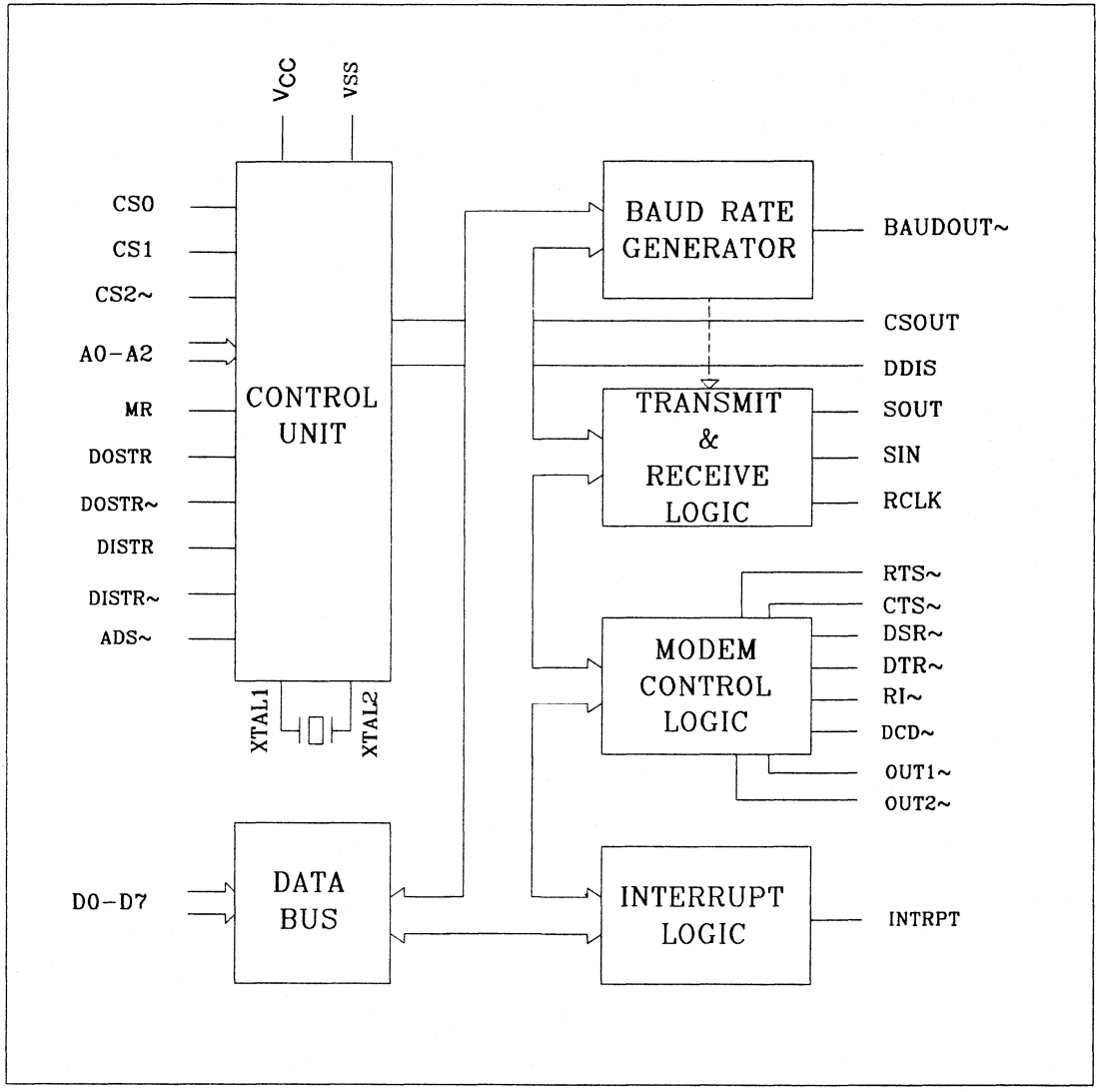
ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-16C450CP	Plastic DIP	0° C to +70° C
XR-16C450CJ	PLCC	0° C to +70° C

SYSTEM DESCRIPTION

The XR-16C450 is an improved version of the INS8250/ NS16C450 UART with higher speed operating access time. The XR-16C450 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The on-board status registers will provide the error conditions, as well as type and status of the transfer operations being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The XR-16C450 can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability.

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN	TYPE	DESCRIPTION
D0-D7	1-8	I/O	Bidirectional data I/O. Eight bit, three-state data bus to transfer information to or from the CPU. D0 is the least significant bit (LSB) of the data bus and is the first serial data bit to be received or transmitted.
RCLK	9	I	Receive clock input. The external clock input to the XR-16C450 receive section, as well as baud rate divisor input.
SIN	10	I	Serial data input. The serial information (data) received from MODEM or RS232 to XR-16C450 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the SIN input is disabled from external connection and connected to the SOUT output internally.
SOUT	11	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The SOUT will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS0	12	I	Chip select 1. (active high) A high at this pin (while CS1 = 1 and CS2~ = 0) will enable the UART / CPU data transfer operation.
CS1	13	I	Chip select 2. (active high) A high at this pin (while CS0 = 1 and CS2~ = 0) will enable the UART / CPU data transfer operation.
CS2~	14	I	Chip select 3. (active low) A low at this pin (while CS0 = 1 and CS1 = 1) will enable the UART / CPU data transfer operation.
BAUDOUT~	15	I	Baud rate generator clock output. This output provides the 16x clock of the internal selected baud rate.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal (parallel resonant) can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock the internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	I	Crystal input 2. See XTAL1.
DOSTR~	18	I	I/O write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the UART.
DOSTR	19	I	I/O write strobe. (active high) Same as DOSTR~, but uses active high input. Note that only an active DOSTR~ or DOSTR input is required to transfer data from CPU to XR-16C450 during write operation (while CS0 = 1, CS1 = 1 and CS2~ = 0). The unused pin should be tied to VCC or VSS(DOSTR~ = VSS or DOSTR = VCC) .
VSS	20	O	Signal and power ground.
DISTR~	21	I	I/O read strobe. (active low) A low level on this pin (while CS0 = 1, CS1 = 1 and CS2~ = 0) will transfer the contents of the XR-16C450 data bus to the CPU.

PIN DESCRIPTION

SYMBOL	PIN	TYPE	DESCRIPTION
DISTR	22	I	I/O read strobe. (active high) Same as DISTR~, but uses active high input. Note that only an active DISTR~ or DISTR input is required to transfer data from XR-16C450 to CPU during read operation (while CS0 = 1, CS1 = 1 and CS2~ = 0). The unused pin should be tied to VCC or VSS(DISTR~ = VSS or DISTR = VCC) .
DDIS~	23	O	Drive disable. (active low) This pin goes low when CPU is reading data from XR-16C450 to disable the external transceiver or logic.
CSOUT	24	O	Chip select out. A high on this pin indicates that the chip has been selected by the chip select input pins.
ADS~	25	I	Address strobe. (active low) A low on this pin will latch the state of the chip selects and addressed register. A rising edge is required if register and chip select pins are not stable during read and write operation.
A2	26	I	Address line 2. To select internal registers.
A1	27	I	Address line 1. To select internal registers.
A0	28	I	Address line 0. To select internal registers.
INTRPT	30	O	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
OUT2~	31	O	General purpose output. (active low) User defined output. See bit-3 modem control register (BIT-3 = 1 makes OUT2~ = 0).
RTS~	32	O	Request to send. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset this pin will be set to high.
DTR~	33	O	Data terminal ready. (active low) To indicate that XR-16C450 is ready to receive data. This pin can be controled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
OUT1~	34	O	General purpose output. (active low) User defined output. See bit-2 of modem control register (BIT-2 = 1 makes OUT1~ = 0).
MR	35	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS~	36	I	Clear to send. (active low) The CTS~is a modem control input. It's startup can be tested by reading the MSR Bit-4. CTS~has no effect on the transmitter output.

PIN DESCRIPTION

SYMBOL	PIN	TYPE	DESCRIPTION
DSR~	37	I	Data set ready. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART.
DCD~	38	I	Carrier detect. (active low) A low on this pin indicates that carrier has been detected by the modem.
RI~	39	I	Ring detect indicator. (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.
V_{CC}	40	I	Power supply input.

PROGRAMMING TABLE

DLAB	A2	A1	A0	READ MODE	WRITE MODE
0	0	0	0	Receive Holding Register	Transmit Holding Register
0	0	0	1		Interrupt Enable Register
x	0	1	0	Interrupt Status Register	
x	0	1	1		Line Control Register
x	1	0	0		Modem Control Register
x	1	0	1	Line Status Register	
x	1	1	0	Modem Status Register	
x	1	1	1	Scratchpad Register	Scratchpad Register
1	0	0	0		LSB of Divisor Latch
1	0	0	1		MSB of Divisor Latch

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC}= 5.0V ±10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
T_1	Address strobe width	30			ns	
T_2	Address setup time	30			ns	
T_3	Address hold time	5			ns	
T_4	Chip select setup time	25			ns	
T_5	Chip select hold time	0			ns	
T_6	DISTR/DISTR~ strobe width	75			ns	
T_7	Read cycle delay	50			ns	
T_8	Read cycle=$T_{20}+T_6+T_7$	135			ns	
T_9	DISTR/DISTR~to drive to disable delay			35	ns	100 pF load
T_{10}	Delay from DISTR/DISTR~ to data			75	ns	100 pF load
T_{11}	DISTR/DISTR~ to floating data delay	0		50	ns	100 pF load
T_{12}	DOSTR/DOSTR~ strobe width	50			ns	
T_{13}	Write cycle delay	55			ns	
T_{14}	Write cycle=$T_1+T_{12}+T_{13}$	135			ns	
T_{15}	Data setup time	10			ns	
T_{16}	Data hold time	25			ns	
T_{17}	Chip select output delay from select			50	ns	100 pF load
T_{18}	Address hold time from DISTR/DISTR~	0			ns	Note: 1
T_{19}	Chip select hold time from DISTR/DISTR~	0			ns	Note: 1
T_{20}	DISTR/DISTR~ delay from address	10			ns	Note: 1
T_{21}	DISTR/DISTR~ delay from chip select	10			ns	Note: 1
T_{22}	Address hold time from DOSTR/DOSTR~	5			ns	Note: 1
T_{23}	Chip select hold time from DOSTR/DOSTR~	5			ns	Note: 1
T_{24}	DOSTR/DOSTR ~delay from address	25			ns	Note: 1
T_{25}	DOSTR/DOSTR ~delay from select	10			ns	Note: 1
T_{26}	Reset pulse width	5			ns	
T_{27}	Clock high pulse duration	140				
T_{28}	Clock low pulse duration	140				External clock
TRANSMITTER						
T_{29}	Delay from rising edge of DOSTR/DOSTR~ to reset interrupt			75	ns	100 pF load

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
T_{30}	Delay from initial INT reset to transmit start	24		40	*	
T_{31}	Delay from initial Write to interrupt	16		24	*	
T_{32}	Delay from stop to next start			100	ns	
T_{33}	Delay from start bit low to interrupt high			8	*	
T_{34}	Delay from DISTR/DISTR~ to reset interrupt			75	ns	100 pF load
MODEM CONTROL						
T_{35}	Delay from DOSTR/ DOSTR~ to output			50	ns	100 pF load
T_{36}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{37}	Delay to reset interrupt from DISTR/DISTR~			70	ns	100 pF load
BAUD RATE GENERATOR						
N	Baud rate devisor	1		2^{16}-1		
T_{38}	Baud out negative edge delay			100	ns	100 pF load
T_{39}	Baud out positive edge delay			100	ns	100 pF load
T_{40}	Baud out down time	425			ns	100 pF load , Note: 2
T_{41}	Baud out up time	250			ns	100 pF load , Note: 2
RECEIVER						
T_{42}	Delay from RCLK to sample time			500	ns	
T_{43}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{44}	Delay from DISTR/DISTR~ to reset interrupt			200	ns	100 pF load

Note 1: Applicable only when ADS~ is tied low
Note 2: Fx=3.1 MHz clock
* Baudout~ cycle

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC}= 5.0V ±10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		V_{CC}	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		V_{CC}	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER (THR & RHR)

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register. Writing to this register will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transfered to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input. Receiver status codes will be posted in the Line Status Register.

XR-16C450 ACCESSIBLE REGISTERS

Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word lenght bit-1	word lenght bit-0
MCR	0	0	0	loop back	OP2~	OP1~	RTS~	DTR~
LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
MSR	CD~	RI~	DSR~	CTS~	delta CD~	delta RI~	delta DSR~	delta CTS~
SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

INTERRUPT ENABLE REGISTER (IER)
The Interrupt enable register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0 = disable the receiver ready interrupt
1 = enable receiver ready interrupt

IER BIT-1:
0 = disable transmitter empty interrupt
1 = enable transmitter empty interrupt

IER BIT-2:
0 = disable receiver line status interrupt
1 = enable receiver line status interrupt

IER BIT-3:
0 = disable the modem status register interrupt
1 = enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero

INTERRUPT STATUS REGISTER (ISR)

The XR-16C450 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the XR-16C450 provides the highest interrupt level to be serviced by CPU, no other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level	Source of the interrupts
1	ISR (Receiver Line Status Register)
2	RXRDY (Received Data Ready)
3	TXRDY (Transmitter holding register empty)
4	MSR (Modem Status Register)

ISR BIT-0:
0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropiate interrupt service routine.
1 = no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero.

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length and number of the stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00 = 5 bits word length
01 = 6 bits word length
10 = 7 bits word length
11 = 8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0 = 1 stop bit , when word length = 5, 6, 7, 8 bits
1 = 1 and 1/2 stop bit , when word length = 5 bits
1 = 2 stop bits, word length = 6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0 = no parity
1 = a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0 = odd parity is generated by calculating odd number of 1's in the transmitted data, receiver also checks for same format.
1 = an even parity bit is generated by calculating the number of even 1's in the transmitted or received data.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the stick parity format.
0 = parity bit is forced to "1" in the transmitted and received data.
1 = parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit.
1 = forces the transmitter output (SOUT) to go low to alert the communication terminal.
0 = normal operating condition.

LCR BIT-7:
The internal baud rate counter latch enable(DLAB).
0 = normal operation
1 = select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0 = force DTR~ output to high.
1 = force DTR~ output to low.

MCR BIT-1:
0 = force RTS~ output to high.
1 = force RTS~ output to low.

MCR BIT-2:
0 = set OUT1 output to high.
1 = set OUT1 output to low.

MCR BIT -3:
0 = set OUT2~ output to high.
1 = set OUT2~ output to low.

MCR BIT -4:
0 = normal operating mode.
1 = enable local loop-back mode (diagnostics). The transmitter output (SOUT) is set high (mark condition), the Receiver input (SIN), CTS~, DSR~, DCD~, and RI~ are disabled. Internally the transmitter output is connected to the receiver input and DTR~, RTS~, OUT1~ and OUT2~ are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupt are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)
This register provides the status of data transfer to CPU.

LSR BIT-0:
0 = no data in receive holding register.
1 = data has been received and saved in the receive holding register.

LSR BIT-1:
0 = no overrun error (normal).
1 = overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0 = no parity error (normal).
1 = parity error, received data does not have correct parity information.

LSR BIT-3:
0 = no framing error (normal).
1 = framing error received, received data did not have a valid stop bit.

LSR BIT-4:
0 = no break condition (normal).
1 = receiver received a break signal (SIN was low for one character time frame).

LSR BIT-5:
0 = transmit holding register is full. XR-16C450 will not accept any data for transmission.
1 = transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0 = transmitter holding and shift registers are full.
1 = transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to zero permanently.

MODEM STATUS REGISTER (MSR)
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the XR-16C450 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the XR-16C450 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the XR-16C450 has changed from a low to a high state.

MSR BIT-3:
Indicates that the DCD~ input to the XR-16C450 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS~ in the MCR during loop mode. It is the compliment of the CTS~ input.

MSR BIT-5:
This bit is equivalent to DTR~ in the MCR during loop mode. It is the compliment of the DSR~ input.

MSR BIT-6:
This bit is equivalent to OUT1~ in the MCR during loop mode. It is the compliment of the RI~ input.

MSR BIT-7:
This bit is equivalent to OUT2~ in the MCR during loop mode. It is the compliment to the DCD~ input.

SCRATCHPAD REGISTER (SR)
XR-16C450 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86

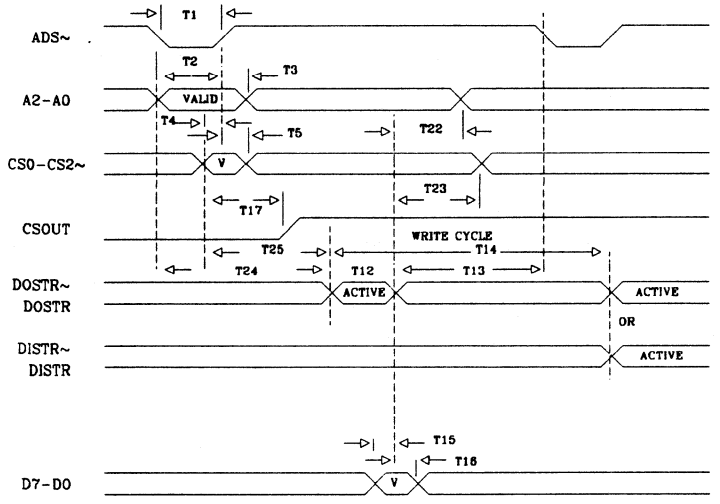
XR-16C450 EXTERNAL RESET CONDITION TABLE:

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1, LSR BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals

SIGNALS	RESET STATE
SOUT	High
OUT1~	High
OUT2~	High
RTS~	High
DTR~	High
INT	BITS 0-3=low

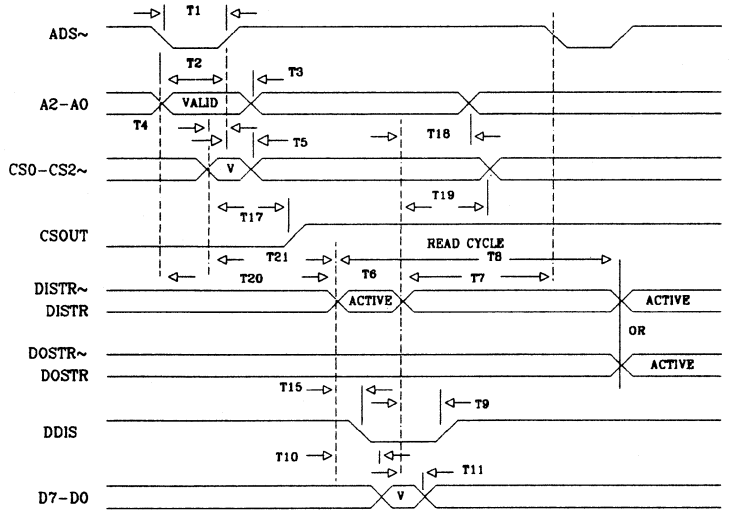
TIMING DIAGRAM

WRITE CYCLE TIMING



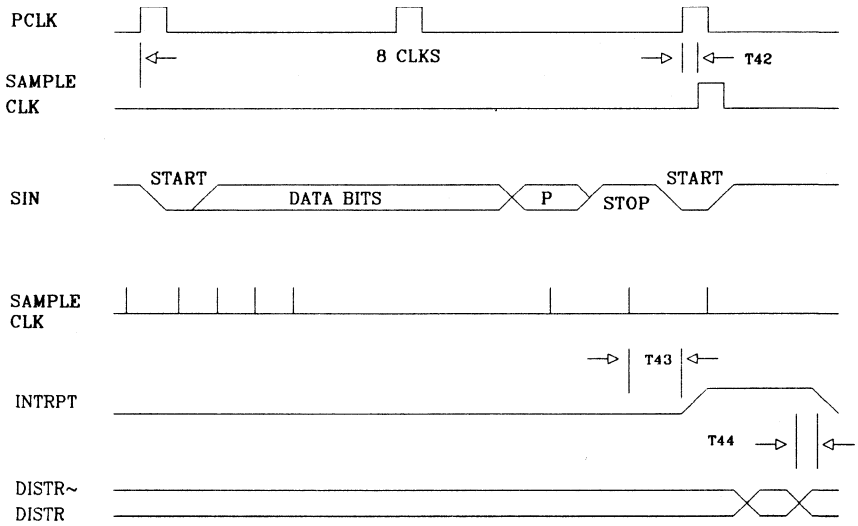
V = VALID
A = ACTIVE
P = PARITY

READ CYCLE TIMING

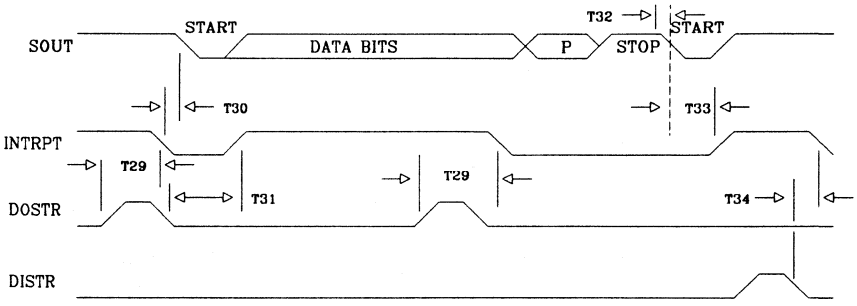


TIMING DIAGRAM

RECEIVER TIMING

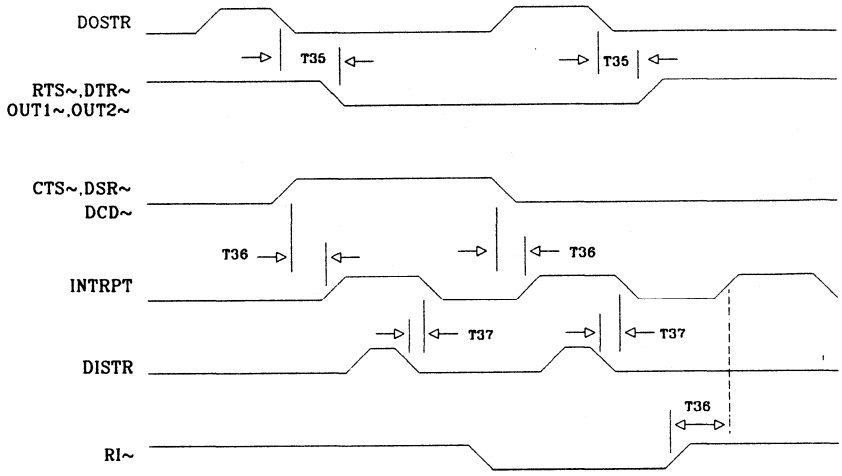


TRANSMITTER TIMING

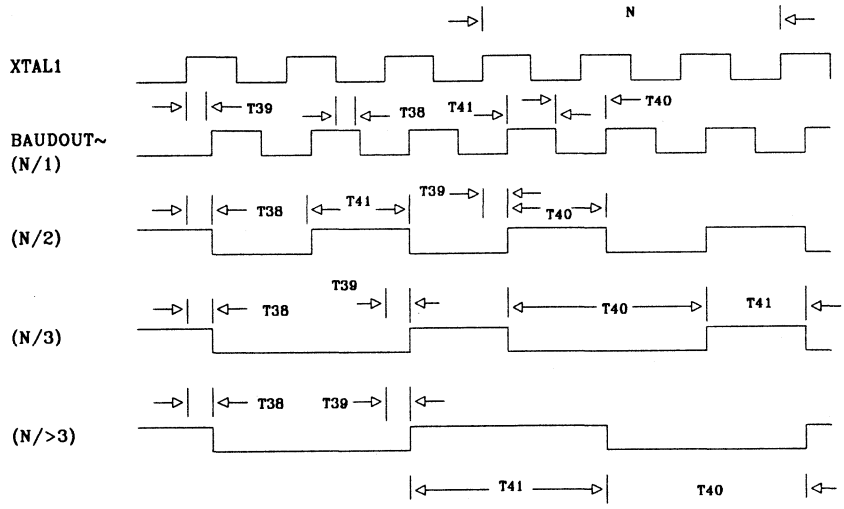


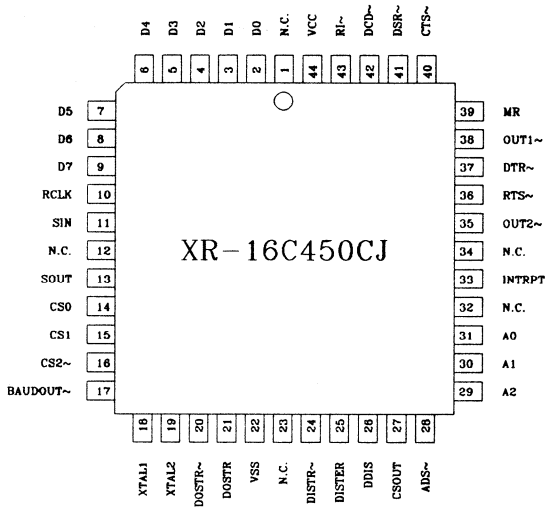
TIMING DIAGRAM

MODEM TIMING



BAUDOUT~ TIMING




D4 6
D3 5
D2 4
D1 3
D0 2
N.C. 1
VCC 44
RI~ 43
DCD~ 42
DSR~ 41
CTS~ 40
D5 7
D6 8
D7 9
RCLK 10
SIN 11
N.C. 12
SOUT 13
CS0 14
CS1 15
CS2~ 16
BAUDOUT~ 17
XR-16C450CJ
39 MR
38 OUT1~
37 DTR~
36 RTS~
35 OUT2~
34 N.C.
33 INTRPT
32 N.C.
31 A0
30 A1
29 A2
16 XTAL1
19 XTAL2
20 DOSTR~
21 DOSTR
22 VSS
23 N.C.
24 DISTR~
25 DISTER
26 DDIS
27 CSOUT
28 ADS~

CMOS Dual Channel UART (DUART)

GENERAL DESCRIPTION

The EXAR Dual Univeral Asynchronous Receiver and Transmitter (DUART) is a data communications device that provides two fully independent full duplex asynchronous communications channels in a single package. The DUART is designed for use in microprocessor based systems and may be used in a polled or interrupt driven environment.

Two basic versions of the DUART are available, each optimized for use with various microprocessor families: XR-88C681 for 8080/85, 8086/88, Z80, Z8000, 68xx and 65xx family based systems, and the XR-68C681 for 68000 family based systems. A programmable mode of the XR-88C681 version provides an interrupt daisy chain capability for use in Z80 and Z8000 based systems. However, the bus interfaces are general enough to allow interfacing with other microprocessors and microcontrollers. The XR-88C681 and XR-68C681 are enhanced versions of the Signetics, Motorola 2681 and 68681 respectively, and are pin and function compatible with those devices.

The DUART is fabricated using advanced two-layer metal high density CMOS process to provide high performance and low power consumption and is packaged in a 40 pin DIP. The XR-88C861 is also available in a 28 pin DIP.

FEATURES

Full Duplex, Dual Channel, Asynchronous Receiver and Transmitter
Quadruple-Buffered Receiver, Dual-Buffered Transmitter
Stop Bits Programmable in 1/16-bit Increments
Internal Bit Rate Generator with 23 Bit Rates
Independent Bit Rate Selection for Each Receiver and Transmitter
Maximum Bit Rate: 1x Clock - 1 Mb/Sec, 16x Clock - 125Kb/Sec
Normal, Autoecho, Local Loopback, and Remote Loopback Modes
Multi-Function 16-Bit Counter/Timer
Interrupt Output with Eight Maskable Interrupting Cond.
Interrupt Vector Output on Acknowledge
Programmable Interrupt Daisy Chain
Up to 15 I/O Pins (Depending on Package and Version)
Change of State Detectors on Inputs
Multidrop Mode Compatible with 8051 Nine-Bit Mode
On-Chip Oscillator for Crystal
Standby Mode to Reduce Operating Power
Advanced CMOS Low Power Technology

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Voltages with Respect to Ground	−0.5 V to +7.0 V

ORDERING INFORMATION

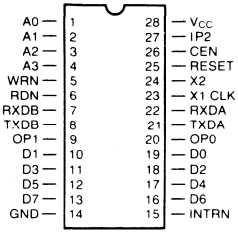
XR-88C681/40XX, XR-88C681/28XX, XR-88C681/24XX* and XR-68C681XX are offered in the following packages:

XX=Suffix	Package	Operating Temperature
CN	Ceramic	0°C to +70°C
N	Ceramic	-40°C to +85°C
M	Ceramic	-55°C to +125°C
ML	Ceramic LCC	-55°C to +125°C
CP	Plastic	0°C to 70°C
P	Plastic	-40°C to 85°C
CJ	PLCC	0°C to 70°C
J	PLCC	-40°C to 85°C

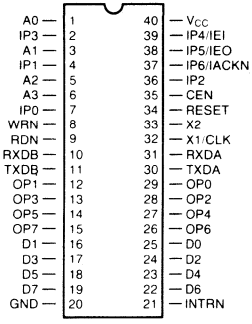
Please refer to back page for additional available packages.
*Ceramic DIP Only.

FUNCTIONAL BLOCK DIAGRAMS

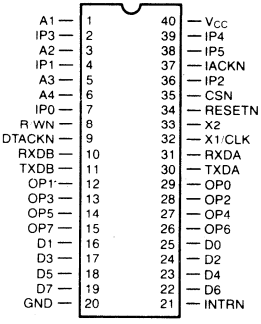
XR-88C681/28



XR-88C681/40



XR-68C681



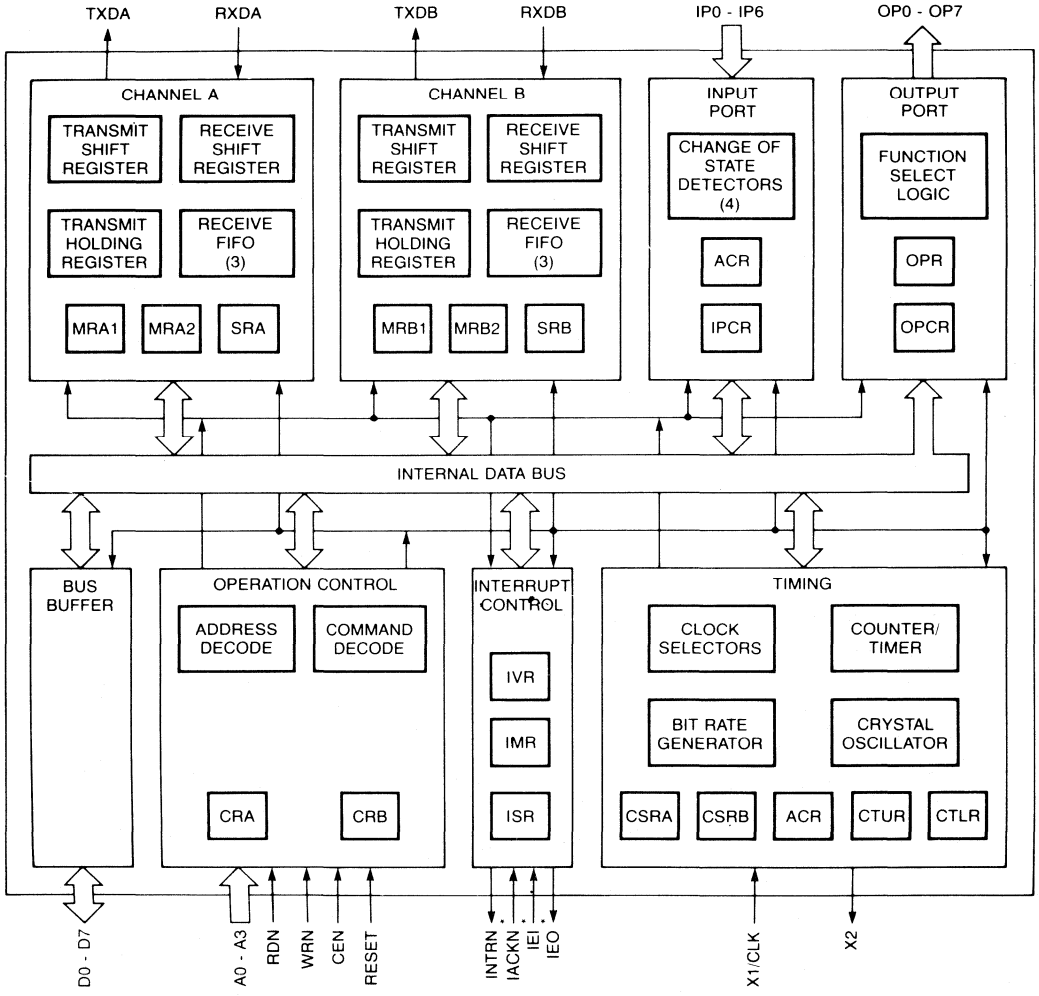
SYSTEM DESCRIPTION

Each channel of the DUART may be independently programmed for operating mode and data format. The operating speed of each receiver and transmitter can be selected from one of 23 internally generated fixed bit rates, from a clock derived from an internal counter/timer, or from an external 1x or 16x clock. The bit rate generator can operate directly from a crystal connected across two pins or from an external clock. The ability to independently program the operating speed of the receiver and transmitter of each channel makes the DUART attractive for split-speed channel applications such as clustered terminal systems.

Received data is quadruple-buffered in an on-chip FIFO to minimize the risk of receiver overrun or to reduce overhead in interrupt-driven applications. The DUART also provides a flow control capability to inhibit transmission from a remote device when the buffer of the receiving DUART is full, thus preventing loss of data.

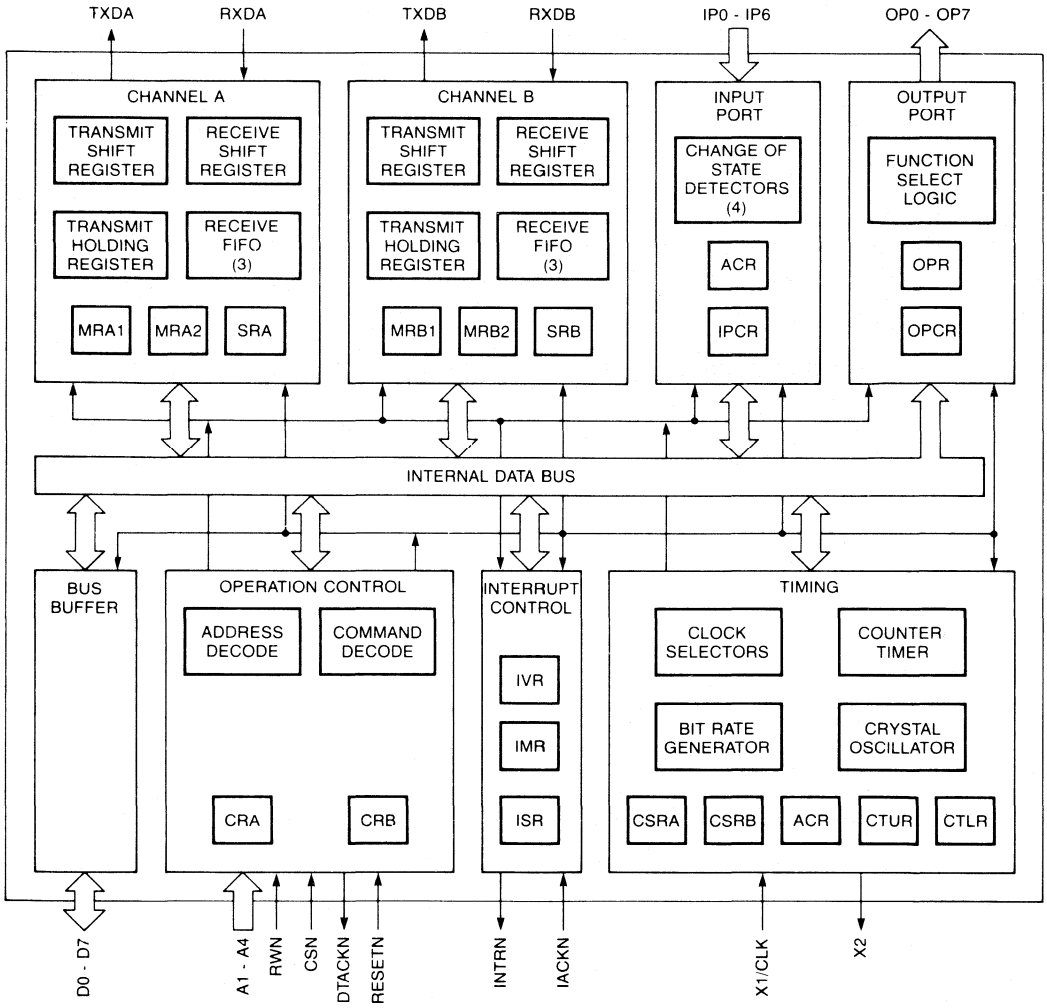
The DUART also provides a general purpose 16-bit counter/timer (which may also be used as a programmable bit rate generator), a multi-purpose input port and a multi-purpose output port. These ports can be used as general purpose I/O ports or can be assigned specific functions such as clock inputs or status/interrupt outputs under program control.

BLOCK DIAGRAM - XR-88C681



*ALTERNATE FUNCTIONS FOR IP4 - IP6

BLOCK DIAGRAM - XR-68C681



DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% [3, 4, 15] unless otherwise specified

Symbol	Parameter	Limits Min.	Typ.	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage (except X1/CLK)	2.0		V_{CC}	V	
V_{IH} [15]	Input High Voltage	2.2				T_A = −55° to 125°C
V_{IH1}	Input High Voltage (X1/CLK)	4.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.4 mA
V_{OH}	Output High Voltage (except open drain outputs)	2.4			V	I_{OH} = −400 µA
I_{IL}	Input Leakage Current (except X1/CLK, X2)	−10		10	µA	V_{IN} = 0 to V_{CC}
I_{X1L}	X1 Input Low Current		−4		mA	V_{IN} = 0
I_{X2L}	X2 Input Low Current		−30		µA	V_{IN} = V_{CC}
I_{X1H}	X1 Input High Current		0.2		mA	V_{IN} = V_{CC}
I_{X2H}	X2 Input High Current		30		µA	V_{IN} = V_{CC}
I_{LL}	Data Bus 3-State Leakage Current	−10		10	µA	V_O = 0 to V_{CC}
I_{OC}	Open Drain Output Leakage Current	−10		10	µA	V_O = 0 to V_{CC}
I_{CCA}	Power Supply Current [5]		10	15	mA	Active mode
I_{CCS}	Power Supply Current [5]		7	10	mA	Standby mode

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% [3, 4, 6]

Symbol	Parameter	Limits Min.	Typ.	Max.	Units
Reset Timing (Figure 4)					
t_{RES}	RESET Pulse Width	1.0			µs
XR88C681 Read and Write Cycle Timing (Figures 5 and 6) [7]					
t_{AS}	A0-A3 Setup Time to RDN, WRN Low	10			ns
t_{AH}	A0-A3 Hold Time from RDN, WRN High	0			ns
t_{CS}	CEN Setup Time to RDN, WRN Low	0			ns
t_{CH}	CEN Hold Time from RDN, WRN High	0			ns
t_{RW}	RDN, WRN Pulse Width	225			ns
t_{DD}	Data Valid from RDN Low			175	ns
t_{DF}	Data Bus Floating from RDN High	10		100	ns
t_{DS}	Data Setup Time to WRN High	100			ns
t_{DH}	Data Hold Time from WRN High	5			ns
t_{RWD}	High Time Between Reads and/or Writes [8, 9]	200			ns
XR88C681 Z-mode Interrupt Cycle Timing (Figure 6)					
t_{DIO}	IEO Delay Time from IEI			100	ns
t_{IAS}	IACKN Setup Time to RDN Low	Note 10			ns
t_{IAH}	IACKN Hold Time from RDN High	0			ns
t_{EIS}	IEI Setup Time to RDN Low	50			ns
t_{EOD}	IEO Delay Time from INTRN Low			100	ns

Notes: See page 23

AC ELECTRICAL CHARACTERISTICS continued

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% [3, 4, 6]

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units
XR68C681 Read, Write and Interrupt Cycle Timing (Figures 7, 8, 9)					
t_{AS}	A1-A4 Setup Time to CSN Low	10			ns
t_{AH}	A1-A4 Hold Time from CSN High	0			ns
t_{RWS}	RWN Setup Time to CSN Low	0			ns
t_{RWH}	RWN Hold Time from CSN High	0			ns
t_{CSW}	CSN High Pulse Width [9, 11]	90			ns
t_{CSD}	CSN or IACKN High from DTACKN Low [12]	20			ns
t_{DD}	Data Valid from CSN or IACKN Low			175	ns
t_{DF}	Data Bus Floating from CSN or IACKN High	10		100	ns
t_{DS}	Data Setup Time to CLK High	100			ns
t_{DH}	Data Hold Time from CSN High	0			ns
t_{DAL}	DTACKN Low from Read Data Valid	0			ns
t_{DCR}	DTACKN Low (Read Cycle) from CLK High			125	ns
t_{DCW}	DTACKN Low (Write Cycle) from CLK High			125	ns
t_{DAH}	DTACKN High from CSN or IACKN High			100	ns
t_{DAT}	DTACKN High Impedance from CSN or IACKN High			125	ns
t_{CSC}	CSN or IACKN Setup Time to CLK High [13]	90			ns
Port Timing (Figure 10) [7]					
t_{PS}	Port Input Setup Time to RDN/CSN Low	0			ns
t_{PH}	Port Input Hold Time from RDN/CSN High	0			ns
t_{PD}	Port Output Valid from WRN/CSN High			400	ns
Interrupt Output Timing (Figure 11)					
t_{IR}	INTRN or OP3-OP7 When Used As Interrupts High from:				
	Clear of Interrupt Status Bit in ISR or IPCR			300	ns
	Clear of Interrupt Mask Bit in IMR			300	ns
Clock Timing (Figure 12)					
t_{CLK}	X1/CLK (External) High or Low Time	100			ns
f_{CLK}	X1/CLK Crystal or External Frequency	2.0	3.6864	4.0	MHz
t_{CTC}	Counter/Timer External Clock High or Low Time (IP2)	100			ns
f_{CTC}	Counter/Timer External Clock Frequency (IP2)	0		4.0	MHz
t_{RTX}	RXC and TXC (External) High or Low Time [14]	220			ns
f_{RTX}	RXC and TXC (External) Frequency				
	16x	0		2.0	MHz
	1x	0		1.0	MHz
Transmitter Timing (Figure 13)					
t_{TXD}	TXD Output Delay from TXC (External) Low			350	ns
t_{TCS}	TXD Output Delay from TXC (Internal) Output Low	0		150	ns
Receiver Timing (Figure 14)					
t_{RXS}	RXD Data Setup Time to RXC (External) High	240			ns
t_{RXH}	RXD Data Hold Time from RXC (External) High	200			ns

Notes: See page 23

PIN DESCRIPTIONS - XR-88C681

Mnemonic	Type	Description
D0-D7	I/O	**8-bit Bidirectional Three-state Data Bus.** Bit 0 is the LSB and bit 7 is the MSB. All transfers between the CPU and the DUART take place over this bus. The bus is three-stated when the CEN input is high, except during an IACKN cycle in the Z-mode.
A0-A3	I	**Address Inputs.** These inputs select the DUART register or port for the current read/write operation.
CEN	I	**Chip Enable.** Active low. The data bus is three-stated when CEN is high. Transfers between the CPU and the DUART via D0-D7 are enabled when CEN is low.
WRN	I	**Write Strobe.** Active low. A low on this input while CEN is also low writes the contents of the data bus into the addressed destination. The transfer occurs on the rising edge of WRN.
RDN	I	**Read Strobe.** Active low. A low on this input while CEN is also low places the contents of the addressed source on the data bus. The transfer begins on the falling edge of RDN.
RESET	I	**Master Reset.** A high on this pin clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to 0FH, stops the counter/timer, puts OP0-OP7 in the high state, and places both serial channels in the inactive state with the TXDA and TXDB outputs marking (high).
INTRN	O	**Interrupt Request.** Active low, open drain. INTRN is asserted upon the occurrence of one or more of the chip's maskable interrupting conditions.
X1/CLK	I	**Crystal or External Clock Input.** This pin is the connection for one side of the crystal and a capacitor to ground when the internal oscillator is used (see figure 12). If the oscillator is not used, an external clock signal must be supplied at this input.
X2	I	**Crystal Input.** Connection for other side of the crystal. If the oscillator is used a capacitor must also be connected from this pin to ground. This pin may be connected to ground or left open if an external clock is supplied at X1/CLK.
RXDA, RXDB	I	**Receiver Serial Data Inputs.** The least significant bit is received first. If external receiver clock is specified, the data is sampled on the rising edge of the clock.
TXDA, TXDB	O	**Transmitter Serial Data Outputs.** The least significant bit is transmitted first. Held in the marking (high) state when the transmitter is idle or disabled or when the channel operates in local loopback mode. If external transmitter clock is specified, the data is shifted out on the falling edge of the clock.
OP0	O	**Output 0.** Can be programmed as a general purpose output or as the channel A request-to-send output (RTSAN). Active low.
OP1	O	**Output 1.** Can be programmed as a general purpose output or as the channel B request-to-send output (RTSBN). Active low.
OP2	O	**Output 2.** Can be programmed as a general purpose output, the channel A transmitter 1x or 16x clock output, or the channel A receiver 1x clock output. Active low. (40-pin package only).
OP3	O	**Output 3.** Can be programmed as a general purpose output, the channel B transmitter 1x clock output, the channel B receiver 1x clock output, or an open drain counter/timer ready output. Active low. (40-pin package only).
OP4	O	**Output 4.** Can be programmed as a general purpose output or as an open drain channel A RXRDY/FFULL output. Active low. (40-pin package only).
OP5	O	**Output 5.** Can be programmed as a general purpose output or as an open drain channel B RXRDY/FFULL output. Active low. (40-pin package only).
OP6	O	**Output 6.** Can be programmed as a general purpose output or as an open drain channel A TXRDY output. Active low. (40-pin package only).

Mnemonic	Type	Description
OP7	O	**Output 7.** Can be programmed as a general purpose output or as an open drain channel B TXRDY output. Active low. (40-pin package only).
IP0	I	**Input 0.** General purpose input or CTSAN, the channel A active low clear-to-send input. (40-pin package only).
IP1	I	**Input 1.** General purpose input or CTSBN, the channel B active low clear-to-send input. (40-pin package only).
IP2	I	**Input 2.** In the 40-pin package version, when configured in I-mode, IP2 is a general purpose input or the counter/timer external clock input. When configured in Z-mode, IP2 is a general purpose input, the counter/timer external clock input, or the channel B transmitter and receiver external clock input. In the 28-pin package version, IP2 is a multi-purpose input. It can be used as a general purpose input, the channel A and B receiver and transmitter external clock input, or as the external clock input for the counter/timer.
IP3	I	**Input 3.** When configured in I-mode, IP3 is a general purpose input or the channel A transmitter external clock input. When configured in Z-mode, IP3 is a general purpose input or the channel A transmitter and receiver external clock input. (40-pin package only).
IP4/IEI	I	**Input 4 or Interrupt Enable Input.** When configured in I-mode, this pin is a general purpose input or the channel A receiver external clock input (IP4). When configured in Z-mode, this pin is the interrupt enable active high input (IEI). (40-pin package only).
IP5/IEO	I/O	**Input 5 or Interrupt Enable Output.** When configured in I-mode, this pin is a general purpose input or the channel B transmitter external clock input (IP5). When configured in Z-mode, this pin is the interrupt enable active high output (IEO). (40-pin package only).
IP6/IACKN	I	**Input 6 or Interrupt Acknowledge Input.** When configured in I-mode, this pin is a general purpose input or the channel B receiver external clock input (IP6). When configured in Z-mode, this pin is the interrupt acknowledge active low input (IACKN). (40-pin package only).
V_{CC}	I	**+5 Volt Power Input.**
GND	I	**Signal and Power Ground.**

PIN DESCRIPTIONS - XR-68C681

Mnemonic	Type	Description
D0-D7	I/O	**8-bit Bidirectional Three-state Data Bus.** Bit 0 is the LSB and bit 7 is the MSB. All transfers between the CPU and the DUART take place over this bus. The bus is three-stated when the CSN input is high, except during an IACKN cycle.
A1-A4	I	**Address Inputs.** These inputs select the DUART register or port for the current read/write operation.
CSN	I	**Chip Select.** Active low. The data bus is three-stated when CSN is high. Transfers between the CPU and the DUART via D0-D7 are enabled when CSN is low.
R/WN	I	**Read/Write.** A high input while CSN is low indicates a read cycle while a low input while CSN is also low indicates a write cycle.
DTACKN	O	**Data Transfer Acknowledge.** Three-state, active low. Assertion of DTACKN indicates that data is present on the bus during a read or interrupt acknowledge cycle and that the data from the bus has been written into the addressed destination during a write cycle.
RESETN	I	**Master Reset.** A low on this pin clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to 0FH, stops the counter/timer, puts OP0-OP7 in the high state, and places both serial channels in the inactive state with the TXDA and TXDB outputs marking (high).

Mnemonic	Type	Description
INTRN	O	**Interrupt Request.** Active low, open drain. INTRN is asserted upon the occurrence of one or more of the chip's maskable interrupting conditions.
IACKN	I	**Interrupt Acknowledge.** Active low. Assertion of IACKN indicates that the current bus cycle is an interrupt acknowledge cycle. If the DUART has an interrupt active, it responds by placing the interrupt vector on the data bus and asserting DTACKN.
X1/CLK	I	**Crystal or External Clock Input.** This pin is the connection for one side of the crystal and a capacitor to ground when the internal oscillator is used (see figure 12). If the oscillator is not used an external clock signal must be supplied at this input.
X2	I	**Crystal Input.** Connection for other side of the crystal. If the oscillator is used a capacitor must also be connected from this pin to ground. This pin may be connected to ground or left open if an external clock is supplied at X1/CLK.
RXDA, RXDB	I	**Receiver Serial Data Inputs.** The least significant bit is received first. If external receiver clock is specified, the data is sampled on the rising edge of the clock.
TXDA, TXDB	O	**Transmitter Serial Data Outputs.** The least significant bit is transmitted first. Held in the marking (high) state when the transmitter is idle or disabled or when the channel operates in local loopback mode. If external transmitter clock is specified, the data is shifted out on the falling edge of the clock.
OP0	O	**Output 0.** Can be programmed as a general purpose output or as the channel A request-to-send output (RTSAN). Active low.
OP1	O	**Output 1.** Can be programmed as a general purpose output or as the channel B request-to-send output (RTSBN). Active low.
OP2	O	**Output 2.** Can be programmed as a general purpose output, the channel A transmitter 1x or 16x clock output, or the channel A receiver 1x clock output. Active low.
OP3	O	**Output 3.** Can be programmed as a general purpose output, the channel B transmitter 1x clock output, the channel B receiver 1x clock output, or an open drain counter/timer ready output. Active low.
OP4	O	**Output 4.** Can be programmed as a general purpose output or as an open drain channel A RXRDY/FFULL output. Active low.
OP5	O	**Output 5.** Can be programmed as a general purpose output or as an open drain channel B RXRDY/FFULL output. Active low.
OP6	O	**Output 6.** Can be programmed as a general purpose output or as an open drain channel A TXRDY output. Active low.
OP7	O	**Output 7.** Can be programmed as a general purpose output or as an open drain channel B TXRDY output. Active low.
IP0	I	**Input 0.** General purpose input or CTSAN, the channel A active low clear-to-send input.
IP1	I	**Input 1.** General purpose input or CTSBN, the channel B active low clear-to-send input.
IP2	I	**Input 2.** General purpose input, counter/timer external clock input, or channel B receiver external clock input.
IP3	I	**Input 3.** General purpose input or channel A transmitter external clock input.
IP4	I	**Input 4.** General purpose input or channel A receiver external clock input.
IP5	I	**Input 5.** General purpose input or channel B transmitter external clock input.
V_{CC}	I	**+5 Volt Power Input.**
GND	I	**Signal and Power Ground.**

PRINCIPLES OF OPERATION

As illustrated in the block diagram, the DUART consists of the following major blocks:

Data Bus Buffer
Operation Control
Interrupt Control
Timing Circuits
Input Port
Output Port
Serial Channels A and B

Data Bus Buffer

The data bus buffer provides the interface between the internal and external data busses. It is controlled by the operation control block to allow data transfers to take place between the host CPU and the DUART.

Operation Control

The operation control logic receives operating commands from the CPU and generates signals to various sections of the DUART to appropriately control the device's operation. It contains address decoding and read and write circuits to permit communications with the microprocessor and registers to store configuration commands and device status.

The XR-68C681 version includes a data transfer acknowledge (DTACKN) output which is asserted during data transfer cycles to verify that the requested operation has been completed. It indicates that the input data has been latched during a write cycle, that the requested data is on the data bus during a read cycle, or that the interrupt vector is on the data bus during an interrupt acknowledge cycle.

The addressing of the internal elements of the DUART is described in Table 1. Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to point to MR1x by a hardware reset or by invoking a 'reset pointer' command to the appropriate channel via its command register. Any read or write operation to the mode register while the pointer is pointing at MR1x switches the pointer to point to MR2x. The pointer then remains pointing to MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset as described above.

Interrupt Control

An interrupt request output signal (INTRN) is provided which may be programmed to be asserted upon the occurrence of any of the following events:

Transmit holding register A or B empty
Receive holding register A or B ready
Receive FIFO A or B full
Start or end of received break, channel A or B
Counter terminal count reached
Change of state on input pins IP0, IP1, IP2 or IP3

Associated with the interrupt system are the interrupt status register (ISR), the interrupt mask register (IMR), and the interrupt vector register (IVR). The ISR indicates the current state of all the potential interrupting conditions

Table 1. DUART Port and Register Addressing

A3	A2	A1	A0	Read	Write
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	Interrupt Status Register, Masked (ISR)	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Auxiliary Control Register (ACR)
0	1	0	1	Interrupt Status Register, Unmasked (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper Byte (CTU)	Counter/Timer Upper Register (CTUR)
0	1	1	1	Counter/Timer Lower Byte (CTL)	Counter/Timer Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	RESERVED	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	Interrupt Vector Register (IVR)	Interrupt Vector Register (IVR)
1	1	0	1	Input Port	Output Port Configuration Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

Note: In XR68C681 version, replace A3-A0 above with A4-A1 respectively.

listed above. The IMR may be programmed to select only certain of these conditions to assert the INTRN output. The ISR can be read by the CPU either masked or unmasked by the IMR. If read masked by the IMR, only the state of the conditions which have been programmed to cause an interrup is output. If read unmasked, the state of all conditions, whether programmed to cause an interrupt or not, is output.

The XR-88C681/40 version may be programmed to operate in two modes to accommodate different CPU interface requirements. In the 'I-mode', which is the default mode after a hardware reset, interrupt prioritization and interrupt vector generation, if required, are implemented using external hardware. In this mode, the on-chip interrupt vector register is not utilized and is available for use as an auxiliary read/write register for any purpose.

In the 'Z' mode, which is invoked via a command to command register B, pins 37, 38 and 39 are designated as interrupt acknowledge input (IACKN), interrupt enable output (IEO) and interrupt enable input (IEI) respectively. IEI and IEO are the input and output of an interrupt daisy chain, as illustrated in Figure 1. IEi high means that the DUART may generate an interrupt request. A device with IEI high which is requesting an interrupt sets its IEO low to inhibit lower priority devices from generating their own interrupt requests. A device with its IEI low is inhibited from generating an interrupt and must also keep its IEO output low.

Sometime after the interrupt request is issued, the CPU will respond with an interrupt acknowledge cycle, asserting the IACKN and RDN inputs as shown in Figure 1. Assertion of IACKN must precede assertion of RDN. The time between the assertion of IACKN and the assertion of RDN allows the daisy chain to stabilize. The DUART is inhibited from issuing a new interrupt request while IACKN is asserted.

If the DUART is requesting an interrupt and its IEI is high when the leading edge of RDN is received, it is the highest priority device making the request. It sets its internal 'interrup under service' (IUS) latch, which keeps its IEO negated regardless of what happens to the interrupt request (which may be negated, for example, by the read of the RHR). It also places the vector from the IVR on the data bus. Keeping IEO low prevents lower priority devices in the daisy chain from requesting an interrupt until the higher priority interrupt has been serviced. Upon completing the service routine, the CPU must issue a 'reset IUS latch' command to the chip, which resets the latch and returns the daisy chain to its normal condition.

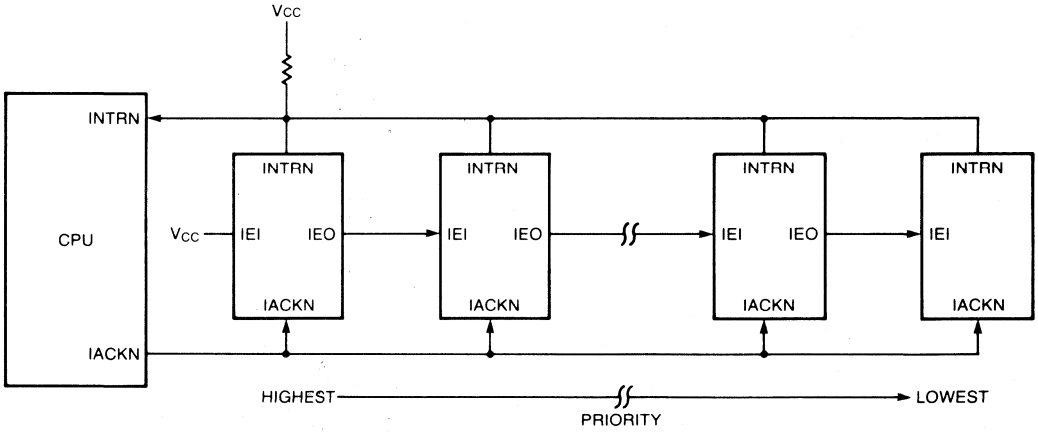


Figure 1A. Daisy Chained Interrupt Block Diagram

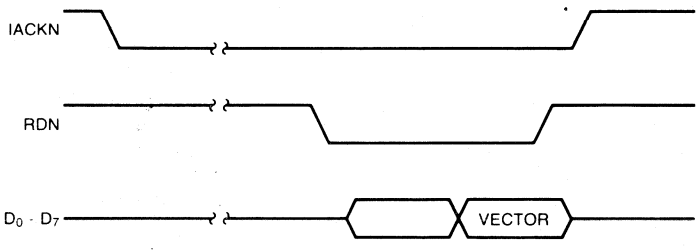


Figure 1B. Daisy Chained Interrupt Timing

In the XR-68C681 version, if the DUART has its interrupt request active, it responds to assertion of its IACKN input by placing the vector from the IVR on the data bus and asserting DTACKN. Otherwise, it ignores IACKN.

In either version, outputs OP3-OP7 can be programmed to provide separate open drain interrupt requests for transmitters A and B, receivers A and B, and the counter/timer. See pin description.

Timing Circuits

The timing block contains a crystal oscillator, a bit rate generator (BRG), a programmable 16-bit counter/timer (C/T), and four clock selectors. A detailed block diagram of this section is shown in Figure 2.

Crystal Oscillator

The crystal oscillator operates from a crystal connected between the X1/CLK and X2 pins. A crystal frequency of 3.6864 MHz is required for generation of standard bit rates by the bit rate generator (see Table 5). If an external clock is available, it may be connected to X1/CLK, with X2 left open or connected to ground. The output of the oscillator is used by the BRG, the C/T and other internal circuits. This requires that a clock within the specified limits always be supplied to the DUART.

Bit Rate Generator

The BRG uses the crystal oscillator or external clock as an input and generates the clock for 23 commonly used data communications bit rates ranging from 50 to 115.2K bits per second. The actual clock frequencies output from the BRG are at 16 times these rates. The counter/timer can also be used as a programmable bit rate generator to produce a 16x clock for any bit rate not provided by the BRG. The four clock select multiplexers allow each receiver and transmitter to independently select its operating frequency as one of the outputs from the BRG, the output of the counter/timer, or an external clock. Table 4 defines the input pins for external clocking for the three version of the DUART.

Counter/Timer

The C/T is a programmable 16-bit down-counter which can use one of several timing sources as its input. The C/T output is available to the clock selectors for use as a programmable bit rate for any receiver or transmitter, can be programmed to generate an interrupt each time it reaches its terminal count of 0000H, and can also be programmed as an output at OP3.

In the **timer** mode, the C/T acts as a programmable divider and generates a square wave whose period is twice the value (in clock periods) of the contents of the counter/timer registers CTUR and CTLR. The contents of these registers may be changed at any time, but will only begin to take effect at the next half cycle of the square wave. The C/T begins operation using the values in CTUR/CTLR upon receipt of a 'startcounter' command (see Table 1). The C/T then runs continuously. A subsequent 'start counter' command causes the C/T to terminate the current timing cycle and to begin a new timing cycle using the current values

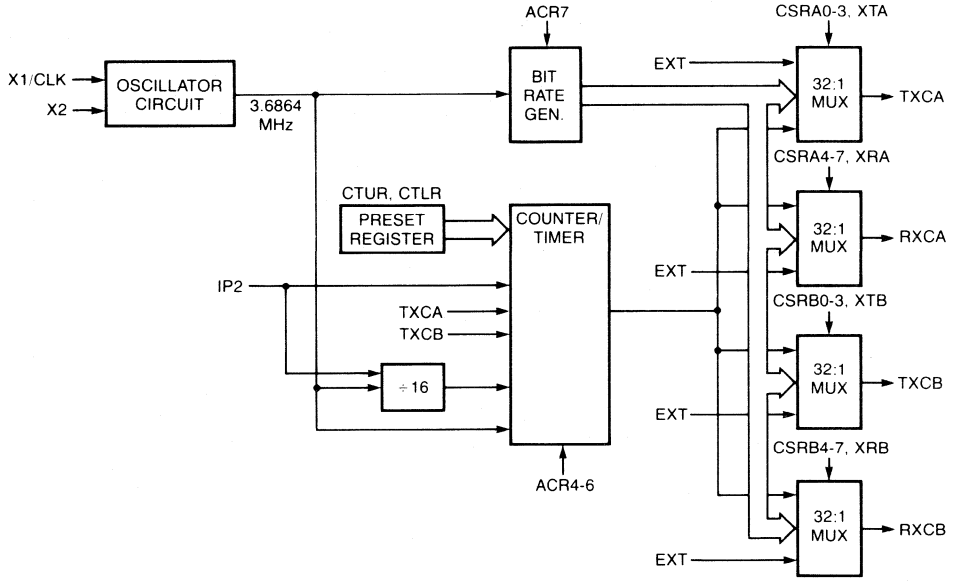


Figure 2. Timing Circuits Block Diagram

in CTUR and CTLR. The counter ready status bit (ISR[3]) is set once each cycle of the square wave. This allows use of the C/T as a periodic interrupt generator if the condition is programmed to generate an interrupt via the interrupt mask register. The status bit can be reset by issuing a 'stop counter' command (see Table 1). In this mode, however, the command does not actually stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the **counter** mode, the C/T counts down the number of pulses written into CTUR/CTLR, beginning at the receipt of a 'start counter' command. The counter ready status bit (ISR[3]) is set upon reaching the count of 0000H. The C/T will continue to count past this (with the next count being FFFFH) until it is stopped by the CPU via a 'stop counter' command. If OP3 is programmed to be the output of the C/T, the output remains high until the terminal count is reached, at which time the output goes low. OP3 returns to the high state and ISR[3] is cleared when the counter is stopped. A 'start counter' command while the counter is running restarts the counter with the values in CTUR/CTLR. The CPU may change CTUR or CTLR at any time but the new count takes effect only on the next start counter command. If new values are not programmed, the previous values are preserved and used for the next cycle.

In counter mode, the current value in the C/T may be read by the CPU by ready the upper and lower halves of the C/T separately (see Table 1). Stopping the counter when it is read is recommended in order to prevent potential problems which may occur if a carry from the lower half to the upper half occurs between the times that the two halves are read. However, note that a new start counter command will cause the counter to begin counting using the values in CTUR/CTLR.

Input Port

The current state of the inputs to this unlatched port can be read by the CPU by performing a read as described in Table 1. A high input results in a logic "1" while a low input results in a logic "0". The pin description tables describe the alternate uses for the input pins, such as clock inputs and interrupt control signals. A read of the input port will show the state at the pin, regardless of its programmed function. When the port is read, bit 7 will always read as a logic "1" in both versions of the DUART, and D6 will reflect the state of IACKN in the XR-68C681 version.

Change of state detectors are provided for inputs IP0-IP3. These inputs are sampled by the 38.4 kHz output of the BRG (2.4 Kbps x 16). A high-to-low or low-to-high transition at these inputs lasting at least two clock periods (approximately 50 μs) will guarantee that the corresponding bit in the input port change register (IPCR) will be set, although it may be set by a change of state as short as 25 μs. The status bits in the IPCR are cleared when the register is read by the CPU. Any change of state can also be programmed to generate an interrupt.

Output Port

The 8-bit output port can be used as a general purpose output port or can be used to output timing and status signals by appropriate programming of the mode registers (MR1A, MR2A, MR1B, MR2B) and with output port configuration register. When used to output status signals the pins ae open drain, which allows their use in a wire-OR interrupt scheme.

When used as a general purpose output port, the outputs are the complements of the output port register (OPR). $OPR_{(n)}$ = 1 results in $OP_{(n)}$ low while $OPR_{(n)}$ = 0 results in $OP_{(n)}$ high. Bits of OPR can be set and reset individually. A bit is set by the address-triggered 'set output port bits' command (see Table 1) with the accompanying data specifying the bits to be set (1 = set, 0 = no change). A bit is reset by the address-triggered 'reset output port bits' command (see Table 1) with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Serial Channels A and B

Each serial channel of the DUART comprises a full duplex asynchronous receiver and transmitter. The two channels can independently select their operating frequency (from the BRG, the C/T, or an external clock) as well as operating mode. Besides the normal mode in which the receiver and transmitter of each channel operate independently, the DUART can be configured to operate in various looping modes, which are useful for local and remote diagnostics, as well as in a wake-up mode used for multi-drop applications.

Note: In the descriptions which follow, the transmitter and receiver are described for either channel. References to input and output pins and control and status bits and registers apply to either channel unless otherwise noted.

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream at the TXD pin, adding start, stop and optional parity bits as required by the asynchronous protocol.

The DUART is conditioned to transmit data when the transmitter is enabled via the command register. It indicates that it is ready to accept a character from the CPU for serialization by setting the TXRDY bit in the status register. This condition can be programmed to assert an interrupt request via the INTRN output and can also be programmed to assert the OP6 output (channel A) or the OP7 output (channel B). These conditions are negated when the CPU loads a character into the transmit holding register (THR). Data is transferred from the THR to the transmit shift register (TSR) immediately if the TSR is idle or when it completes serialization of the previous

character. The TXRDY condition is then asserted again. Thus, one full character time of buffering is provided. Note that the THR will not accept characters while the transmitter is disabled.

The transmitter sends a start bit followed by the programmed number of data bits (least significant bit first), an optional parity bit, and the programmed number of stop bits and then begins transmission of the next character if one has been loaded into the THR. Otherwise, the TXD output will remain high and the TXEMT status bit will be set following the transmission of the stop bits. Transmission resumes and the TXEMTstatus bit is cleared when the CPU loads a new character into the THR. The transmitter can be forced to send a continuous low at TXD by invoking a 'send break' command.

If the transmitter is disabled, it continues operating until the character currently being serialized, and any in the THR, are completely sent out. The transmitter can be reset by a software command. In this case, operation ceases immediately and the transmitter must be re-enabled before resuming operation.

Setting MR2[4] of the appropriate channel programs its transmitter to begin transmission of a character only if the channel's clear-to-send input pin (IP0 for channel A, IP1 for channel B) is low. If CTSN goes high in the middle of a transmission, the transmission of the current character is completed but TXD remains high and the next character will not be sent until CTSN is low again. Setting MR2[5] of the appropriate channel programs the transmitter to automatically deactivate its request-to-send output pin (OP0 for channel A, OP1 for channel B). If so programmed, and the transmitter has been disabled, the RTSN output will be negated one bit time after the characters in the TSR and THR (if any) are completely sent.

Receiver

The receiver accepts serial data at its RXD pin, checks for a proper start bit, converts the serial input to parallel form, checks the parity bit (if parity is specified), checks for presence of a stop bit, performs several other tests on the received data, and sends the assembled character to the CPU.

Each receiver is conditioned to receive data when it is enabled via the command register. It looks for a high to low (mark to space) transition indicating a start bit at the RXD input. If a transition is detected, the state of RXD is sampled each 16x clock for 7½ clocks (16x clock mode) or at the next rising edge of the bit time clock (x clock mode). If RXD is detected high at these sample times, the start bit is invalid and the search for a start bit begins again. If RXD remains low, a valid start bit is assumed and the receiver continues to sample the data at one bit time intervals, at the theoretical center of the bit, until the programmed number of data bits (LSB first), the parity bit (if any), and one stop bit have been assembled. The data is then transferred to the receive holding register (RHR) with the most significant unused bits set to zero. The status conditions (parity error, framing error, overrun error, and break received) are set to indicate to the CPU that a character is available to be read. Setting of RXRDY can be programmed to generate an interrupt request via INTRN and to assert OP4 (channel A) or OP5 (channel B).

After the stop bit position is sampled, the receiver will immediately begin to look for the start bit of the next character. However, if a non-zero character was received without a stop bit (framing error) and RXD remains low for half a bit time after sampling of the stop bit, the receiver operates as if a new start bit transition had been detected at that point (half a bit time after the sampling of the stop bit).

If a break is received (an all zeroes character including the first stop bit), only a single character consisting of all zeroes will be loaded into the FIFO and the break received status bit will be set, no matter how long the break condition persists. RXD must return to a high condition for at least half a bit time before the search for a new start bit begins again.

The RHR consists of a first-in-first-out (FIFO) stack with a capacity of three characters. Data is transferred from the receive shift register into the topmost empty position in the FIFO. RXRDY is set whenever one or more characters are in the FIFO, and the FFULL status bit is set if the FIFO is filled with data. Either of these bits can be selected to assert an interrupt. A read of the RHR outputs the data at the top of the FIFO and any remaining characters are pushed up, thus freeing a FIFO position for new data.

In addition to the data word, three status bits are appended to each character position in the FIFO. These are parity error, framing error, and received break. Status can be provided in two ways, as programmed by MR1[5] in the channel's mode register. In the 'character' mode status is provided on a character by character basis: the status applies only to the character at the top of the FIFO. In the block mode, these three bits in the status register are the cumulative logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode, reading the status register does not affect the FIFO. The FIFO is popped only when the RHR is read. Therefore, the status register should be read prior to reading the RHR. Also note that PE, FE and received break status bits are valid only when RXRDY in the status register is asserted.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If a new start bit is detected while this condition exists, the character previously in the shift register is lost and the overrun error status bit is set. The contents of the FIFO are not affected when this occurs.

If the receiver is disabled, the contents of the FIFO are maintained and can be read by the CPU. Resetting the receiver initializes the FIFO pointers and clears the status bits

immediately. In either case, any character currently being assembled is lost and operation does not resume until the receiver is re-enabled.

Setting MR[7] of the appropriate channel programs the receiver to automatically control de-activation of the request-to-send output (OP0 for channel A, OP1 for channel B). If so programmed, RTSN will be negated when a valid start bit is received while the FIFO is full, and will automatically be re-asserted when a FIFO position becomes available for that character. This feature can be used to prevent an overrun in the receiver by connecting the RTSN output to the CTSN input of the transmitting device.

Multidrop (8051 9-bit) Mode

Each serial channel of the DUART can be configured to operate in a wake-up mode useful for multidrop or multiprocessor applications. This mode is compatible with the serial 'Nine-bit Mode' of 8051-family microcomputers. In this mode of operation a master station, connected to a maximum of 256 slave stations, transmits an address character followed by a block of data characters targeted for the addressed slave station. The slave stations normally have their receivers disabled. However, in this mode, the slave receivers monitor the incoming data stream and wake up the CPU (by asserting RXRDY) when any address character is detected. The slave station CPU then compares the received address to its own assigned address and enables the receiver, if it wishes, to receive the subsequent block of data, or leaves the receiver disabled if it does not. Upon completion of reception of the block of data, the receiver is disabled to re-initiate the process.

The multidrop mode is selected by programming MR[4:3] of the channel to '11'. In this mode, a transmitted character consists of a start bit, the programmed number of data bits, an addresss/data flag bit (A/D), and the programmed number of stop bits. A/D = 0 indicates that the character is data, while A/D = 1 identifies it as an address. The CPU controls the state of A/D in the transmitted character by programming MR1[2] of the channel prior to loading the data bits into the THR. MR1[2] = 0 results in A/D = 0 and MR1[2] = 1 results in A/D = 1.

In the multidrop mode, the receiver continously looks at RXD whether enabled or not. When disabled, it loads a character into the RHR and sets RXRDY if its A/D bit is one (address flag) but discards the character if its A/D bit is zero (data flag). If the receiver is enabled, all characters received are transferred to the RHR. In either case, the received data bits are loaded into the RHR while the A/D bit is loaded into SR[5], the status register position normally used for parity error. Framing error, overrun error, and break detect status bits operate normally.

Standby Mode

The DUART may be placed in a standby mode to conserve power when its operation is not required. Upon reset the DUART will be in the 'active operation' mode. A 'set standby mode' command issued via the channel A command register disables all clocks on the device except for the crystal oscillator, which significantly reduces the operating current. In this mode the only functions which will operate correctly are reading the input port, writing the output port and the 'set active mode' command. The latter, also invoked via the channel A command register, restores the device to normal operation within 25μs. Resetting the transmitters and receivers and writing 00H into the interrupt mask register before going into the standby mode is recommended to prevent any spurious interrupts from being generated. The chip should be reprogrammed after the 'set active mode' command since register contents are not guaranteed to remain stable during the standby mode. Active operation can also be restored via hardware reset.

PROGRAMMING

Operation of the DUART is programmed by writing control words into the appropriate registers, while operational feedback is provided by status registers which can be read by the CPU. Register addressing is shown in Table 1.

A hardware reset clears the contents of SRA, SRB, IMR, ISR, OPR and OPCR and initializes the IVR to 0FH. During operation, care should be exercised if the contents of control registers are to be changed, since certain changes may result in improper operation. For example, changing the number of bits per character while data is being received may result in reception of an erroneous character. In general, changes to registers which control receiver or transmitter operation should be made only while the transmitter or receiver are disabled, and certain changes to the ACR should be made only when the C/T is stopped.

Mode, command, clock select, and status registers are duplicated for each channel to provide totally independent operation. Table 2 illustrates the bit assignments for each register.

Note: In the descriptions which follow, registers which are duplicated for each channel are described generically. References to input and output pins and control and status bits and registers apply to each channel unless otherwise noted.

MR1A, MR1B - Channel A/B Mode Register 1

MR1 for each channel is accessed when the channel's MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command invoked via the channel's command register. After reading or writing MR1, the pointer will point to MR2.

MR1[7] - Receiver Request-to-Send Control

This bit controls the negation of the RTSN output (OP0 for channel A, OP1 for channel B) by the receiver. RTSN is normally asserted by setting OP0 or OP1 for channels A and B respectively, and negated by resetting the same bit. MR1[7] = 1 causes RTSN to be negated automatically

Table 2. Register Bit Formats

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	Rx RTS Control	Rx Int Select	Error Mode	Parity Mode		Parity Type	Bits Per Char.	
MR1A MR1B	0 = no 1 = yes	0 = RXRDY 1 = FFULL	0 = char 1 = block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multi-drop Mode		0 = even 1 = odd	00 = 5 01 = 6 10 = 7 11 = 8	

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	Channel Mode		Tx RTS Control	CTS Enable Tx	Stop Bit Length*			
MR2A MR2B	00 = Normal 01 = Auto Echo 10 = Local Loop 11 = Remote Loop		0 = no 1 = yes	0 = no 1 = yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

*Add 0.5 to values shown for 0-7 if channel is programmed for 5 bits/character.

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CSRA	Receiver Clock Select				Transmitter Clock Select			
CSRB	See Table 3				See Table 3			

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	Miscellaneous Commands				Disable Tx	Enable Tx	Disable Rx	Enable Rx
CRA CRB	See Text				0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	Received Break	Framing Error	Parity Error	Overrun Error	TXEMT	TXRDY	FFULL	RXRDY
SRA SRB	0 = no 1 = yes *	0 = no 1 = yes *	0 = no 1 = yes *	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

*These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits (7:5) from the top of the FIFO together with bits 4:0. These bits are cleared by a 'reset error status' command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	OP7	OP6	OP5	OP4	OP3		OP2	
OPCR	0 = OPR[7] 1 = TXRDYB	0 = OPR[6] 1 = TXRDYA	0 = OPR[5] 1 = RXRDY/ FFULLB	0 = OPR[4] 1 = RXRDY/ FFULLA	00 = OPR[3] 01 = C/T Output 10 = TxCB (1X) 11 = RxCB (1X)		00 = OPR[2] 01 = TXCA (16X) 10 = TXCA (1X) 11 = RXCA (1X)	

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	BRG Set Select	Counter/Timer Mode and Source			Delta IP3 Int	Delta IP2 Int	Delta IP1 Int	Delta IP0 Int
ACR	0 = Set1 1 = Set2	See Table 6			0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

Table 2. Register Bit Formats (continued)

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IPCR	Delta IP3 0 = No 1 = Yes	Delta IP2 0 = No 1 = Yes	Delta IP1 0 = No 1 = Yes	Delta IP0 0 = No 1 = Yes	IP3 0 = Low 1 = High	IP2 0 = Low 1 = High	IP1 0 = Low 1 = High	IP0 0 = Low 1 = High

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ISR	Input Port Change 0 = No 1 = Yes	Delta Break B 0 = No 1 = Yes	RXRDY/ FFULLB 0 = No 1 = Yes	TXRDYB 0 = No 1 = Yes	Counter Ready 0 = No 1 = Yes	Delta Break A 0 = No 1 = Yes	RXRDY/ FFULLA 0 = No 1 = Yes	TXRDYA 0 = No 1 = Yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IMR	Input Port Change Int 0 = Off 1 = On	Delta Break B Int 0 = Off 1 = On	RXRDY/ FFULLB Int 0 = Off 1 = On	TXRDYB Int 0 = Off 1 = On	Counter Ready Int 0 = Off 1 = On	Delta Break A Int 0 = Off 1 = On	RXRDY/ FFULLA Int 0 = Off 1 = On	TXRDYA Int 0 = Off 1 = On

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTU CTUR	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTL CTLR	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IVR	IVR[7]	IVR[6]	IVR[5]	IVR[4]	IVR[3]	IVR[2]	IVR[1]	IVR[0]

upon receipt of a valid start bit if the channel's FIFO is full and to be re-asserted again when an empty FIFO position becomes available. This flow control feature can be used to prevent overrun of the receiver by using the RTSN output to control transmission of characters to the DUART.

MR1[6] - Receiver Interrupt Select

This bit selects either the RXRDY status bit or the FFULL status bit of the channel to be used for CPU interrupts. It also causes the selected bit to be output on OP4 (channel A) or OP5 (channel B) if the pin is programmed as an interrupt output via the OPCR.

MR1[5] - Error Mode Select

This bit controls the operation of the three FIFOed status bits (PE, FE, received break) for the channel. In the character mode these status bits apply only to the character currently at the top of the FIFO. In the block mode these bits are the cumulative logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command for the channel was issued.

MR1[4:3] - Parity Mode Select

If 'with parity' or 'force parity' operation is programmed a parity bit is added to the transmitted characters and the receiver performs a parity check on received characters. See OPERATION section for description of multidrop mode operation.

MR1[2] - Parity Type Select

This bit selects odd or even parity if 'with parity' mode is programmed and the state of the forced parity bit if the 'force parity' mode is programmed. In the multidrop mode it selects the state of the A/D flag bit. This bit has no effect if 'no parity' mode is programmed.

MR1[1:0] - Bits per Character Select

Selects the number of bits to be transmitted and received in the data field of the character. This does not include start, parity and stop bits.

MR2A, MR2B - Channel A/B Mode Register 2

MR2 for each channel is accessed when the channel's MR pointer points to MR2, which occurs after any access to the channel's MR1. Reading or writing MR2 does not change the pointer.

MR2[7:6] - Channel Mode Select

Each channel can operate in one of four modes. MR2[7:6] = 00 in the normal mode where the receiver and transmitter operate independently.

MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions apply while in this mode:

1. Received data is transmitted on the channel's TXD output.
2. The receiver must be enabled but the transmitter need not be enabled.
3. The channel's TXRDY and TXEMT status bits are inactive.
4. The received parity is checked but is not regenerated for transmission. Thus, transmitted parity is as received.
5. Character framing is checked but the stop bits are retransmitted as received.
6. A received break is echoed as received until the next valid start bit is detected.
7. CPU to receiver communications operate normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. The first is the local loopback mode, selected by MR2[7:6] = 10. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The channel's TXD output is held marking (high).
4. The channel's RXD input is ignored.
5. The transmitter is enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is transmitted on the channel's TXD output.
2. Received data is not sent to the CPU and the error status conditions are not checked.
3. Parity and framing (stop bits) are transmitted as received.
4. The receiver must be enabled.
5. A received break is echoed as received until the next valid start bit is detected.

Care must be taken when switching into and out of the various modes. The selected mode will be activated immediately after it is programmed even if this occurs in the middle of transmitting or receiving a character. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RXRDY), and the transmitter is enabled, the transmitter will remain in autoecho or remote loopback mode until one entire stop bit has been transmitted.

MR2[5] - Transmitter Request-to-Send Control

This bit controls the negation of the RTSN output (OP0 for channel A, OP1 for channel B) by the transmitter RTSN is normally asserted by setting OP0 or OP1 for channels A and B respectively, and negated by resetting the same bit. MR2[5] = 1 causes OP0 (channel A) or OP1 (channel B) to be reset automatically one bit time after the characters in the channel's transmit shift register and THR, if any, are completely transmitted, including the programmed number of stop bit, if the transmitter has been disabled. This feature can be used to automatically negate RTSN at the conclusion of a message as follows:

1. Program auto-reset mode (MR2[5] = 1).
2. Enable transmitter and assert the channel's RTSN output by setting the appropriate bit in the output port register.
3. Send message.
4. Disable the transmitter after the last character of the message is loaded into the THR.

MR2[4] - Clear-to-Send Control

If this bit is a 0, the channel's CTSN input (IP0 for channel A, IP1 for channel B) has no effect on the transmitter. If the bit is a 1, the transmitter checks the state of its CTSN each time it is ready to send a character. If CTSN is low, the character is transmitted. If CTSN is high, TXD remains

in the marking state and the transmission of the next character is delayed until CTSN goes low. Changes in CTSN while a character is being serialized do not affect transmission of that character.

MR2[3:0] - Stop Bit Length

This field programs the duration of the stop bit appended to each transmitted character. Stop bit durations of 9/16 to 1 bit time a 1-9/16 to 2 bit times, in increments of 1/16 bit, can be programmed for character lengths of 6, 7 and 8 bits. For a 5-bit character, the stop bit duration can be programmed from 1-1/16 to 2 bit times.

If an external 1x clock is programmed for the transmitter, MR2[3] = 0 selects a stop bit duration of one bit time and MR2[3] = 1 selects a duration of two bit times for transmission.

The receiver only checks for a mark condition at the center of the first stop bit (that is, one bit time after the last data or parity bit is sampled) regardless of the programmed transmitted stop bit length.

CSRA, CSRB - Channel A/B Clock Select Register

CSR[7:4] and CSR[3:0] of each channel operate in conjunction with ACR[7] and the channel's 'set/clear BRG select extend' commands to allow independent selection of the bit rates for the receiver and transmitter respectively. The BRG can generate 23 different bit rates, of which 22 are available simultaneously. The set of 22 is selected by programming ACR[7]. The bit rates generated when using a 3.6864 MHz crystal or an external clock of the same frequency are shown in Table 3, where 'X' refers to the current state of the extend bit. Note that the actual outputs from the BRG are at 16x the bit rates shown in the table. See Table 4 for the source of EXT (external clock) for the three DUART versions.

CRA, CRB - Channel A/B Command Register

Each channel of the DUART has a command register used to supply commands to the respective channel. Multiple commands may be invoked simultaneously be a single write to the command register as long as the commands are non-conflicting.

CR[7:4] - Miscellaneous Commands

The encoded value of this field specifies a single command as follows:

0 0 0 0 - Null Command.

0 0 0 1 - Reset MR Pointer - causes the channel's MR pointer to point to MR1.

Table 3. CSR[3:0] Bit Rate Selection

Field				Bit Rate			
CSR[7:4]				ACR[7] = 0		ACR[7] = 1	
CSR[3:0]				X = 0	X = 1	X = 0	X = 1
0	0	0	0	50	75	75	50
0	0	0	1	110	110	110	110
0	0	1	0	134.5	134.5	134.5	134.5
0	0	1	1	200	150	150	200
0	1	0	0	300	3600	300	3600
0	1	0	1	600	14.4K	600	14.4K
0	1	1	0	1200	28.8K	1200	28.8K
0	1	1	1	1050	57.6K	2000	57.6K
1	0	0	0	2400	115.2K	2400	115.2K
1	0	0	1	4800	4800	4800	4800
1	0	1	0	7200	1800	1800	7200
1	0	1	1	9600	9600	9600	9600
1	1	0	0	38.4K	19.2K	19.2K	38.4K
1	1	0	1	Timer	Timer	Timer	Timer
1	1	1	0	EXT - 16x	EXT - 16x	EXT - 16x	EXT - 16x
1	1	1	1	EXT - 1x	EXT - 1x	EXT - 1x	EXT - 1x

Table 4. External Clock Source Input Pin

Function	XR88C681/28	XR88C681/40 **I-mode**	XR88C681/40 **Z-mode**	XR68C681
Transmitter A	IP2	IP3	IP3	IP3
Transmitter B	IP2	IP5	IP2	IP5
Receiver A	IP2	IP4	IP3	IP4
Receiver B	IP2	IP6	IP2	IP2
Counter/Timer	IP2	IP2	IP2	IP2

0 0 1 0 - Reset Receiver - resets the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.

0 0 1 1 - Reset Transmitter - resets the transmitter as if a hardware reset had been applied. The TXD output is forced to a high level.

0 1 0 0 - Reset Error Status - clears the received break, parity error, framing error and overrun error status bits, SR[7:3]. Used in character mode to clear the OE status bit (although the RB, PE, and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.

0 1 0 1 - Reset Break Change Interrupt - clears the channel's break change interrupt status bit.

0 1 1 0 - Start Break - forces the TXD output low. The transmitter must be enabled to start a break. If the transmitter is empty, the start of the break may be delayed up to two bit times. If the transmitter is active, the break begins when the transmission of that character in the THR is completed, viz., TXEMT must be true before the break will begin.

0 1 1 1 - Stop Break - the TXD line will go high within two bit times. TXD will remain high for one bit time before the next character, if any, is transmitted.

1 0 0 0 - Set Rx BRG Select Extend Bit - sets the receiver BRG select extend bit for the channel to 1.

1 0 0 1 - Clear Rx BRG Select Extend Bit - clears the receiver BRG select extend bit for the channel to 0.

1 0 1 0 - Set Tx BRG Select Extend Bit - sets the transmitter BRG select extend bit for the channel to 1.

1 0 1 1 - Clear Tx BRG Select Extend Bit - clears the transmitter BRG select extend bit for the channel to 0.

1 1 0 0 - Set Standby Mode (A)/Reset IUS Latch (B)

When this command is invoked via the channel A command register, power is removed from the transmitters, receivers, counter/timer and additional circuits to place the DUART in the standby mode. Normal operation is restored by a hardware reset or by invoking the 'set active mode' command.

When this command is invoked via the channel B command register, and the DUART (XR-88C681 version) is operating in Z-mode, it causes the interrupt-under-service latch to be reset.

1 1 0 1 - Set Active Mode (A)/Set Z-mode (B).

When this command is invoked via the channel A command register the DUART is removed from the standby mode and resumes normal operation.

When this command is invoked via the channel B command register, the DUART is conditioned to operate in the Z-mode. This applies only to the XR-88C681 version.

1 1 1 0 - Reserved - do not invoke during operation.

1 1 1 1 - Reserved - do not invoke during operation.

CR[3] - Disable Transmitter

This command terminates operation of the channel's transmitter and resets the TXRDY and TXEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before going into the inactive state.

CR[2] - Enable Transmitter

This command enables operation of the channel's transmitter and asserts the TXRDY status bit.

CR[1] - Disable Receiver

This command immediately terminates operation of the channel's receiver. Any character being received will be lost. The command has no effect on the receiver status bits or on any other control registers. If the multi-drop mode is programmed, the receiver operates even it it is disabled. See OPERATION section.

CR[0] - Enable Receiver.

This command enables operation of the receiver. If not in the multidrop mode, it also forces the receiver to start searching for the start bit.

SRA, SRB - Channel A/B Status Register

SR[7] - Received Break

This bit indicates that an all zero character of the programmed length was received without a stop bit. Only a single FIFO position is occupied when a break is received. Additional transfers into the FIFO are inhibited until theRXD line returns to the marking state for at least half a bit time. This is defined as two successive edges of the internal or external 1 x clock.

When this bit is set, the channel's change in break status bit in the ISR is set. The bit in the ISR is also set when the end of the break condition, as defined above, is detected.

The chip's break detect logic can detect breaks that begin in the middle of a character. However, the break must persist until the end of the next character time in order for it to be detected.

SR[6] - Framing Error

When set, this bit indicates that RXD was low when the stop bit of the character is the FIFO was sampled. The stop bit check is made in the middle of the first stop bit position (one bit time after sampling the last data bit or the parity bit at its midpoint) regardless of the stop bit length programmed.

SR[5] - Parity Error

This bit is set when the 'with parity' or 'force parity' modes are programmed if the corresponding character in the data FIFO was received with incorrect parity.

In the multidrop mode, this status bit indicates the state of received address/data (A/D) flag bit.

SR[4] - Overrun Error

If set, this bit indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its error status) is overwritten.

This bit is cleared by a 'reset error status' command.

Table 5. Bit Rate Generator Characteristics Crystal or Clock Input = 3.6864 MHz

Nominal Rate (bps)	Actual Clock (KHz)	Error (Percent)
50	0.8	0
75	1.2	0
110	1.759	- 0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	- 0.26
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
3600	57.6	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
14.4K	230.4	0
19.2K	307.2	0
28.8K	460.8	0
38.4K	614.4	0
57.6K	921.6	0
115.2K	1843.2	0

Table 6. ACR[6:4] Field Definition

ACR[6:4]			Mode	Clock Source
0	0	0	Counter	External - IP2 Input
0	0	1	Counter	TXCA - 1x Clock of Channel A Tx
0	1	0	Counter	TXCB - 1x Clock of Channel B Tx
0	1	1	Counter	X1/CLK Input Divided by 16
1	0	0	Timer	External - IP2 Input
1	0	1	Timer	External Divided by 16 - IP2 Input
1	1	0	Timer	X1/CLK Input
1	1	1	Timer	X1/CLK Input Divided by 16

SR[3] - Transmitter Empty (TXEMT)

This bit is set when the transmitter underruns. It is set after transmission of the last stop bit of a character if there is no character is the THR awaiting transmission. It is reset when the THR is loaded by the CPU and when the transmitter is disabled.

SR[2] - Transmitter Ready (TXRDY)

This bit, when set, indicates that the THR is empty and ready to accept a character. The bit is cleared when the THR is loaded by the CPU and is set when that character is transferred to the transmit shift register. TXRDY is set when the transmitter is initially enabled and is reset when the transmitter is disabled. Characters loaded into the THR while the transmitter is disabled will not be transmitted.

SR[1] - FIFO Full (FFULL)

This bit is set when a character is transferred from the receive shift register to the FIFO and the transfer causes it to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SR[0] - Receiver Ready (RXRDY)

This bit indicates that a character has been received and is waiting in the FIFO to be ready by the CPU. It is set when a character is transferred from the receive shift register to the FIFO and reset when the CPU reads the last character currently stored in the FIFO.

OPCR - Output Port Configuration Register

This register programs the output port to provide alternate functions. Note that when an output is programmed as an interrupt, it is not masked by the contents of the IMR.

OPCR[7] - OP7 Output Select

This bit programs the OP7 output to provide one of the following:

0 - The complement of OPR[7]

1 - The channel B transmitter interrupt output, TXRDYB, which is the complement of SRB[2]. In this mode, OP7 is an open drain output.

OPCR[6] - OP6 Output Select

This bit programs the OP6 output to provide one of the following:

0 - The complement of OPR[6].

1 - The channel A transmitter interrupt output, TXRDYA, which is the complement of SRA[2]. In this mode OP6 is an open drain output.

OPCR[5] - OP5 Output Select

This bit programs the OP5 output to provide one of the following:

0 - The complement of OPR[5]

1 - The channel B receiver interrupt output, which is the complement of ISR[5]. In this mode OP5 is an open drain output.

OPCR[4] - OP4 Output Select

This bit programs the OP4 output to provide one of the following:

0 - The complement of OPR[4].

1 - The channel A receiver interrupt output, which is the complement of ISR[1]. In this mode OP4 is an open drain output.

OPCR[3:2] - OP3 Output Select

These bits program the OP3 output to provide one of the following:

00 - The complement of OPR[3].

01 - The counter/timer output, in which case OP3 is an open drain output. In the timer mode the output is a square wave at the programmed frequency. In counter mode the output remains high until the terminal count is reached, at which time it goes low. The output returns to the high state when the counter is stopped by a stop counter command.

10 - The 1x clock which shifts the output data for the channel B transmitter. A free running 1x clock is output if data is not being transmitted.

11 - The 1x clock which samples the input data for the channel B receiver. A free running 1x clock is output if data is not being received.

OPCR[1:0] - OP2 Output Select

These bits program the OP2 output to provide one of the following:

00 - The complement of OPR[2].

01 - The 16x clock selected for the channel A transmitter by CSRA[3:0]. This will be a 1x clock if external 1x clock is programmed.

10 - The 1x clock which shifts the output data for the channel A transmitter. A free running 1x clock is output if data is not being transmitted.

11 - The 1x clock which samples the input data for the channel A receiver. A free running 1x clock is output if data is not being received.

ACR - Auxiliary Control Register

ACR[7] - Bit Rate Set Select

This bit selects one of two sets of bit rates to be generated by the BRG. The bit rates provided are selected by the channel A and B receiver and transmitter as described in the Clock Select Register description. Bit rate generator characteristics are shown in Table 5.

ACR[6:4] - Counter/Timer Mode and Clock Source Select

This field selects the operating mode and clock source for the counter/timer. See Table 6.

ACR[3:0] - Change of State Interrupt Enables

These bits select which bits of the input port cause the input port change bit in the interrupt status register (ISR[7]) to be set. If one of these bits is 'on', the setting of the corresponding bit in the IPCR by a change of state on the input will set ISR[7], and will also cause the interrupt request pin to be asserted if IMR[7] is set. However, if the bit is 'off', the setting of the corresponding bit in the IPCR has no effect on ISR[7].

IPCR - Input Port Change Register

IPCR[7:4] - IP3, IP2, IP1, IP0 Change of State

These bits are set when a change of state occurs at the respective input pins (see Input Port section). The bits are cleared when the CPU reads the IPCR.

The setting of these bits can be programmed to cause an interrupt to the CPU via ACR[3:0], ISR[7] and IMR[7].

IPCR[3:0] - IP3, IP2, IP1, IP0 Current State

These bits indicate the current state of the respective inputs at the time the IPCR is read.

ISR - Interrupt Status Register

This register provides the current status of all possible interrupt conditons. If a bit in the ISR is a '1' and the corresponding bit in the interrupt mask register (IMR) is also a '1' the interrupt request output will be asserted. If the corresponding bit in the IMR is a '0' the state of the bit in the ISR has no effect on the interrupt request output. The contents of this register can be read by the CPU either unmasked or masked by the IMR. See Table 1.

ISR[7] - Input Port Change Status

This bit is a '1' when a change of state has occurred at the IP0, IP1, IP2 or IP3 inputs and that event has been programmed to cause an interrupt via ACR[3:0]. It is cleared when the CPU reads the IPCR.

ISR[6] - Channel B Change in Break

This bit indicates that the channel B receiver has detected the beginning or end of a received break. It is reset when the CPU invokes a channel B 'reset break change interrupt' command.

ISR[5] - Channel B Receiver Ready or FIFO Full

The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that data is in the FIFO. It is set when a character is transferred from the receive shift register to the FIFO and cleared when the CPU reads the RHR. If there are still more characters in the FIFO after the read operation, the bit will be set again after the FIFO is 'popped.'

If this bit is programmed as FIFO full, it is set when a character is transferred from the receive shift register to the receive shift register to the FIFO if that transfer causes the FIFO to become full. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, this bit will be set again after the read operation, when that character is loaded into the FIFO.

ISR[4] - Channel B Transmitter Ready

This bit is a duplicate of TXRDYB, SRB[2].

ISR[3] - Counter Ready

In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a 'stop counter' command.

In the timer mode, this bit is set once each cycle of the generated square wave. It is also set each time a 'start counter' command is issued if the output is, at that time, in the second (high) half of the square wave cycle. The bit is reset by a 'stop counter' command. The command, however, does not stop the C/T.

ISR[2] - Channel A Change in Break

This bit indicates that the channel A receiver has detected the beginning or end of a received break. It is reset when the CPU invokes a channel A 'reset break change interrupt' command.

ISR[1] - Channel A Receiver Ready or FIFO Full

The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that data is in the FIFO. It is set when a character is transferred from the receive shift register to the FIFO and cleared when the CPU reads the RHR. If there are still more characters in the FIFO after the read operation, the bit will be set again after the FIFO is 'popped.'

If this bit is programmed as FIFO full, it is set when a character is transferred from the receive shift register to the FIFO if that transfer causes the FIFO to become full. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, this bit will be set again after the read operation, when that character is loaded into the FIFO.

ISR(0) - Channel A Transmitter Ready

This bit is a duplicate of TXRDYA, SRA(2).

IMR - Interrupt Mask Register

This register selects which bits in the ISR cause an interrupt to be asserted. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the interrupt request output will be asserted. If the corresponding bit in the IMR is a '0', the state of the bit in the ISR has no effect on the interrupt request output. Note that the IMR does not mask the programmable interrupt outputs, OP3-OP7.

CTUR/CTLR - Counter/Timer Registers

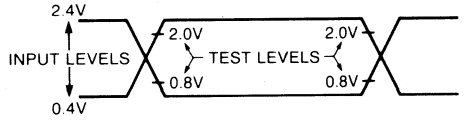
The CTUR and CTLR hold the eight MSBs and eight LSBs respectively of the value to be used the the counter/timer in both of its modes of operation. The minimum value which may be loaded into CTUR/CTLR is 0001H. These registers are write-only and cannot be read by the CPU.

IVR-Interrupt Vector Register

The IVR holds the value which the DUART places on the data bus in response to assertion of the interrupt acknowledge input. This applies to the XR-68C681 and to the XR-88C681 when operating in Z-mode. The register is not used for any function when the XR-88C681 operates in I-mode but remains writeable and readable by the CPU, and can be used for any purpose. The contents of this register are initialized to 9FH by a hardware reset.

NOTES:

1. Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the Electrical Characteristics section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltage larger than the rated maxima.
3. Parameters are valid over the specified temperature and operating supply ranges. Typical values are at 25°C, V_{CC} = 5V and typical processing parameters.
4. All voltages are referenced to ground (GND). For testing, input signal levels are 0.4V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate. See Figure 3.
5. Measured operating with a 3.6864MHz crystal and with all outputs open.
6. AC test condition for outputs: C_L = 150pF, except interrupt outputs: C_L = 50pF, R_L = 2.7K ohm to V_{CC}.
7. For the XR88C681, timing is illustrated and referenced to the RDN and WRN inputs. The device may also be operated using CEN as the 'strobing' input. In this case, all specifications apply referenced to the falling and rising edges of CEN.
8. If CEN is used as the strobing input, this parameter defines the minimum high time between CENs.
9. Consecutive write operations to the same register require at least three edges of the X1 clock between writes.
10. This parameter is system dependent. For any DUART in the daisy chain, t_{IAS} must be greater than the sum of t_{EOD} for the highest priority device in the daisy chain, t_{EIS} for the DUART, and t_{DIO} for each device separating them in the daisy chain.
11. This specification imposes a 6MHz maximum 68000 clock frequency if a read or write cycle follows immediately after the previous read or write cycle. A higher 68000 clock can be used if this is not the case.
12. This specification imposes a lower bound on CSN and IACKN low, guaranteeing that they will be low for at least one CLK period.
13. This parameter is specified only to insure that DTACKN is asserted with respect to the rising edge of X1/CLK as shown in the timing diagram, not to guarantee operation of the part. If the specified setup time is violated, DTACKN may be asserted as shown or may be asserted one clock cycle later.
14. The minimum high time must be at least 1.5 times the X1/CLK period and the minimum low time must be at least equal to the X1/CLK period if either channel's R_X is operating in external 1x clock mode.
15. For prime grade N, P, J, L, M, ML, V_{CC} = 5 V ±10%.



AC testing inputs are driven at 0.4V for a logic '0' and 2.4V for a logic '1', except for −40 to 85°C and −55 to 125°C, logic '1' shall be 2.6V. Timing measurements are made at 0.8V for a logic '0' and 2.0V for a logic '1'.

Figure 3. Input and Output Levels for Timing Measurements

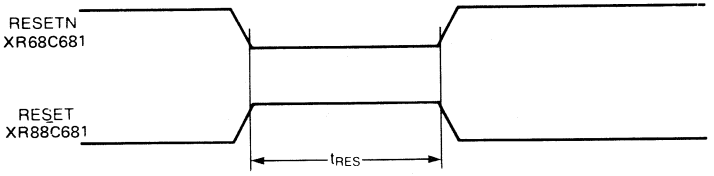


Figure 4. Reset Timing

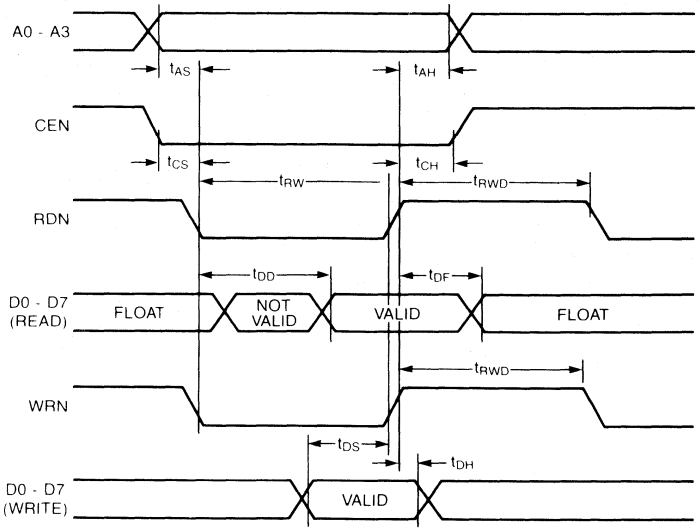


Figure 5. XR-88C681 Read and Write Cycle Timing

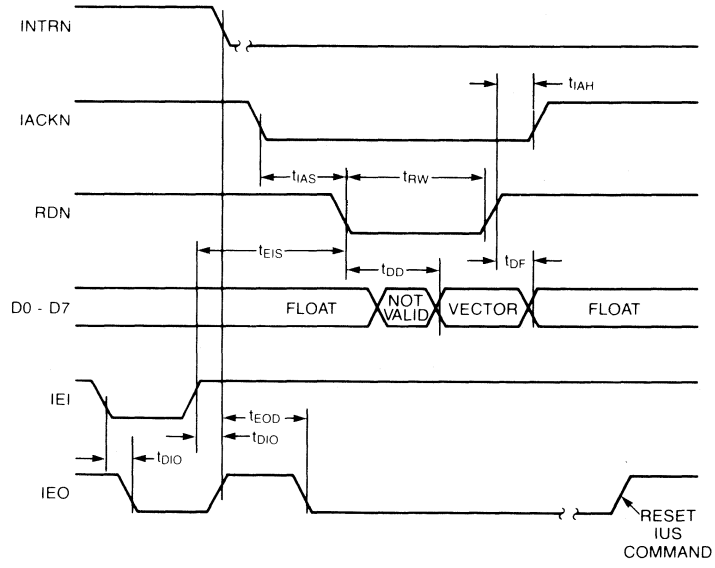


Figure 6. XR-88C681 Z-mode Interrupt Cycle Timing

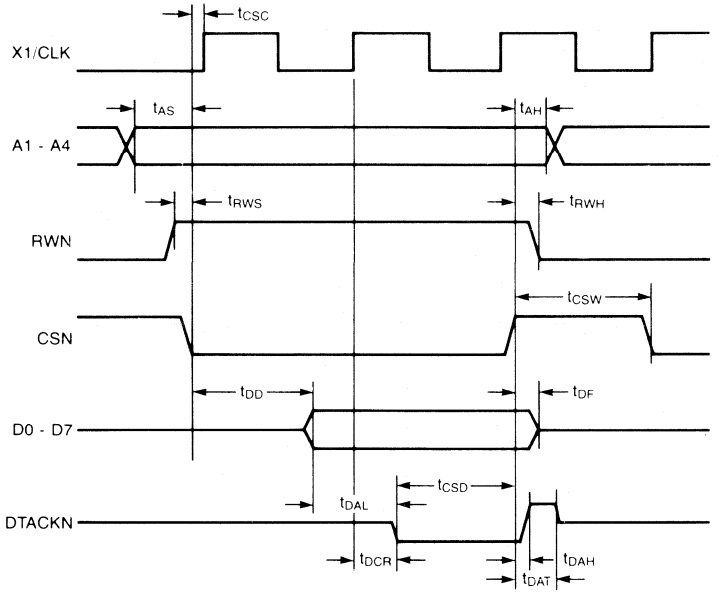


Figure 7. XR-68C681 Read Cycle Timing

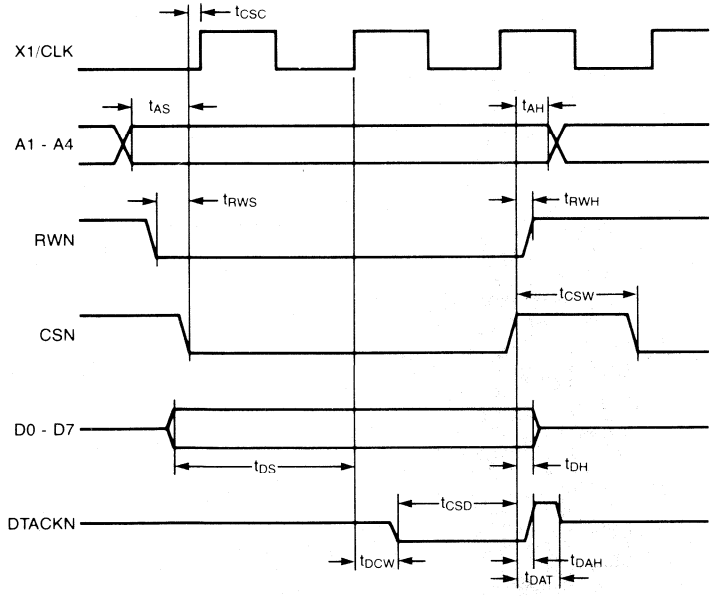


Figure 8. XR-68C681 Write Cycle Timing

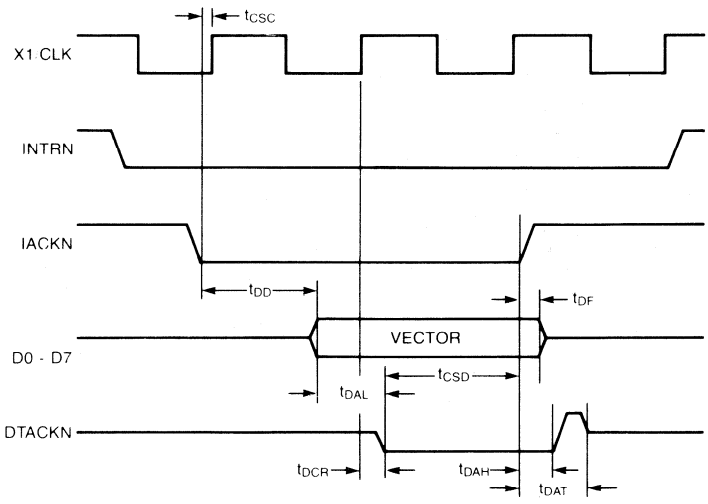


Figure 9. XR-68C681 Interrupt Cycle Timing

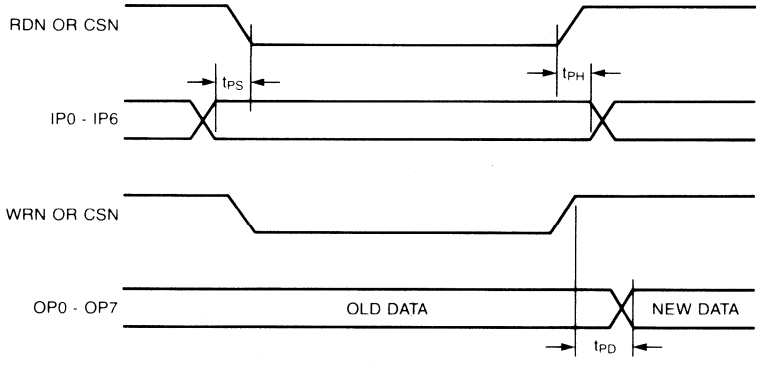
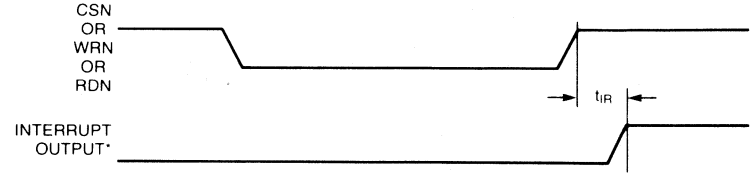


Figure 10. Port Timing



*INTRN or OP3 - OP7 when used as interrupt outputs.

Figure 11. Interrupt Timing

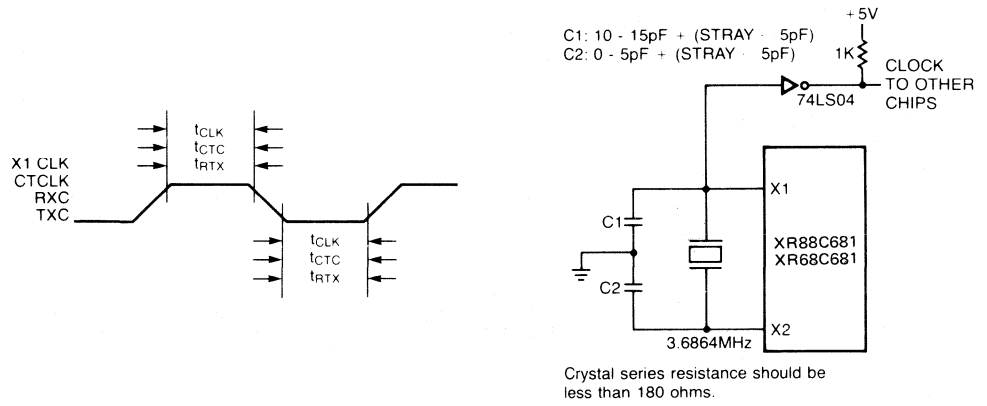


Figure 12. Clock Timing

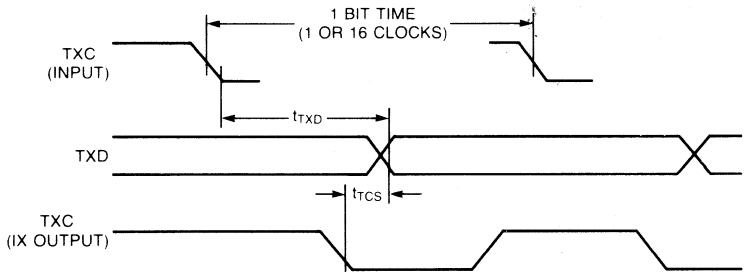


Figure 13. Transmitter Timing

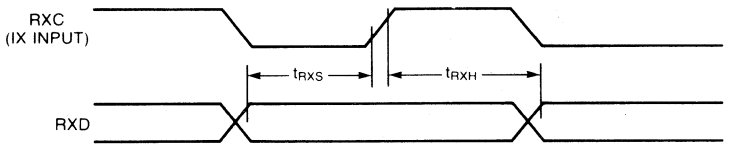
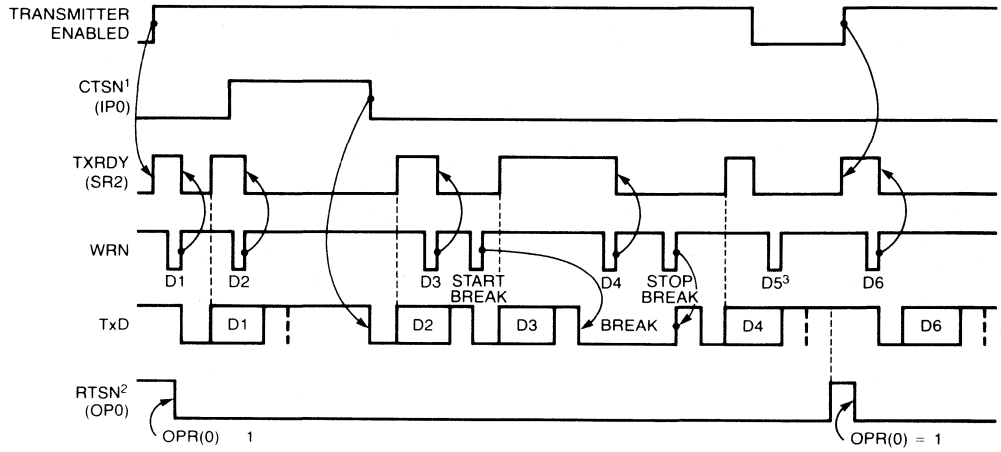
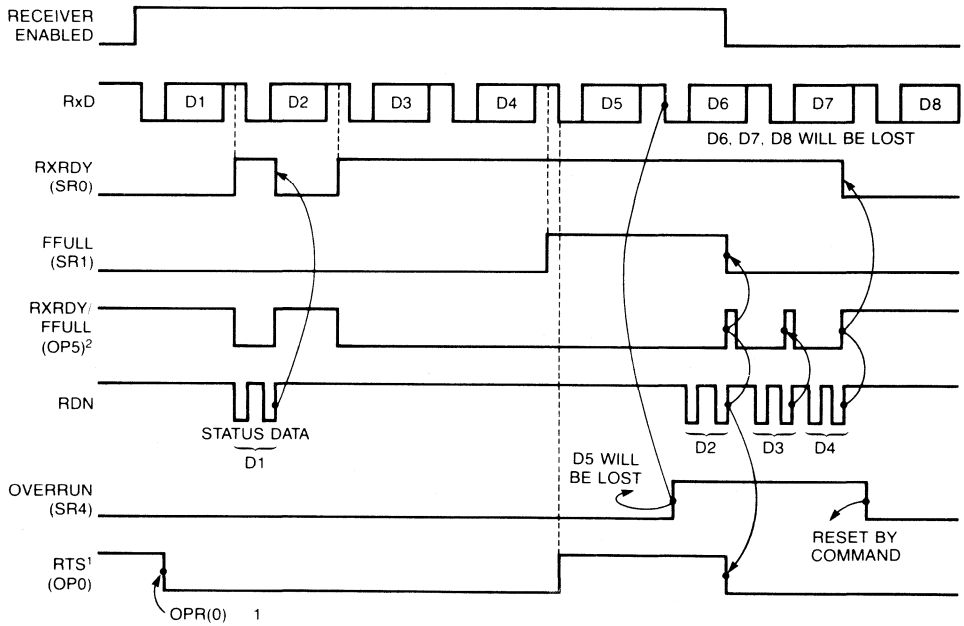


Figure 14. Receiver Timing



NOTES
1. Operation shown for MR2(4) = 1
2. Operation shown for MR2(5) = 1
3. D5 will not be transmitted

Figure 15. Transmitter Operation



NOTES
1. Operation shown for MR1(7) = 1
2. Shown for OPCR(4) = 1 and MR1(6) = 0

Figure 16. Receiver Operation

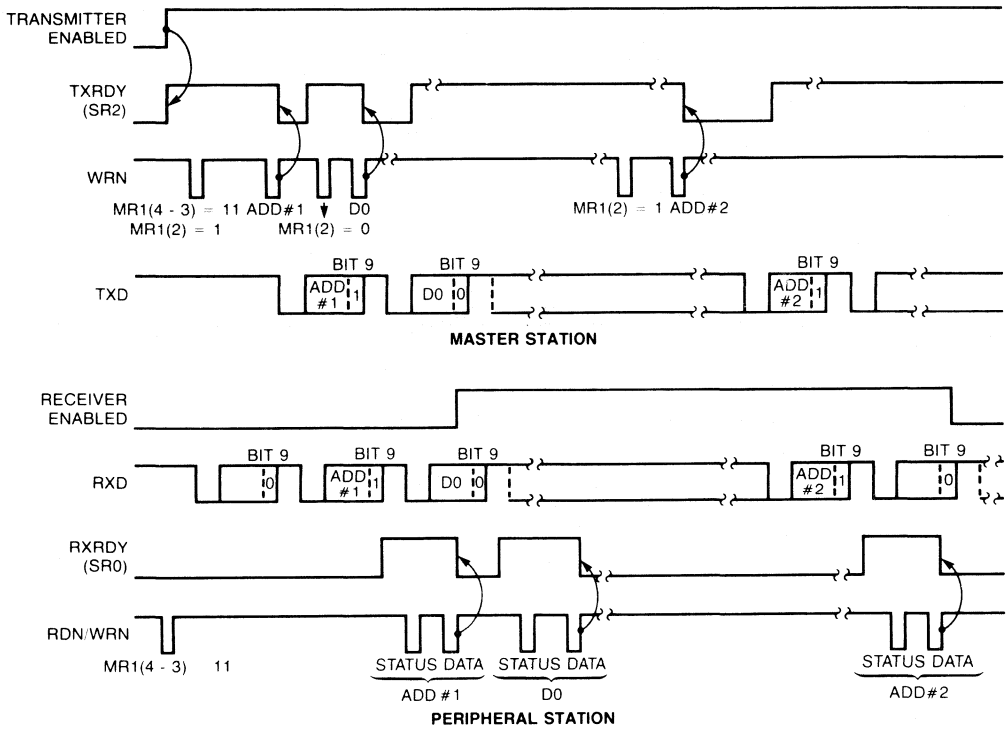
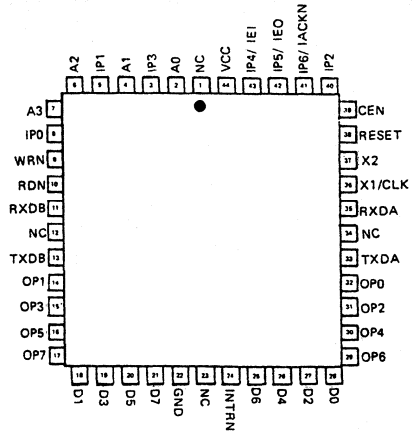
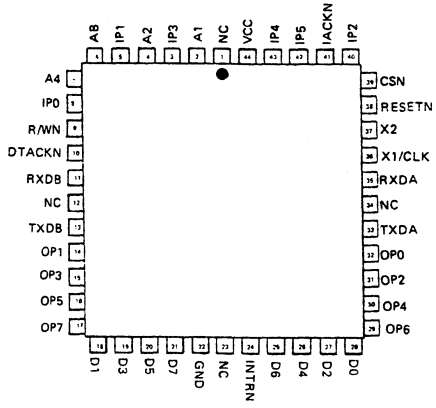


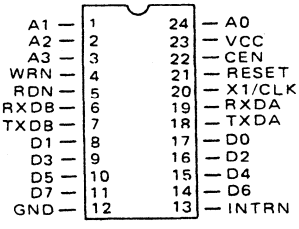
Figure 17. Transmitter and Receiver Operation in Multidrop Mode



XR-88C681CJ
(PLCC)



XR-68C681CJ
(PLCC)



XR-88C681/24

CMOS Quad Channel UART (QUART)

PRELIMINARY

GENERAL DESCRIPTION

The EXAR Quad Universal Asynchronous Receiver and Transmitter (QUART) is a data communications device that provides four fully independent full duplex asynchronous communications channels in a single package. The QUART is designed for use in microprocessor based systems and may be used in a polled or interrupt driven environment.

The XR-82C684 offers a single IC solution for various microprocessor families. The 88 and 68 modes can be selected by tying SEL pin to VDD or VSS.

The QUART is fabricated using advanced two layer metal, with a high density EPI/CMOS 1.8µ process to provide high performance and low power consumption.

FEATURES

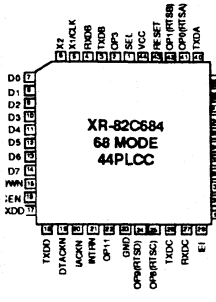
Four Full Duplex, Independent Channels, Asynchronous Receiver and Transmitter
Quadruple Receive and Transmit Buffer
Programmable Stop Bits in 1/16 Bit Increments
Pin Selectable 88 and 68 mode
Four Independent Internal Bit Rate Generators with more than 33 Bit Rates
Independent Bit Rate Selection for each Transmitter and Receiver
External Clock Capability
Normal, Autoecho, Local Loop Back and Remote Loopback Modes
Two Multifunction 16-Bit Counter/ Timer
Interrupt Output with Sixteen Maskable Interrupt Conditions
Prioritized Interrupt Vector Output on Acknowledge
Programmable Interrupt Daisy Chain
16 General Purpose Outputs
16 General Purpose Inputs with Eight Change of State Detectors on Inputs
Multidrop Mode Compatible with 8051 Nine-Bit Mode
On Chip Oscillator for Crystal
Stand-by Mode to Reduce Operating Power

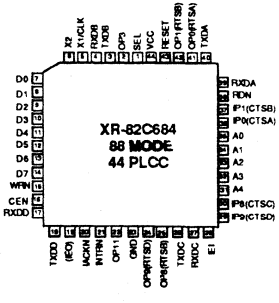
ABSOLUTE MAXIMUM RATINGS

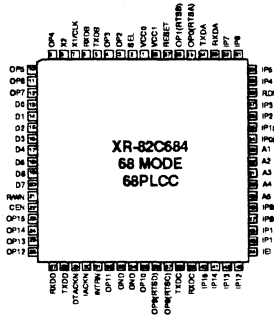
DC Supply Voltage	7V
Storage Temperature	-65°C to150°C
All Voltages with respect to ground	-0.5 V to +7 V

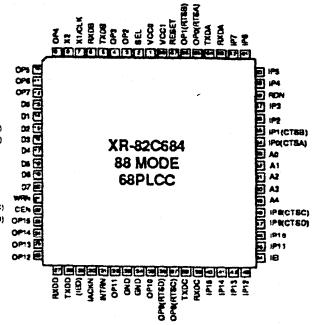
ORDERING INFORMATION

Part no.	Package	Operating Temperature
XR-82C684CJ/44	PLCC44 PIN	0° C to 70° C
XR-82C684J/44	PLCC44 PIN	-40° C to 85° C
XR-82C684CJ	PLCC68 PIN	0° C to 70° C
XR-82C684J	PLCC68 PIN	-40° C to 85° C









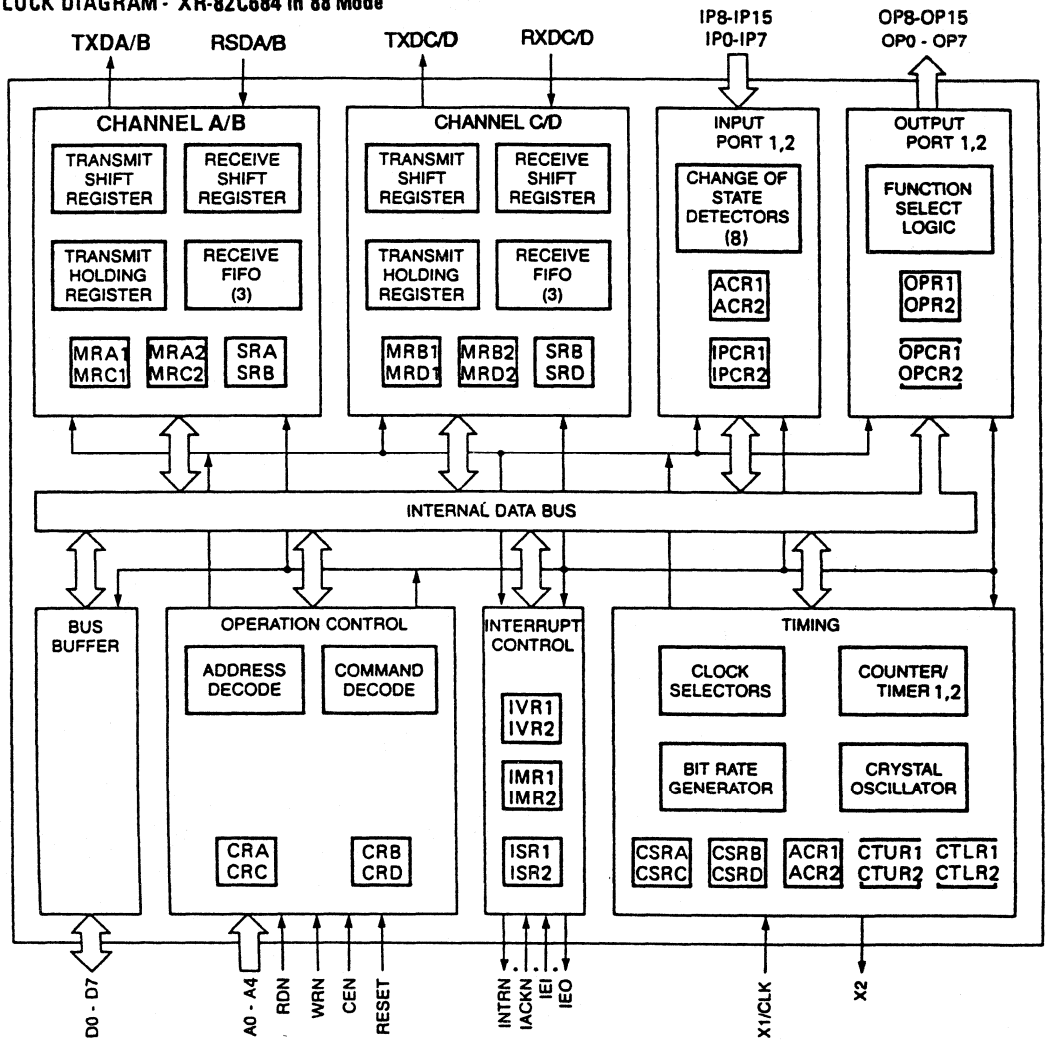
SYSTEM DESCRIPTION

Each channel of the QUART may be independently programmed for operating mode and data format. The operating speed of each receiver and transmitter may be selected from one of 33 internally generated fixed bit rates, from a clock derived from an internal counter/timer, or from an external 1x or 16x clock. The bit rate generator can operate directly from a crystal connected across two pins or from an external clock. The ability to independently program the operating speed of the receiver and transmitter of each channel makes the QUART attractive for split speed channel applications such as clustered terminal systems.

Receiver and transmitter data are quadruple-buffered in an on chip FIFO to minimize the risk of receiver or transmitter overrun and to reduce overhead in interrupt driven applications. The QUART also provides a flow control capability to inhibit transmission from a remote device when the buffer of the receiving QUART is full, thus preventing loss of data.

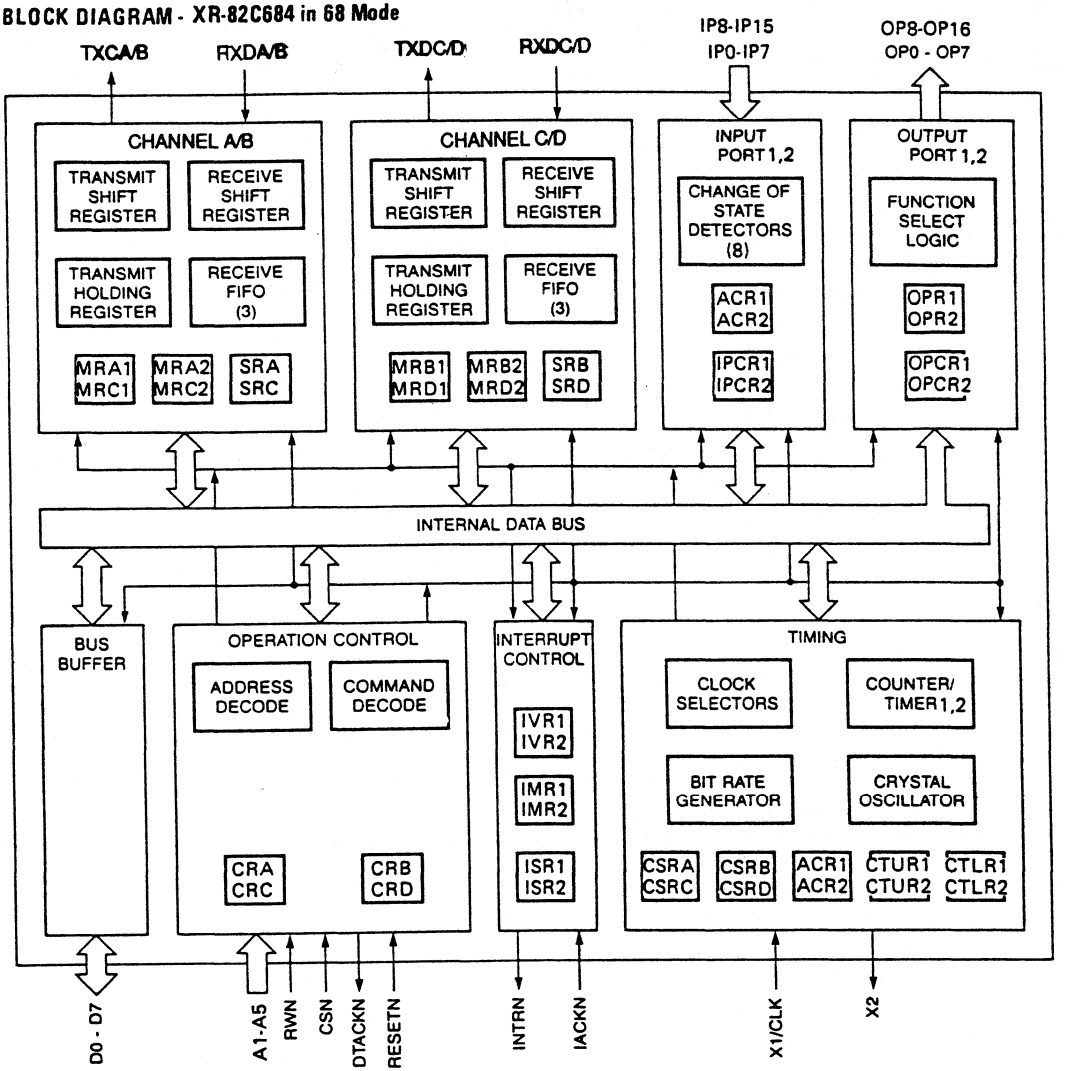
The QUART also provides two general purpose16 bit counter/timers (which may also be used as programmable bit rate generators), two multi-purpose input ports and two multi-purpose output ports.

BLOCK DIAGRAM - XR-82C684 in 88 Mode



* ALTERNATE FUNCTIONS FOR IP4 - IP6

BLOCK DIAGRAM - XR-82C684 in 68 Mode



DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25° C, V_{CC} = 5.0V ± 5% unless otherwise specified.

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH15}	Input High Voltage	2.0		V_{CC}	V	
V_{IH}	Input High Voltage	2.2			V	-55° C to 125° C
V_{IH1}	Input High Voltage (X1/CLK)	4.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.4 mA
V_{OH}	Output High Voltage (Except Open Drain Output)	2.4			V	I_{OH} = -400 µA
I_{IL}	Input Leakage Current	-25		25	µA	V_{IN} = 0 to V_{CC}
I_{X1L}	X1 Input Low Current		-20		µA	V_{IN} = 0
I_{X2L}	X2 Input Low Current		-7		mA	0
I_{X1H}	X1 Input High Current		20		µA	V_{IN} = V_{CC}
I_{X2H}	X2 Input High Current		20		µA	V_{IN} = V_{CC}
I_{LL}	Data Bus Tri-State Leakage Current	-10		10	µA	V_O = 0 to V_{CC}
I_{OC}	Open Drain Output Leakage Current	-10		10	µA	V_O = 0 to V_{CC}
I_{CCA}	Power Supply Current		6	15	mA	Active Mode
I_{CCS}	Power Supply Current		3	10	mA	Standby Mode

AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{CC} = 5.0 V ± 5% unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Reset Timing (Figure 4)						
t_{RES}	Reset Pulse Width	1.0			µs	
XR-82C684 Read and Write Cycle Mode (Figure 5 & 6)[7]						
t_{AS}	A0-A4 Setup Time to RD, WR Low	10			ns	
t_{AH}	A0-A4 Hold Time from RD, WR High	0			ns	
t_{CS}	CS Setup Time to RD, WR Low	0			ns	
t_{CH}	CS Hold Time from RD, WR High	0			ns	
t_{RW}	RD, WR Pulse Width	225			ns	
t_{DD}	Data Valid from RD Low		60	175	ns	
t_{DF}	Data Bus Floating from RD High	10		100	ns	
t_{DS}	Data Setup Time to WR High	100			ns	
t_{DH}	Data Hold Time from WR High	5			ns	
t_{RWD}	High Time Between Reads and/or Writes[8,9]		100		ns	
XR-82C684 Z-mode Interrupt Cycle Timing (Figure 6)						
t_{DIO}	IEO Delay Time from IEI			100	ns	
t_{IAS}	IACK Setup Time to RD Low		Note 10		ns	
t_{IAH}	IACK Hold Time from RD High		0		ns	
t_{EIS}	IEI Setup Time to RD Low		50		ns	
t_{EOD}	IEO Delay Time from INTR Low			100	ns	

XR-82C684 Read, Write and Interrupt Cycle Timing 68 Mode (Figure 7, 8, 9)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{AS}	A1-A5 Setup Time to CS Low	10			ns	
t_{AH}	A1-A5 Hold Time from CS High	0			ns	
t_{RWS}	R/W Setup Time to CS Low	0			ns	
t_{RWH}	R/W Setup Time from CS High	0			ns	
t_{CSW}	CS High Pulse Width[9,11]	90			ns	
t_{CSD}	CS or IACK High from DTACK Low[12]	20			ns	
t_{DD}	Data Valid from CS or IACK Low			175	ns	
t_{DF}	Data Bus Floating from CS or IACK High	10		100	ns	
t_{DS}	Data Setup Time to CS Low	0			ns	
t_{DH}	Data Hold Time from CS Low	125			ns	
t_{DAL}	DTACK Low from Read Data Valid	100			ns	
t_{DCR}	DTACK Low (read cycle) from CLK High			125	ns	
t_{DCW}	DTACK Low (write cycle) from CLK High			125	ns	
t_{DAH}	DTACK High from CS or IACK High			100	ns	
t_{DAT}	DTACK High Impedance from CS or IACK High			125	ns	
t_{CSC}	CS or IACK Setup Time to CLK High[13]	90			ns	

Port Timing 82C684 (Figure 10)[7]

t_{PS}	Port Input Setup Time to RD/CS Low	0			ns	
t_{PH}	Port Input Hold Time from RD/CS High	0			ns	
t_{PD}	Port Output Valid from WR/CS High			400	ns	

Interrupt Output Timing 82C684 (Figure11)

t_{IR}	INTR or OP3-OP7/OP10-OP15 When Used As Interrupts High from:					
	Clear of Interrupt Status Bits in ISR or IPCR			300	ns	
	Clear of Interrupt Mask in IMR			300	ns	

Clock Timing 82C684 (Figure 12)

t_{CLK}	X1/ CLK (External) High or Low Time	100			ns	
tCLK	X1/ CLK Crystal or External Frequency	2.0	3.684	7.372	MHz	
t_{CTC}	Counter/Timer External Clock High or Low Time (IP2 / IP10)	100			ns	
t_{CTC}	Counter/Timer External Clock Frequency	0		7.372	MHz	
t_{RTX}	RXC and TXC (External) High or Low Time[14]	220			ns	
fRTX	RXC and TXC (External) Frequency					
	16x	0		16.0	MHz	
	1x	0		1.0	MHz	

Transmitter Timing 82C684 (Figure 13)

t_{TXD}	TXD Output Delay - TXC (External) Low			350	ns	
t_{TCS}	TXD Output Delay - TXC (Internal) Output Low			150	ns	

Receiver Timing 82C684 (Figure 14)

t_{RXS}	RXD Data Setup Time to RXC External High	240			ns	
t_{RXH}	RXD Data Hold Time from RXC External High	200			ns	

PIN DESCRIPTIONS XR-82C684

MNEMONIC	TYPE	DESCRIPTION
D0-D7	I/O	**8-bit Bidirectional Three-state Data Bus.** Bit 0 is the LSB and bit 7 is the MSB. All transfers between the CPU and QUART take place over this bus. The bus is three-stated when the CS input is high, except during an IACK cycle or in the Z-mode.
A1-A5	I	**Address Inputs.** These inputs select the QUART registers or port for the current read/write operation.
CS	I	**Chip Select low.** The data bus is three-stated when CS is high. Transfers between the CPU and the QUART via D0-D7 are enabled when CS is low.
WR	I	**Write Strobe.** (88 mode) Active low. A low on this input while CS is also low writes the contents of the data bus into the addressed register.The transfer occurs on the rising edge of WR.
R/W	I	**Read / Write.** (68 mode) A high input while CS is low indicates a read cycle while a low input while CS is low indicates a write cycle.
RD	I	**Read Strobe.** (88 mode) Active low on this input while CS is also low places the contents of the addressed source on the data bus. The transfer begins on the falling edge of RD.
RESET	I	**Master Reset.** (Active high for 88 mode and Active low for 68 mode). Clears internal registers SRn, ISRn, IMRn, OPRn, OPCRn and initializes the IVRn to 0FH, stops the counter/timer, puts OP0-OP15 in the high state, and places both serial channels in the inactive state with the TXDA, TXDB, TXDC and TXDD outputs marking (high).
INTRN	O	**Interrupt Request.** Active low, open drain. INTRN is asserted upon the occurrence of one or more of the chip's maskable interrupting conditions.
IACK	I	**Interrupt Acknowledge.** (68 mode) Active low. Assertion of IACK indicates that the current bus cycle is an interrupt acknowledge cycle. If the QUART has an interrupt active, it responds by placing the interrupt vector on the data bus and asserting DTACK.
IEI	I	**Interrupt Enable Input.** (88 mode) Active high.
IEO	O	**Interrupt Enable Output.** (88 mode) Active high.
DTACK	O	**Data Transfer Acknowledge** (68 mode) Three state, active low. Assertion of DTACK indicates that data is present on the bus during a read or interrupt acknowledge cycle and that the data from the bus has been written into the addressed destination during a write cycle.
X1 / CLK	O	**Crystal Output or External Clock Input.** This pin is the connection for one side of the crystal and a capacitor to ground when the internal oscillator is used. If the oscillator is not used, an external clock signal must be supplied at this input.
X2	I	**Crystal Input.** Connection for other side of the crystal. If the oscillator is used, a capacitor must also be connected from this pin to ground. This pin must be left open if an external clock is supplied at X1 / CLK.

RXD-A RXD-B RXD-C RXD-D	I	**Receive Serial Data Inputs**. The least significant bit is received first. If external receiver clock is specified, the data is sampled on the rising edge of the clock.
TXD-A TXD-B TXD-C TXD-D	O	**Transmitter Serial Data Outputs**. The least significant bit is transmitted first. Held in the high (marking) state when the transmitter is idleordisabled and also when the channel operates in local loopback mode. If external transmitter clock is specified, the data is shifted out on the falling edge of the clock.
OP0	O	**Output 0.** Active low. Can be programmed as a general purpose output or as the channel A request-to-send output (RTS-A).
OP1	O	**Output 1.** Active low. Can be programmed as a general purpose output or as the channel B request-to-send output (RTS-B).
OP2	O	**Output 2.** Active low. Can be programmed as a general purpose output, the channel A transmitter 16x or 1x clock output, or the channel A receiver 1x clock output.
OP3	O	**Output 3**. Active low. Can be programmed as a general purpose output, the channel B transmitter 1x clock output, the channel B receiver 1x clock output, or an open drain counter/timer 1 ready output.
OP4	O	**Output 4**. Active low. Can be programmed as a general purpose output or as an open drain channel A RXRDY/FFULL output.
OP5	O	**Output 5**. Active low. Can be programmed as a general purpose output or as an open drain channel B RXRDY/FFULL output.
OP6	O	**Output 6.** Active low. Can be programmed as a general purpose output or as an open drain channel A TXRDY output.
OP7	O	**Output 7.** Active low. Can be programmed as a general purpose output or as an open drain channel B TXRDY output.
OP8	O	**Output 8**. Active low. Can be programmed as a general purpose output or as the channel C request-to-send output (RTS-C).
OP9	O	**Output 9.** Active low. Can be programmed as a general purpose output or as the channel D request-to-send output (RTS-D).
OP10	O	**Output 10.** Active low. Can be programmed as a general purpose output, the channel C transmitter 16x or 1x clock output, or the channel C receiver 1x clock output.
OP11	O	**Output 11.** Active low. Can be programmed as a general purpose output, the channel D transmitter 1x clock output, the channel D receiver 1x clock output, or an open drain counter/timer 2 ready output.
OP12	O	**Output 12**. Active low. Can be programmed as a general purpose output or as an open drain channel C RXRDY/FFULL output.
OP13	O	**Output 13**. Active low. Can be programmed as a general purpose output or as an open drain channel D RXRDY/FFULL output.
OP14	O	**Output 14.** Active low. Can be programmed as a general purpose output or as an open drain channel C TXRDY output.

OP15	O	**Output 15.** Active low. Can be programmed as a general purpose output or as an open drain channel D TXRDY output.
IP0	I	**Input 0.** General purpose input or CTS-A, the channel A active low clear- to-send input.
IP1	I	**Input 1.** General purpose input or CTS-B, the channel B active low clear to send input.
IP2	I	**Input 2.** General purpose input or the counter/timer 1 external clock input.
IP3	I	**Input 3.** General purpose input or the channel A transmitter external clock input.
IP4	I	**Input 4.** General purpose input or the channel A receiver external clock input.
IP5	I	**Input 5.** General purpose input or the channel B transmitter external clock input.
IP6	I	**Input 6.** General purpose input or the channel B receiver external clock input.
IP7	I	**Input 7.** General purpose input.
IP8	I	**Input 8.** General purpose input or CTS-C, the channel C active low clear-to-send input.
IP9	I	**Input 9.** General purpose input or CTS-D, the channel D active low clear-to-send input.
IP10	I	**Input 10.** General purpose input or the counter/timer 2 external clock input.
IP11	I	**Input 11.** General purpose input or the channel C transmitter external clock input.
IP12	I	**Input 12.** General purpose input or the channel C receiver external clock input.
IP13	I	**Input 13.** General purpose input or the channel D transmitter external clock input.
IP14	I	**Input 14.** General purpose input or the channel D receiver external clock input.
IP15	I	**Input 15.** General purpose input.
SEL	I	**Mode Select.** 88 mode can be selected by tying this pin to ground; connecting this pin to Vcc will select the 68 mode.
VCC	I	**+5 Volt Power Input**
GND	I	**Signal and Power Ground**

PRINCIPLES OF OPERATION

As illustrated in the block diagram, the QUART consists of the following major blocks:

Bus Buffer
Operation Control
Interrupt Control
Timing
Input Ports
Output Ports
Serial Communication Channels A, B, C and D

BUS BUFFER

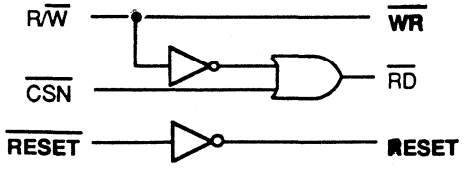
The data bus buffer provides the interface between the internal and external data buses. It is controlled by the operation control block to allow data transfers to take place between the host CPU and the QUART.

OPERATION CONTROL

The control logic receives operating commands from the CPU and generates proper signals to the various sections of the QUART. It contains address decoding and read/write circuits to permit communication with the microprocessor and internal registers, to set configuration commands and to monitor device status.

In the 68 mode (68000 Microprocessor Family), the QUART includes a data transfer acknowledge (DTACK) output which is asserted during data transfer cycle to verify that the requested operation has been completed. It indicates that the input data has been latched during a write cycle, that the requested data is on the data bus during a read cycle, or that the interrupt vector is on the data bus during an interrupt acknowledge cycle.

When using a 6800 family processor, the QUART should be used in the 88 mode. This can be readily achieved by implementing the minor external logic change as shown in the figure below:



Note: This is required for 6800 based microprocessors and is not necessary for 68000 based machines.

The addressing of the internal registers of the QUART is described in Table 1. The mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The MR1n pointer is set by a hardware reset or by 'reset pointer' command from command register (CRn bit4-7). Any read or write operation to the mode register while the pointer is pointing at MR1n switches the pointer to MR2n and remains there such that any subsequent accesses are always to MR2n unless the pointer is reset back to MR1n.

INTERRUPT CONTROL

An interrupt request output signal (INTRN) is provided which may be programmed to be asserted upon the occurrence of any of the following events:

Transmit Hold register A,B,C or D ready.
Receive Hold register A,B,C or D ready.
Receive FIFO A,B,C or D Full.
Start or End of received Break A,B,C or D
End of Counter/Timer count reached.
Change of State on input pins IP0,
IP1, IP2, IP3, IP8, IP9, IP10 or IP11

Associated with the interrupt system are the interrupt status register (ISRn), the interrupt mask register (IMRn), and the interrupt vector register (IVRn).The ISRn indicates the current state of all the potential interrupting conditions listed above. The IMRn may be programmed to select only certain of these conditions to assert the INTR output.

In the 88 mode, the QUART may be programmed to operate in two modes to accommodate different CPU interface requirements.

In the "I mode", which is the default mode, after a hardware reset, interrupt prioritization and interrupt vector generation, if required, are implemented using external hardware. In this mode, the on-chip interrupt vector register is not utilized and is available for use as an auxiliary read/write register for any purpose.

In the "Z mode", which is invoked via a command to command register B three pins are designated as an interrupt acknowledge (IACK), interrupt enable input (IEI) and interrupt enable output (IEO). IEI and IEO are the input and output of an interrupt daisy chain, as illustrated in Figure 1A. IEI high means that the QUART may generate an interrupt request.

A device with IEI high inhibits other devices by setting IEO low. Looking down the daisy chain; a device with IEI low must keep its IEO output low. This way it is possible to set up a predetermined priority chain in the system. The priority sequence is as follows: THR (channels A,B,C and D), RHR (channel A,B,C and D), Receive FIFO Full (channels A,B,C and D), Start or End of received break (channels A,B,C and D), End of

Counter/Timer (either DUART 1 or 2 as needed), and last the change of state on the inputs IP0, IP1, IP2, IP3, IP8, IP9, IP10 or IP11 (either DUART 1or 2 and sequence as shown).

Sometime after the interrupt request, the CPU will respond with an interrupt acknowledge cycle, followed by a RD cycle (Figure 1B). The time between IACK and RD allows the daisy chain to stabilize. Also as long as IACK is asserted, the QUART is inhibited from issuing a new interrupt request. The device making the request sets its internal 'interrupt under service' (IUS) latch and places the vector from the IVR (Interrupt Vector Register) on the data bus. Upon completion, the CPU must issue a reset IUS latch command to the chip, which resets the latch and returns the daisy chain to its normal condition. In the 68 mode, the QUART has its interrupt request active and responds to the IACK input by placing the vector from the IVR on the data bus and asserting DTACK. Otherwise, it ignores IACK.

In either mode, outputs OP3-OP7 and OP11-OP15 can be programmed to provide separate open drain interrupt requests for transmitters A,B,C and D, receivers A,B,C and D, and the timer/counter 1, 2. See pin description.

TIMING

The timing block as illustrated in Figure 2 contains a crystal oscillator, a bit rate generator (BRG), a programmable 16-bit counter/timer (C/T), and four clock selectors.

The crystal oscillator operates from a parallel crystal connected between the X1/CLK and X2 pins. A crystal frequency of 3.6864 or 7.3728 MHz is required for generation of standard bit rates by the bit rate generator (see Table 3). A crystal clock or an external TTL clock signal on the X1/CLK pin can be used either directly or it can be divided by two before being used to generate the internal system clock. After reset, the device is in the divide by two mode. To select direct system clock, write "CO" in channel C of the command register. If an external clock is available, it may be connected to X1/CLK, with X2 left open.

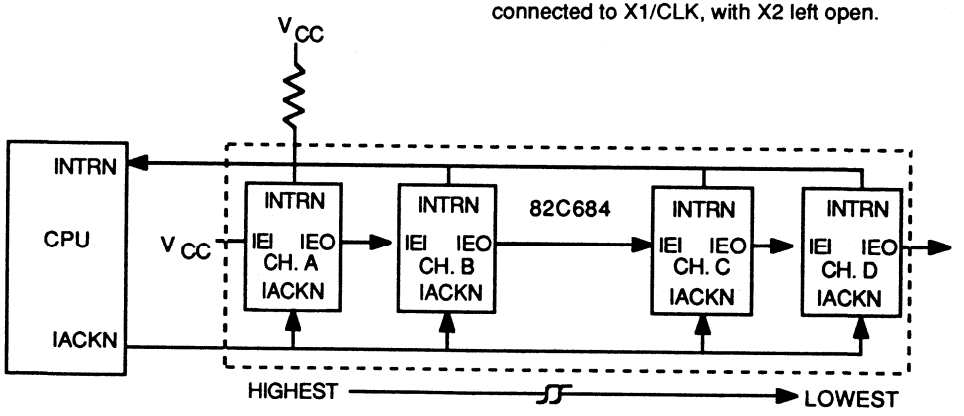


Figure 1A. Daisy Channel Interrupt Block Diagram

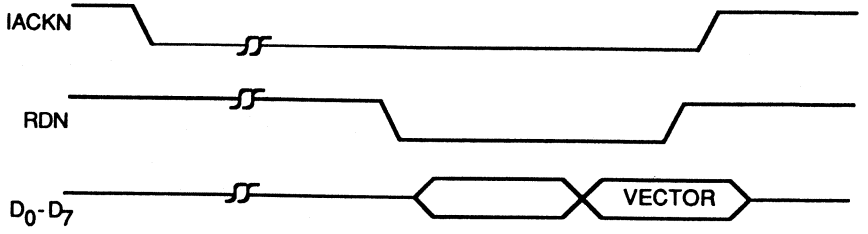


Figure 1B. Daisy Chained Interrupt Timing

The output of the oscillator is used by the BRG, the C/T and other internal circuits. This requires that a clock within the specified limits always be supplied to the QUART.

Bit Rate Generator

The BRG uses the crystal oscillator or external clock as an input and generates the clock for 33 commonly used data communications bit rates ranging from 50 to 230.4K bits per second. The actual clock frequencies output from the BRG are at 16 times these rates. The counter/timer can also be used as a programmable bit rate generator to produce a 16x clock for any bit rate not provided by the BRG. The four clock select multiplexers/per channel allow each receiver and transmitter to independently select its operating frequency as one of the outputs from the BRG, the output of the counter/timer, or an external clock. (See Input Port Selection in the Pin Description Table, page 8)

Counter /Timer

Each C/T is a programmable 16-bit down-counter which can use one of several timing sources as their input. The C/T outputs are available to the clock selectors for use as a programmable bit rate for any receiver or transmitter (note that counter/timer 1 is used for A/B receiver and transmitter, counter/timer 2 is used for C/D receiver and transmitter), each can be programmed to generate an interrupt each time it reaches its terminal count of OOOOH, and can also be programmed as an output at OP3 and OP11.

In the timer mode, the C/T acts as a programmable divider and generates a square wave whose period is twice the value (in clock periods) of the contents of the counter/timer registers CTUR and CTLR. The contents of these registers may be changed at any time, but will only begin to take effect at the next half cycle of the square wave. The C/T begins operation using the values in CTUR/CTLR upon receipt of a 'start counter' command (see Table 1).

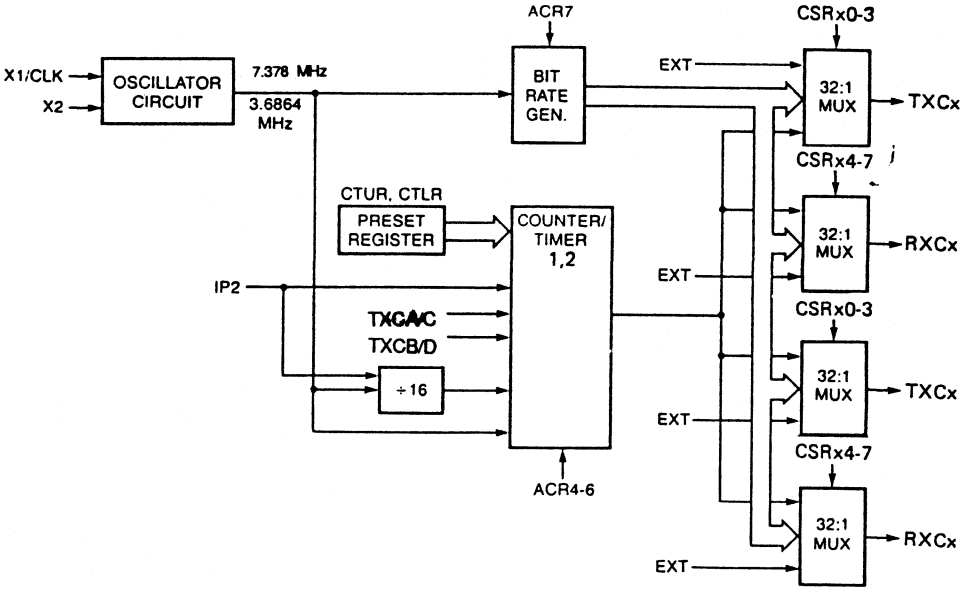


Figure 2. Half of QUART Timing Circuit Block Diagram

The C/T then runs continuously. A subsequent 'start counter' command causes the C/T to terminate the current timing cycle and begin a new timing cycle using the current values in CTUR and CTLR. The counter ready status bit (ISRn) is set once each cycle of the square wave. This allows use of the C/T as a periodic interrupt generator if the condition is programmed to generate an interrupt via the interrupt mask register. The status bit can be reset by issuing a 'stop counter' command (see Table 1). In this mode, however, the command does not actually stop the C/T. The generated square wave is output on OP3 or OP11 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses written into CTUR/CTLR, beginning at the receipt of a 'start counter' command. The counter ready status bit (ISR [3]) is set upon reaching the count of OOOOH. The C/T will continue to count past this (with the next count being FFFFH) until it is stopped by the CPU via a 'stop counter' command. If OP3 or OP11 is programmed to be the output of the C/T, the output remains high until the terminal count is reached, at which time the output goes low. It then returns to the high state and ISR[3] is cleared when the counter is stopped. A 'start counter' command while the counter is running restarts the counter with the values in CTUR/CTLR. The CPU may change CTUR or CTLR at any time but the new count takes effect only on the next start counter command. If new values are not programmed, the previous values are preserved and used for the next cycle.

In counter mode, the current value in the C/T may be read by the CPU by reading the upper and lower halves of the C/T separately (see Table 1). Stopping the counter when it is read is recommended in order to prevent potential problems which may occur if a carry form the lower half to the upper half occurs between the times that the two halves are read. However, note that a new start counter command will cause the counter to begin counting using the values in CTUR/CTLR.

INPUT PORT

The current state of the inputs to this unlatched port can be read by the CPU by performing a read as described in Table 1. A high input results in a logic "1" while a low input results in a logic "0". The pin description tables describe the alternate uses for the input pins, such as clock inputs and interrupt control signals. A read of the input port will show the state at the pin, regardless of it s programmed function.

Change of state detectors are provided for inputs IP0-IP3 and IP8 to IP11. These inputs, for example, are sampled by the 38.4 kHz output of the BRG (2.4 Kbps x 16). A high-to-low or low-to-high transition at these inputs lasting at least two clock periods (approximately 50 µs) will guarantee that the corresponding bit in the input port change register (IPCR) will be set, although it may be set by a change of state as short as 25 µs. The status bits in the IPCR are cleared when the register is read by the CPU. Any change of state can also be programmed to generate an interrupt.

OUTPUT PORT

The output ports can be used as a general purpose output or can be used to output timing and status signals by appropriately programming of the mode registers (MR1A-D, MR2A-D) and also the output port configuration registers. When used to output status signals the pins are open drain, which allows their use in a wire OR interrupt scheme.

When used as a general purpose output port, the outputs are the complements of the output port register (OPR). $OPR_{(n)}$ = 1 results in $OP_{(n)}$ low while $OPR_{(n)}$ = 0 results in $OP_{(n)}$ high. Bits of OPR can be set and reset individually. A bit is set by the address-triggered 'set output port bits' command (see Table 1) with the accompanying data specifying the bits to be set (1 = set, 0 = no change). A bit is reset by the address-triggered 'reset output port bits' command (see Table 1) with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

SERIAL CHANNELS A, B, C and D

Each serial channel of the QUART comprises a full duplex asynchronous receiver and transmitter. The four channels can independently select their operating frequency (from the BRG, the C/T, or an external clock) as well as operating mode. Besides the normal mode in which the receiver and transmitter of each channel operate independently, the QUART can be configured to operate in various looping modes, which are useful for local and remote diagnostics, as well as in a wake-up mode used for multi-drop applications.

Note: In the descriptions which follow, the transmitter and receiver are described for either channel. References to input and output pins and control and status bits and registers apply to either channel unless otherwise noted.

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream at the TXD pin, adding start, stop and optional parity bits as required by the asynchronous protocol.

The QUART is conditioned to transmit data when the transmitter is enabled via the command register. It indicates that it is ready to accept a character from the CPU for serialization by setting the TXRDY bit in the status register. This condition can be programmed to assert an interrupt request via the INTRN output and can also be programmed to assert the OP6/14 output (channel A/C) or the OP7/15 output (channel B/D). These conditions are negated when the CPU loads a character into the transmit holding register (THR). Data is transferred form the THR to the transmit shift register (TSR) immediately if the TSR is idle or when it completes serialization of the previous character. The TXRDY condition is then asserted again. Thus, one full character time of buffering is provided. Note that the THR will not accept characters while the transmitter is disabled.

The transmitter sends a start bit followed by the programmed number of data bits (least significant bit first), an optional parity bit, and the programmed number of stop bits and begins transmission of the next character if one has been loaded into the THR. Otherwise, the TXD output will remain high and the TXEMT status bit will be set following the transmission of the stop bits. Transmission resumes and the TXEMT status bit is cleared when the CPU loads a new character into the THR. The transmitter can be forced to send a continuous low at TXD by invoking a 'send break' command.

If the transmitter is disabled, it continues operating until the character currently being serialized, and any in the THR, are completely sent out. The transmitter can be reset by a software command. In this case, operation ceases immediately and the transmitter must be re-enabled before resuming operation.

Setting MR2n[4] of the appropriate channel programs its transmitter to begin transmission of a character only if the channels clear-to-send input pin (IP0 for channel A, IP1 for channel B, IP8 for channel C and IP9 for channel D) is low. If CTSN goes high in the middle of a transmission, the transmission of the current character is completed but TXD remains high and the next character will not be sent until CTSN is low again. Setting MR2[5] of the appropriate channel programs the transmitter to automatically deactivate its request-to-send output pin (OP0 for channel A, OP1 for channel B, OP8 for channel C and OP9 for channel D). If so programmed, and the transmitter has been disabled, the RTSN output will be negated one bit time after the characters in the TSR and THR (if any) are completely sent.

Receiver

The receiver accepts serial data at its RXD pin, checks for a proper start bit, converts the serial input to parallel form, checks the parity bit (if parity is specified), checks for presence of a stop bit, performs several other tests on the received data, and sends the assembled character to the CPU.

Each receiver is conditioned to receive data when it is enabled via the command register. It looks for a high to low (mark to space) transition indicating a start bit at the RXD input. If a transition is detected, the state of RXD is sampled each 16x clock for 7 1/2 clocks (16x clock mode) or at the next rising edge of the bit time clock (1x clock mode). If RXD is detected high at these sample times, the start bit is invalid and the search for a start bit begins again. If RXD remains low, a valid start bit is assumed and the receiver continues to sample the data at one bit time intervals, at the theoretical center of the bit , until the programmed number of data bits (LSB first), the parity bit (if any), and one stop bit have been assembled. The data is then transferred to the receive holding register (RHR) with the most significant unused bits set to zero. The status conditions (parity error, framing error, overrun error, and break received) are set to indicate to the CPU that a character is available to be read. Setting of RXRDY can be programmed to generate an interrupt request via INTRN and to assert OP4 (channel A), OP5 (channel B), OP12 (channel C) and OP13 (channel D).

After the stop bit position is sampled, the receiver will immediately begin to look for the start bit of the next character. However, if a non-zero character was received without a stop bit time after sampling of the stop bit, the receiver operates as if a new start bit transition had been detected at that point (half a bit time after the sampling of the stop bit).

If a break is received (an all zeroes character including the first stop bit), only a single character consisting of all zeroes will be loaded into the FIFO and the break received status bit will be set, no matter how long the break condition persists. RXD must return to a high condition for at least half a bit time before the search for a new start bit begins again.

The RHR consists of a first-in-first-out (FIFO) stack with a capacity of three characters. Data is transferred from the receive shift register into the topmost empty position in the FIFO. RXRDY is set whenever one or more characters are in the FIFO, and the FFULL status bit is set if the FIFO is filled with data. Either of these bits can be selected to assert an interrupt. A read of the RHR outputs the data at the top of the FIFO and any remaining characters are pushed up, thus freeing a FIFO position for new data.

In addition to the data word, three status bits are appended to each character position in the FIFO. These are parity error, framing error, and received break. Status can be provided in two ways, as programmed by MR1[5] in the channels mode register. In the 'character' mode, status is provided on a character by character basis: the status applies only to the character at the top of the FIFO. In the block mode, these three bits in the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode, reading the status register does not affect the FIFO. The FIFO is popped only when the RHR is read. Therefore, the status register should be read prior to reading the RHR. Also note that PE, FE and received break status register is asserted.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If a new start bit is detected while this condition exists, the character previously in the shift register is lost and the overrun error status bit is set. The contents of the FIFO are not affected when this occurs.

If the receiver is disabled, the contents of the FIFO are maintained and can be read by the CPU. Resetting the receiver initializes the FIFO pointers and clears the status bits immediately. In either case, any character currently being assembled is lost and operation does not resume until the receiver is re-enabled.

Setting MR[7] of the appropriate channel programs the receiver to automatically control de-activation of the request-to-send output (OP0 for channel A, OP1 for channel B). If so programmed, RTSN will be negated when a valid start bit is received while the FIFO is full, and will automatically be re-asserted when a FIFO position becomes available for that character. This feature can be used to prevent an overrun in the receiver by connecting the RTSN output to the CTSN input of the transmitting device.

Multidrop (8051 9-bit) Mode

Each serial channel of the QUART can be configured to operate in a wake-up mode useful for multidrop or multiprocessor applications. This mode is compatible with the serial 'Nine-bit Mode' of 8051-family microcomputers. In this mode of operation a master station, connected to a maximum of 256 slave station, transmit an address character followed by a block of data characters targeted for the addressed slave station. The slave stations normally have their receivers disabled. However, in this mode, the slave receivers monitor the incoming data stream and wake up the CPU (by asserting RXRDY) when any address character is detected. The slave station CPU then compares the received address to its own assigned address and enables the receiver, if it wishes, to receive the subsequent block of data, or leaves the receiver disabled if it does not. Upon completion of reception of the block of data, the receiver is disabled to re-initiate the process.

The multidrop mode is selected by programming MR[4:3] of the channel to '11'. In this mode, a transmitted character consists of a start bit, the programmed number of data bits, and address/data flag bit (A/D), and the programmed number of stop bits. A/D = 0 indicates that the character is data, while A/D = 1 identifies it as an address. The CPU controls the state of A/D in the transmitted character by programming MR1[2] of the channel prior to loading the data bits into the THR. MR1[2] = 0 results in A/D = 0 and MR1[2] =1 results in A/D =1.

In the multidrop mode, the receiver continuously looks at RXD whether enabled or not. When disabled, it loads a character into the RHR and sets RXRDY if its A/D bit is one (address flag) but discards the character if its A/D bit is zero (data flag). If the receiver is enabled, all characters received are transferred to the RHR. In either case, the received data bits are loaded into the RHR while the A/D bit is loaded into SR[5], the status register position normally used for parity error. Framing error, overrun error, and break detect status bits operate normally.

Standby Mode

The QUART may be placed in a standby mode to conserve power when its operation is not required. Upon reset, the QUART will be in the 'active operation' mode. A 'set standby mode' command issued via the channel A command register disables all clocks on the device except for the crystal oscillator, which significantly reduces the operating current. In this mode the only functions which will operate correctly are reading the input port, writing the output port and the 'set active mode' command. The latter, also invoked via the channel A command register, restores the device to normal operation within 25 µs. Resetting the transmitters and receivers and writing 00H into the interrupt mask register before going into the standby mode is recommended to prevent any spurious interrupts from being generated. The chip should be reprogrammed after the 'set active mode' command since register contents are not guaranteed to remain stable during the standby mode. Active operation can also be restored via hardware reset.

TABLE 1. QUART PORT AND REGISTER ADDRESSING

Address (HEX)	Reading From The Registers	Writing To The Registers
0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
1	Status Register A (SRA)	Clock Select Register A (CSRA)
2	Masked Interrupt Status Register 1(MISRA)	Command Register A (CRA)
3	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
4	Input Port Change Register 1 (IPCR1)	Auxiliary Control Register A (ACRA)
5	Interrupt Status Register 1 (ISR1)	Interrupt Mask Register 1 (IMR1)
6	Counter/Timer 1 Upper byte (CTU1)	Counter/Timer 1 Upper Register (CTUR1)
7	Counter/Timer 1 Lower byte (CTL1)	Counter/Timer 1 Lower Register (CTLR1)
8	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
9	Status Register B (SRB)	Clock Select Register B (CSRB)
A	RESERVED	Command Register B (CRB)
B	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
C	Interrupt Vector Register A (IVR1)	Interrupt Vector Register 1 (IVR1)
D	Input Port A (IP1)	Output Port Configuration Register 1 (OP0-OP7), (OPCRA)
E	Start Counter/Timer 1 (SCC1)	Set Output Port Bits Command 1 (SOPBC1)
F	Stop Counter/Timer Command 1 (STC1)	Reset Output Port Bits Command 1 (ROPBC1)
10	Mode Register C (MR1C, MR2C)	Mode Register C (MR1C, MR2C)
11	Status Register C (SRC)	Clock Select Register C (CSRC)
12	Masked Interrupt Status Register 2(MILSRB)	Command Register C (CRC)
13	Rx Holding Register C (RHRC)	Tx Holding Register C (THRC)
14	Input Port Change Register 2 (IPCR2)	Auxiliary Control Register B (ACRB)
15	Interrupt Status Register 2 (ISR2)	Interrupt Mask Register B (IMR2)
16	Counter/Timer 2 Upper byte (CTU2)	Counter/Timer 2 Upper Register (CTUR2)
17	Counter/Timer 2 Lower byte (CTL2)	Counter/Timer 2 Lower Register (CTLR2)
18	Mode Register D (MR1D, MR2D)	Mode Register D (MR1D, MR2D)
19	Status Register D (SRD)	Clock Select Register D (CSRD)
1A	RESERVED	Command Register D (CRD)
1B	Rx Holding Register D (RHRD)	Tx Holding Register D (THRD)
1C	Interrupt Vector Register B (IVR2)	Interrupt Vector Register 2 (IVR2)
1D	Input Port B (IP2)	Output Port Configuration Register 2 (OP8-OP15), (OPCRB)
1E	Start Counter/Timer 2 (SCC2)	Set Output Port Bits Command 2 (SOPBC2)
1F	Stop Counter/Timer Command 2 (STC2)	Reset Output Port Bits Command 2 (ROPBC2)

TABLE 2. REGISTER BIT FORMATS

MR1A-D

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Rx RTS Control	Rx Int Select	Error Mode	Parity Mode		Parity Type	Bits Per Char.	
0 = no 1 = yes	0 = RXRDY 1 = FFULL	0 = char 1 = block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multi-drop Mode		0 = even 1 = odd	00 = 5 01 = 6 10 = 7 11 = 8	

MR2A-D

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Channel Mode		Tx RTS Control	CTS Enable Tx	Stop Bit Length*			
00 = Normal 01 = Auto Echo 10 = Local Loop 11 = Remote Loop		0 = no 1 = yes	0 = no 1 = yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

*Add 0.5 to values shown for 0-7 if channel is programmed for 5 bits/character.

CSRA-D

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Receiver Clock Select				Transmitter Clock Select			
See Table 3				See Table 3			

CRA-D

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Miscellaneous Commands				Disable Tx	Enable Tx	Disable Rx	Enable Rx
See Text				0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

SRA-D

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Received Break	Framing Error	Parity Error	Overrun Error	TXEMT	TXRDY	FFULL	RXRDY
0 = no 1 = yes *	0 = no 1 = yes *	0 = no 1 = yes *	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

*These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits (7:5) from the top of the FIFO together with bits 4:0. These bits are cleared by a 'reset error status' command. In character mode they are discarded when the corresponding data character is read from the FIFO.

OPCR1,2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OP7/OP15	OP6/OP14	OP5/OP13	OP4/OP12	OP3/OP11		OP2/OP10	
0 = OPR[7/15] 1=TXRDYB/D	0 = OPR[6/14] 1=TXRDYA/C	0 = OPR[5/13] 1 = RXRDY/ FFULLB/D	0 = OPR[4/12] 1 = RXRDY/ FFULLA/C	00 = OPR[3/11] 01 = C/T Output 10 = TxCB/D(1X) 11 = RxCB/D(1X)		00 = OPR[2/10] 01 = TXCA/C(16X) 10 = TXCA/C(1X) 11 = RXCA/C(1X)	

ACR1,2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BRG Set Select	Counter/Timer Mode and Source			Delta IP3/IP11	Delta IP2/IP10	Delta IP1/IP9	Delta IP0/IP8 Int
0 = Set1 1 = Set2	See Table 6			0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

TABLE 2. REGISTER BIT FORMATS (continued)

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IPCR1,2	Delta IP3/IP11 0 = No 1 = Yes	Delta IP2/IP10 0 = No 1 = Yes	Delta IP1/IP9 0 = No 1 = Yes	Delta IP0/IP8 0 = No 1 = Yes	IP3 IP11 0 = Low 1 = High	IP2 IP10 0 = Low 1 = High	IP1 IP9 0 = Low 1 = High	IP0 IP8 0 = Low 1 = High

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ISR1,2	Input Port Change 1, 2 0 = No 1 = Yes	Delta Break B/D 0 = No 1 = Yes	RXRDY/ FFULLB/D 0 = No 1 = Yes	TXRDYB/D 0 = No 1 = Yes	Counter Ready 1, 2 0 = No 1 = Yes	Delta Break A/C 0 = No 1 = Yes	RXRDY/ FFULLA/C 0 = No 1 = Yes	TXRDYA/C 0 = No 1 = Yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IMR1,2	Input Port Change Int 1, 2 0 = Off 1 = On	Delta Break B/D Int 0 = Off 1 = On	RXRDY/ FFULLB/D Int 0 = Off 1 = On	TXRDYB/D Int 0 = Off 1 = On	Counter Ready Int 1, 2 0 = Off 1 = On	Delta Break A/C Int 0 = Off 1 = On	RXRDY/ FFULLA/C Int 0 = Off 1 = On	TXRDYA/C Int 0 = Off 1 = On

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTU1,2	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTUR1,2								

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTL1,2	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTLR1,2								

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IVR1,2	IVR[7]	IVR[6]	IVR[5]	IVR[4]	IVR[3]	IVR[2]	IVR[1]	IVR[0]

PROGRAMMING

Operation of the QUART is programmed by writing control words into the appropriate registers, while operational feedback is provided by status registers which can be read by the CPU. Register addressing is shown in Table 1.

A hardware reset clears the contents of SRA, SRB, IMR, ISR, OPR and OPCR and initializes the IVR to 0FH. During operation, care should be exercised if the contents of control registers are to be changed, since certain changes may result in improper operation. For example, changing the number of bits per character while data is being received may result in reception of an erroneous character. In general, changes to registers which control receiver or transmitter operation should be made only while the transmitter or receiver are disabled, and certain changes to the ACR should be made only when the C/T is stopped.

Mode, command, clock select, and status registers are duplicated for each channel to provide totally independent operation. Table 2 illustrates the bit assignments for each register.

Note: In the descriptions which follow, registers which are duplicated for each channel are described generically. References to input and output pins and control and status bits and registers apply to each channel unless otherwise noted.

MODE REGISTER 1 (Channels A - D)

MR1 for each channel is accessed when the channel's MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command invoked via the channel's command register. After reading or writing MR1, the pointer will point to MR2.

MR1(7) - Receiver Request-to-Send Control

This bit controls the negation of the RTSN output (OP0 for channel A, OP1 for channel B, OP8 for channel C and OP9 for channel D) by the receiver. RTSN is normally asserted by setting the respective output bit (OP 1/2/8/9 for channels A/B/C/D), and negated by resetting the same bit. MR1(7) = 1 causes RTSN to be negated automatically upon receipt of a valid start bit if the channel's FIFO is full and to be re-asserted again when an empty FIFO position becomes available. This flow control feature can be used to prevent overrun of the receiver by using the RTSN output to control transmission of characters to the QUART.

MR1(6) - Receiver Interrupt Select

This bit selects either the RXRDY status bit or the FFULL status bit of the channel to be used for CPU interrupts. It also causes the selected bit to be output on OP4 channel A, OP5 channel B, OP12 channel C or OP13 channel D.

MR1(5) - Error Mode Select

This bit controls the operation of the three FIFO status bits (PE, FE, received break) for the channel. In the character mode these status bits apply only to the character currently at the top of the FIFO. In the block mode these bits are the cumulative logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command for the channel was issued.

MR1(4:3) - Parity Mode Select

If 'with parity' or 'force parity' operation is programmed, a parity bit is added to the transmitted characters and the receiver performs a parity check on received characters. See OPERATION section for description of multidrop mode operation.

MR1(2) - Parity Type Select

This bit selects odd or even parity if 'with parity' mode is programmed and the state of the forced parity bit if the 'force parity' mode is programmed. In the multidrop mode it selects the state of the A/D flag bit. This bit has no effect if 'no parity' mode is programmed.

MR1(1:0) - Bits per Character Select

Selects the number of bits to be transmitted and received in the data field of the character. This does not include start, parity and stop bits

MODE REGISTER 2 (Channels A-D)

MR2 for each channel is accessed when the channel's MR pointer points to MR2, which occurs after any access to the channel's MR1. Reading or writing MR2 does not change the pointer.

MR2(7:6) - Channel Mode Select

Each channel can operate in one of four modes. MR2(7:6) = 00 in the normal mode where the receiver and transmitter operate independently.

MR2(7:6) = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions apply while in this mode:

1. Received data is transmitted on the channel's TXD output.

2. The receiver must be enabled but the transmitter need not be enabled.

3. The channel's TXRDY and TXEMT status bits are inactive.

4. The received parity is checked but is not regenerated for transmission. Thus, transmitted parity is as received.

5. Character framing is checked but the stop bits are transmitted as received.

6. A received break is echoed as received until the next valid start bit is detected.

7. CPU to receiver communications operate normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured.

The first is the local loopback mode, selected by MR2(7:6) = 10. In this mode:

1. The transmitter output is internally connected to the receiver input.

2. The transmit clock is used for the receiver.

3. The channel's TXD output is held marking (high).

4. The channel's RXD input is ignored.

5. The transmitter is enabled, but the receiver need not be enabled.

6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2(7:6) = 11. In this mode:

1. Received data is transmitted on the channel's TXD output.

2. Received data is not sent to the CPU and the error status conditions are not checked.

3. Parity and framing (stop bits) are transmitted as received.

4. The receiver must be enabled.

5. A received break is echoed as received until the next valid start bit is detected.

Care must be taken when switching into and out of the various modes. The selected mode will be activated immediately after it is programmed even if this occurs in the middle of transmitting or receiving a character. An exception to this is switching out of autoecho or remote loopback modes: if this deselection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RXRDY), and the transmitter is enabled, the transmitter will remain in autoecho or remote loopback mode until one entire stop bit has been transmitted.

MR2(5) - Transmitter Request-to-Send Control

This bit controls the negation of the RTSN output (OP0 for channel A, OP1 for channel B, OP8 for channel C and OP9 for channel D) by the transmitter. RTSN is normally asserted by setting the respective output port bits (OP1/2/8/9 for channels A/B/C/D) and negated by resetting the same bit. MR2(5) = 1 causes OP1/2/8 or 9 to be reset automatically one bit time after the characters in the channel's transmit shift register and THR, if any, are completely transmitted, including the programmed number of stop bit, if the transmitter has been disabled. This feature can be used to automatically negate RTSN at the conclusion of a message as follows:

1. Program auto-reset mode (MR2[5] =1).

2. Enable transmitter and assert the channel's RTSN output by setting the appropriate bit in the output port register.

3. Send message.

4. Disable the transmitter after the last character of the message is loaded into the THR.

MR2(4) - Clear-to-Send Control

If this bit is a 0, the channels CTSN input (IP0 for channel A, IP1 for channel B, IP8 for channel C and IP9 for channel D) has no effect on the transmitter. If the bit is a 1, the transmitter checks the state of its CTSN each time it is ready to send a character. If CTSN is low, the character is transmitted. If CTSN is high, TXD remains in the marking state and the transmission of the next character is delayed until CTSN goes low. Changes in CTSN while a character is being serialized do not affect transmission of that character.

MR2(3:0) - Stop Bit Length

This field programs the duration of the stop bit appended to each transmitted character. Stop bit durations of 9/16 to 1 bit time a 1-9/16 to 2 bit times, in increments of 1/16 bit, can be programmed for character lengths of 6, 7 and 8 bits. For a 5-bit character, the stop bit duration can be programmed from 1-1/16 to 2 bit times.

If an external 1x clock is programmed for the transmitter, MR2(3) = 0 selects a stop bit duration of one bit time and MR2(3) = 1 selects a duration of two bit times for transmission.

The receiver only checks for mark condition at the center of the first stop bit (that is, one bit time after the last data or parity bit is sampled) regardless of the programmed transmitted stop bit length.

CLOCK SELECT REGISTER (Channels A-D)

CSR (7:4) and CSR (3:0) of each channel operate in conjunction with ACR(7) and the channel's set/clear BRG select extend' commands to allow independent selection of the bit rates for the receiver and transmitter respectively. The BRG can generate 33 different bit rates, of which 22 is selected by programming ACR(7). The bit rates generated when using a 3.6864 MHz crystal or an external clock of the same frequency are shown in Table 3A, where 'X' refers to the current state of the extend bit (see CR [7:4] selection). Note that the actual outputs from the BRG are at 16x the bit rates shown in the table.

COMMAND REGISTER (Channels A-D)

Each channel of the QUART has a command register used to supply commands to the respective channel. Multiple commands may be invoked simultaneously by a single write to the command register as long as the commands are non-conflicting.

CR(7:4) - Miscellaneous Commands

The encoded value of this field specifies a single command as follows:

0 0 0 0 - Null Command.

0 0 0 1 - Reset MR Pointer - causes the channel's MR pointer to point to MR1.

0 0 1 0 - Reset Receiver - reset the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.

0 0 1 1 - Reset Transmitter - resets the transmitter as if a hardware reset had been applied. The TXD output is forced to a high level.

0 1 0 0 - Reset Error Status - clears the received break (RB), parity error (PE), framing error (FE) and overrun error (OE) status bits, SR(7:3). Used in character mode to clear the OE status bit (although the RB, PE, and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.

0 1 0 1 - Reset Break Change Interrupt - clears the channel's break change interrupt status bit.

TABLE 3A CSR [7:4] / [3:0] Bit Rate Selection (3.686 MHz)

Field	Bit Rate			
CSR[7:4]	ACR[7] = 0		ACR[7] = 1	
CSR[3:0]	X = 0	X = 1	X = 0	X = 1
0 0 0 0	50	75	75	50
0 0 0 1	110	110	110	110
0 0 1 0	134.5	134.5	134.5	134.5
0 0 1 1	200	150	150	200
0 1 0 0	300	3600	300	3600
0 1 0 1	600	14.4K	600	14.4K
0 1 1 0	1200	28.8K	1200	28.8K
0 1 1 1	1050	57.6K	2000	57.6K
1 0 0 0	2400	115.2K	2400	115.2K
1 0 0 1	4800	4800	4800	4800
1 0 1 0	7200	1800	1800	7200
1 0 1 1	9600	9600	9600	9600
1 1 0 0	38.4K	19.2K	19.2K	38.4K
1 1 0 1	Timer	Timer	Timer	Timer
1 1 1 0	EXT - 16x	EXT - 16x	EXT - 16x	EXT - 16x
1 1 1 1	EXT - 1x	EXT - 1x	EXT - 1x	EXT - 1x

TABLE 3B CSR [7:4] / [3:0] Bit Rate Selection (7.3728 MHz)

Field	Bit Rate			
CSR[7:4]	ACR[7] = 0		ACR[7] = 1	
CSR[3:0]	X = 0	X = 1	X = 0	X = 1
0 0 0 0	100	150	150	100
0 0 0 1	220	220	220	220
0 0 1 0	269	269	269	269
0 0 1 1	400	300	300	400
0 1 0 0	600	7200	600	7200
0 1 0 1	1200	28.8K	1200	28.8K
0 1 1 0	2400	57.6K	2400	57.6K
0 1 1 1	2100	115.2K	4000	115.2K
1 0 0 0	4800	230.4K	4800	230.4K
1 0 0 1	9600	9600	9600	9600
1 0 1 0	14.4K	3600	3600	14.4K
1 0 1 1	19.2K	19.2K	19.2K	19.2K
1 1 0 0	76.8K	38.4K	38.4K	76.8K
1 1 0 1	Timer	Timer	Timer	Timer
1 1 1 0	EXT - 16x	EXT - 16x	EXT - 16x	EXT - 16x
1 1 1 1	EXT - 1x	EXT - 1x	EXT - 1x	EXT - 1x

0 1 1 0 - Start Break - forces the TXD output low. The transmitter must be enabled to start a break. If the transmitter is empty, the start of the break may be delayed up to two bit times. If the transmitter is active, the break begins when the transmission of that character in the THR is completed, viz., TXEMT must be true before the break will begin.

0 1 1 1 - Stop Break - the TXD line will go high within two bit times. TXD will remain high for one bit time before the next character, if any, is transmitted.

1 0 0 0 - Set Rx BRG Select Extend Bit - sets the receiver BRG select extend bit for the channel to 1.

1 0 0 1 - Clear Rx BRG Select Extend Bit - clears the receiver BRG select extend bit for the channel to 0.

1 0 1 0 - Set Tx BRG Select Extended Bit - sets the transmitter BRG select extend bit for the channel to 1.

1 0 1 1 - Clear Tx BRG Select Extend Bit - clears the transmitter BRG select extend bit for the channel to 0.

1 1 0 0 - Set Standby Mode (Channel A) Reset IUS Latch (Channel B) and Select Direct Systems Clock (Channel C) - when this command is invoked via the channel A command register, power is removed from the transmitters, receivers, counter/timer and additional circuits to place the QUART in the standby mode. Normal operation is restored by a hardware reset or by invoking the 'set active mode' command.

When this command is invoked via the channel B command register, and the QUART (88 Mode) is operating in Z-mode, it causes the interrupt-under-service latch to be reset.

When this command is invoked via the channel C command register, the QUART will generate its internal system clock and take a direct crystal or TTL clock signal to generate a set of standard baud rates described in Table 3A.

1 1 0 1 - Set Active Mode (Channel A) Set Z-mode (Channel B) and Select Divided System Clock (Channel C) - when this command is invoked via the channel A command register the QUART is removed from the stand-by mode and resumes normal operation.

When this command is invoked via the channel B command register, the QUART is conditioned to operate in the Z-mode. This applies only in the 88 mode.

When this command is invoked via the channel C command register, the QUART is set to generate internal system clock after dividing the external clock input frequency by two. In this mode an external 7.3728 MHz clock may be used.

1 1 1 0 - Set Special MR Pointer - this single command, invoked through channel A of the QUART, sets a special pointer which points to all 4 shadow mode registers simultaneously.

1 1 1 1 - Reset Special MR Pointer - this command resets the special mode register pointer and enables access to the normal mode registers.

Note: When writing 'O4H' at the mode register address of the selected channel, this value is written into the selected shadow mode register since the normal mode register address are disabled by the special pointer. In this step the TXFIFO mode bit (bit 2) is set. This procedure can be executed regardless of the state of the normal mode register pointer whose value stays intact throughout the procedure. Note also that the TXFIFO can be activated independently for each channel of the QUART. The lowest two bits (bits 0 and 1) of the shadow mode register are reserved for factory testing and must never be set to 1's.

CR[3] - Disable Transmitter

This command terminates operation of the channel's transmitter and resets the TXRDY and TXEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before going into the inactive state.

CR[2] - Enable Transmitter

This command enables operation of the channel's transmitter and asserts the TXRDY status bit.

CR[1] - Disable Receiver

This command immediately terminates operation of the channel's receiver. Any character being received will be lost. The command has no effect on the receiver status bits or on any other control registers. If the multidrop mode is programmed, the receiver operates even if it is disabled. See OPERATION section.

CR[0] - Enable Receiver

This command enables operation of the receiver. If not in the multidrop mode, it also forces the receiver to start searching for the start bit.

STATUS REGISTER (Channels A-D)

SR[7] - Received Break

This bit indicates that an all zero character of the programmed length was received without a stop bit. Only a single FIFO position is occupied when a break is received. Additional transfers into the FIFO are inhibited until the RXD line returns to the marking state for at least half a bit time. This is defined as two successive edges of the internal or external 1 x clock.

When this bit is set, the channel's change in break status bit in the ISR is set. The bit in the ISR is also set when the end of the break condition, as defined above, is detected.

The chip's break detect logic can detect breaks that begin in the middle of a character. However, the break must persist until the end of the next character time in order for it to be detected.

SR[6] - Framing Error

When set, this bit indicates that RXD was low when the stop bit of the character is the FIFO was sampled. The stop bit check is made in the middle of the first stop bit position (one bit time after sampling the last data bit or the parity bit at its midpoint) regardless of the stop bit length programmed.

SR[5] - Parity Error

This bit is set when the 'with parity' or 'force parity' modes are programmed if the corresponding character in the data FIFO was received with incorrect parity.

In the multidrop mode, this status bit indicates the state of received address/data (A/D) flag bit.

SR[4] - Overrun Error

If set, this bit indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its error status) is overwritten.

This bit is cleared by a 'reset error status' command.

TABLE 5. BIT RATE GENERATOR CHARACTERISTICS
Crystal or Clock Input = 3.6864 MHz or 7.3728 MHz

Nominal Rate (bps)	Actual Clock (KHz)	Error (Percent)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.26
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
3600	57.6	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
14.4K	230.4	0
19.2K	307.2	0
28.8K	460.8	0
38.4K	614.4	0
57.6	921.6	0
115.2K	1843.2	0

TABLE 6. ACR [6:4] FIELD DEFINITIONS

ACR [6:4]	Mode	Clock Source
0 0 0	Counter	External - IP2/10 Input
0 0 1	Counter	TXCA/C 1x Clock of Channel A/CTx
0 1 0	Counter	TXCB/D 1x Clock of Channel B/DTx
0 1 1	Counter	X1/CLK Input Divided by 16
1 0 0	Timer	External - IP2/10 Input
1 0 1	Timer	External Divided by 16 - IP2/10 Input
1 1 0	Timer	X1/CLK Input
1 1 1	Timer	X1/CLK Input Divided by 16

SR[3] - Transmitter Empty (TXEMT)

This bit is set when the transmitter underruns. It is set after transmission of the last stop bit of a character, if there is no character, the THR is awaiting transmission. It is reset when the THR is loaded by the CPU and when the transmitter is disabled.

SR[2] - Transmitter Ready (TXRDY)

This bit, when set, indicates that the THR is empty and ready to accept a character. The bit is cleared when the THR is loaded by the CPU and is set when that character is transferred to the transmit shift register. TXRDY is set when the transmitter is initially enabled and is reset when the transmitter is disabled. Characters loaded into the THR while the transmitter is disabled will not be transmitted.

SR[1] - FIFO Full (FFULL)

This bit is set when a character is transferred from the receive shift register to the FIFO and the transfer causes it to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SR[0] - Receiver Ready (RXRDY)

This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when a character is transferred from the receive shift register to the FIFO and reset when the CPU reads the last character currently stored in the FIFO.

OUTPUT PORT CONFIGURATION REGISTER (1, 2)

This register programs the output port to provide alternate functions. Note that when an output is programmed as an interrupt, it is not masked by the contents of the IMR.

OPCR [7/15] - OP7/OP15 Output Select

This bit programs the OP7/OP15 output to provide one of the following:

0 - The complement of OPR[7]/[15].

1 - The channel B/D transmitter interrupt TXRDY B/D which is the complement of SRB/D [2]. In this mode, OP7, and/or OP15 are open drain outputs.

OPCR [6/14] - OP6/OP14 Output Select

This bit programs the OP6/OP14 output to provide one of the following:

0 - The complement of OPR[6]/[14].

1 - The channel A/C transmitter interrupt output, TXRDY A/C which is the complement of SRA/C[2]. In this mode OP6/OP14 are open drain outputs.

OPCR [5/13] - OP5/OP13 Output Select

This bit programs the OP5/OP13 output to provide one of the following:

0 - The complement of OPR[5]/[13].

1 - The channel B/D receiver interrupt output, which is the complement of ISR[5]. In this mode OP5/OP13 are open drain outputs.

OPCR [4/12] - OP4/OP12 Output Select

This bit programs the OP4/OP12 output to provide one of the following:

0 - The complement of OPR[4]/ [12].

1- The channel A/C receiver interrupt output, which is the complement of ISR[5]. In this mode OP5/OP12 are open drain outputs.

OPCR[3:2] - OP3/OP12 Output Select

These bits program the OP3/OP11 output to provide one of the following:

00 - The complement of OPR[3]/[11].

01 - The counter/timer output, in which case OP3/OP11 is an open drain output. In the timer mode the output is a square wave at the programmed frequency. In counter mode the output remains high until the terminal count is reached, at which time it goes low. The output returns to the high state when the counter is stopped by a stop counter command.

10 - The 1x clock which shifts the output data for the channel B/D transmitter. A free running 1x clock is output if data is not being transmitted.

11 - The 1x clock which samples the input data for the channel B/D receiver. A free running 1x clock is output if data is not being received.

OPCR [1:0] - OP2/OP10 Output Select

These bits program the OP2/OP10 output to provide one of the following:

00 - The complement of OPR[2]/[10].

01 - The 16x clock selected for the channel A transmitter by CSRA/C[3:0]. This will be a 1x clock if external 1x clock is programmed.

10 - The 1x clock which shifts the output data for the channel A/C transmitter. A free running 1x clock is output if data is not being transmitted.

11 - The 1x clock which samples the input data for the channel A/C receiver. A free running clock is output if data is not being received.

AUXILIARY CONTROL REGISTER (1,2)

ACR[7] - Bit Rate Set Select

This bit selects one of two bit rates to be generated by the BRG. The bit rates provided are selected by the channel A through D receiver and transmitter as described in the Clock Select Register description. Bit rate generator characteristics are shown in Table 5.

ACR [6:4] - Counter/Timer Mode and Clock Source Select

This field selects the operating mode and clock source for the counter/timer. See Table 6.

ACR [3:0] - Change of State Interrupt Enables

These bits select which bits of the input port cause the input port change bit in the interrupt status register (ISR[7]) to be set. If one of these bits is 'on', the setting of the corresponding bit in the IPCR by a change of state on the input will set ISR[7], and will also cause the interrupt request pin to be asserted if IMR[7] is set. However, if the bit is 'off', the setting of the corresponding bit in the IPCR has no effect on ISR[7].

INPUT PORT CHANGE REGISTER (1,2)

IPCR [7:4] - IP0 - IP3, IP8 - IP11 Change of State

These bits are set when a change of state occurs at the respective input pins (see Input Port Section). The bits are cleared when the CPU reads the IPCR1,2.

The setting of these bits can be programmed to cause an interrupt to the CPU via ACR[3:0], ISR[7] and IMR[7].

IPCR [3:0] - IP3 - IP0, IP11 - IP8 Current State

These bits indicate the current state of the respective inputs at the time the IPCR is read.

INTERRUPT STATUS REGISTER

This register provides the current status of all possible interrupt conditions. If a bit in the ISR is a '1' and the corresponding bit in the interrupt mask register (IMR) is also a '1' the interrupt request output will be asserted. If the corresponding bit in the IMR is a '0' the state of the bit in the ISR has no effect on the interrupt request output. The contents of this register can be read by the CPU either unmasked or masked by the IMR. See Table 1.

ISR[7] - Input Port Change Status

This bit is a '1' when a change of state has occurred at the IP0 - IP3 or IP8 - IP11 inputs and that event has been programmed to cause an interrupt via ACR[3:0]. It is cleared when the CPU reads the IPCR.

ISR[6] - Channel B/D Receiver Ready or FIFO Full

This bit indicates that the channel B or D receiver has detected the beginning or end of a received break. It is reset when the CPU invokes a channel B/D 'reset break change interrupt' command.

ISR[5] - Channel B/D Receiver Ready or FIFO Full

The function of this bit is programmed by MR1B/D[6]. If programmed as receiver ready, it indicates that data is in the FIFO. It is set when a character is transferred from the receive shift register to the FIFO and cleared when the CPU reads the RHR. If there are still more characters in the FIFO after the read operation, the bit will be set again after the FIFO is 'popped.'

If this bit is programmed as FIFO full, it is set when a character is transferred from the receive shift register to the FIFO and the transfer causes the FIFO to become full. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, this bit will be set again after the read operation, when that character is loaded into the FIFO.

ISR[4] - Channel B/D Transmitter Ready

This bit is a duplicate of TXRDYB/D, SRB/D[2]

ISR[3] - Counter Ready

In the counter mode, this bit is set when the counter reaches the terminal count and is reset when the counter is stopped by a 'stop counter' command. The command, however, does not stop the C/T.

ISR[2] - Channel A/C Change in Break

This bit indicates that the channel A/C receiver has detected the beginning or end of a received break. It is reset when the CPU invokes a channel A/C 'reset break change interrupt' command.

ISR[1] - Channel A/C Receiver Ready or FIFO Full

The function of this bit is programmed by MR1A/C[6]. If programmed as receiver ready, it indicates that data is in the FIFO. It is set when a character is transferred from the receive shift register to the FIFO and cleared when the CPU reads the RHR. If there are still more characters in the FIFO after the read operation, the bit

will be set again after the FIFO is 'popped.'

If this bit is programmed as FIFO full, it is set when a character is transferred from the receive shift register to the FIFO and the transfer causes the FIFO to become full. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, this bit will be set again after the read operation, when that character is loaded into the FIFO.

ISR[0] - Channel A/C Transmitter Ready

This bit is a duplicate of TXRDYA/C, SRA/C(2).

INTERRUPT MASK REGISTER (1,2)

This register selects which bits in the ISR cause an interrupt to be asserted. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the interrupt request output will be asserted. If the corresponding bit in the IMR is a '0', the state of the bit in the ISR has no effect on the interrupt request output. Note that the IMR does not mask the programmable interrupt outputs, OP3-OP7 and OP11-OP15.

COUNTER/TIMER REGISTERS (CTUR/CTLR)

The CTUR and CTLR hold the eight MSBs and eight LSBs respectively of the value to be used in the counter/timer in both of its modes of operation. The minimum value which may be loaded into CTUR/CTLR is 0001H.

INTERRUPT VECTOR REGISTER (1,2)

The IVR holds the value which the QUART places on the data bus in response to assertion of the interrupt acknowledge input. In the 88 mode the register is not used for any function when the device operates in I-mode but remains writable and readable by the CPU, and can be used for any purpose. The contents of this register are initialized to OFH by a hardware reset.

The following is a list of features which have been modified or enhanced over the DUART.

1). IEI, IEO and IACK are separate pins, no longer shared with IP4, IP5 and IP6.

2). Address A4/A5 has been added to provide additional internal registers.

3). Two additional inputs have been provided IP7 and IP15.

4). Reset input is debounced for Min of 20 n sec (Min).

5). The QUART is designed to operate with 7.3728 MHz crystal or an external TTL level clock.

6). Buffered system clock is provided to drive additional external logics(bonding option).

7). Since the interrupt is prioritized, channel A has highest priority and channel D has lowest priority. This determines the order of interrupt vector response on interrupt acknowledge cycles.

8). The QUART has a three byte FIFO stack behind the Transmit Hold Register in each channel. After a system reset or when coming out of standby mode, only the THR1 is accessible. This maintains DUART compatibility. The transmitter FIFO can be activated via commands in the Command Register A. Following steps are required to set additional FIFO's for each transmitter. Each channel in the QUART contains a shadow mode register, writing "E0" in the command register A will enable the shadow mode registers (A - D). Writing "04" in each channel will enable the additional FIFO registers, by writing "F0" in the command register A will exit the shadow mode.

NOTES:

1. Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the Electrical Characteristics section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltage larger than the rated maxima.
3. Parameters are valid over the specified temperature and operating supply ranges. Typical values are at 25°C, V_{CC} = 5V and typical processing parameters.
4. All voltages are referenced to ground (GND). For testing, input signal levels are 0.4V and2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate. See Figure 3.
5. Measured operation with a OR7.3MHz crystal and with all outputs open.
6. AC test condition for outputs: C_L = 50pF, R_L = 2.7K ohm to V_{CC}.
7. For the 88 mode, timing is illustrated and referenced to the RDN and WRN inputs. The device may also be operated using CEN as the 'strobing' input. In this case; all specifications apply referenced to the falling and rising edges of CEN.
8. If CEN is used as the strobing input, this parameter defines the minimum high time between CENs.
9. Consecutive write operations to the same register require at least three edges of the X1 clock between writes.
10. This parameter is system dependent. For any QUART in the daisy chain, t_{IAS} must be greater than the sum of t_{EOD} for the highest priority device in the daisy chain, t_{EIS} for the QUART, and t_{DIO} for each device separating them in the daisy chain.
11. This specification imposes a 6MHz maximum 68000 clock frequency if a read or write cycle follows immediately after the previous read or write cycle. A higher 68000 clock can be used if this is not he case.
12. This specification imposes a lower bound on CSN and IACKN low, guaranteeing that they will be low for at least one CLK period.
13. The minimum high time must be at least 1.5 times the X1/CLK period and the minimum low time must be at least equal to the X1/CLK period if either channel's R_X is operation in external 1x clock mode.
14. For prime grade N, P, J, L, M, ML, V_{CC} = 5V±10%.

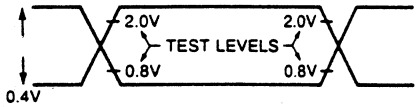


Figure 3. Input and Output levels for Timing Measurements

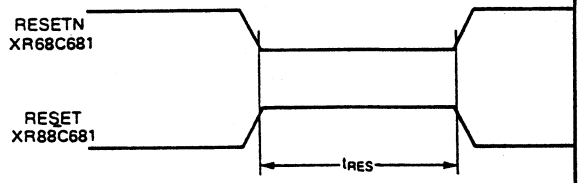


Figure 4. Reset Timing

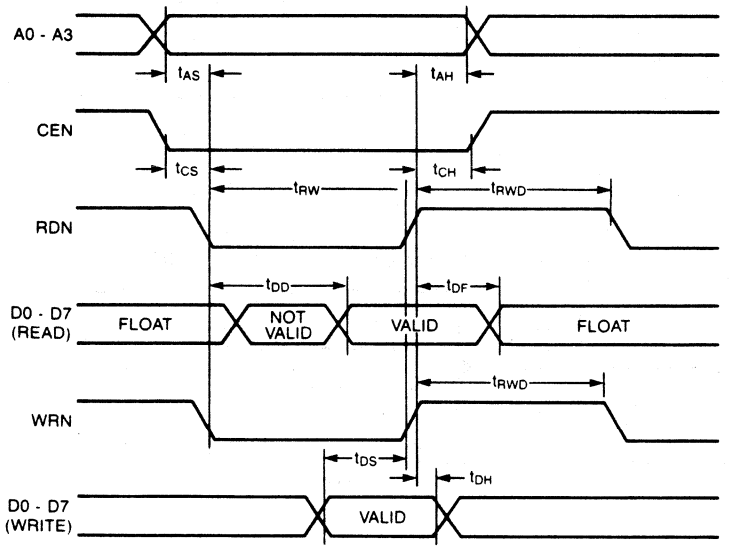


Figure 5. XR 82C684 Read and Write Cycle Timing (88 Mode)

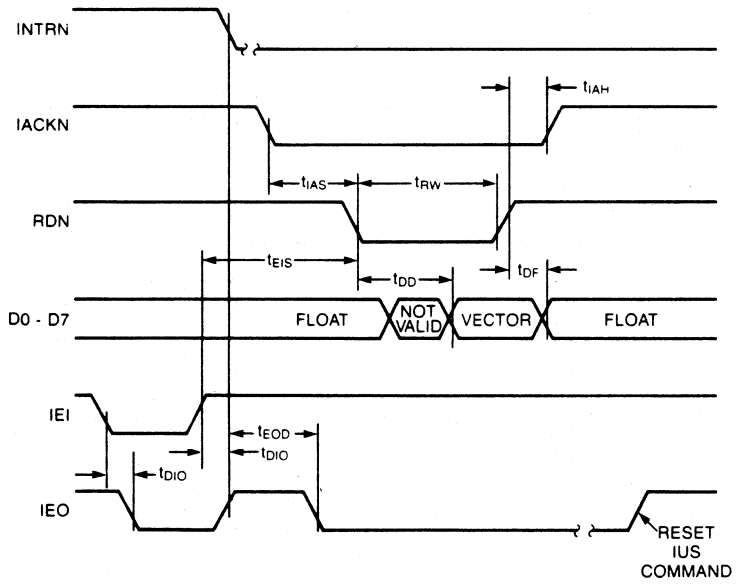


Figure 6. XR 82C684 Z Mode Interrupt Cycle Timing (88Mode)

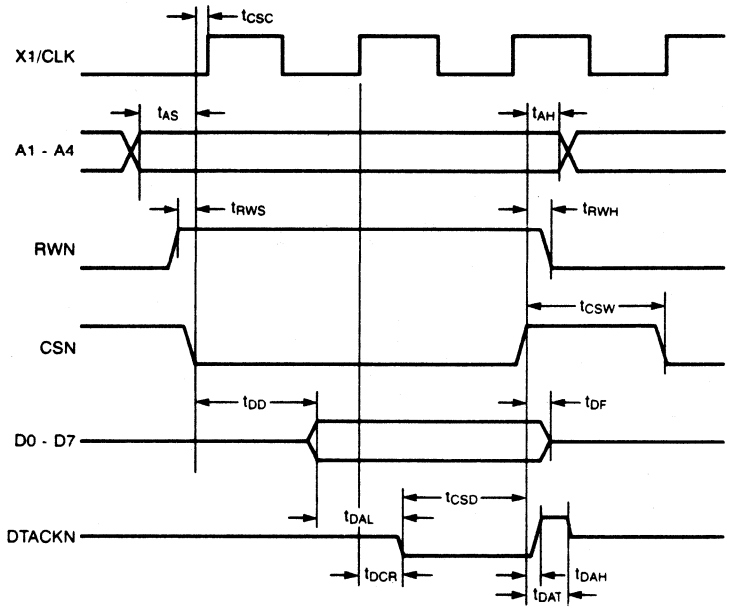


Figure 7. XR 82C684 Read Cycle Timing (68 Mode)

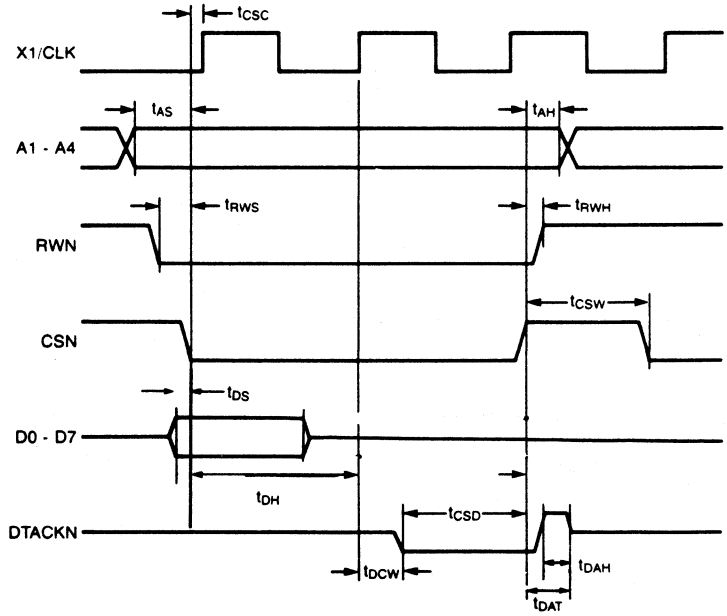


Figure 8. XR 82C684 Write Cycle Timing (68 Mode)

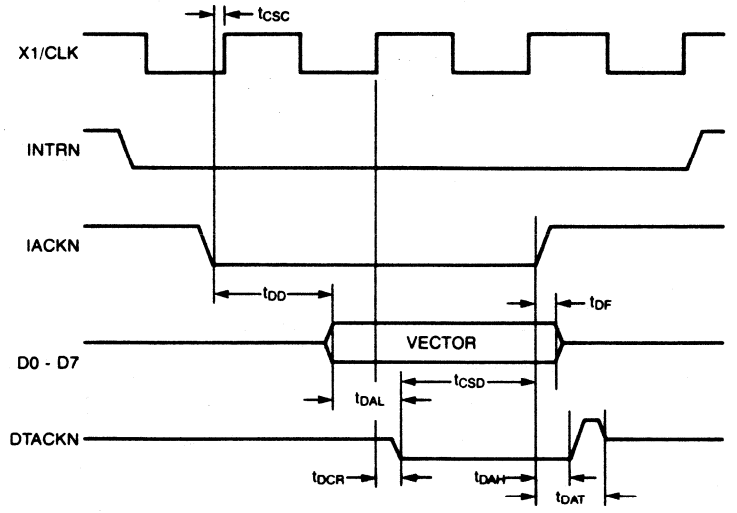


Figure 9. XR 82C684 Interrupt Cycle Timing (68 Mode)

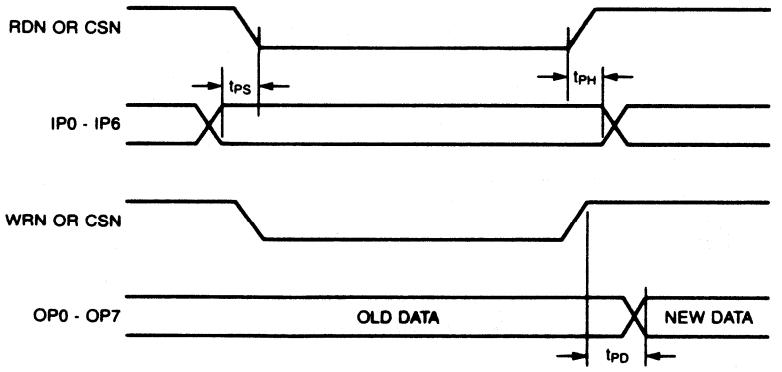
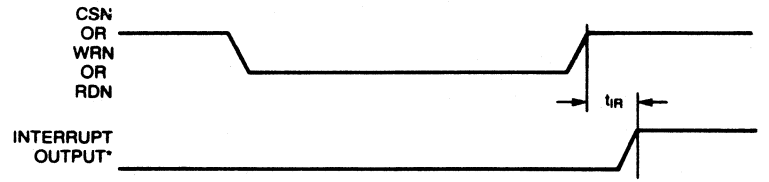


Figure 10. Port Timing



*INTRN or OP3 - OP7 when used as interrupt outputs.

Figure 11. Interrupt Timing

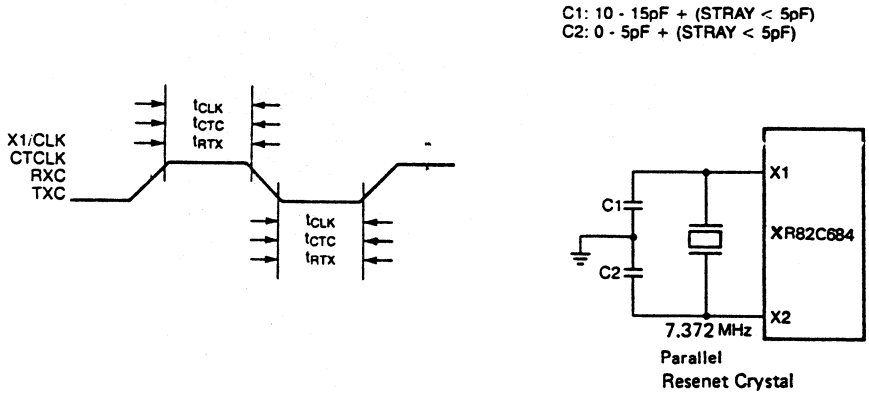


Figure 12. Clock Timing

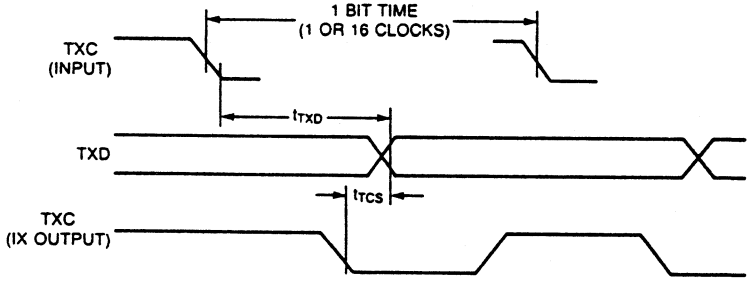


Figure 13. Transmitter Timing

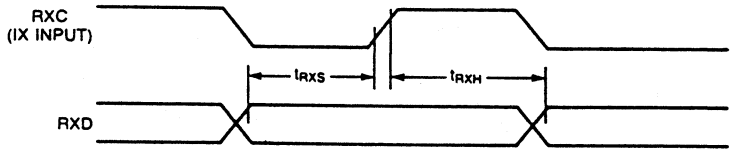


Figure 14. Receiver Timing

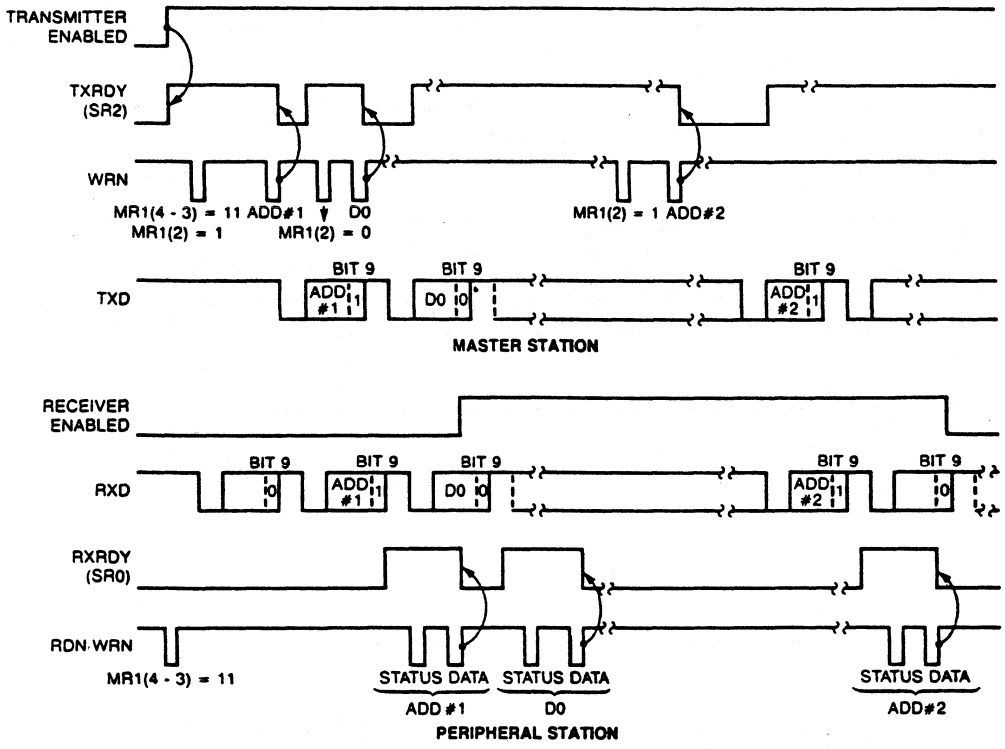
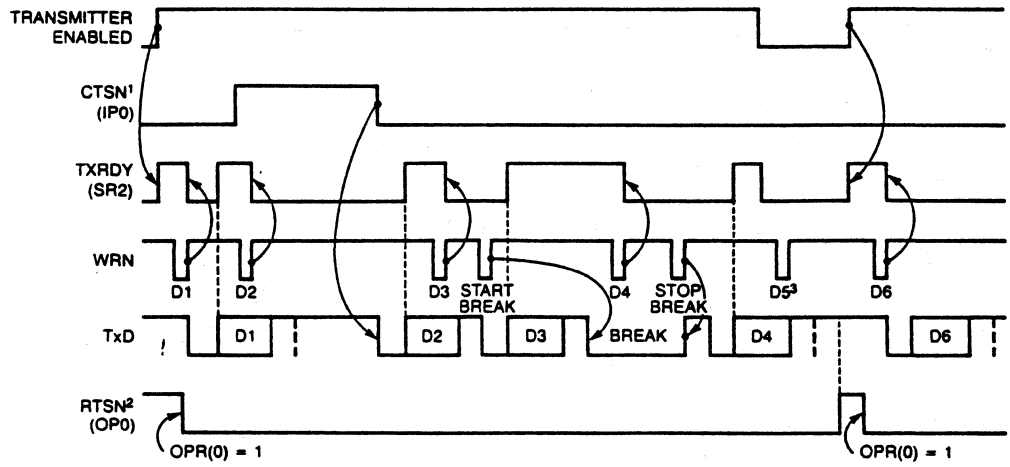
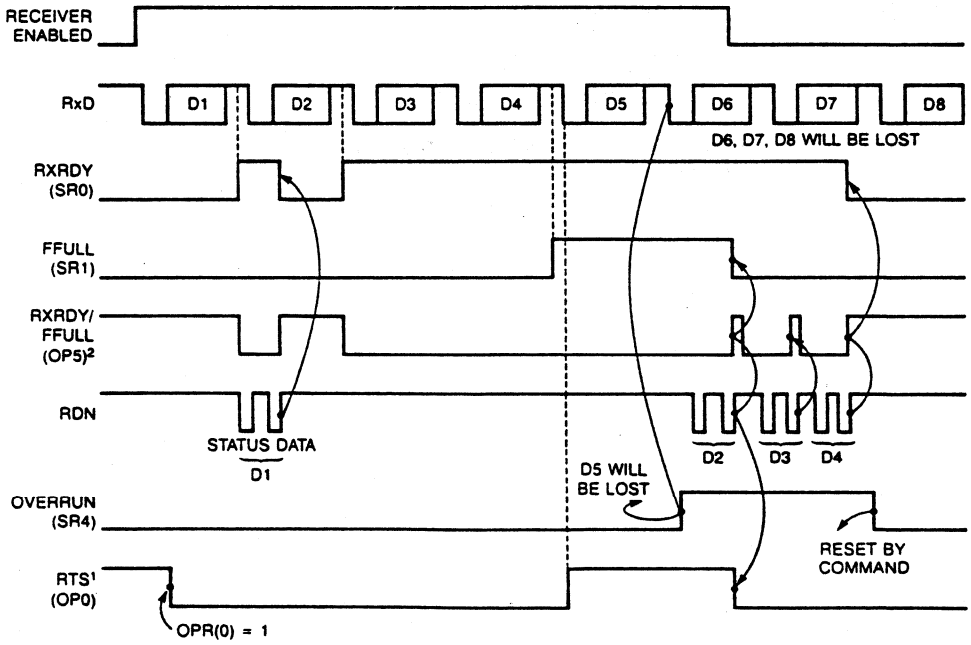


Figure 17. Transmitter and Receiver Operation in Multidrop Mode.



NOTES
1. Operation shown for MR2(4) = 1
2. Operation shown for MR2(5) = 1
3. D5 will not be transmitted

Figure 15. Transmitter Operation



NOTES
1. Operation shown for MR1(7) = 1
2. Shown for OPCR(4) = 1 and MR1(6) = 0

Figure 16. Receiver Operation

Parallel CMOS First-In/First-Out

GENERAL DESCRIPTION

The XR-T7201/2/3 are dual port memories which operate in a 'first-in-first-out' basis. Complementary to this particular algorithm, this devices use full and empty flags to prevent under and/or over flow and also an expansion logic to allow memory expansion in word size and depth. They are fabricated using a high speed 1.25 micron technology and are designed for applications requiring sourcing and absorption of data at different data rates (fast processors interfacing to slower peripherals for example).

Data is internally manipulated through ring pointers to avoid the use of address information to load and unload data. To toggle the bits in and out of the device, the WRITE (W) and the READ (R) pins are used (typical read/write cycle time = 50ns @ 12MHz).

A 9 bit wide data array, which is particularly useful in data communication applications, allows for control of the ninth bit which is used for parity and error checking of transmitted data bytes. Another useful feature is the RETRANSMIT (RT) option which resets the read pointer to its initial position and allows retransmission from the beginning of the data. The flag logic provides a mechanism to control over or underflow conditions and the expansion logic allows several devices to expand in word size and depth.

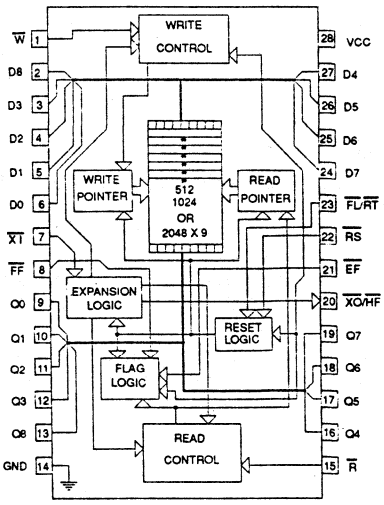
FEATURES

First In First Out Dual Port Memory
Organization: * 512 X 9 (XR-T7201)
* 1024 X 9 (XR-T7202)
* 2048 X 9 (XR-T7203)
Very Low Power Consumption
Ultra High Speed Cycle Time (typ 45ns)
Asynchronous and Simultaneous Read and Write
Expandable by Word Width and Depth
Empty and Full Warning Flags
Auto Retransmit Capability
High Speed 1.25 Micron CMOS Technology
Functionally and Pin Compatible to IDT7201-3 and Mostek MK4501-3

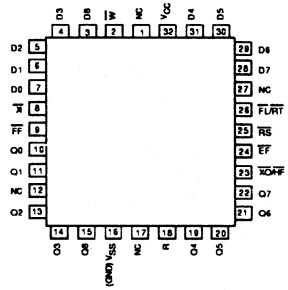
APPLICATIONS

Master / Slave Multiprocessing Applications
Bidirectional and Buffer Applications

PIN ASSIGNMENT



CP, IP PACKAGES



CJ, IJ PACKAGES

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to 150°C
Supply Voltage	-0.5V to 7V
Supply Voltage Surge (10ms)	+25V
Power Dissipation	1.0W
DC Output Current	50mA

Note: Stresses exceeding the ones specified above may cause permanent damage to the device or reliability problems.

ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-T7201	CP (Plastic)	0°C to 70°C
XR-T7201	CJ (LCC)	0°C to 70°C
XR-T7201	IP (Plastic)	-40°C to +85°C
XR-T7201	IJ (LCC)	-40°C to +85°C
XR-T7202	CP (Plastic)	0°C to 70°C
XR-T7202	CJ (LCC)	0°C to 70°C
XR-T7202	IP (Plastic)	-40°C to +85°C
XR-T7202	IJ (LCC)	-40°C to +85°C
XR-T7203	CP (Plastic)	0°C to 70°C
XR-T7203	CJ (LCC)	0°C to 70°C
XR-T7203	IP (Plastic)	-40°C to +55°C
XR-T7203	IJ (LCC)	-40°C to +55°C

* Note: Available access time = 35, 50, 65, 80, 120.
Access time designator follows package information.
Example order: XR-T7202CP-50

DC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V +/- 10%, Ta = 0°C to 70°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage Current	-1		1	µA	$0.4<V_{IN}< V_{CC}$
V_{OL}	Output Leakage Current	-10			µA	Note 1
V_{OH}	Output "Logic 1"	2.4			V	I OUT = -1mA
V_{OL}	Output "Logic 0"			0.4	V	I OUT = 4mA
I_{CC}	Average Supply Current		80		mA	Note 2
I_{CC}	Average Standby Current		8		mA	Note 2
I_{CC}	Power Down Current			500	µA	Note 2

NOTE 1) R> V_{IH}, 0.4 < V_{OUT} < V_{CC}
2) ICC Measurements are made with outputs open.

AC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC = 5V +/- 10%, Ta = 0°C to 70°C
Input Pulse Level = GND to 3.0V
Input Rise and Fall Time = 5ns
Input Timing Reference Level = 1.5V
Output Reference Level = 1.5V

		Ta = 35ns		Ta = 50ns		Ta = 65ns		Ta = 80ns		Ta = 120ns		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t RC	Read Cycle Time	45	-	65	-	80	-	100	-	140	-	ns
t A	Access Time	-	35	-	50	-	65	-	80	-	120	ns
t RR	Read Recovery Time	10	-	15	-	15	-	20	-	20	-	ns
t RPW	Read Pulse Width	35	-	50	-	65	-	80	-	120	-	ns
t RLZ	Read Pulse Low to Data Bus at Low Z	5	-	10	-	10	-	10	-	10	-	ns
t WLZ	Write Pulse High to Data Bus at Low Z	10	-	15	-	15	-	15	-	15	-	ns
t DV	Data Valid from Read Pulse High	5	-	5	-	5	-	5	-	5	-	ns
t RHZ	Read Pulse High to Data Bus at High Z	-	20	-	30	-	30	-	30	-	30	ns
t WC	Write Cycle Time	45	-	65	-	80	-	100	-	140	-	ns
t WPW	Write Pulse Width	35	-	50	-	65	-	80	-	120	-	ns
t WR	Write Recovery Time	10	-	15	-	15	-	20	-	20	-	ns
t DS	Data Setup Time	18	-	30	-	30	-	40	-	40	-	ns
t DH	Data Hold Time	0	-	5	-	10	-	10	-	10	-	ns
t RSC	Reset Cycle Time	45	-	65	-	80	-	100	-	140	-	ns
t RS	Reset Pulse Width	35	-	50	-	65	-	80	-	120	-	ns
t RSR	Reset Recovery Time	10	-	15	-	15	-	20	-	20	-	ns
t RTC	Retransmit Cycle	45	-	65	-	80	-	100	-	140	-	ns
tRT	Retransmit Pulse W.	35	-	50	-	65	-	80	-	120	-	ns
tRTR	Retransmit Recovery	10	-1	15	-	15	-	20	-	20	-	ns
tEFL	Reset to EF Low	-	45	-	65	-	80	-	100	-	1	
tREF	Read Low to EF Low	-	30	-	45	-	60	-	70	-		
t RFF	Read High to FF Low	-	30	-	45	-	60	-	70	-	110	ns
t WEF	Write High to EF High	-	30	-	45	-	60	-	70	-	110	ns
t WFF	Write Low to FF Low	30	-	-	45	-	60	-	70	-	110	ns
t WHF	Write Low to HF Low	-	45	-	65	-	80	-	100	-	140	ns
t RHF	Read High to HF High	-	45	-	65	-	80	-	100	-	140	ns

Note: 1) Timing referenced as in AC Test Conditions.
2) Pulse widths less than minimum are not allowed.
3) Values guaranteed by design, not currently tested.

PIN#	MNEMONIC	DESCRIPTION
1	$\overline{W}$	(Active Low) **WRITE ENABLE** A falling edge on this pin initiates a write cycle provided the FF Flag (FIFO Full) is not set. Timing, such as hold and set-up requirements are measured with respect to the rising edge of this pin.
2-6 24-27	D0-D8	**DATA INPUT**. Data is loaded into the FIFO sequentially and is totally independent of any read operations.
7	$\overline{XI}$	(Active Low) **EXPANSION INDICATOR** pin. When grounded, the single device mode is selected. When connected to XO (Expansion Out), the device is configured in the Depth Expansion or Daisy Chain Mode.
8	$\overline{FF}$	(Active Low) **FULL FLAG**. This pin will go low when the write pointer is one location away from the read pointer and inhibit any further write operations to the device. This is done to prevent data overflow. Upon completion of a read operation the $\overline{FF}$ will go high after tRFF, and a valid write can begin.
9-13 16-19	Q0-Q8	**DATA OUTPUTS**. Data is read from the FIFO whenever the Read Enable line goes low and the $\overline{EF}$ Flag is not set. After reading the data outputs they return to a high impedance state until the next Read operation.
14	GND	**POWER GROUND**
15	$\overline{R}$	(Active Low) **READ ENABLE**. A read operation is initiated on the falling edge of the Read Enable Control, provided the Empty Flag is not set. Data is accessed on a First-In-First-Out basis and is totally independent of any Write operation. At the completion of the Read Cycle the outputs return to a high impedance state until the next read operation.
20	$\overline{XO/HF}$	(Active Low) **EXPANSION OUT/HALF FULL**. This is a dual purpose pin whose functions are: (1) When using this device in the Multiple Device mode, XI (Expansion In) is connected to XO (Expansion Out). This way the output generates a signal to alert the next device in the Daisy Chain that the previous device has reached the last location of memory. (2) When using this device in the single device mode, XI (Expansion In) is grounded and the output acts as an indication of a half full memory. The Half Full Flag will be set to low and remain set until the difference between the write pointer and the read pointer is less than or equal to half the total memory of the device. This flag will be set at the half way point on the falling edge of the Write operation and reset by the rising edge of the Read operation.
21	$\overline{EF}$	(Active Low) **EMPTY FLAG**. When all the data has been read from the FIFO, the EMPTY FLAG will go low, inhibiting further read operations from the device and putting the output buffers in a high impedance state. The flag will be reset, once a valid write operation has been accomplished.
22	$\overline{RS}$	(Active Low) **RESET**. A Reset will put the Read and Write pointers to the first location

PIN #	MNEMONIC	DESCRIPTION
		and reset the Half Full Flag to the high state. It is only required after power-up before performing a write operation and can only take place if the Read Enable and the Write Enable are in the high state.
23	$\overline{FL/RT}$	(Active Low) **FIRST LOAD / RETRANSMIT**. This pin has two functions: (1) When using this device in the Multiple Device Mode, grounding this pin will indicate that this is the first device to be loaded. (2) In the Single Device Mode this pin acts as a retransmit input. In this mode the read pointer is set to the first location and will not affect the write pointer. Note that the Read Enable and the Write Enable need to be in the high state during retransmit. The Retransmit feature is not compatible with Depth Expansion Mode and will only affect the Half Full Flag (HF) depending on the relative locations of the read and write pointers.
28	VCC	**SUPPLY VOLTAGE** (+5 Volt Power Input)

APPLICATIONS

SINGLE DEVICE CONFIGURATION

This configuration is used for applications that require less than the maximum specified memory space of a single device. To configure it, the $\overline{XI}$ (Expansion Input) pin needs to be grounded (Figure 1).

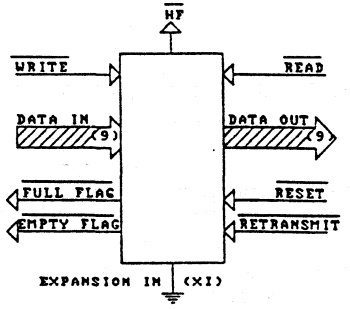


Figure 1. Block Diagram for Single Device Mode

WIDTH EXPANSION CONFIGURATION

In order to expand the width of the FIFO, the input control signals such as the Write Enable, Read Enable, Reset and Retransmit pins need to be connected together. Output Control Signals on the other hand need to be left alone. The Status Control pins such as Full, Half and Empty Flag can be detected from any one device. Figure 2 shows a typical Width Expansion configuration.

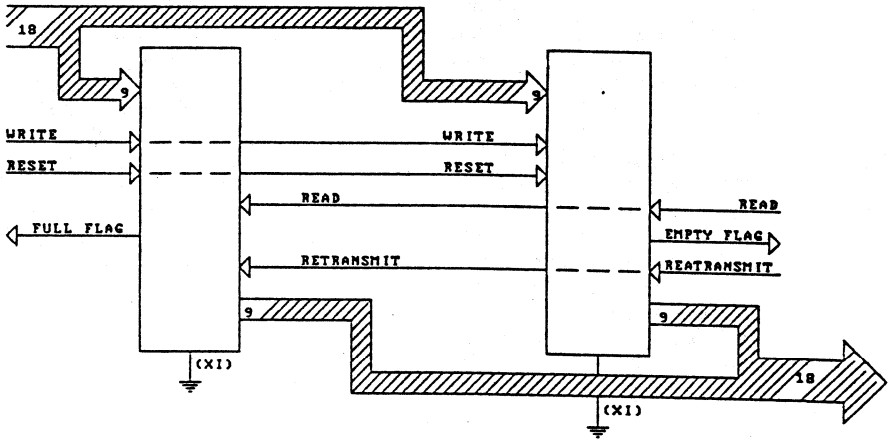


Figure 2. Block Diagram for a FIFO Width Expansion Configuration

TRUTH TABLES

RESET AND RETRANSMIT SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	RS	RT	XI	READ POINTER	WRITE POINTER	EF	FF	HF
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	X	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

Note: 1) Pointer will increment if Flag is high.

DEPTH EXPANSION CONFIGURATION

For applications requiring greater than 2048 words, several of these devices can be Daisy Chained together as long as the following conditions are met:

- The first device of the Daisy Chain is established by grounding the First Load (FL) control pin.
- All other devices must have the $\overline{FL}$ pin in the high state.
- The Expansion Out Pin ($\overline{XO}$) of each device must be connected to the Expansion In Pin ($\overline{XI}$) of the next device. (Figure 3)
- In order to generate a composite Full and/or Empty Flag some external logic is needed to "OR" all the outputs and generate the correct composite output signal.
- The Retransmit ($\overline{RT}$) and the Half Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

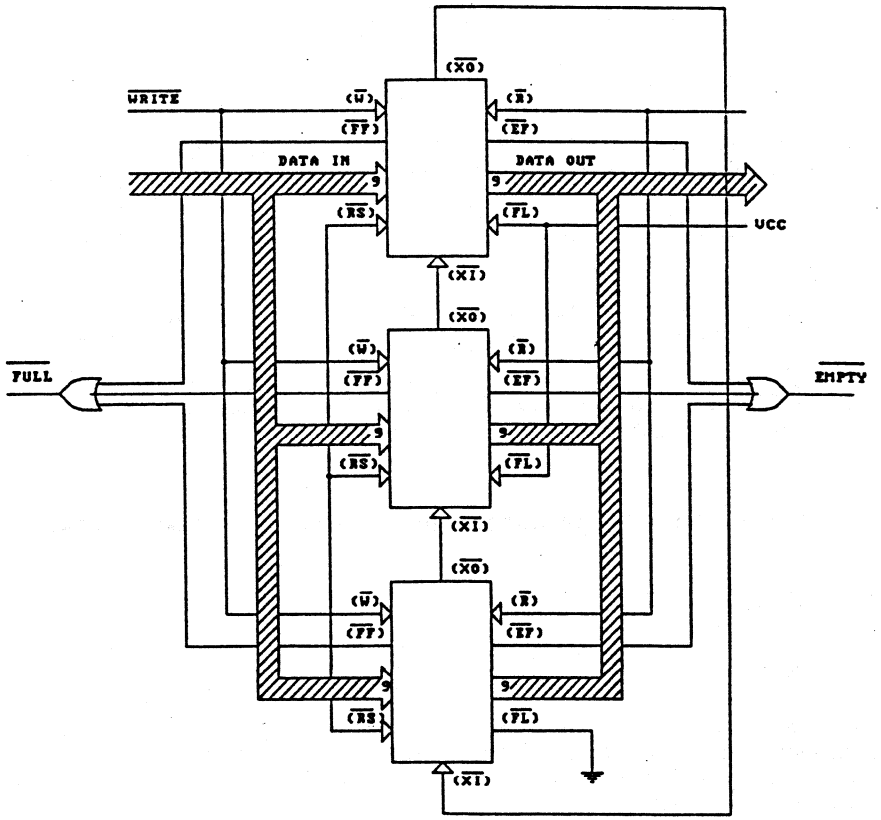


Figure 3. Block Diagram using FIFO's in Depth Expansion Mode

TRUTH TABLE

RESET AND FIRST LOAD TRUTH TABLE
DEPTH EXPANSION / COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	RS	FL	XI	READ POINTER	WRITE POINTER	EF	FF
RESET-FIRST IC	0	0	1	Location Zero	Location Zero	0	1
RESET ALL IC'S	0	1	1	Location Zero	Location Zero	0	1
READ / WRITE	1	X	1	X	X	X	X

NOTE: 1) $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
2) See definition on Pin Description for $\overline{RS}$, $\overline{FL}$, $\overline{XI}$, $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$.

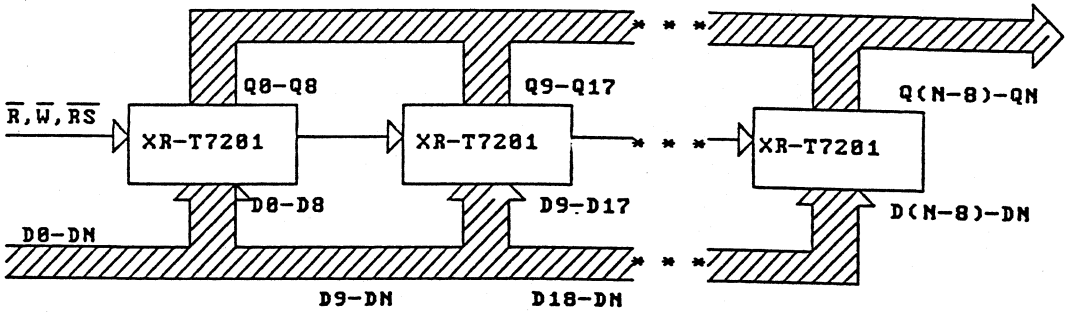


Figure 4. Block Diagram using a Compounded Depth Expansion Approach

BIDIRECTIONAL MODE

For applications that require data buffering between two systems which use independent read and write operations, care must be taken to insure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both, Depth and Width Expansion Modes can be used in this mode.

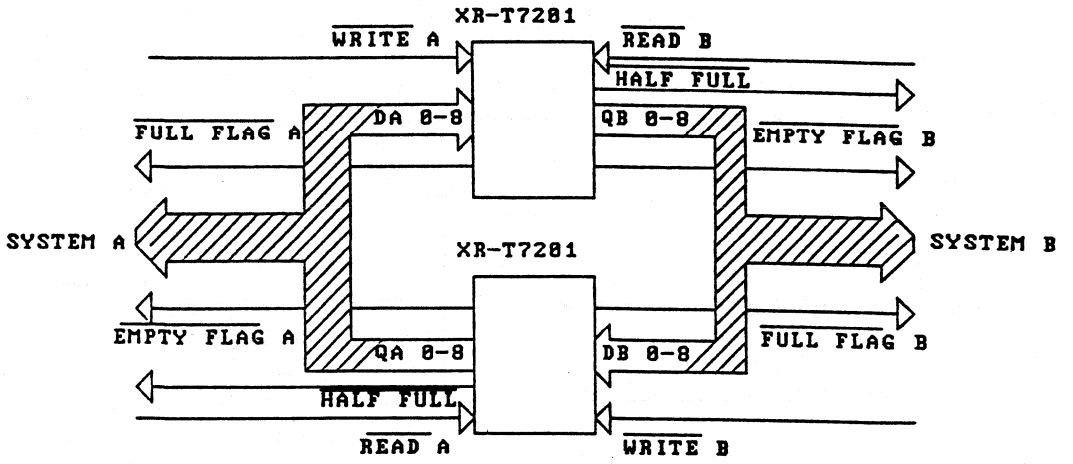


Figure 5. Bidirectional FIFO Mode

DATA FLOW THRU MODE

The XR-T7201-3 allows for two types of flow through modes:

- A read flow through mode permits a reading of a single word of data immediately after writing one word of data into the completely empty FIFO.
- A write flow through mode permits a writing of a single word of data immediately after reading one word of data from a completely full FIFO.

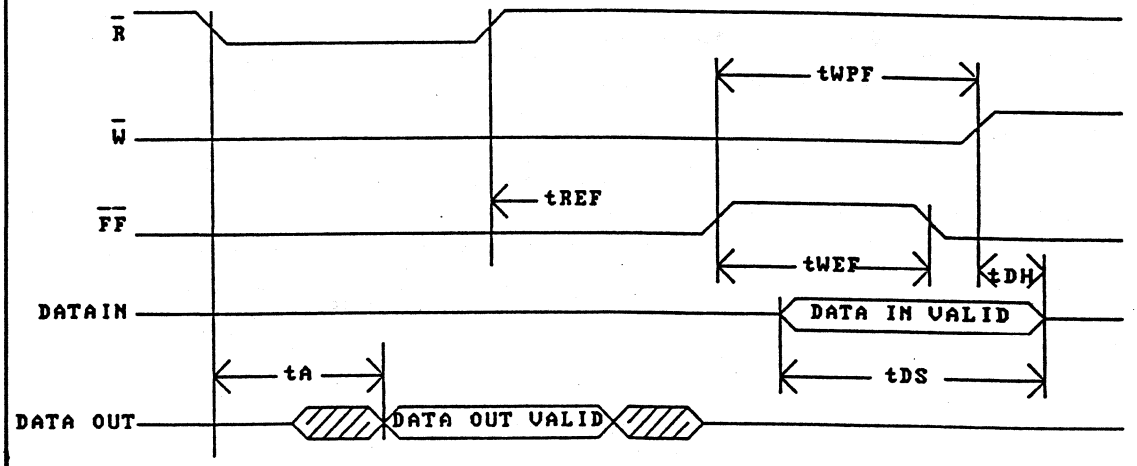


Figure 6. Write Flow Through Mode

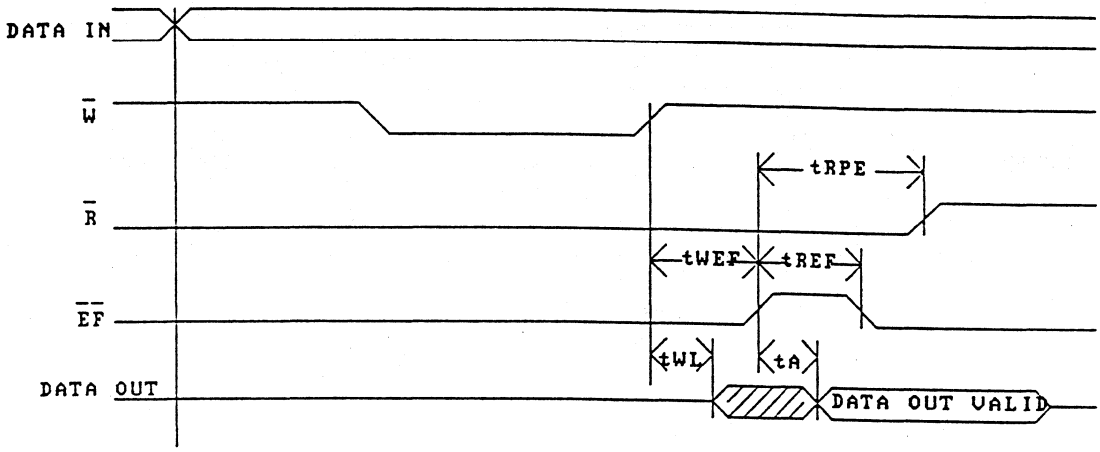


Figure 7. Read Flow Through Mode

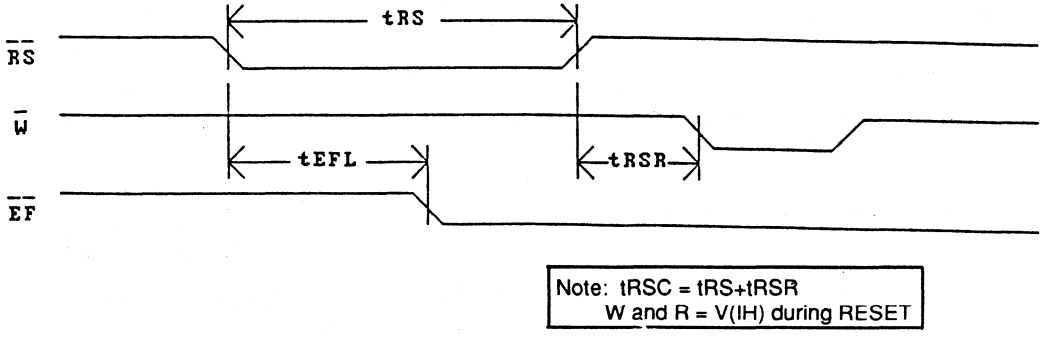


Figure 8. Reset Timing

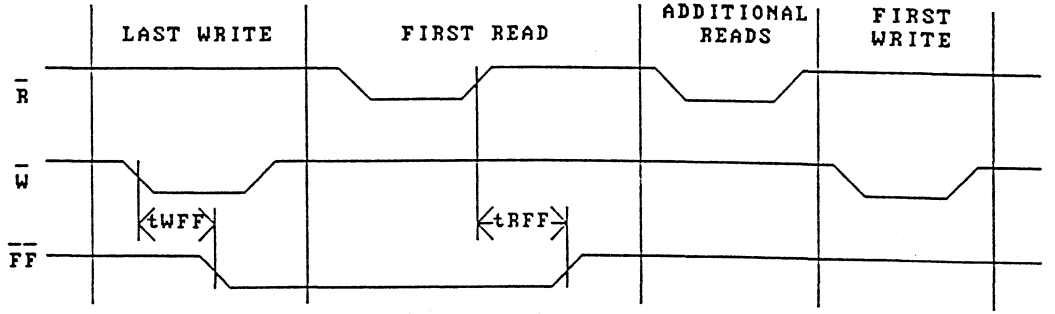


Figure 9. Full Flag From Last Write To First Read

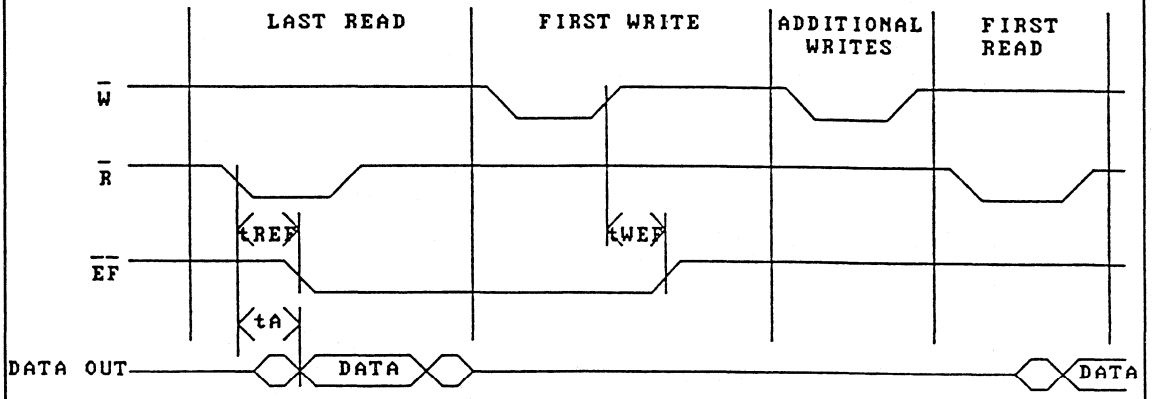
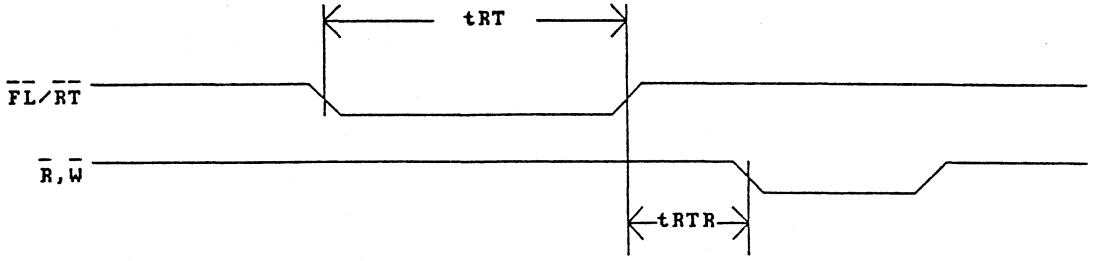


Figure 10. Empty Flag From Last Read To First Write



Note: 1) tRTC = tRT + tRTR
2) EF, HF, and FF may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at tRTC.

Figure 11. Retransmit

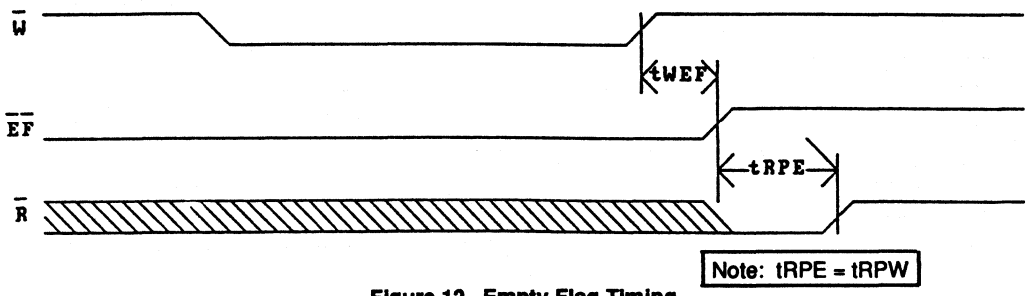


Figure 12. Empty Flag Timing

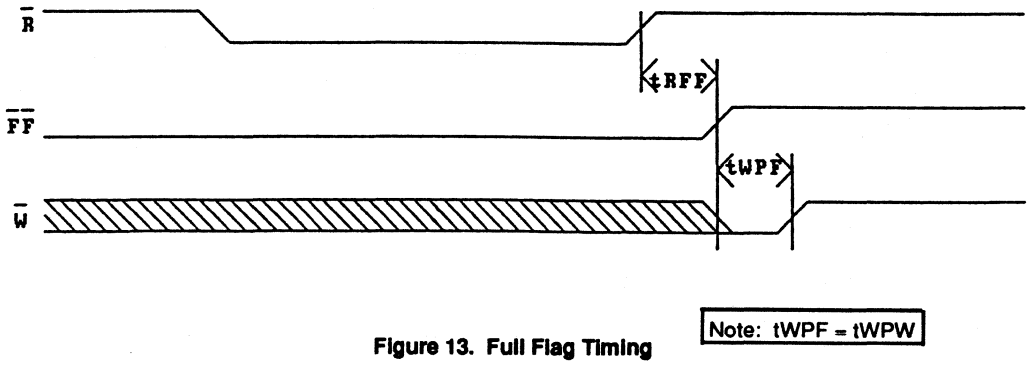


Figure 13. Full Flag Timing

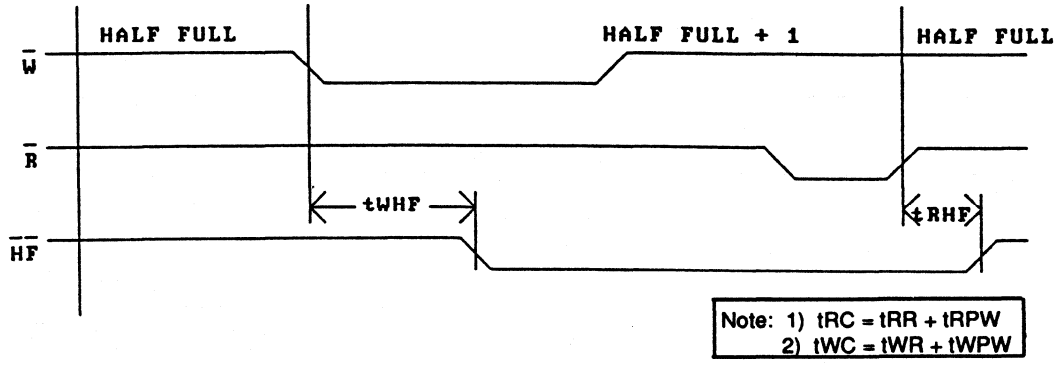


Figure 14. Half Full Flag Timing

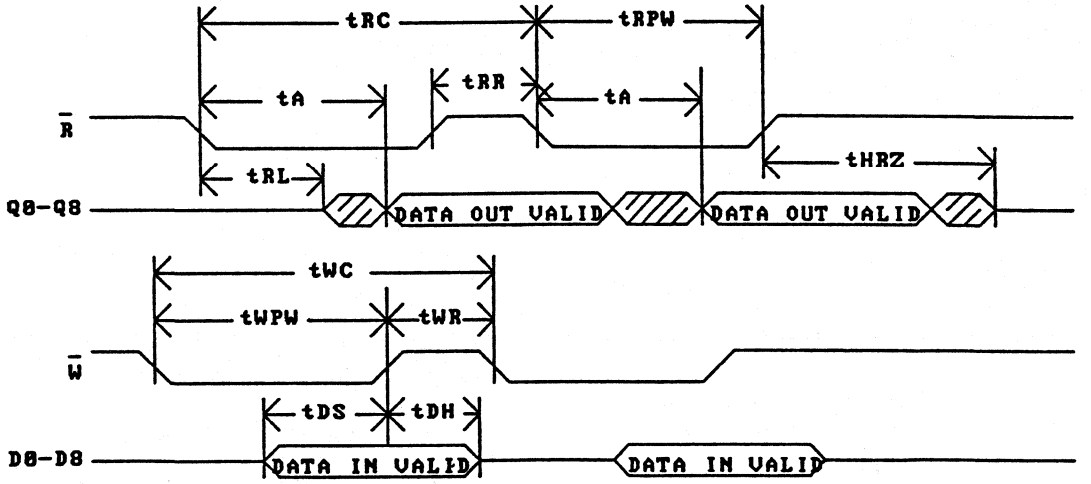


Figure 15. Asynchronous Write And Read Operation

Full-Duplex 1200 BPS/300 BPS Modem System

INTRODUCTION

This application note describes the construction of a full-duplex modem system which operates at either 1200 BPS with phase shift keying encoding (PSK) or 300 BPS with frequency shift keying (FSK). The 1200 BPS is in a synchronous format or 300 BPS asynchronous.

This system is not intended to be directly connected to the telephone network as this requires FCC approval.

PRINCIPLES OF OPERATION

The heart of this system is three LSI integrated circuits. The XR-2120 is a switched-capacitor filter (SCF) to provide precise bandpass filtering at 1200 Hz and 2400 Hz. The XR-2123 performs the 1200 BPS PSK modulation/demodulation and the XR-14412 the 300 BPS FSK modulation/demodulation. These three devices are shown with the necessary external functions to perform a 212A type synchronous modem in Figure 1. These other functions are described as follows:

LINE INTERFACE. Provide DC isolation between modem and telephone network. This section, known as a direct-access arrangement, must be approved by the FCC for direct connection to the telephone network.

AGC. Automatic gain control to provide a constant signal level to other portions of the circuit. Its received signal range can vary from about 0 dBm to −45 dBm.

ADJUSTMENT: The XR-2123A require tuning of the external 600Hz filter to achieve - 180°C of phase shift when measured from input to output. If off by a few degrees performance on a worst case line (C0) is degraded.

DEMUX. Demultiplexer to switch transmitted carrier (Txc) and received data (Rxd) between 300 BPS and 1200 BPS.

SLICER. A voltage comparator used to convert analog receive carriers (Rxcar) into digital signals suitable for the XR-2123A and XR-14412 Rxcar inputs.

CARRIER DETECT (CD). A level sensor with a digital output to indicate when a Rxcar is present.

TIMING CIRCUIT. This circuit extracts a 600 Hz receive signal timing from the Rxcar for synchronization purposes in the XR-2123A.

SCRAMBLER/DESCRAMBLER. These sections scramble the data to be transmitted (Txd) while descrambling the received data (Rxd).

DELAY CIRCUIT. To provide a delay between the request to send (RTS) data and clear to send (CTS) data commands.

Figure 2 shows the complete circuit implementation of modem, with Table 1 listing the recommended circuit values.

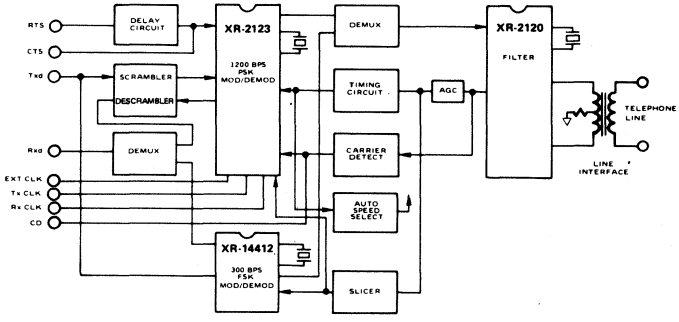


Figure 1. 212A Type Modem System.

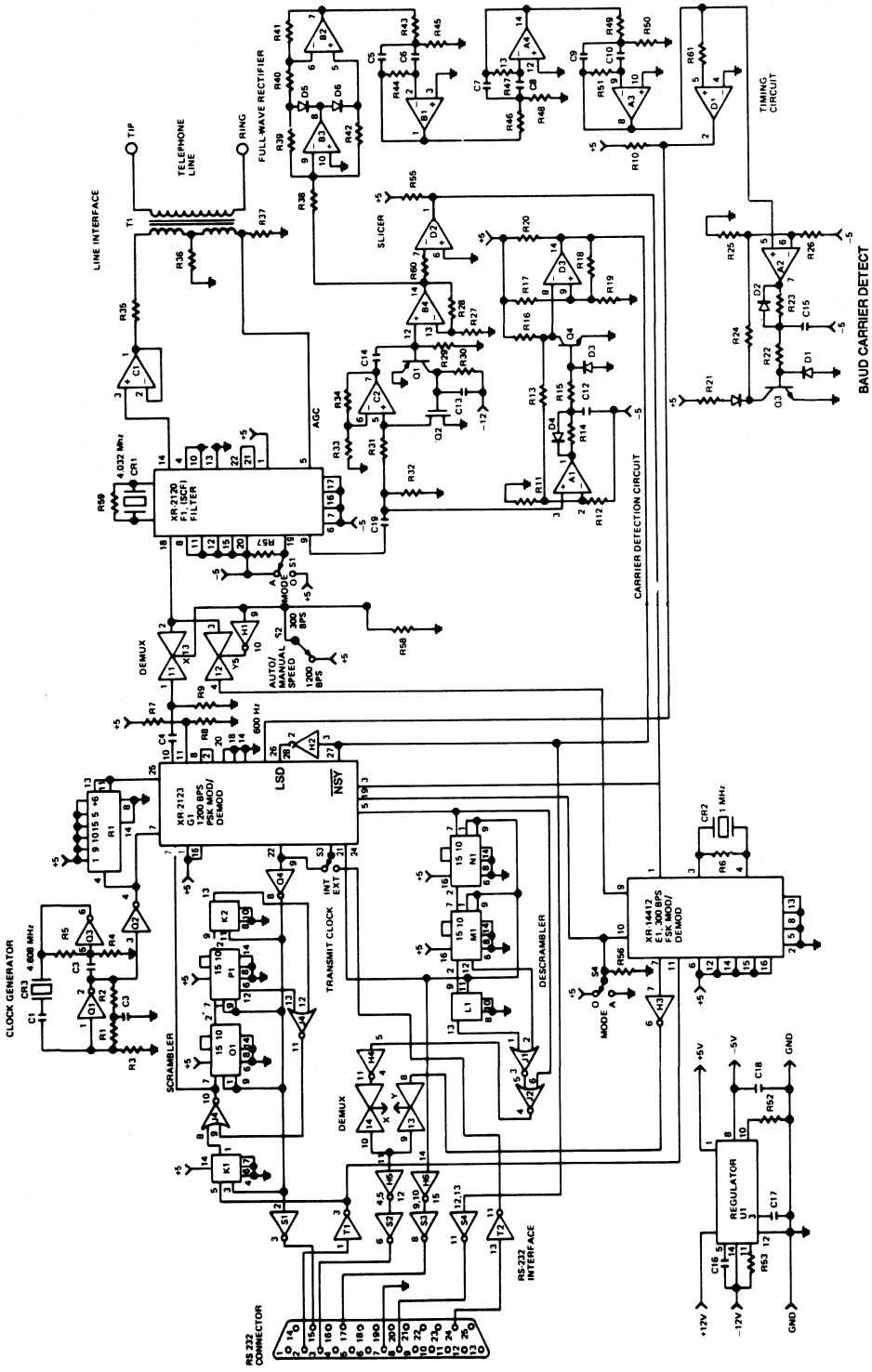


Figure 2. XR-212A Type Modem.

A.	XR-4741 Quad Op Amp
B.	XR-4741 Quad Op Amp
C.	XR-1458 Dual Op Amp
D.	LM-339 Quad Comparator
E.	XR-14412 FSK Mod/Demod 300 BPS
F.	XR-2120 Filter-Switched Cap
G.	XR-2123 PSK Mod/Demod 1200 BPS
H.	CD-4049 Hex Inverter
I.	CD-4016 Quad B1-Lateral Switch
J.	CD-4030 Quad Exclusive-OR Gate
K.	CD-4013 Dual D Flip-Flop
L.	CD-4013 Dual D Flip-Flop
M.	Dual 4 Bit Static Register 4015
N.	Dual 4 Bit Static Register 4015
O.	Dual 4 Bit Static Register 4015
P.	Dual 4 Bit Static Register 4015
Q.	MM7404 Hex Inverter
R.	DM74193 Synchronous Up/Down Counter
S.	**MC-1488 Quad Line Driver**
T.	**MC-1489 Quad Line Receiver**
U.	**RC-4194 Dual Tracking Regulator**

R_1	2.2K	R_2	2.2K	R_3	2.2K
R_4	2.2K	R_5	1.2K	R_6	1M
R_7	10K	R_8	10K	R_9	1M
R_{10}	10K	R_{11}	1K	R_{12}	62K
R_{13}	100K	R_{14}	47K	R_{15}	62K
R_{16}	10K	R_{17}	100K	R_{18}	470K
R_{19}	100K	R_{20}	10K	R_{21}	10K
R_{22}	62K	R_{23}	47K	R_{24}	100K
R_{25}	18K	R_{26}	62K	R_{27}	1K
R_{28}	4.7K	R_{29}	10K	R_{30}	1M
R_{31}	120K	R_{32}	10K	R_{33}	1K
R_{34}	68K	R_{35}	600	R_{36}	300
R_{37}	600	R_{38}	10K	R_{39}	10K
R_{40}	10K	R_{41}	10K	R_{42}	10K
R_{43}	39K*	R_{44}	180K*	R_{45}	392*
R_{46}	39K*	R_{47}	180K*	R_{48}	392*
R_{49}	39K*	R_{50}	464*	R_{51}	180K*
R_{52}	13K	R_{53}	71.5K		
R_{55}	10K	R_{56}	10K	R_{57}	10K
R_{58}	10K	R_{59}	1M	R_{60}	10K
R_{61}	10K				

All resistor values are in ohms.
* = >1% tolerance.

C_1	82 pF	C_{14}	1 μF
C_2	.033 μF	C_{15}	.1 μF
C_3	.022 μF	C_{16}	.001 μF
C_4	.1 μF	C_{17}	.001 μF
C_5	.033 μF	C_{18}	4.7 μF
C_6	.033 μF	C_{19}	2.2 μF
C_7	.033 μF	C_{20}	4.7 μF
C_8	.033 μF	C_{21}	4.7 μF
C_9	.033 μF	C_{22}	.1 μF
C_{10}	.033 μF	C_{23}	.1 μF
C_{11}	.1 μF	C_{24}	4.7 μF
C_{12}	0.22 μF	C_{25}	4.7 μF
C_{13}	4.7 μF	C_{26}	4.7 μF

Crystals

CR1 — 4.032 MHz	MTRON
CR2 — 1,000 MHz	FOX
CR3 — 4.608 MHz	X-TRON

Transformer

T1 — **671-1489 MIDCOM**

Transistors

Q1 — **Q1 - 2N4403**
Q3 — **Q3 - 2N440**
Q4 — **Q4 - 2N440**

FETs

Q2 — 2N4861

Component List for 212A Type Modem System

For asynchronous operation, the XR-2135 can be used to provide the asynchronous to synchronous conversion, as well as the synchronous for asychronous conversion.

CMOS DUART

INTRODUCTION

Asynchronous serial data communications is one of the most established, least costly, and easiest to implement means of transferring data from one electronic system to another. It is also the most widely used protocol of data communications today, due primarily to the expanding popularity of low cost microcomputer based products requiring data communications interfacing.

GENERAL DESCRIPTION

The XR-68C681 and XR-88C681 are intended for use in multichannel serial communication applications. They are fabricated using low power silicon gate CMOS process. They are also pin-for-pin and functionally compatible with the NMOS version of Signetics 2681, 68681 and Motorola 68681.

In addition to the two full duplex asynchronous serial channels which they provide, the XR-68C681 and XR-88C681 contain several other versatile system supports such as Timer/counter and I/O functions within the same package.

DUART COMPARISON CHART

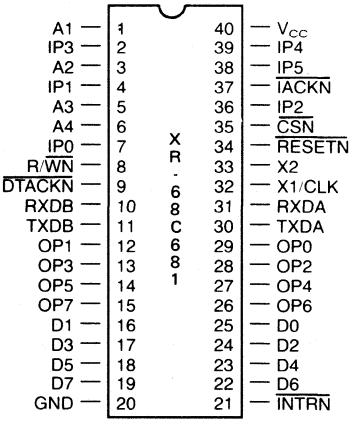
FEATURES	NMOS	CMOS
Predefined internal baud rates	23	28
Bus vector interrupts	No	Yes
Daisy chain interrupt Priority signals	No	Yes
Masked interrupt status register	No	Yes
Multi-drop mode	No	Yes
Standby mode	No	Yes

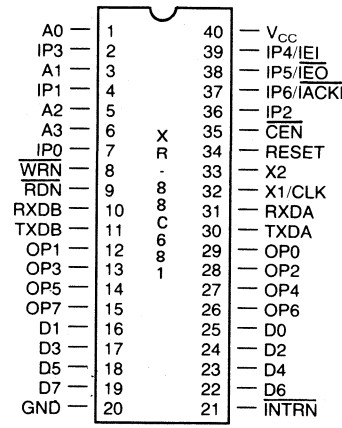
Two basic versions of the DUART are available, the XR-68C681 and the XR-88C681. Each version is optimized for interfacing with various microprocessors as follows:

EXAR DUART	MICROPROCESSORS
XR-68C681	65xx, 65C0x 65C1x 63xx, 68xx 68000, 68010 68200

EXAR DUART	MICROPROCESSORS
XR-88C681	Z80, Z800 Z8000 8048 8080, 8085 8086, 8088 80286, 80286

Both versions of the EXAR DUARTs are provided in a 40 pin DIP and 44 pin PLCC package. The additional option in 24 and 28 pin DIP packages are available for the XR-88C681.

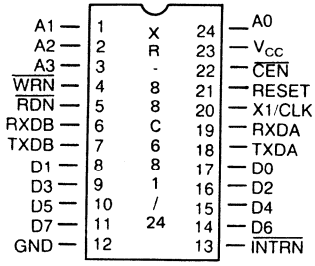


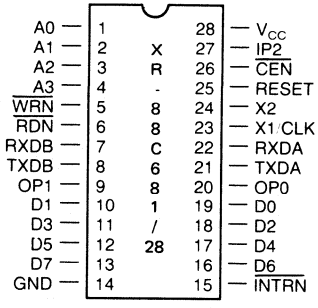


The pin configurations are as follows:

24 Pin	28 Pin	40 Pin
VDD	VDD	VDD
GND	GND	GND
A0-A3	A0-A3	A0-A3
WR	WR	WR
RD	RD	RD
CE	CE	CE
RX A,B	RX A,B	RX A,B
TX A,B	TX A,B	TX A,B
RST	RST	RST
D0-D7	D0-D7	D0-D7
INT	INT	INT
CLK1	CLK1	CLK1
	CLK0	CLK0
	OP0-OP1	OP0-OP1
		OP0-OP7
		IP0-IP1
	IP2	IP2
		IP3-IP6

Other options include extended temperature range and military products.





FUNCTIONAL ENHANCEMENTS OVER THE NMOS DUART

In addition to compatibility and low power, the XR-68C-681 and XR-88C681 features several functional enhancements.

More Bit Rate Selection

The EXAR DUARTs provide additional interal fixed baud rates which are not offered in the Signetics and Motorola versions; these rates are 3.600 KHz, 14.4 KHz, 28.8 KHz, 57.6 KHz, 115.2 KHz. Customized transmission rates can be configured by supplying an external clock to IP2 pin up to 2 MHz.

Bus Vectored Interrupts

The standard procedure of responding to an interrupt is the status polling of all possible interrupting devices. Depending on the application and the number of devices involved, this could consume a substantial amount of time and software code. To alleviate this overhead, some CPUs are capable of receiving an "interrupt vector" on the data bus. This vector causes the program to jump directly to the interrupt routine for the peripheral device which supplied the vector.

The XR-88C681 does not have a separate, dedicated interrupt acknowledge input as does the XR-68C681. Instead, a special mode called "Z mode" can be programmed to designate three of the general pupose inputs to be interrupt control signals. One of these control signals is IACK, the interrupt acknowledge. While in "Z mode", the CPU can respond to a DUART interrupt with an interrupt acknowledge. The DUART will then place the interrupt vector on the data bus when both IACK and RD are asserted.

Daisy Chained Interrupt Priority Signals

When more than one device capable of generating interrupts is used in a system, it is often necessary to implement additional logic that provides prioritization of simultaneous interrupts.

The XR-88C681 DUART has a built in Daisy chained prioritization scheme that is common to many other existing peripheral devices. The Daisy chained prioritization scheme implemented in "Z mode" via the interrupt enable in (IEI) and interrupt enable out (IEO) pins, assures that only the interrupting device with the highest priority responds with the interrupt vector. It also prevents lower priority devices from generating interrupts until the service for the higher priority device has been completed.

Masked Interrupt Status Register

The XR-68C681 and XR-88C681 provide an interrupt mask register (IMR) that can be programmed to mask out any of the eight interrupt conditions from generating interrupts to the CPU via the INTR output. When an interrupt is generated, it is necessary to read the interrupt status register (ISR) to find out which condition caused the interrupt. The ISR register shows all the interrupting conditions regardless of whether they had been masked out or not. The XR-68C681 and XR-88C681 DUARTs provide additional interrupt status registers (MISR) which show only the masked interrupt conditions.

Reading Reserved Addresses Locations

If the user tried to read address 2 Hex and A Hex in the NMOS version of the DUART, it will enter a test mode which will alter the function of its internal timing circuit. Once this is done, the NMOS DUART will not function properly until a hardware reset has been issued. Since the EXAR DUARTs do not use this method to invoke its special test modes, they allow any address to be read without adversely affecting operation.

Mutli-drop Mode -- 8051 Series Compatible

A special multi-drop mode feature in the XR-88C681, compatible with the nine bit mode of the 8051 series microcomputer, allows the implementation of a simplified local area network configuration of up to 256 stations. Current XR-68C681 users can achieve this feature by switching to the XR-88C681 and implementing minor external logic changes as shown below in Figure 1.

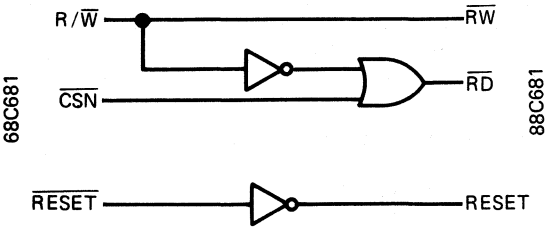


Figure 1.

Standby Mode

The XR-68C681 and XR-88C681 DUART can be programmed to be in standby mode when it is not needed for communications and timer/counter function mode. While it is in standby mode, the input ports and output ports can still be used for general system control. Standby mode is exited by issuing a "set active mode" command which returns the DUART to normal operation within 25 μs.

With the external clock source, the DUART can enter into standby mode by stopping the external clock to the DUART, this approach will not change or affect any of the DUARTs internal registers or programmed functions. This application is useful for portable computers or battery operated communication equipment.

Clock Drive Capability

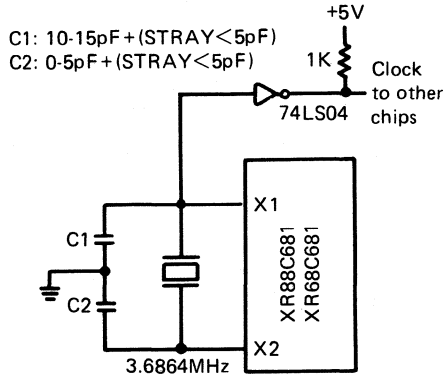
The XR-68C681 and XR-88C681 crystal output can drive an additional DUART crystal input to Daisy chain the clock circuit, and to reduce the additional crystal cost. If additional clock drive is required, it is recommended to use CMOS 4069 or 4049/4050, LS 7404 to buffer the crystal output of the DUART.

The number of DUARTs that can be driven from one crystal for NMOS parts is eight, and for CMOS parts, three.

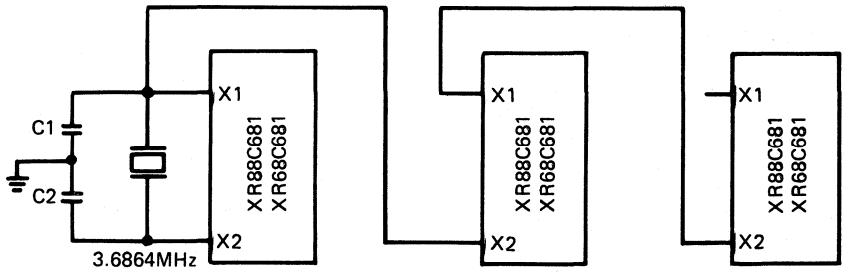
Crystal Information

The XR-68C681 and XR-88C681 DUART uses a standard 3.6864 MHz crystal available from several crystal manufacturers, including Q-Matic, McCoy, M-Tron, Crystek and US Crystal. If other bit rates are necessary, the DUART can derive bit rates from its internal programmable timer or by using external 16x and 1x clock sources through the input port.

KSS Crystal	KR-037	C1,C2 = 19 pF
Crystek	CY3JM	C1 = 18 pF
NYmph	NYP037-20	C1,C2 = 20 pF
MYmph	NYP037	Series



Crystal series resistance should be less than 180 ohms.



DESIGN HINTS FOR NEW USERS

Since XR-68C681 and XR-88C681 are asynchronous devices, read and write cycles are not DUART clock dependent, so only internal gate delays are counted.

If the user does not utilize the DTACK and IACK signals (like 65xx, 68xx CPU's users), the IACK input should be tied to VDD and ignore the DTACK signal output.

The EXAR DUART offers two types of output configurations for genral purpose output pins, push pull or open drain. The table below shows the different types of output configuration.

OPEN DRAIN OUTPUT	PUSH PULL OUTPUT
OP0	General Purpose Channel A RTS Out
OP1	General Purpose Channel B RTS Out
OP2	General Purpose TxA 1x Clock Out TxA 16x Clock Out RxA 1x Clock Out
OP3 Timer/Counter	General Purpose TxB 1x Clock Out RxB 1x Clock Out
OP4 RxRdy A /Ffull A	General Purpose
OP5 RxRdy B /Ffull B	General Purpose
OP6 TxRdy A	General Purpose
OP7 TxRdy B	General Purpose

All outputs will be inverted from Set Output Port Bits Command register or Output Port Configuration register.

INITIALIZATION AND POWER-UP HINTS:

It is possible after power-up to get a character in the transmit and/or Receive Hold Register. This happens after release of the master reset and before it receives a character from the CPU. The way to clear this situation is during the initialization routine. It is recommended to enable the loopback mode after a master reset, load the baud rate generator, wait one character time and then clear the receive buffer by reading it. This will clear any uncertain states of the transmit or receive holding registers. Following this, disable the loopback mode. Programming of the baud rate generator during initialization is also important to assure the correct operation of the RTS/CTS output port pins.

STATUS OF DUART AFTER RESET

All outputs will be set to high state, interrupt registers will be masked, the following registers will be set to "00 Hex", Status register A (SRA), Status register B (SRB), Masked Interrupt Status register (MISR), Stop Counter/Timer Command (SCC), Command register A (CRA), Command register B (CRB), Interrupt Mask register (IMR), Output Port Configuration (OPCR), Reset Output Port Bits (ROPBC), and Interrupt Vector register (IVR) to "0F Hex."

SIMPLE PROGRAMMING STEPS

Programming Timer Mode

```
LDAA  70  Hex
STAA  04  Hex      Set Timer Mode
LDAA  04  Hex
STAA  0D  Hex      Set Timer Output
LDAA  0E  Hex
STAA  06  Hex      Load Upper Count Value
LDAA  64  Hex
STAA  07  Hex      Load Lower Count Value
LDAA  00  Hex
STAA  05  Hex      Disable All Interrupts
LDAA  0E  Hex      Start The Timer
```

OP3 will generate 1 KHz square wave output.

Programming Counter Mode

```
LDAA  30  Hex
STAA  04  Hex      Set Counter Mode
LDAA  04  Hex
STAA  0D  Hex      Set Counter Output
LDAA  08  Hex
STAA  05  Hex      Set Counter Interrupt
LDAA  12  Hex
STAA  06  Hex      Load Upper Count Value
LDAA  38  Hex
STAA  07  Hex      Load Lower Count Value
LDAA  0E  Hex      Start The Counter
CLI                Clear the CPU Interrupt
WAI                Wait For Interrupt
LDAA  0F  Hex      Stop The Counter
```

Programming Output Port Bits

```
LDAA  00  Hex
STAA  0D  Hex      Make All Output Ports
LDAA  00  Hex
STAA  05  Hex      Disable The Interrupt
LDAA  55  Hex                    LHLHLHLH
STAA  0E  Hex      Set Output To HLHLHLHL
```

Reset The Output Bits

```
LDAA  55  Hex
STAA  0F  Hex      Reset All Outputs to H
```

Reset All Outputs to H

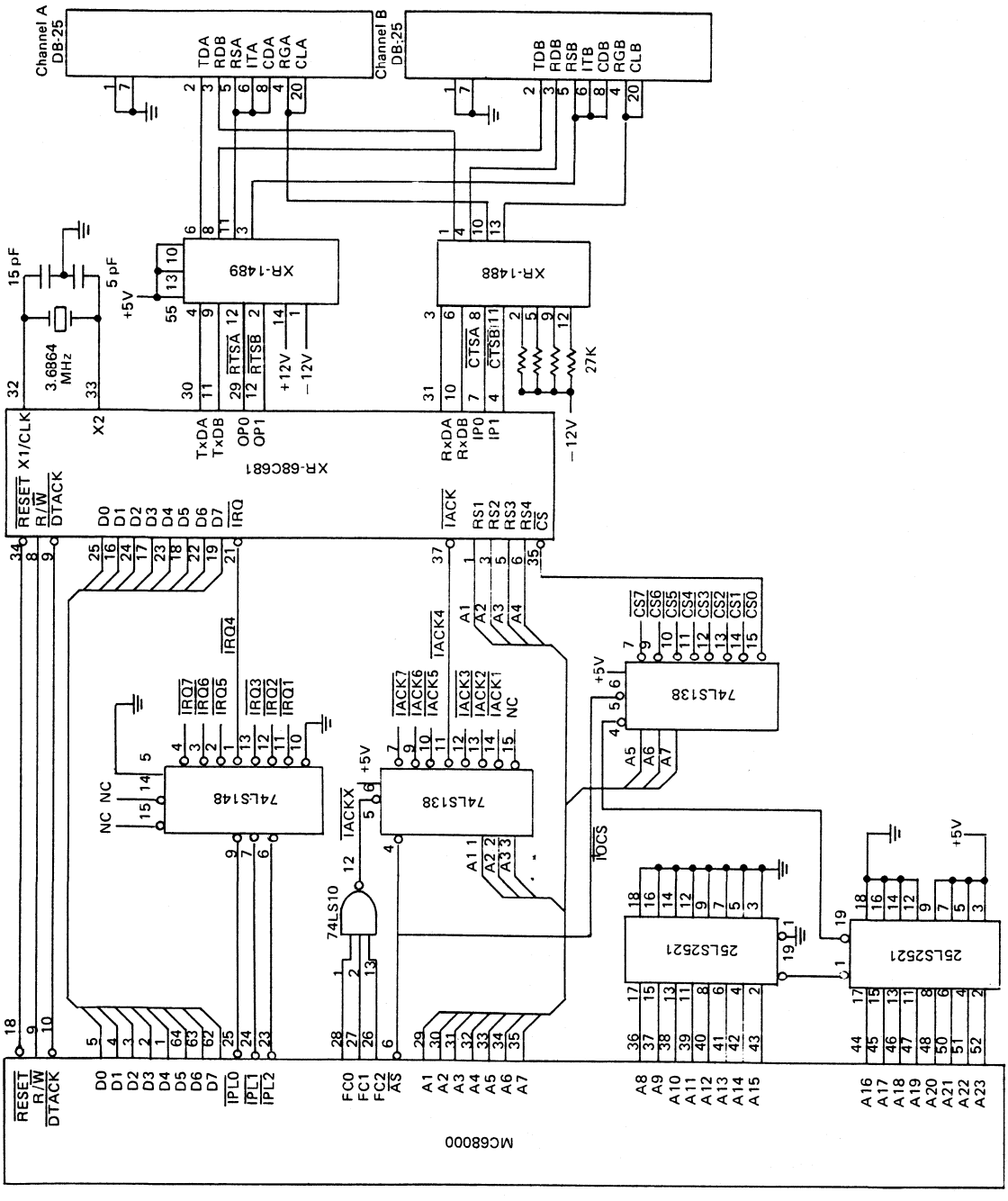
Programming For Transmit Mode A

```
LDAA  92  Hex
STAA  00  Hex      7 Bits/Char, No Parity
LDAA  07  Hex
STAA  00  Hex      1 Stop Bit
LDAA  06  Hex
STAA  01  Hex      Set 1200 Baud Rate
LDAA  42  Hex
STAA  0D  Hex      Set TX Clock Out, TXRDY
LDAA  00  Hex
STAA  04  Hex      Select Standard Baud Rate
LDAA  00  Hex
STAA  05  Hex      Disable The Interrupt
LDAA  04  Hex
STAA  02  Hex      Enable The Transmitter
LDAA  01  Hex Loop
CMPA  04  Hex      See It TXRDY Is High
BNE   Loop
LDAA  55  Hex
STAA  03  Hex      Load The Data Into THRA
JMP   Loop         Continue
```

Programming for Receive Mode A

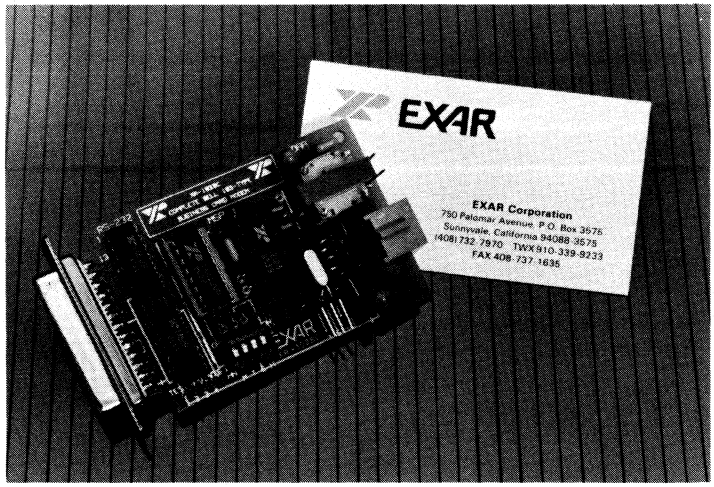
The RX Hold Register consists of a First In First Out (FIFO) stack with a capacity of three characters. Data is transferred from the receive shift register into the top most empty position in the FIFO. RxRdy is set whenever one or more characters are in the FIFO, and the FFULL status bit is set if the FIFO is filled with data. A read of the Rx Holding Register outputs, the data at the top of the FIFO and any remaining characters are pushed up, thus freeing a FIFO position for new data. Therefore, the status register must be read prior to reading the Rx Holding Register. With reset FIFO pointers are initialized and old data is still in the FIFO.

```
LDAA  92  Hex
STAA  00  Hex      7 Bits/Char, No Parity
LDAA  03  Hex
STAA  00  Hex      1 Stop Bit
LDAA  60  Hex
STAA  01  Hex      Set To Receive 1200 Baud
LDAA  13  Hex
STAA  00  Hex      RXRDY and RX Clock Out
LDAA  00  Hex
STAA  04  Hex      Select Standard Baud Rate
LDAA  02  Hex
STAA  05  Hex      Enable RXRDY Interrupt
LDAA  01  Hex
STAA  02  Hex      Enable The Receiver
CLI            Loop  Clear CPU Interrupt
WAI                Wait For Interrupt
LDAA  03  Hex      Get The Received Data
JMP            Loop  Continue
```



TYPICAL APPLICATION CIRCUIT USING 68000 CPU

Using the XR-103BC-A Business Card Sized Bell 103 Compatible Modem System



INTRODUCTION

System houses requiring telephone-based data communications links but lacking modem expertise should find the XR103BC modem demonstration/evaluation tool very useful. Manufacturers of alarm systems, remote diagnostic equipment, point of sale vendors, as well as many others, all use modems as an integral portion of their system. Like many technical blocks, modems require specialized design experience. The XR-103BC provides a fully debugged functional modem which enables the user to devote time to other aspects of the system design.

System manufacturers requiring modem communications currently have three options: (1) purchase a complete modem board from a modem house; (2) hire a modem consultant, or (3) utilize EXAR's resources for complete modem block design. Purchasing modem boards offers the advantages of design ease and short turn around times. Unfortunately, this is usually the most expensive route, as both board cost and adding a separate board into your system must be amortized. A modem consultant can integrate a modem onto already allocated system boards , yet is expensive. EXAR provides the advantages of both previous options at the lowest cost. The XR-103BC allows OEM style modem board evaluation ease, and with the included printed circuit board artwork, allows integrating the design directly on a portion of an existing board in the system. All without requiring extra modules or consultant fees. The XR-103BC demands no modem expertise. EXAR offers your lowest cost modem solution.

WHAT IS IT?

The XR-103BC is a Bell 103 compatible modem evaluation system. Requiring only ±8V to ±15V supplies, the XR-103BC links any standard RS-232C digital equipment to a dial-up type standard telephone line. Communications is handled in both directions simultaneously (full duplex) at data rates up to 300 baud.

The XR-103BC consists of three main blocks: the modem signal processor (MSP), the main portion of the modem; the RS-232 interface; and the telephone line interface.

The MSP function is performed by two low cost EXAR integrated circuits. The XR-14412 modulates data onto a carrier wave suitable for phone line transmission and simultaneously demodulates a similar incoming wave back into its data component. The XR-2103 filter separates and amplifies the two signals. RS-232 interfacing is accomplished by the XR-1488 line driver and the XR-1489A line receiver. CMOS logic levels to and from the MSP are converted to the ±3V to ±15V RS-232 levels.

Telephone line interfacing is the job of the Data Access Arrangement (DAA). The DAA, a legal requirement for interfacing to the public telephone system, protects both the telephone system and the modem from damage and holds the 20-100 mA signalling current supplied by the telephone company during operation. A coupling transformer provides isolation and an active current sink holds the DC line current. Using a physically larger transformer

would eliminate the need for the current sink, but our size and cost goals would be exceeded. The DAA circuitry on the XR-103BC is for evaluation purposes only. It has not been registered.

USING THE XR-103BC

This section describes operation on a private (PBX-type) system. Although connection to the public telephone lines is possible, such connection would be in violation of FCC regulations as the DAA design on the XR-103BC has not received Part 68 type acceptance.

Originating a data communications session requires the XR-103BC, an RS-232 equipped terminal, and a telephone or dialer. The terminal (or computer with appropriate software), should be set for 300 baud operation. The telephone or dialer is connected via a 2 to 1 (Y) adapter to both the XR-103BC and a private telephone system. For dedicated lines, please note that any 600Ω nominal impedance twisted wire line may be driven.

The XR-103BC requires ±8V to ±15V for operation. A simple power supply is two 9V batteries. Hook-up is shown in Figure 1.

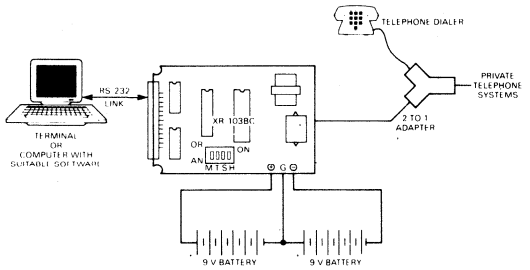


Figure 1. XR-103BC Operational Connections

Place the XR-103BC in originate mode for standard operation by turning DIP switches M, T and S ON. Leave switch H OFF. Dial a number known to have an operating modem on line. When an "answer" tone is heard, flip switch H ON and hang up the telephone/dialer. Hit carriage return on the terminal several times and communications should be established. Follow the answering system's operating procedure for logging on if necessary.

Answer mode operation is similar. Place switch M in the OFF position and have someone call. Flip switch H ON for connection.

Unattended operation requires detecting ringing and answering incoming calls. As the XR-103BC is designed for simplicity and low cost, these features were not included. Ring detection and automatic answering capabilities are implemented with the circuitry of Figure 2.

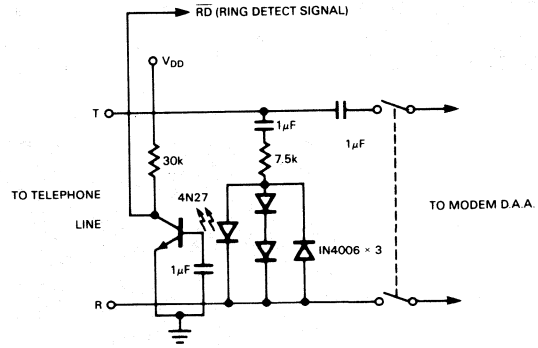


Figure 2. A Simple Ring Detection Circuit

XR-103BC SWITCH POSITIONS

Switch/Label	Name/Function	ON	OFF
M	Mode Select	Originate	Answer
T	Transmit Carrier Enable	Carrier On	Carrier Off
S	Self Test	Normal	Self Test
H	Hook Switch	Operate (On Line)	Off Line

Figures 3A, 3B, 3C, 3D, 3E XR-103BC Switch Positions

Normal Originate Mode Operation

M	ON
T	ON
S	ON
H	ON

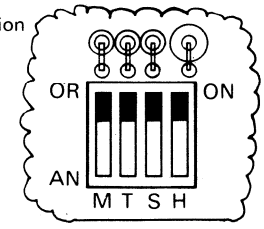


Figure 3A.

Normal Answer Mode Operation

M	OFF
T	ON
S	ON
H	ON

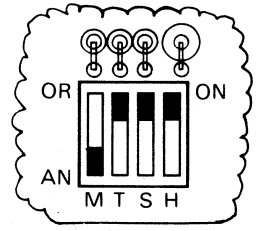


Figure 3B.

Self Test (Loop Back) Mode

M	X(either)
T	ON
S	OFF
H	OFF

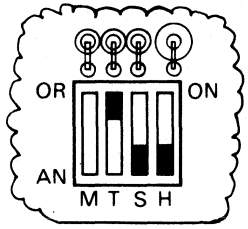


Figure 3C.

Bench Testing Received Signal Amplitude

M	X
T	OFF
S	ON
H	OFF*

***May be on line for testing in half duplex mode.**

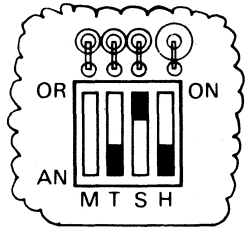


Figure 3D.

Bench Testing Bit Error Rate

M	X
T	ON
S	ON
H	OFF

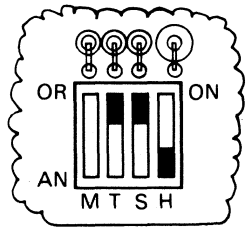


Figure 3E

IN CASE OF DIFFICULTY

If the operating procedures fail, try the following:

1) Recheck both modem power supplies and verify proper voltages.
2) Recheck both RS-232 and RJ-11 connections.
3) Verify the DTE is set to 300 baud.
4) Recheck DIP switch positions for proper setting (see Figures 3 depending upon application).

If the above steps fail to produce proper operation, try the following:

1) Verify the station called has an operating Bell 103 compatible modem placed in ANSWER mode.

2) Check that data bits, nulls, parity bits, start bits, and stop bits are compatible. Both systems should use the same format. The predominant format is one start bit, eight data bits, no parity bits, and one stop bit.

If this still fails, try the self test procedure. This is a loop back mode that tests the modem. Data from the DTE is routed through the modem and looped back to the DTE. Place the modem in self test originate mode by flipping DIP switches M and T ON and S and H OFF (see Figure 3C). Characters typed on the terminal will be echoed back to the terminal.

XR-103BC PARTS LIST

Active Components

ICs

XR-2103
XR-14412
XR-1488
XR-1489A
LM340LAZ5.0 or 78L95ACZ

Other Semiconductors

2N2222	TO-92
2N6724 (Darlington)	TO-127/237
1N4007	x4
22V Zener	x2

Passive Components

Resistors

100k	5%	x2	¼W
510k	5%	x1	¼W
10M	5%	x1	¼W
20k	5%	x3	¼W
3.3k	5%	x1	¼W
602Ω	1%	x1	¼W
22Ω	5%	x1	¼W
100Ω	5%	x1	½W

Capacitors

10μF	x1
1μF	**x2**
0.1μF	x2
220pF	x1

Miscellaneous Components

1.000 MHz Crystal
4 position DIP Switch
RJ-11 telephone line connector
DB-25 RS-232 connector
600:600Ω isolation transformer

TYPICAL PERFORMANCE SPECIFICATIONS

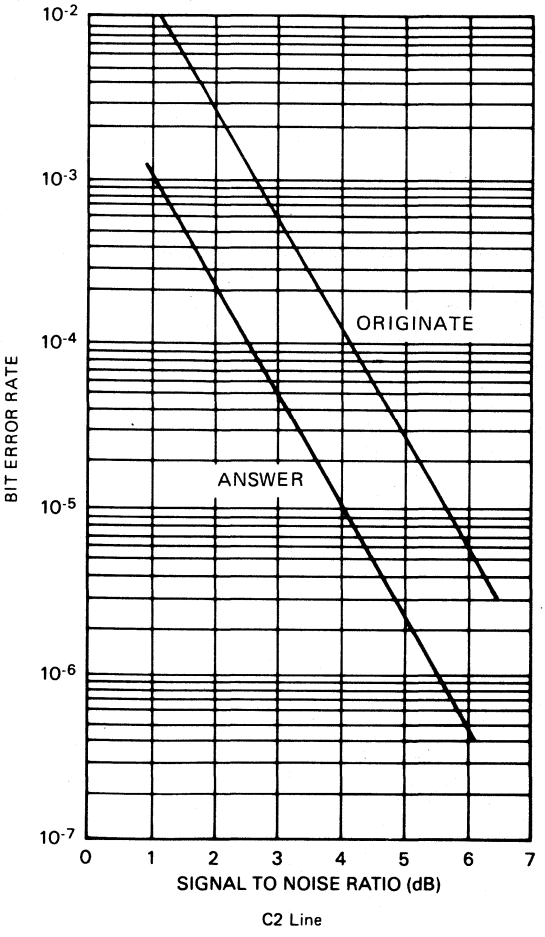
Function: Bell 103 Compatible Full Duplex Modem

Power Supply Voltage Range: ±8V to ±15V

Power Supply Current:

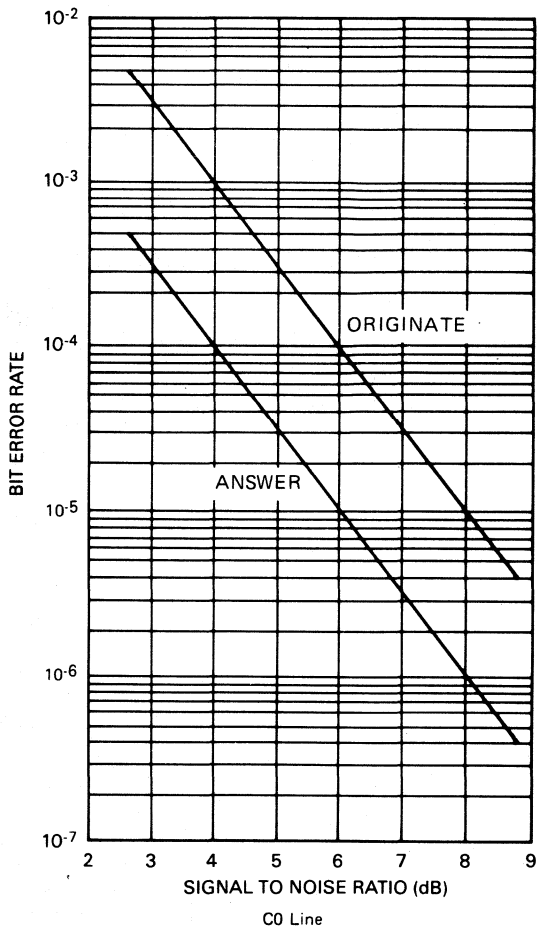
XR-2103 & XR-14412	10 mA @ 5V
Complete modem with RS-232	30 mA @ 12V 15 mA @ −12V 25 mA @ 9V 10 mA @ −9V

Modem Performance



C2 Line

Figure 4(a)



C0 Line

Figure 4(b)

Test Conditions: Received Carrier Level = −30 dBm. 511 Pseudo-Random Test Pattern.

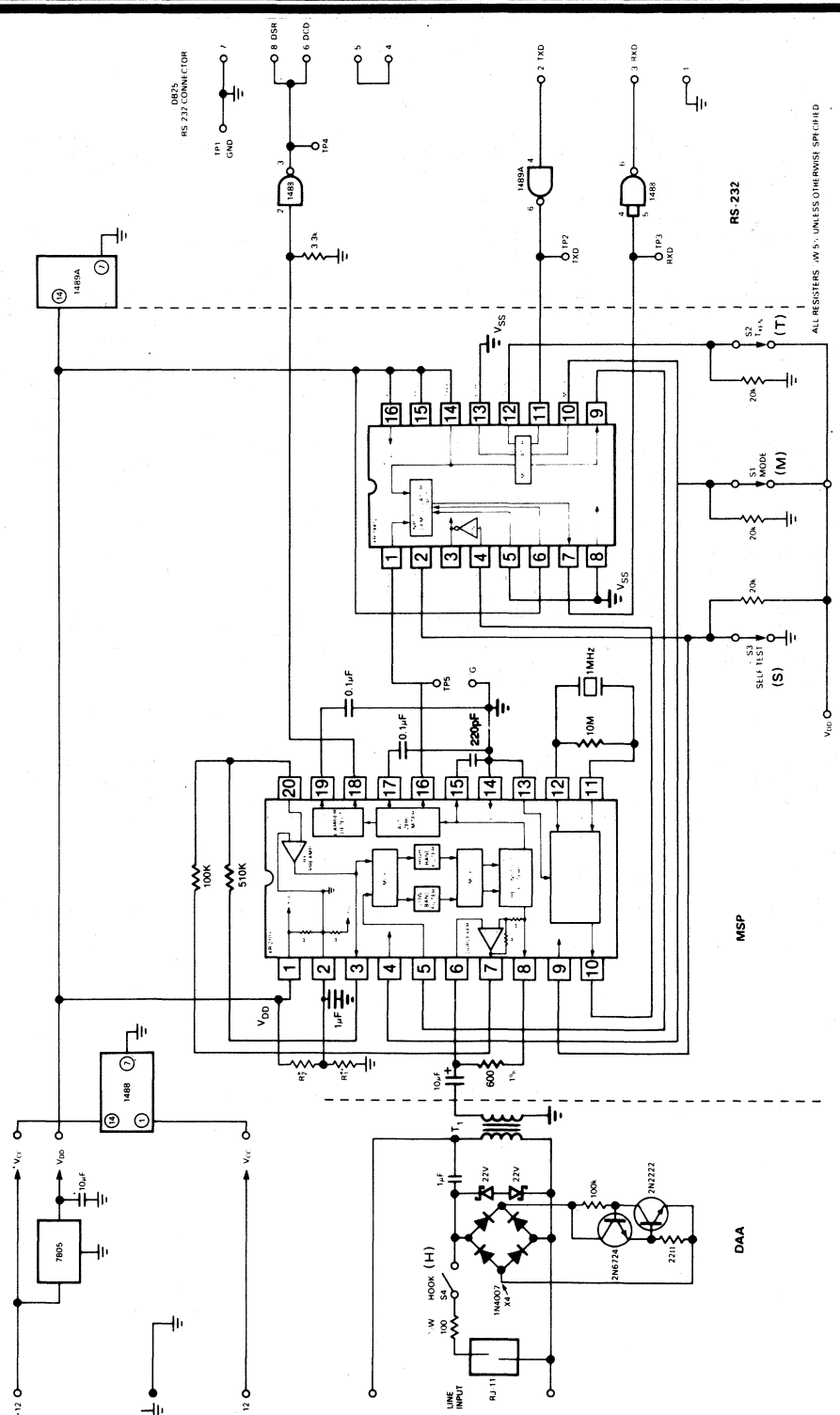


Figure 5. XR-103BC Schematic Diagram

USER CUSTOMIZATION

The XR-103BC is designed as an easy-to-use modem evaluation tool. For example, a modem designed for installation inside a computer would not require RS-232 interfacing. An originate only modem on a dedicated line would not need mode switching, a current sink, or an isolation transformer. On the other hand, a system designed for full-featured operation on the public telephone lines would need a dialer, ring detector, auto answering circuitry, and DAA type acceptance.

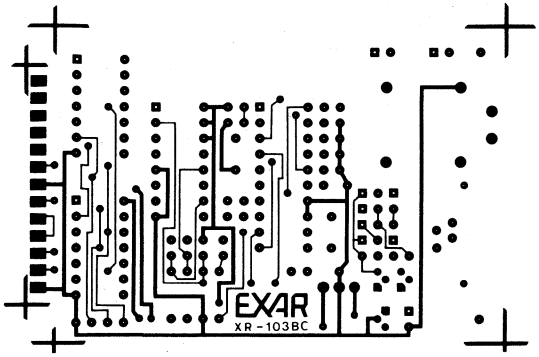
Circuit modification may be made without excessive worry over layout; the devices are not prone to unwanted oscillation. Ring detection and auto answering circuit diagrams appear in Figure 2. Dialing functions are easily added using the XR-T5990 pulse and tone dialer. See the XR-T5990 data sheet for further information. If a microprocessor is available, many functions could be implemented into it.

Systems requiring higher data rates are accommodated with the 300/1200 BPS Bell 212A compatible XR-212AS.

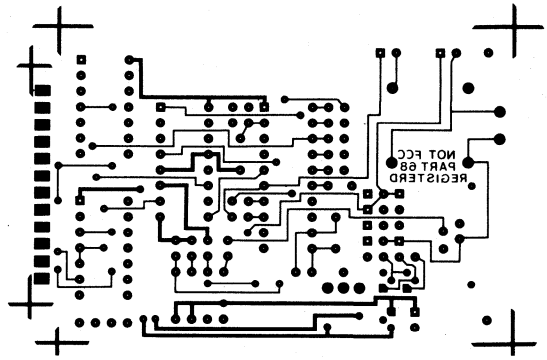
CONCLUSION

The XR-103BC, designed for system houses requiring a modem but lacking in-house modem specialists, is a simple yet fully functional modem block. Its basic design allows easy user customization. Even modem design professionals will appreciate how straightforward a modem based on the low cost XR-14412 and XR-2103 can be. These building blocks are your easiest and lowest cost modem implementation.

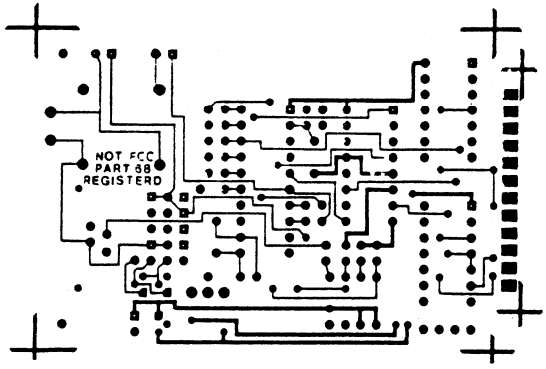
EXAR Corporation designs, manufacturers and markets a wide variety of linear and digital semiconductors. For further information, contact EXAR at **408-434-6400.**



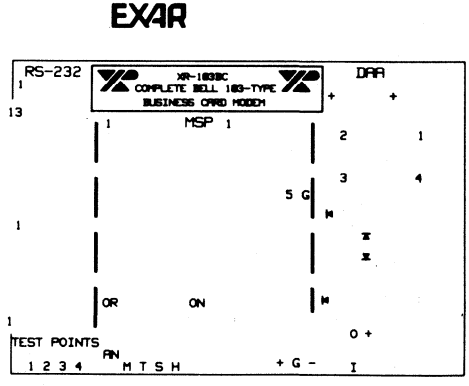
XR-103BC TOP FOIL



XR-103BC BOTTOM FOIL XRAY FROM TOP



XR-103BC BOTTOM FOIL



XR-103BC SILKSCREEN

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Disk Drive Product Selection Guide

Part Number	Technology	Supply Voltages	Product Features	Description	Packages
XR-117 XR-117R	High Speed Bipolar	+5, +12	Two, Four & Six Channels Industry Standard	Hard Disk Read/ Write Amplifier	PLCC (CJ) 28 JEDEC SO (D) 18, 24, 28 DIP (CP) 18, 22, 28
XR-501 XR-501R	High Speed Bipolar	+5, +12	Six & Eight Channnels High Performance	Hard Disk Read/ Write Amplifier	PLCC (CJ) 28,44 JEDEC SO (D) 28, 32 DIP (CP) 28,40
XR-505 XR-505R	High Speed Bipolar	+5	Low Power Operation High Performance Single Supply Two & Four Channels	Low Power, Single +5V Read/Write Amplifier	JEDEC SO (D) 16, 20, 24 JEDEC SO (G) 16 DIP (CP) 18, 22, 28
XR-510A XR-510AR	High Speed Bipolar	+5, +12	Two, Four & Six Channels Enhanced Performance Same Pinout as XR-117	Improved Performance Hard Disk Read/ Write Amplifier	PLCC (CJ) 28 JEDEC (D) 18, 24, 28 DIP (CP) 18, 22, 28
XR-511 XR-511R	High Speed Bipolar	+5, +12	Two, Four & Six Channels Enhanced Performances Same Pinout as XR-501	Improved Performance Hard Disk Read/ Write Amplifier	PLCC (CJ) 28, 44 JEDEC (D) 24, 28, 32 DIP (CP) 28, 40
XR-532	BiCMOS	+5	Low Power Operation (150mW) Improved Speed and Performance	Low Power, High Speed RLL (2, 7) Data Separator	PLCC (CJ) 28 (TBD)
XR-541	High Speed Bipolar	+5, +12	RLL & MFM Compatible High Accuracy (1nS available)	Disk Drive Pulse Detector	PLCC (CJ) 28 JEDEC SO (D) 24 DIP (CP) 24

Hard Disk Read/Write

GENERAL DESCRIPTION

The XR-117 is a high speed head interface integrated circuit for hard disk drives, performing both read and write functions. The XR-117 is compatible with 3½" to 14" single and multiple platter drives, and features high bandwidth, large dynamic range, and low noise. Several packaging options extend usefulness to applications requiring two, four, or six center-tapped read/write heads; multiple devices are easily cascaded for drives with more heads.

The XR-117R includes internal damping resistors, facilitating use in circuits requiring minimum external complexity and mass.

The XR-117, manufactured with a high speed bipolar process, operates on +5 V and +12 V.

FEATURES

Complete Head Interfacing Functions, Read and Write
High Bandwidth and Dynamic Range
Low Noise
Available in Two, Four, and Six Head Versions
Easily Cascaded for Larger Systems
Power Monitor
TTL Compatible Inputs

APPLICATIONS

Single or Multiple Platter Hard Disk Drives

ABSOLUTE MAXIMUM RATINGS

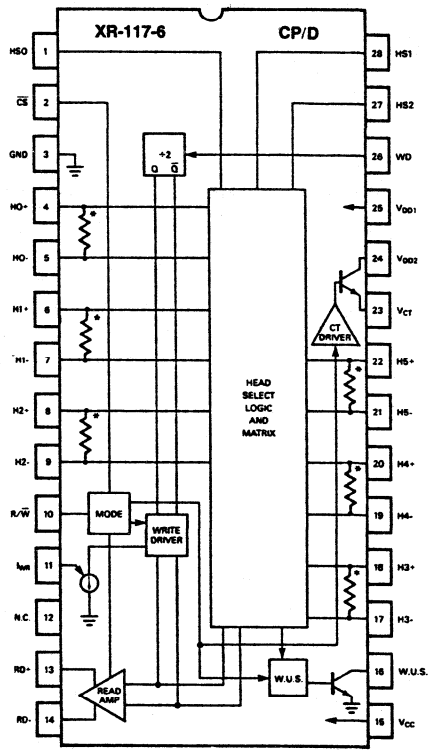
V_{DD1} and V_{DD2}	15 V
V_{CC}	6 V
Digital Inputs	−0.3 V to V_{CC} +0.3 V
Write Current	60 mA
Junction Temperature	150°C
Storage Temperature	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-117-2CP	18 Pin Plastic	0°C to 70°C
XR-117-4CP	22 Pin Plastic	0°C to 70°C
XR-117-6CP	28 Pin Plastic	0°C to 70°C
XR-117-xD	Surface Mount	0°C to 70°C
XR-117-6CJ	28 Pin PLCC	0°C to 70°C
XR-117R-xCP	Plastic	0°C to 70°C
XR-117R-x D*	Surface Mount	0°C to 70°C
XR-117R-6CJ	28 Pin PLCC	0°C to 70°C

x = 2, 4 or 6, depending on number of heads required
* = contact factory for availability

FUNCTIONAL BLOCK DIAGRAM



*XR-117R Versions Only

SYSTEM DESCRIPTION

Four major blocks comprise the XR-117: a multiplexer for head selection, write data control circuitry, read signal amplifiers and buffers. Designed for six read/write heads, the XR-117 is also available in smaller packages for systems requiring only two or four heads. The 30 MHz minimum bandwidth facilitates data rates exceeding 25 Mbits per second.

Less than 1.3 $nV/\sqrt{Hz}$ (nominal) noise allows error free operation with small input signals. Up to 50 mA of write current output means the disk signal can be large, further enhancing the readback signal-to-noise ratio for very low error rates.

Cascading multiple XR-117s is accomplished by alternately enabling and disabling devices via the chip select (CS) pin. Guaranteed write current tolerances allow close write matching between devices.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 12$ V, $V_{CC} = 5$ V, $R_W = 3.1$ kΩ, $L_h = 10\mu H$, $R_d = 750\Omega$, C_L (R_{D+}, R_{D-}), ≤ 20 pF, Data Rate = **5 MHz, unless specified otherwise.**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DC CHARACTERISTICS						
I_{CC}	Supply Current			25	mA	V_{CC} = 5.5 V, Read or Idle Mode
				30	mA	V_{CC} = 5.5 V, Write Mode
I_{DD}	Supply Current			25	mA	V_{DD} = 13.2 V, Idle Mode
				50	mA	V_{DD} = 13.2 V, Read Mode
				30	mA	V_{DD} = 13.2 V, Write Mode, I_W = 0 mA
P_D	Power Dissipation			400	mW	V_{CC} = 5.5 V, V_{DD} = 13.2 V, Idle Mode
				600	mW	Read Mode
				700	mW	Write Mode, I_W = 50 mA, R_{CT} = 130Ω
				1050	mW	Write Mode, I_W = 50 mA, R_{CT} = 0Ω
V_{CT}	Center Tap Voltage		4.0		V	Read Mode
			6.0		V	Write Mode
WUS	Write Unsafe Output					
V_{OL}	Saturation Voltage		**0.2**	**0.5**	V	I_{OL} = 8 mA
I_{OH}	Leakage Current			100	μA	V_{OH} = 5 V
DIGITAL INPUTS						
V_{IL}	Input "Low" Voltage			0.8	V	
V_{IH}	Input "High" Voltage	2.0			V	
I_{IL}	Input Current, Low	−0.4			mA	
I_{IH}	Input Current, High			100	μA	
WRITE CHARACTERISTICS						
	Write Current Accuracy	−5		+5	%	Note 1
I_W	Recommended Write Current Range	10	45	50	mA	
	Differential Head Voltage Swing	5.7			Vpeak	
	Unselected Differential Head Current			2	mApeak	
C_O	Differential Output Capacitance			15	pF	
R_O	Differential Output Resistance	10			kΩ	XR-117
		635	750	865	Ω	XR-117R
	WD Rate (Transisition Frequency)	125	500	625	kHz	
K_I	Current Source Factor		20			$K_I = I_W/(\text{Current Through } R_W)$

READ CHARACTERISTICS						
A_V	Differential Voltage Gain	80	100	120	V/V	V_{in} = 1 mVp-p @ 300 kHz $R_{L+} = R_{L-}$ = 1 kΩ
	Dynamic Range	−2		2	mV	DC input voltage where gain drops 10%. $V_{in} = V_i$ + 0.5 mVp-p @ 300 kHz.
R_{in}	Differential Input Resistance	2 500	8 675	 850	kΩ Ω	XR-117 XR-117R
C_{in}	Differential Input Capacitance			23	pF	f = 5 MHz
e_{ni}	Input Noise Voltage		1.3	2.1	$nV/\sqrt{Hz}$	L_h = 0, R_h = 0, BW = 15 MHz
BW	Bandwidth	30	60		MHz	−3dB point $\|Zs\| < 5\Omega$, V_{in} = 1 mVp-p
I_B	Input Bias Current		10	45	μA	
CMRR	Common Mode Rejection Ratio	50	60		dB	$V_{CM} = V_{CT}$ + 100 mVp-p at 5 MHz
PSRR	Power Supply Rejection Ratio	45	60		dB	100 mVp-p at 5 MHz Superimposed on V_{DD1}, V_{DD2} or V_{CC}
	Channel Separation	45	60		dB	Unselected Channel: V_{in} = 100 mVp-p at 5 MHz. Selected Channel V_{in} = 0 V
	Output Offset Voltage	−480	± 50	480	mV	
V_{CM}	Common Mode Output Voltage	5	6	7	V	
SWITCHING CHARACTERISTICS						
R/W	Read to Write		0.1	1	μS	Note 2 Write to Read
	Write to Read		0.1	1	μS	Note 3, Note 4
CS	Start-Up Delay		0.1	1	μS	Delay to 90% of I_W or to 90% of 100 mV 10 MHz read signal envelope.
	Inhibit Delay		0.1	1	μS	Note 4
	Head Switching Delay		0.1	1	μS	Note 3, Switching between any heads.
WUS	Write Unsafe					
	Safe to Unsafe	1.6	2.5	8.0	μS	I_W = 50 mA, See Figure 1, TD1
	Unsafe to Safe		0.2	1	μS	I_W = 20 mA, See Figure 2, TD2
I_W	Head Current					
	Propagation Delay		4	25	nS	L_h = 0 μH, R_h = 0Ω, Note 5
	Asymmetry			2	nS	Note 6. See Figure 1, TD3
	Rise or Fall Time		9	20	nS	10% to 90% or 90% to 10% points

4

)te 1: Error from $I_W = \frac{140}{R_W}\left(\frac{V}{\Omega}\right)$
)te 2: Delay to 90% of I_W
)te 3: Delay to 90% of 100 mVp-p 10 MHz read single envelope
)te 4: Delay to 90% decay of I_W
)te 5: From 50% points
)te 6: Input WD has 50% duty cycle and 1 nS rise and fall times.

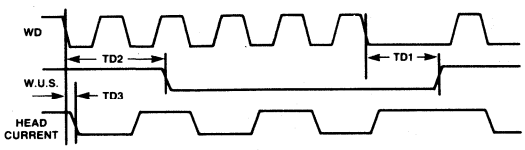


Figure 1. Write Mode Timing Diagram

CAUTION: This device may be damaged by electrostatic discharge. ESD precautions should be taken.

PRINCIPLES OF OPERATION

Write Mode

Before writing may begin, both chip select ($\overline{CS}$) and Read/Write (R/W) must be pulled low. The desired head, selected by HS0 to HS2, is driven by a differential current sink of magnitude I_W set by R_{IW}. Input data is applied to a falling edge triggered toggle flip-flop, which in turn selects the active side of the center tapped write head.

Current is sourced through the center tap driver, V_{CT}, which is "high" in the write mode. Write unsafe (WUS) signals the disk controller whenever one of six error conditions exist and writing should be discontinued. The six faults are: open head, open center tap, no write current, write data frequency too low, device unselected, and writing attempted while the device is in the read mode.

Read Mode

Pulling R/W high enables the data readback mode. A low noise, high gain differential amplifier increases the weak signal amplitude and provides low output impedance.

APPLICATIONS INFORMATION

As with all high frequency, high gain systems, layout is critical. Lead lengths should be minimized and supplies should be well bypassed. The XR-117 is available in small outline surface mount and PLCC packages, facilitating installation near the drive heads. The XR-117R option has 750Ω internal damping resistors across each head input, further aiding the goal of short lead lengths by eliminating the need for external resistors. The XR-117R option is especially convenient when the device is mounted on the flexible cable connecting the heads, as internal damping resistors reduce layout complexity, parts counts, and mass.

The high frequency characteristics of the XR-117 lead to a certain degree of electrostatic discharge (ESD) susceptability, so static reducing precautions should be taken.

Write Mode Design Considerations

Write current, I_W, typically between 20 mA and 50 mA, is determined by a single resistor, R_{IW}.

$$R_{IW} = \frac{140{,}000}{I_W}$$

where I_W is in mA and R_{IW} is in ohms.

The V_{CC} supply monitor disables writing when V_{CC} drops below about 4 V.

Device power dissipation is reduced by a resistor, R_{CT}, connecting V_{DD2} to the +12 V supply. Some of the center tap driver voltage drop then is across the resistor.

With the nominal 12 V supply, R_{CT}, is calculated as

$$R_{CT} = 130\ (\frac{55}{I_W})$$

where R_{CT} is in ohms and I_W is in milliamperes.

Internal dissipation reduction is primarily a consideration with high write current levels and small outline packages. For low write currents, R_{CT} may be deleted, with V_{DD2} directly connected to the supply.

Write center tap circuitry is designed for higher stability than similar devices from other manufacturers. If extreme conditions exist, a ferrite bead around the V_{CT} line to the heads will reduce or eliminate overshoot and ringing.

Write unsafe (WUS) pulls high whenever one or more of six write error conditions exist. Four conditions; open head, open center tap, no write current and write data transition rate too low, are detected with a differential capacitor charge/discharge circuit. Device unselected and read mode digital conditons also force WUS high.

After removal of the fault condition, two negative write data transitions are required to clear WUS. This output is for indication only, intended for signaling a controller, and does not directly impede device operation. A pull-up resistor of about 2 kΩ to 10 kΩ is necessary for operation of this open collector output.

Read Mode Design Considerations

The read amp has a fully differential input and output and provides approximately 100 V/V gain. Its 60 MHz bandwidth and low noise characteristics (**1.3 nV/** $\sqrt{Hz}$ typical) provide substantial margins in most drives. The output should be AC coupled to delete the approximately 6 V output common mode voltage. Best results are obtained by limiting load capacitance to 20 pF and load current to 100 μA.

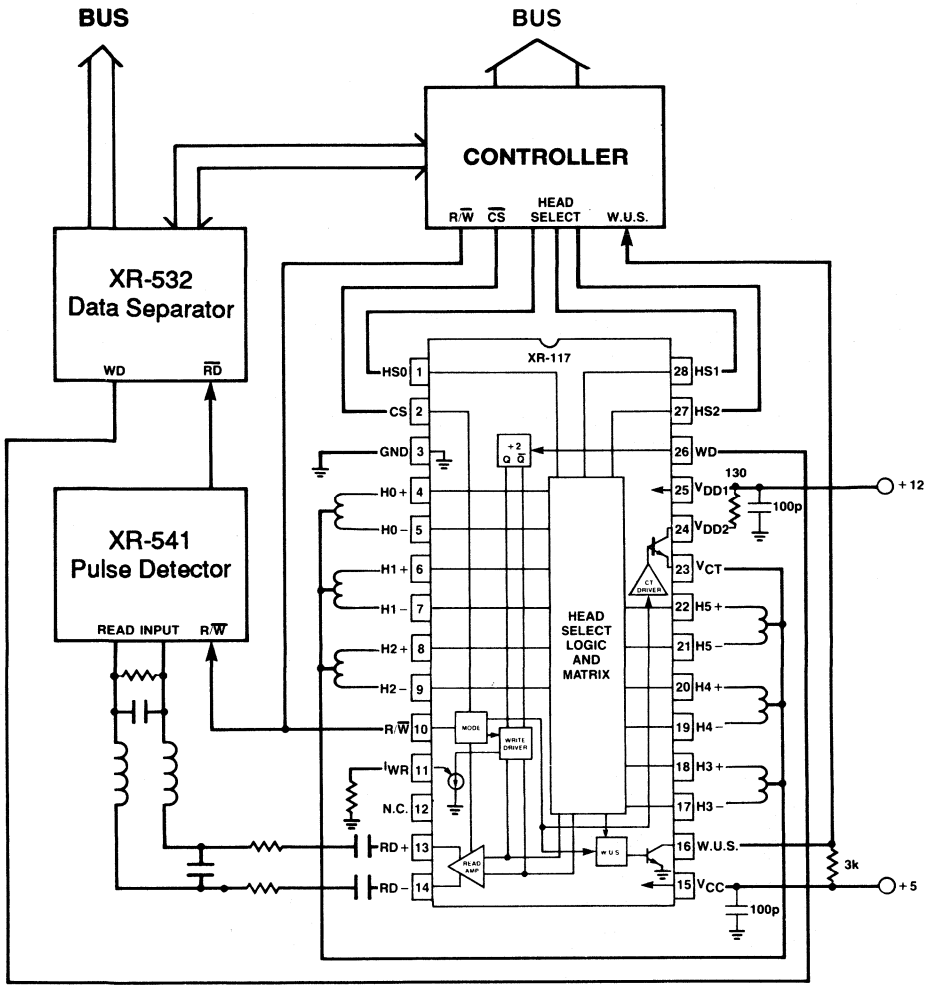
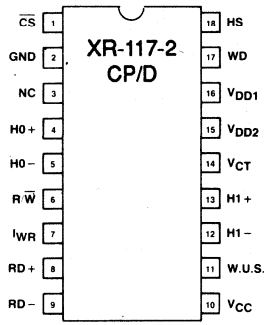
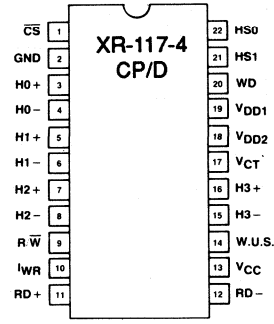
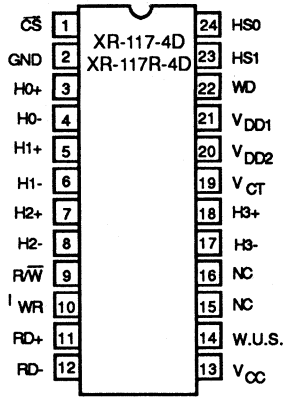


Figure 2. Hard Disk Read/Write Applications Circuit
Note: Circuit shown for XR-117R. Non-R versions require damping resistors across each head.







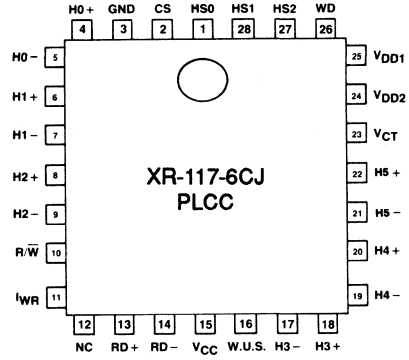


Figure 3. Additional Packages for XR-117 (Six head DIP shown in Functional Block Diagram, page 1)

Hard Disk Read/Write

GENERAL DESCRIPTION

The XR-501 is a high speed, low noise head interface integrated circuit for hard disk drives, performing both read and write functions. The XR-501 is compatible with 3½" to 14" multiple platter drives and features low noise, large dynamic range, and high bandwidth. Several packaging options extend usefulness to applications requiring six or eight center-tapped read/write heads. Multiple devices are easily cascaded for drives with more heads.

The XR-501 features a pinout with all head ports on one side of the circuit. This eases flex cable or PC board layout by eliminating crossovers. The XR-501R option includes internal damping resistors facilitating use in systems requiring minimum external circuit complexity.

XR-501, manufactured with a high speed bipolar process, operates on +5 V and +12 V. It is offered in a variety of packages, both surface mount and DIP.

FEATURES

Complete Head Interfacing Functions, Read and Write
Low Noise Preamplifier
High Dynamic Range and Bandwidth
Pinout Optimized for Easy Layout
Available in Six and Eight Head Versions
Easily Cascaded for Larger Systems
Full Featured Power Monitor
TTL Compatible Control Inputs

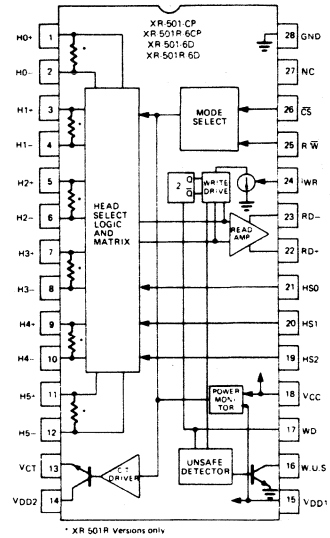
APPLICATIONS

Hard Disk Drives

ABSOLUTE MAXIMUM RATINGS

V_{DD}	15 V
V_{CC}	6 V
Digital Inputs	−0.3 V to V_{CC} +0.3 V
Write Current	60 mA
Junction Temperature	150°C
Storage Temperature	−65°C to 150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-501-6CP	28 Pin Plastic DIP	0°C to 70°C
XR-501-6CJ	28 Pin PLCC	0°C to 70°C
XR-501-6D	28 Pin SO	0°C to 70°C
XR-501-8CP	40 Pin Plastic DIP	0°C to 70°C
XR-501-8CJ	44 Pin PLCC	0°C to 70°C
XR-501-8D	32 Pin SO	0°C to 70°C
XR-501R-6CP*	28 Pin Plastic DIP	0°C to 70°C
XR-501R-6CJ	28 Pin PLCC	0°C to 70°C
XR-501R-6D	28 Pin SO	0°C to 70°C
XR-501R-8CP*	40 Pin Plastic DIP	0°C to 70°C
XR-501R-8CJ	44 Pin PLCC	0°C to 70°C
XR-501R-8D	32 Pin SO	0°C to 70°C

*Contact Factory for availability

SYSTEM DESCRIPTION

The XR-501 consists of a low noise preamplifier for reading from center tapped magnetic heads, a write current source for writing to the heads, a switching matrix to select one of eight heads, and associated control and monitoring functions. Less than **1.0 nV/√Hz** (nominal) noise allows error free operation with small input signals. Over 50 mA of write current output (user adjustable) means the disk signal can be large, further enhancing the read back signal-to-noise ratio for very low error rates.

ELECTRICAL SPECIFICATIONS

Test Conditions: $T_A = 25°C$, $V_{CC} = 5$ V, $V_{DD} = 12$ V, $I_W = 40$ mA, $R_D = 750\Omega$, C_L (R_{D+},R_{D-}) ≤ 20 pF, Data Rate = 5 MHz, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
I_{CC}	Supply Current			25	mA	$V_{CC} = 5.5$ V, Read or Idle Mode
				26	mA	$V_{CC} = 5.5$ V, Write Mode
I_{DD}	Supply Current			20	mA	$V_{DD} = 13.2$ V, Idle Mode
				40	mA	$V_{DD} = 13.2$ V, Read Mode
				20	mA	$V_{DD} = 13.2$ V, Write Mode, $I_W = 0$ mA
PD	Power Dissipation			400	mW	Idle Mode - $V_{CC} = 5.5$ V, $V_{DD} = 13.2$ V
				600	mW	Read Mode - $V_{CC} = 5.5$ V, $V_{DD} = 13.2$ V
				750	mW	$I_W = 50$ mA, $R_{CT} = 160\Omega$
				1050	mW	$I_W = 50$ mA, $R_{CT} = 0\Omega$
V_{CT}	Center Tap Voltage		4.5		V	Read Mode
			6.5		V	Write Mode
V_{PM}	Power Monitor Protection	3.7	4.0	4.4	V	V_{CC} to Disable Write
		8.5	9.6	10.5	V	V_{DD1} to Disable Write
DIGITAL CHARACTERISTICS						
W.U.S.	Write Unsafe Output					
V_{OL}	Saturation Voltage		0.2	0.5	V	$I_{OL} = 8$ mA
I_{OH}	Leakage Current			100	μA	$V_{OH} = 5$ V
V_{IL}	Input Low Voltage			0.8	V	All digital inputs
V_{IH}	Input High Voltage	2.0			V	All digital inputs
I_{IL}	Input Low Current	−0.4			mA	All digital inputs, $V_{IL} = 0.8$ V
I_{IH}	Input High Current			100	μA	All digital inputs, $V_{IH} = 2.0$ V
WRITE CHARACTERISTICS						
	Write Current Accuracy	−7		7	%	Error from $I_W = \frac{140}{R_W}$
	Recommended Write Current Range	10		50	mA	
	Differential Head Voltage Swing	7.0	11		V	Peak (Inductive Load)
	Unselected Differential Head Current			85	μA	
	Unselected Transient Current			2	mA	Peak
	Differential Output Capacitance			15	pF	

	Differential Output Resistance	10 635	750	865	kΩ Ω	XR-501 XR-501R
	WD Rate/Transistion Freq.	125	500		kHz	
K_I	Current Source Factor		20			$K_I = I_W/(\text{Current through } R_W)$
K	Write Current Constant	129	140	151	V	$I_W = K/R_W$
	Write Protection Leakage Current	−200		200	μA	Per Side, $V_{CC} \leq 3.7$ V $V_{DD} \leq 8.7$ V
V_{OS}	Preamplifier Output Offset Voltage	−20		+20	mV	Write or Idle Mode
V_{CM}	Preamplifier Output Common Mode Voltage		5.3		V	Write or Idle Mode
	Preamplifier Output Leakage Current	−50		50	μA	Write or Idle Mode, $R_{D+} = R_{D-} = 6$ V
READ MODE						
A_V	Differential Voltage Gain	80		120	V/V	V_{IN} = 1 mVp-p at 300 kHz, $R_{L+} = R_{L-} = 1k\Omega$
	Dynamic Range	−3		+3		DC input voltage where gain drops 10%. $V_{IN} = V_i + 0.5$ mVp-p at 300 kHz.
R_{IN}	Differential Input Resistance	2 530	8 650	790	kΩ Ω	XR-501 XR-501R
C_{IN}	Differential Input Capacitance			23	pF	
e_{ni}	Input Noise Voltage		1.0	1.5	$nV/\sqrt{Hz}$	$L_h = 0$, $R_h = 0$, BW = 15 MHz
BW	Bandwidth	30	60		MHz	−3 dB Point, $\lvert Z_s \rvert \leq 5\Omega$, V_{in} = 1 mVp-p
I_B	Input Bias Current		10	100	μA	
CMRR	Common Mode Rejection Ratio	50	60		dB	$V_{CM} = V_{CT}$ + 100 mVp-p at 5 MHz
PSRR	Power Supply Rejection Ratio	45	60		dB	100 mVp-p at 5 MHz Superimposed on V_{DD1}, V_{DD2} or V_{CC}
	Channel Separation	45	60			Unselected Channel: V_{IN} = 100 mVp-p at 5 MHz. Selected Channel V_{IN} = 0 V
	Output Offset Voltage	−480	±50	480	mV	
V_{CM}	Common Mode Output Voltage	5.0	6.2	7	V	
	Head Current Leakage	−200		200	μA	Per Side

R_O	Single Ended Output Resistance			30	Ω	f = 5 MHz
I_O	Output Current	2.1			mA	AC Coupled, Source or Sink
SWITCHING CHARACTERISTICS						
R/W	Read to Write		0.1	0.6	µS	Note 1
	Write to Read		0.1	0.6	µS	Note 1,3
CS	Start-up Delay		0.1	0.6	µS	Note 1,2
	Inhibit Delay		0.1	0.6	µS	Note 3
	Head Switching Delay		0.1	0.6	µS	Note 2, Switching between any heads.
WUS	Write Unsafe					
	Safe to Unsafe	1.6		8.0	µS	I_W = 50 mA, See Figure 1, TD1
	Unsafe to Safe		0.2	1	µS	I_W = 20 mA, See Figure 1, TD2
I_W	Head Current					
	Propagation Delay			30	nS	Note 4, See Figure 1, TD3
	Asymmetry			2	nS	Note 5
	Rise or Fall Time			20	nS	10% to 90% or 90% to 10% point

Note 1: Delay to 90% of I_W.
Note 2: Delay to 90% of 100 mVp-p 10 MHz Read Signal Envelope.
Note 3: Delay to 90% Decay of I_W.
Note 4: From 50% Points. L_h = 0H, R_h = 0Ω.
Note 5. Write Data with 1 nS rise and fall times and 50% duty cycle.

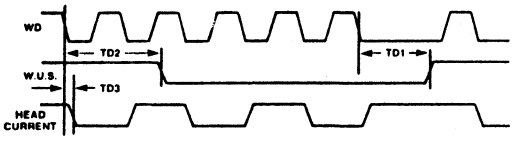


Figure 1. Write Mode Timing Diagram

A full-featured power monitor circuit disables the write mode during power-up and low operating voltage conditions, protecting data integrity.

CAUTION: This device may be damaged by electrostatic discharge. ESD precautions should be taken.

PRINCIPLES OF OPERATION

Write Mode

Before writing may begin, both chip select ($\overline{CS}$) and Read/Write (R/$\overline{W}$) must be pulled low. The desired head, selected by HS0 to HS2, is driven by a differential current sink of magnitude I_W, set by R_{IW}. Input data is applied to a falling edge triggered toggle flip-flop, which in turn selects the active side of the center tapped write head.

Current is sourced through the center tap driver, V_{CT}, which is "high" in the write mode. Write unsafe (W.U.S.) signals the disk controller whenever one of six error conditions exist and writing should be discontinued. The six faults are: open head, open center tap, no write current, write data frequency too low, device unselected, and writing attempted while the device is in the read mode. The power supply monitor disables writing when V_{CC} drops below 4 V and/or V_{DD1} drops below 9 V.

Read Mode

Pulling R/$\overline{W}$ high enables the data readback mode. A low noise, high gain differential amplifier increases the weak read signal amplitude and provides low output impedance drive for the following stage (Pulse Detector).

APPLICATIONS INFORMATION

As with all high frequency, high gain systems, layout is critical. Lead lengths should be minimized and supplies should be well bypassed. The XR-501 is available in small outline surface mount and PLCC packages, facilitating installation near the drive heads. The XR-501R option has 750Ω internal damping resistors across each head input, further aiding the goal of short lead lengths by eliminating the need for external resistors. The XR-501R option is especially convenient when the device is mounted on the flexible cable connecting the heads, as internal damping resistors reduce layout complexity, parts counts, and mass.

The high frequency characteristics of the XR-501 lead to a certain degree of electrostatic discharge (ESD) susceptability, so static reducing precautions should be taken.

Write Mode Design Considerations

Write current, I_W, typically between 20 mA and 50 mA, is determined by a single resistor, R_{IW}.

$$R_{IW} = \frac{140{,}000}{I_W}$$

where I_W is in mA and R_{IW} is in ohms.

Device power dissipation is reduced by a resistor, R_{CT}, connecting V_{DD2} to the +12 V supply. Some of the center tap driver voltage is then dropped across the resistor.

With the nominal 12 V supply, R_{CT}, is calculated as

$$R_{CT} = 130\left(\frac{55}{I_W}\right)$$

where R_{CT} is in ohms and I_W is in milliamperes.

Internal dissipation reduction is primarily a consideration with high write current levels and small surface mount packages. All XR-501 packages are suitable for continuous operation under worst case conditions without requiring R_{CT}. If R_{CT} is not used, V_{DD2} is directly connected to V_{DD1}.

Write center tap circuitry is designed for higher stability than similar devices from other manufacturers. If extreme conditions exist, a ferrite bead around the V_{CT} line to the heads will reduce overshoot and ringing .

Write Unsafe Indicator (W.U.S.)

Write unsafe (W.U.S.) pulls high whenever one or more of six write error conditions exist. Four conditions; open head, open center tap, no write current and write data transition rate too low are detected with a differential capacitor charge/discharge circuit. Device unselected and read mode digital ccnditions also force W.U.S. high.

After removal of the fault condition, two negative write data transitions are required to clear W.U.S. This output is for indication only, intended for signaling a controller, and does not directly impede device operation. A pull-up resistor of from 2 kΩ to 10 kΩ is necessary for operation of this open collector output.

Power Monitor Considerations

A power monitor circuit protects data integrity by preventing erroneous writing during power up and low voltage periods. The power monitor disables write current when V_{CC} is below about 4 V and/or V_{DD1} is below about 9 V. Hysteresis avoids unwanted toggling about the thresholds. At V_{CC} and V_{DD1} levels above these thresholds, operation is fully controllable.

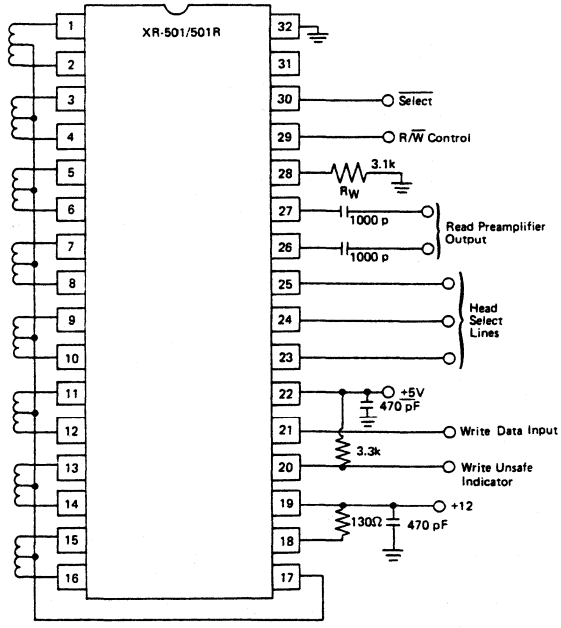
Device operation at standard voltages (V_{CC} = 5 V ± 10%, V_{DD1} = 12 V ± 10%) is not affected in any way and is fully specified.

Read mode operation is not affected by the power monitor circuitry.

Read Mode Design Considerations

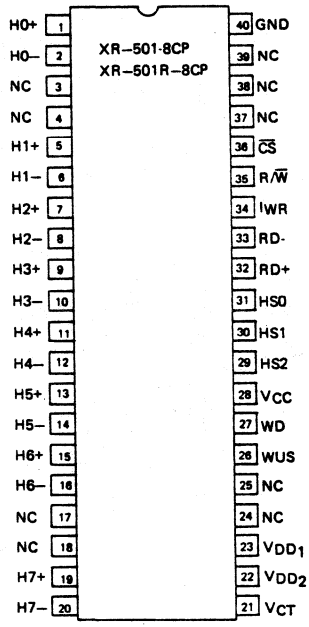
The read amp has a fully differential input and output and provides approximately 100 V/V gain. Its 60 MHz bandwidth and low noise characteristics (1.0 nV/ $\sqrt{Hz}$ typical) provide substantial margins in most drives. The output should be AC coupled to delete the approximately 5.5 V output common mode voltage. Best results are obtained by limiting load capacitance to 20 pF and load current to 100 μA.

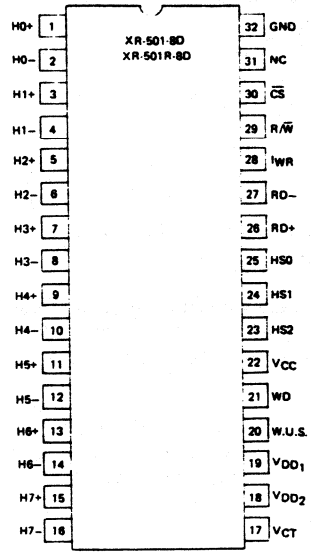
The XR-501 read preamplifier is specially designed to minimize output common mode voltage changes between write mode and read mode, thus reducing switching transients that slow write to read recovery time.

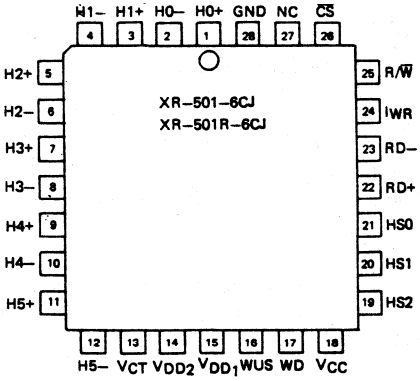


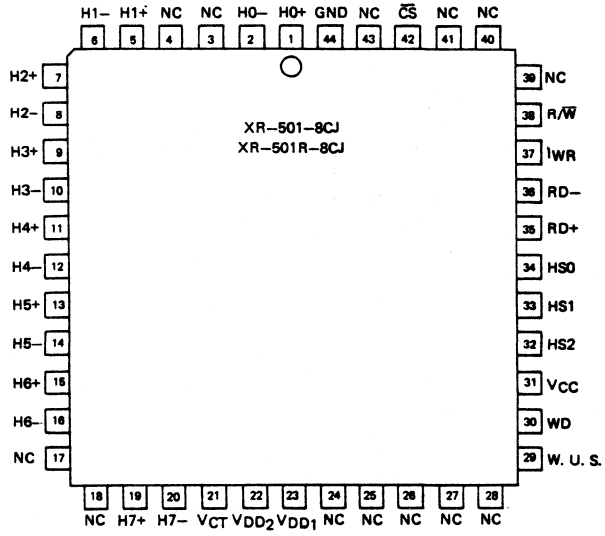
XR-501R Typical Application Circuit

NOTE: Non 'R' Versions Require External Damping Resistors









XR-501-6CP/501R-6CP/501-6D/501R-6D 28 Pin Package Pinout shown on front page.

Low Power Single Supply Disk Drive Read/Write Amplifier

GENERAL DESCRIPTION

The XR-505 is a monolithic disk drive integrated circuit providing read mode preamplification, write current control, and head selection. It requires a single +5V power supply and consumes far less power than similar devices.

Up to four read/write heads can be switched with one device; multiple devices are cascadable. A low noise read signal preamplifier provides two user selectable gain levels.

All digital controls are TTL compatible. The XR-505 is available in 16, 20 and 24 pin SO packages. A 24 Pin DIP version is available for evaluation.

FEATURES

Complete Head Interface Functions, Read and Write
Low Power, Single +5V Operation
High Bandwidth and Dynamic Range
Low Noise Preamplifier
Error Preventing Power Monitor
Pinout Designed for Layout Ease
Digitally Selectable Preamplifier Gain
Digitally Selectable Write Current

APPLICATIONS

Battery operated Winchester disk drives
Low power disk drives
High density floppy disk drives
Digital tape drives
Dedicated servo read/write

ABSOLUTE MAXIMUM RATINGS

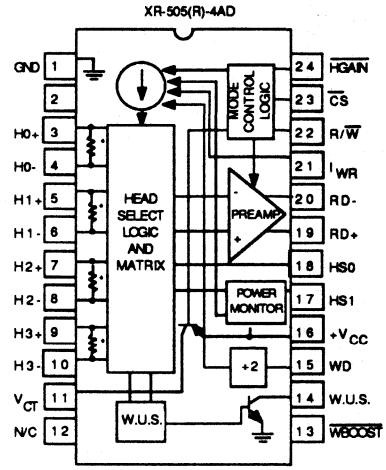
V_{CC}	8 Volts
Digital Inputs	-0.3V to V_{CC} +0.3V
Write Current	70mA
Junction Temperature	150° C
Storage Temperature	-65° C to +150°C

SYSTEM DESCRIPTION

The XR-505 is a low power four channel Winchester Disk Drive Read/Write Amplifier ideally suited for laptop computer system drives and other applications where power consumption is important. Similar in function to other Exar Read/Write amplifiers, the XR-505 provides equivalent or superior performance at one-fourth the power consumption and requires only a single +5V power supply.

The read preamplifier section consists of a 55MHz bandwidth 1nV/$\sqrt{Hz}$ noise level differential amplifier. Preamplifier gain of either 100 V/V or 200 V/V is digitally selectable. The write driver controls up to 50mA of write current. A full featured power monitor circuit positively disables write mode operation during low voltage fault conditions to preserve data integrity.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-505-4D	24 JEDEC SO	0° C to 70° C
XR-505R-4D	24 JEDEC SO	0° C to 70° C
XR-505R-4AD	20 JEDEC SO	0° C to 70° C
XR-505R-4BD	20 JEDEC SO	0° C to 70° C
XR-505R-2AD	16 JEDEC SO	0° C to 70° C
XR-505-2BD	16 JEDEC SO	0° C to 70° C
XR-505R-2AD	16 JEDEC SO	0° C to 70° C
XR-505R-2BD	16 JEDEC SO	0° C to 70° C
XR-505R-2AG	16 JEDEC SO	0° C to 70° C
XR-505R-2BG	16 JEDEC SO	0° C to 70° C
XR-505- 4CP	24 DIP	0° C to 70° C

(other versions and packages available upon request)

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25° C, V_{CC} = 4.5V to 5.5V (5.0V nominal), I_W = 25 mA, R_D = 750Ω, C_L (R_{D+}, R_{D-}) ≤ 20 pF, Lh = 10 µH, Data Rate = 5 MHz, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{CC}	Supply Current		25	35	mA	V_{CC} = 5.5V, Read
			20	30	mA	V_{CC} = 5.5V, Write Mode I_W = 0
P_D	Power Dissipation		0.5	1	mW	Idle Mode. V_{CC} = 5.5V
			125	170	mW	Read Mode. V_{CC} = 5.5V,
			100	150	mW	Write Mode: I_W = 0mA . V_{CC} = 5.5V
V_{CT}	Center Tap Voltage		2.1		V	Read Mode. V_{CC} = 5V
			4.5		V	Write Mode. V_{CC} = 5V
V_{PM}	Power Monitor Protection	3.7	4.0	4.4	V	V_{CC} to Disable Write
DIGITAL CHARACTERISTICS						
W.U.S. V_{OL}	Write Unsafe Output Saturation Voltage		0.2	0.5	V	I_{OL} = 8mA
I_{OH}	Leakage Current			100	µA	V_{OH} = 5V
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IL}	Input Low Current	-0.4			mA	V_{IL} = 0.8V
I_{IH}	Input High Current			100	µA	V_{IH} = 2.0V
WRITE CHARACTERISTICS						
	Write Current Accuracy	-7	±2	7	%	Error from $I_W = \frac{0.47V}{R_W}$ See Fig.2
	Recommended Write Current Range	10		40	mA	
WBOOST	Write Current Boost Factor	1.20	1.25	1.30	I/I	$\overline{\text{WBOOST}}$ = Low
	Differential Head Voltage Swing	7.0	8.2		V	Peak (Inductive Load), L_h =10µH Iw = 40mA
	DC Swing	3.5	4		V	DC Load, One Side
	Unselected Differential Head Current			85	µA	
	Unselected Transient Current			2	mA	Peak
	Differential Output Capacitance			15	pF	
	Differential Output Resistance	10			kΩ	XR-505
		635	750	865	Ω	XR-505R
W.U.S.	WD Rate/Transition Freq.	125			kHz	
K_I	Current Source Factor		1			K_I = I_W/(Current through R_W)
K	Write Current Constant	440	470	500	mV	K = 1000 I_W • R_W
	Write Protection Shut-off Leakage Current	-200		+200	µA	Per Side, V_{CC} ≤ 3.7V
V_{OS}	Preamplifier Output Offset Voltage	-20		+20	mV	Write or Idle Mode

4

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{CM}	Preamplifier Output Common Mode Voltage		1.5		V	Write Mode
	Preamplifier Output Leakage Current	-100		+100	µA	Write or Idle Mode, $R_{D+} = R_{D-} = 6V$
READ MODE						
A_V	Differential Voltage Gain	85	100	115	V/V	$\overline{HGAIN}$= High, V_{IN} =1mVp-p at 300 kHz, $R_{L+} = R_{L-} = 1k\Omega$
		170	200	230	V/V	$\overline{HGAIN}$ = Low
	Dynamic Range	-3		+3	mV	DC input voltage where gain drops 10%. $V_{in} = V_i + 0.5$ mVp-p at 300 kHz.
R_{IN}	Differential Input Resistance	2	8		kΩ	XR-505
		500	650	850	Ω	XR-505R
C_{IN}	Differential Input Capacitance			20	pF	
e_{ni}	Input Noise Voltage		1.0	1.5	nV /√Hz	$L_h = 0$, $R_h = 0$, BW = 15MHz
BW	Bandwidth	30	60		MHz	-3dB Point, $\|Z_s\| \leq 5\Omega$, V_{in} = 1mVp-p
I_B	Input Bias Current		10	45	µA	
CMRR	Common Mode Rejection Ratio	60	80		dB	$V_{CM} = V_{CT}$ + 100mVp-p at 5MHz
PSRR	Power Supply Rejection Ration	60	80		dB	100mVp-p at 5 MHz Superimposed on V_{CC}
	Channel Separation	45	60			Unselected Channel: V_{IN} = 100 mVp-p at 5 MHz. Selected Channel V_{IN} = 0V
V_{OS}	Output Offset Voltage	-200	±50	+200	mV	
ΔV_{OS}	Output Offset Voltage Change	-100	±20	+100	mV	Switching Between Any Two Heads
V_{CM}	Common Mode Output Voltage	1.25	1.50	1.75	V	
ΔV_{CM}	V_{CM} Change from Write to Read	-200	+100	+200	mV	Common Mode Output Voltage Change from Write to Read or Read to Write
	Head Current Leakage	-200		+200	µA	Per Side
R_O	Single Ended Output Resistance			30	Ω	f = 5 MHz
I_O	Output Current	2.1			mA	AC Coupled, Source or Sink

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
SWITCHING CHARACTERISTICS						
R/$\overline{W}$	Read to Write		0.1	1	µS	Note 1
	Write to Read		0.1	1	µS	Notes 2, 3
$\overline{CS}$	Start-up Delay		0.1	1	µS	Notes 1, 2
	Inhibit Delay		0.1	1	µS	Note 3
	Head Switching Delay		0.1	1	µS	Note 2, Switching between any heads.
W.U.S.	Write Unsafe					
	Safe to Unsafe	1.6		8.0	µS	I_W = 25 mA, See Figure 1, TD1
	Unsafe to Safe		0.2	1	µS	I_W = 25 mA, See Figure 1, TD2
I_W	Head Current					
	Propagation Delay		2	25	nS	Note 4, See Figure 1, TD3
	Asymmetry		0.1	2	nS	Note 5
	Rise or Fall Time		1	20	nS	10% to 90% or 90% to 10% point

Note 1: Delay to 90% of I_W.
Note 2: Delay to 90% of 100 mVp-p 10 MHz Read Signal Envelope.
Note 3: Delay to 90% Decay of I_W.
Note 4: From 50% Points. L_h = 0H, R_h =0Ω
Note 5: Write Data with 1 nS rise and fall times and 50% duty cycle.

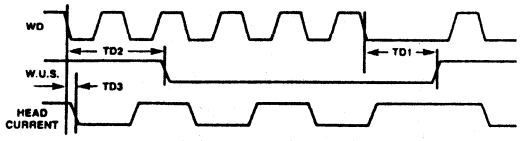


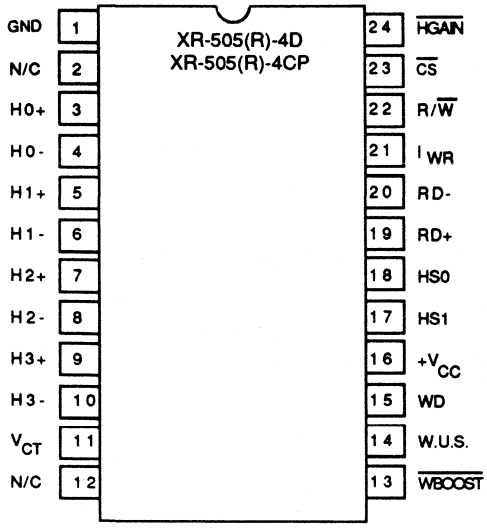
Figure 1. Write Mode Timing Diagram

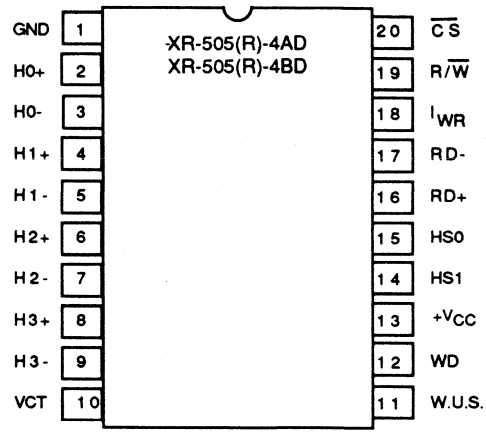
XR-505 PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
$\overline{CS}$	Chip Select	Low enables device operation
R/$\overline{W}$	Read/Write Select	High selects read mode Low selects write mode
WD	Write Data Input	
$\overline{HGAIN}$	High Gain Select	Low selects preamp gain of 200V/V High selects preamp gain of 100V/V
W.U.S.	Write Unsafe Output	Open collector output. High indicates write fault condition
HS0, HS1	Head Select	Selects head for Read/Write operation
V_{CC}	+5V Supply Input	
R_{D+}, R_{D-}	Read Preamplifier	Differential preamplifier output
I_{WR}	Write Current	Resistor to ground programs peak write current level
$\overline{WBOOST}$	Write Current Boost	Low Selects, I_W Boost of $I_W = 1.25 \cdot \frac{0.47}{R_W}$ High Selects Nominal $I_W = \frac{0.47}{R_W}$

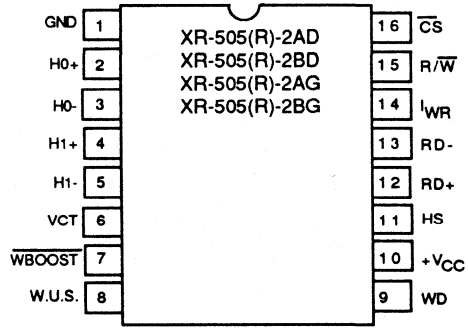
XR-505 DIGITAL CONTROLS

CONTROL PIN						FUNCTION
$\overline{CS}$	R/$\overline{W}$	$\overline{HGAIN}$	$\overline{WBOOST}$	HS1	HS0	
1	X	X	X	X	X	Device Disabled
0	0	X	0	0	0	Write Mode, Head 0, Iw = Boost
0	0	X	0	0	1	Write Mode, Head 1, Iw = Boost
0	0	X	0	1	0	Write Mode, Head 2, Iw = Boost
0	0	X	0	1	1	Write Mode, Head 3, Iw = Boost
0	0	X	1	0	0	Write Mode, Head 0, Iw = Normal
0	0	X	1	0	1	Write Mode, Head 1, Iw = Normal
0	0	X	1	1	0	Write Mode, Head 2, Iw = Normal
0	0	X	1	1	1	Write Mode, Head 3, Iw = Normal
0	1	0	X	0	0	Read Mode, Head 0, Preamp A_V = 200
0	1	0	X	0	1	Read Mode, Head 1, Preamp A_V = 200
0	1	0	X	1	0	Read Mode, Head 2, Preamp A_V = 200
0	1	0	X	1	1	Read Mode, Head 3, Preamp A_V = 200
0	1	1	X	0	0	Read Mode, Head 0, Preamp A_V = 100
0	1	1	X	0	1	Read Mode, Head 1, Preamp A_V = 100
0	1	1	X	1	0	Read Mode, Head 2, Preamp A_V = 100
0	1	1	X	1	1	Read Mode, Head 3, Preamp A_V = 100





Fixed Gain Version



Two Head Version

XR-505 Packaging Options

Device	HGain	WBoost	Package
XR-505(R)-4D	100/200	1.0/1.25	24 SO
XR-505(R)-4AD	100	1.0	20 SO
XR-505(R)-4BD	200	1.0	20 SO
XR-505(R)-2AD	100	1.0/1.25	16 SO
XR-505(R)-2BD	200	1.0/1.25	16 SO
XR-505(R)-2AG	100	1.0/1.25	16 SO
XR-505(R)-2BG	200	1.0/1.25	16 SO
XR-505(R)-4CP	100/200	1.0/1.25	24 DIP

"G" Package is 150 mil JEDEC S.O.

PRELIMINARY DATA SHEET

GENERAL DESCRIPTION

The XR-510A is a high speed, low noise head interface integrated circuit for hard disk drives, performing both read and write functions. The XR-510A is compatible with 2" to 14" single and multiple platter drives and features low noise, large dynamic range, and high bandwidth. Several packaging options extend usefulness to applications requiring from two to six center-tapped read/write heads. Multiple devices are easily cascaded for drives with more heads.

The XR-510AR option includes internal damping resistors facilitating use in systems requiring minimum external circuit complexity.

XR-510A, manufactured with a high speed bipolar process, operates on +5 V and +12 V. It is offered in a variety of packages, both surface mount and DIP.

FEATURES

Complete Head Interfacing Functions, Read and Write
Low Noise Preamplifier
High Dynamic Range and Bandwidth
Available in Two, Four and Six Head Versions
Easily Cascaded for Larger Systems
Full Featured Power Monitor
TTL Compatible Control Inputs
Optional Internal Damping Resistors
Fast Settling Time

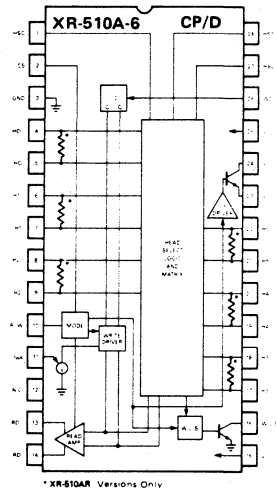
APPLICATIONS

Hard Disk Drives
"Wedge" Servo Drives

ABSOLUTE MAXIMUM RATINGS

V_{DD}	15 V
V_{CC}	6 V
Digital Inputs	−0.3 V to V_{CC} +0.3 V
Write Current	60 mA
Junction Temperature	150°C
Storage Temperature	−65°C to 150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-510A-2CP	18 Pin Plastic DIP	0°C to 70°C
XR-510A-2D	18 Pin S.O.	0°C to 70°C
XR-510A-4CP	22 Pin Plastic DIP	0°C to 70°C
XR-510A-4D	24 Pin S.O.	0°C to 70°C
XR-510A-6CP	28 Pin Plastic Dip	0°C to 70°C
XR-510A-6CJ	28 Pin PLCC	0°C to 70°C
XR-510A-6D	28 Pin S.O.	0°C to 70°C
XR-510AR-2CP	18 Pin Plastic DIP	0°C to 70°C
XR-510AR-2D	18 Pin S.O.	0°C to 70°C
XR-510AR-4CP	22 Pin Plastic DIP	0°C to 70°C
XR-510AR-4D	24 Pin S.O.	0°C to 70°C
XR-510AR-6CP	28 Pin Plastic DIP	0°C to 70°C
XR-510AR-6CJ	28 Pin PLCC	0°C to 70°C
XR-510AR-6D	28 Pin S.O.	0°C to 70°C

SYSTEM DESCRIPTION

The XR-510A consists of a low noise preamplifier for reading from center tapped magnetic heads, a write current source for writing to the heads, a switching matrix to select one of six heads, and associated control and monitoring functions. Less than 1.0nV/$\sqrt{Hz}$ (nominal) noise allows error free operation with small input signals. Over 40 mA of write current output (user adjustable) means the disk signal can be large, further enhancing the read back signal-to-noise ratio for very low error rates. Preamplifier offset voltages are low, aiding use in "wedge" servo drives and in other applications where rapid system settling times are needed.

ELECTRICAL SPECIFICATIONS

Test Conditions: $T_A = 25°C$, $V_{CC} = 5$ V, $V_{DD} = 12$ V, $I_W = 40$ mA, $R_D = 750\Omega$, C_L (R_{D+},R_{D-}) ≤ 20 pF, Data Rate = 5 MHz, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
I_{CC}	Supply Current			35	mA	V_{CC} = 5.5 V, Read or Idle Mode
				30	mA	V_{CC} = 5.5 V, Write Mode
I_{DD}	Supply Current			20	mA	V_{DD} = 13.2 V, Idle Mode
				40	mA	V_{DD} = 13.2 V, Read Mode
				20	mA	V_{DD} = 13.2 V, Write Mode, I_W = 0 mA
PD	Power Dissipation			400	mW	Idle Mode - V_{CC} = 5.5 V, V_{DD} = 13.2 V
				600	mW	Read Mode - V_{CC} = 5.5 V, V_{DD} = 13.2 V
				670	mW	I_W = 40 mA, R_{CT} = 160Ω
				800	mW	I_W = 40 mA, R_{CT} = 0Ω
V_{CT}	Center Tap Voltage		5.0		V	Read Mode
			7.0		V	Write Mode
V_{PM}	Power Monitor Protection	3.7	4.0	4.4	V	V_{CC} to Disable Write
		8.5	9.6	10.5	V	V_{DD1} to Disable Write
DIGITAL CHARACTERISTICS						
WUS	Write Unsafe Output					
V_{OL}	Saturation Voltage		0.2	0.5	V	I_{OL} = 8 mA
I_{OH}	Leakage Current			100	μA	V_{OH} = 5 V
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IL}	Input Low Current	−0.4			mA	V_{IL} = 0.8 V
I_{IH}	Input High Current			100	μA	V_{IH} = 2.0 V
WRITE CHARACTERISTICS						
	Write Current Accuracy	−5		5	%	Error from $I_W = \frac{2.5V}{R_W}$
	Recommended Write Current Range	10		40	mA	
	Differential Head Voltage Swing	7.0	11		V	Peak (Inductive Load)
	Unselected Differential Head Current			85	μA	Peak
	Unselected Transient Current			2	mA	Peak

4

	Differential Output Capacitance			15	pF	
	Differential Output Resistance	10 635	 750	 865	kΩ Ω	XR-510A XR-510AR
	WD Rate/Transistion Freq.	250	500		kHz	
K_I	Current Source Factor		1			$K_I = I_W/(\text{Current through } R_W)$
K	Write Current Constant	2.375	2.50	2.625	V	$I_W = K/R_W$
	Write Protection Leakage Current	−200		200	μA	Per Side, $V_{CC} \leq 3.7$ V and/or $V_{DD} \leq 8.5$ V
V_{OS}	Preamplifier Output Offset Voltage	−20		+20	mV	Write or Idle Mode
V_{CM}	Preamplifier Output Common Mode Voltage		5.3		V	Write or Idle Mode
	Preamplifier Output Leakage Current	−100		100	μA	Write or Idle Mode, $R_{D+} = R_{D-} = 6$ V
READ MODE						
A_V	Differential Voltage Gain	85		115	V/V	$V_{IN} = 1$ mVp-p at 300 kHz, $R_{L+} = R_{L-} = 1k\Omega$
	Dynamic Range	−3		+3	mV	DC input voltage where gain drops 10%. $V_{in} = V_i + 0.5$ mVp-p at 300 kHz.
R_{IN}	Differential Input Resistance	2 500	8 650	 850	kΩ Ω	XR-510 XR-510AR
C_{IN}	Differential Input Capacitance			20	pF	
e_{ni}	Input Noise Voltage		1.0	1.5	$nV/\sqrt{Hz}$	$L_h = 0$, $R_h = 0$, BW = 15 MHz
BW	Bandwidth	30	60		MHz	−3 dB Point, $\lvert Z_s \rvert \leq 5\Omega$, $V_{in} = 1$ mVp-p
I_B	Input Bias Current		10	45	μA	
CMRR	Common Mode Rejection Ratio	50	60		dB	$V_{CM} = V_{CT} + 100$ mVp-p at 5 MHz
PSRR	Power Supply Rejection Ratio	45	60		dB	100 mVp-p at 5 MHz Superimposed on V_{DD1}, V_{DD2} or V_{CC}

	Channel Separation	45	60		dB	Unselected Channel: V_{IN} = 100 mVp-p at 5 MHz. Selected Channel V_{IN} = 0 V
V_{OS} Out	Output Offset Voltage	—440	±50	440	mV	
ΔV_{OS}	Output Offset Voltage Change		±20		mV	Switching between any two heads
V_{CM}	Common Mode Output Voltage	4.5	5.5	6.5	V	
ΔV_{CM}	V_{CM} Change from Write to Read		500		mV	Common Mode Output Voltage Change from Write to Read or Read to Write
	Head Current Leakage	—200		200	μA	Per Side
R_O	Single Ended Output Resistance			30	Ω	f = 5 MHz
I_O	Output Current	2.1			mA	AC Coupled, Source or Sink
SWITCHING CHARACTERISTICS						
R/$\overline{W}$	Read to Write		0.1	1	μS	Note 1
	Write to Read		0.1	1	μS	Notes 2,3
$\overline{CS}$	Start-up Delay		0.1	1	μS	Notes 1,2
	Inhibit Delay		0.1	1	μS	Note 3
	Head Switching Delay		0.1	1	μS	Note 2, Switching between any heads.
W.U.S.	Write Unsafe					
	Safe to Unsafe	1.6	2	8.0	μS	I_W = 35 mA, See Figure 1, TD1
	Unsafe to Safe		0.2	1	μS	I_W = 35 mA, See Figure 1, TD2
I_W	Head Current					
	Propagation Delay		2	25	nS	Note 4, See Figure 1, TD3
	Asymmetry		0.1	2	nS	Note 5
	Rise or Fall Time		1	20	nS	10% to 90% or 90% to 10% point

Note 1: Delay to 90% of I_W.
Note 2: Delay to 90% of 100 mVp-p 10 MHz Read Signal Envelope.
Note 3: Delay to 90% Decay of I_W.
Note 4: From 50% Points. L_h = 0H, R_h = 0Ω.
Note 5: Write Data with 1 nS rise and fall times and 50% duty cycle.

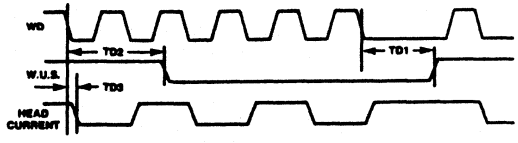


Figure 1. Write Mode Timing Diagram

A full-featured power monitor circuit disables the write mode during power-up and low operating voltage conditions, protecting data integrity. Improved write stability over 117-type devices is achieved by employing a unity gain write current constant.

CAUTION: This device may be damaged by electrostatic discharge. ESD precautions should be taken.

PRINCIPLES OF OPERATION

Write Mode

Before writing may begin, both chip select ($\overline{CS}$) and Read/Write (R/$\overline{W}$) must be pulled low. The desired head, selected by HS0 to HS2, is driven by a differential current sink of magnitude I_W, set by R_{IW}. Input data is applied to a falling edge triggered toggle flip-flop, which in turn selects the active side of the center tapped write head.

Current is sourced through the center tap driver, V_{CT}, which is "high" in the write mode. Write unsafe (W.U.S.) signals the disk controller whenever one of six error conditions exist and writing should be discontinued. The six faults are: -open head, open center tap, no write current, write data frequency too low, device unselected, and writing attempted while the device is in the read mode. The power supply monitor disables writing when V_{CC} drops below 4 V and/or V_{DD1} drops below 9 V.

Read Mode

Pulling R/$\overline{W}$ high enables the data readback mode. A low noise, high gain differential amplifier increases the weak read signal amplitude and provides low output impedance drive for the following stage (Pulse Detector).

APPLICATIONS INFORMATION

As with all high frequency, high gain systems, layout is critical. Lead lengths should be minimized and supplies should be well bypassed. The XR-510A is available in small outline surface mount and PLCC packages, facilitating installation near the drive heads. The XR-510AR option has 750Ω internal damping resistors across each head input, further aiding the goal of short lead lengths by eliminating the need for external resistors. The XR-510AR option is especially convenient when the device is mounted on the flexible cable connecting the heads, as internal damping resistors reduce layout complexity, parts counts, and mass.

The high frequency characteristics of the XR-510A lead to a certain degree of electrostatic discharge (ESD) susceptability, so static reducing precautions should be taken.

Write Mode Design Considerations

Write current, I_W, typically between 20 mA and 40 mA, is determined by a single resistor, R_{IW}.

$$R_{IW} = \frac{2500}{I_W}$$

where I_W is in mA and R_{IW} is in ohms.

Device power dissipation is reduced by a resistor, R_{CT}, connecting V_{DD2} to the +12 V supply. Some of the center tap driver voltage is then dropped across the resistor.

With the nominal 12 V supply, R_{CT}, is calculated as

$$R_{CT} = 150\ (\frac{40}{I_W})$$

where R_{CT} is in ohms and I_W is in milliamperes.

Internal dissipation reduction is primarily a consideration with high write current levels and small surface mount packages. If R_{CT} is not used, V_{DD2} is directly connected to V_{DD1}.

Write Unsafe Indicator (W.U.S.)

Write unsafe (W.U.S.) pulls high whenever one or more of six write error conditions exists. Four conditions; open head, open center tap, no write current and write data transition rate too low are detected with a differential capacitor charge/discharge circuit. Device unselected and read mode digital conditions also force W.U.S. high.

After removal of the fault condition, two negative write data transitions are required to clear W.U.S. This output is for indication only, intended for signaling a controller, and does not directly impede device operation. A pull-up resistor of from 2 kΩ to 10 kΩ is necessary for operation of this open collector output.

Power Monitor Considerations

A power monitor circuit protects data integrity by preventing erroneous writing during power up and low voltage periods. The power monitor disables write current when V_{CC} is below about 4 V and/or V_{DD1} is below about 9 V. Hysteresis avoids unwanted toggling about the thresholds. At V_{CC} and V_{DD1} levels above these thresholds, operation is fully controllable.

Device operation at standard voltages (V_{CC} = 5 V ± 10%, V_{DD1} = 12 V ± 10%) is not affected in any way and is fully specified.

Read mode operation is not affected by the power monitor circuitry.

Read Mode Design Considerations

The read amp has a fully differential input and output and provides approximately 100 V/V gain. Its 60 MHz bandwidth and low noise characteristics (1.0nV/ $\sqrt{Hz}$ typical) provide substantial margins in most drives. The output should be AC coupled to delete the approximately 5.3 V ouput common mode voltage. Best results are obtained by limiting load capacitance to 20 pF and load current to 100 μA.

The XR-510A read preamplifier is specifically designed to minimize output common mode voltage changes between write mode and read mode, thus reducing switching transients that slow write to read recovery time. DC shifts are typically held under 500 mV from the 5.3 V nominal bias level.

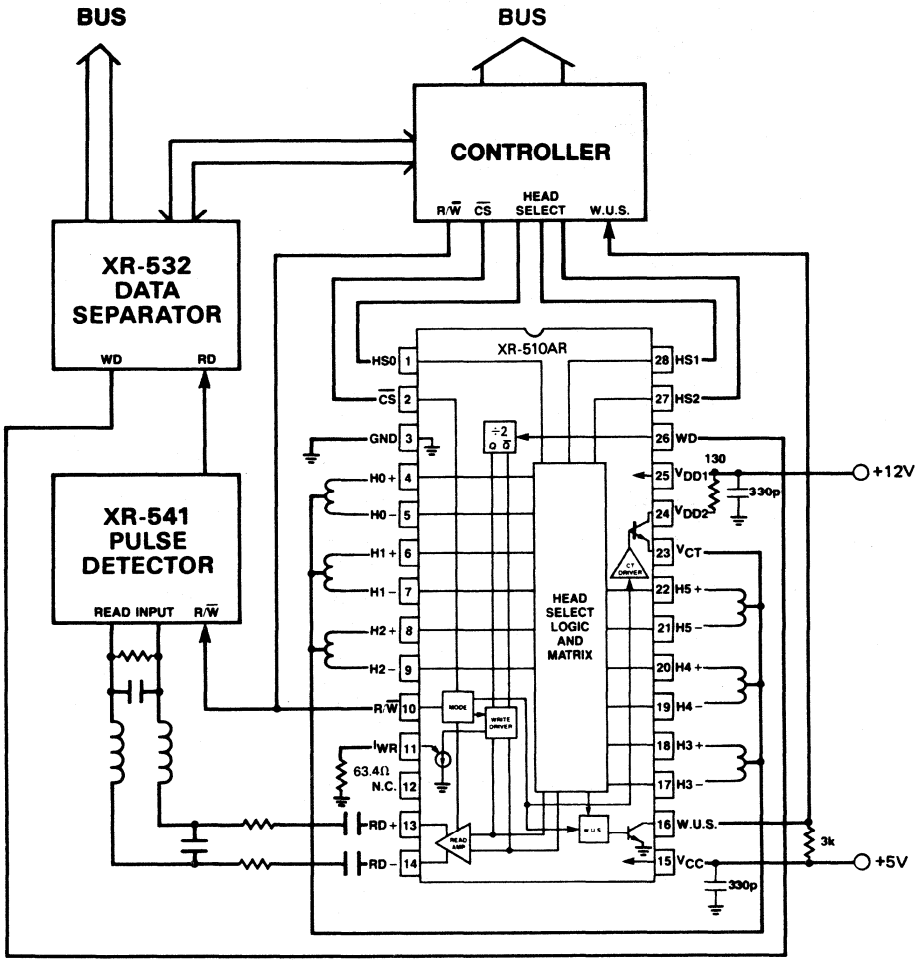


Figure 2. Hard Disk Read/Write Applications Circuit
Note: Circuit shown for XR-510AR . Non-R versions require damping resistors across each head.

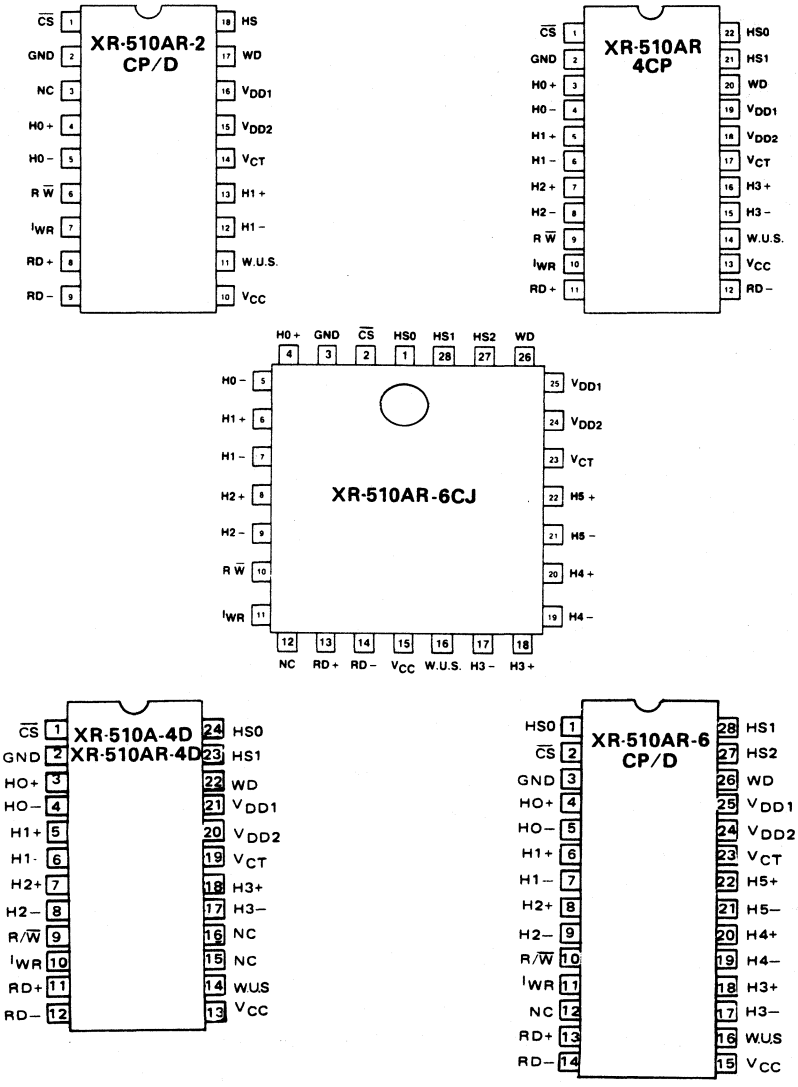


Figure 3. Additional Packages for XR-510A

Hard Disk Read/Write

GENERAL DESCRIPTION

The XR-511 is a high speed, low noise head interface integrated circuit for hard disk drives, performing both read and write functions. The XR-511 is compatible with 3½" to 14" multiple platter drives and features low noise, large dynamic range, and high bandwidth. Several packaging options extend usefulness to applications requiring six or eight center-tapped read/write heads. Multiple devices are easily cascaded for drives with more heads.

The XR-511 features a pinout with all head ports on one side of the circuit. This eases flex cable or PC board layout by eliminating crossovers. The XR-511R option includes internal damping resistors facilitating use in systems requiring minimum external circuit complexity.

XR-511, manufactured with a high speed bipolar process, operates on +5 V and +12 V. It is offered in a variety of packages, both surface mount and DIP.

FEATURES

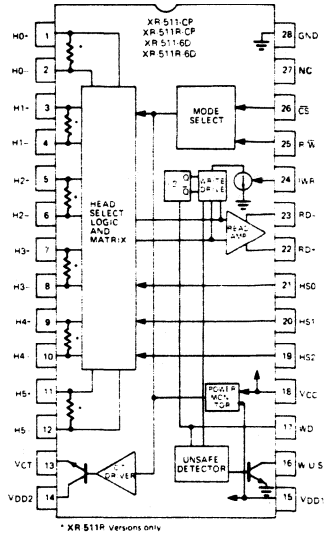
Complete Head Interfacing Functions, Read and Write
Low Noise Preamplifier
High Dynamic Range and Bandwidth
Pinout Optimized for Easy Layout
Available in Six and Eight Head Versions
Easily Cascaded for Larger Systems
Full Featured Power Monitor
TTL Compatible Control Inputs
Optional Internal Damping Resistors

APPLICATIONS

Hard Disk Drives

ABSOLUTE MAXIMUM RATINGS

V_{DD}	15 V
V_{CC}	6 V
Digital Inputs	−0.3 V to V_{CC} +0.3 V
Write Current	60 mA
Junction Temperature	150°C
Storage Temperature	−65°C to 150°C



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-511-4D	24 Pin SO	0°C to 70°C
XR-511-6CP	28 Pin Plastic DIP	0°C to 70°C
XR-511-6CJ	28 Pin PLCC	0°C to 70°C
XR-511-6D	28 Pin SO	0°C to 70°C
XR-511-8CP	40 Pin Plastic DIP	0°C to 70°C
XR-511-8CJ	44 Pin PLCC	0°C to 70°C
XR-511-8D	32 Pin SO	0°C to 70°C
XR-511R-4D	24 Pin SO	0°C to 70°C
XR-511R-6CP	28 Pin Plastic DIP	0°C to 70°C
XR-511R-6CJ	28 Pin PLCC	0°C to 70°C
XR-511R-6D	28 Pin SO	0°C to 70°C
XR-511R8CP	40 Pin Plastic DIP	0°C to 70°C
XR-511R8CJ	44 Pin PLCC	0°C to 70°C
XR-511R-8D	32 Pin SO	0°C to 70°C

SYSTEM DESCRIPTION

The XR-511 consists of a low noise preamplifier for reading from center tapped magnetic heads, a write current source for writing to the heads, a switching matrix to select one of eight heads, and associated control and monitoring functions. Less than **1.0** nV/$\sqrt{Hz}$ (nominal) noise allows error free operation with small input signals. Over 40 mA of write current output (user adjustable) means the disk signal can be large, further enhancing the read back signal-to-noise ratio for very low error rates.

ELECTRICAL SPECIFICATIONS

Test Conditions: $T_A = 25°C$, $V_{CC} = 5$ V, $V_{DD} = 12$ V, $I_W = 40$ mA, $R_D = 750\Omega$, C_L (R_{D+},R_{D-}) ≤ 20 pF, Data Rate = 5 MHz, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
I_{CC}	Supply Current			35	mA	V_{CC} = 5.5 V, Read or Idle Mode
				30	mA	V_{CC} = 5.5 V, Write Mode
I_{DD}	Supply Current			20	mA	V_{DD} = 13.2 V, Idle Mode
				40	mA	V_{DD} = 13.2 V, Read Mode
				20	mA	V_{DD} = 13.2 V, Write Mode, I_W = 0 mA
PD	Power Dissipation			400	mW	Idle Mode - V_{CC} = 5.5 V, V_{DD} = 13.2 V
				600	mW	Read Mode - V_{CC} = 5.5 V, V_{DD} = 13.2 V
				670	mW	I_W = 40 mA, $R_{CT} = 160\Omega$
				800	mW	I_W = 40 mA, $R_{CT} = 0\Omega$
V_{CT}	Center Tap Voltage		5.0		V	Read Mode
			7.0		V	Write Mode
V_{PM}	Power Monitor Protection	3.7	4.0	4.4	V	V_{CC} to Disable Write
		8.5	9.6	10.5	V	V_{DD1} to Disable Write
DIGITAL CHARACTERISTICS						
WUS	Write Unsafe Output					
V_{OL}	Saturation Voltage		0.2	0.5	V	I_{OL} = 8 mA
I_{OH}	Leakage Current			100	μA	V_{OH} = 5 V
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IL}	Input Low Current	−0.4			mA	V_{IL} = 0.8 V
I_{IH}	Input High Current			100	μA	V_{IH} = 2.0 V
WRITE CHARACTERISTICS						
	Write Current Accuracy	−5		5	%	Error from $I_W = \frac{2.5V}{R_W}$
	Recommended Write Current Range	10		40	mA	
	Differential Head Voltage Swing	7.0	11		V	Peak (Inductive Load)
	Unselected Differential Head Current			85	μA	
	Unselected Transient Current			2	mA	Peak

	Differential Output Capacitance			15	pF	
	Differential Output Resistance	10 635	 750	 865	kΩ Ω	XR-511 XR-511R
	WD Rate/Transistion Freq.	125	500		kHz	
K_I	Current Source Factor		1			$K_I = I_W/$(Current through R_W)
K	Write Current Constant	2.375	2.50	2.625	V	$I_W = K/R_W$
	Write Protection Leakage Current	−200		200	μA	Per Side, $V_{CC} \leq 3.7$ V $V_{DD} \leq 8.5$ V
V_{OS}	Preamplifier Output Offset Voltage	−20		+20	mV	Write or Idle Mode
V_{CM}	Preamplifier Output Common Mode Voltage		5.3		V	Write or Idle Mode
	Preamplifier Output Leakage Current	−100		100	μA	Write or Idle Mode, $R_{D+} = R_{D-} = 6$ V
READ MODE						
A_V	Differential Voltage Gain	85		115	V/V	V_{IN} = 1 mVp-p at 300 kHz, $R_{L+} = R_{L-} = 1k\Omega$
	Dynamic Range	−3		+3		DC input voltage where gain drops 10%. $V_{in} = V_i + 0.5$ mVp-p at 300 kHz.
R_{IN}	Differential Input Resistance	2 **530**	8 650	 **790**	kΩ Ω	XR-511 XR-511R
C_{IN}	Differential Input Capacitance			20	pF	
e_{ni}	Input Noise Voltage		**1.0**	1.5	nV/√Hz	$L_h = 0$, $R_h = 0$, BW = 15 MHz
BW	Bandwidth	30	60		MHz	−3 dB Point, $\|Z_S\| \leq 5\Omega$, V_{in} = 1 mVp-p
I_B	Input Bias Current		10	45	μA	
CMRR	Common Mode Rejection Ratio	50	60		dB	$V_{CM} = V_{CT}$ + 100 mVp-p at 5 MHz
PSRR	Power Supply Rejection Ratio	45	60		dB	100 mVp-p at 5 MHz Superimposed on V_{DD1}, V_{DD2} or V_{CC}

	Channel Separation	45	60			Unselected Channel: V_{IN} = 100 mVp-p at 5 MHz. Selected Channel V_{IN} = 0 V
	Output Offset Voltage	−440	±50	440	mV	
V_{CM}	Common Mode Output Voltage	4.5	5.5	6.5	V	
ΔV_{CM}	V_{CM} Change from Write to Read		500		mV	Common Mode Output Voltage Change from Write to Read or Read to Write
	Head Current Leakage	−200		200	μA	Per Side
R_O	Single Ended Output Resistance			30	Ω	f = 5 MHz
I_O	Output Current	2.1			mA	AC Coupled, Source or Sink
SWITCHING CHARACTERISTICS						
R/W	Read to Write		0.1	1	μS	Note 1
	Write to Read		0.1	1	μS	Notes 2,3
CS	Start-up Delay		0.1	1	μS	Notes 1,2
	Inhibit Delay		0.1	1	μS	Note 3
	Head Switching Delay		0.1	1	μS	Note 2, Switching between any heads.
WUS	Write Unsafe					
	Safe to Unsafe	1.6		8.0	μS	I_W = 35 mA, See Figure 1, TD1
	Unsafe to Safe		0.2	1	μS	I_W = 35 mA, See Figure 1, TD2
I_W	Head Current					
	Propagation Delay		2	25	nS	Note 4, See Figure 1, TD3
	Asymmetry		0.1	2	nS	Note 5
	Rise or Fall Time		1	20	nS	10% to 90% or 90% to 10% point

Note 1: Delay to 90% of I_W.
Note 2: Delay to 90% of 100 mVp-p 10 MHz Read Signal Envelope.
Note 3: Delay to 90% Decay of I_W.
Note 4: From 50% Points. L_h = 0H, R_h = 0Ω.
Note 5: Write Data with 1 nS rise and fall times and 50% duty cycle.

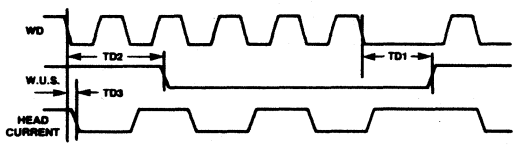


Figure 1. Write Mode Timing Diagram

A full-featured power monitor circuit disables the write mode during power-up and low operating voltage conditions, protecting data integrity. Improved write stability over 501-type devices is achieved by employing a unity gain write current constant.

CAUTION: This device may be damaged by electrostatic discharge. ESD precautions should be taken.

PRINCIPLES OF OPERATION

Write Mode

Before writing may begin, both chip select ($\overline{CS}$) and Read/Write (R/$\overline{W}$) must be pulled low. The desired head, selected by HS0 to HS2, is driven by a differential current sink of magnitude I_W, set by R_{IW}. Input data is applied to a falling edge triggered toggle flip-flop, which in turn selects the active side of the center tapped write head.

Current is sourced through the center tap driver, V_{CT}, which is "high" in the write mode. Write unsafe (W.U.S.) signals the disk controller whenever one of six error conditions exist and writing should be discontinued. The six faults are: open head, open center tap, no write current, write data frequency too low, device unselected, and writing attempted while the device is in the read mode. The power supply monitor disables writing when V_{CC} drops below 4 V and/or V_{DD1} drops below 9 V.

Read Mode

Pulling R/$\overline{W}$ high enables the data readback mode. A low noise, high gain differential amplifier increases the weak read signal amplitude and provides low output impedance drive for the following stage (Pulse Detector).

APPLICATIONS INFORMATION

As with all high frequency, high gain systems, layout is critical. Lead lengths should be minimized and supplies should be well bypassed. The XR-511 is available in small outline surface mount and PLCC packages, facilitating installation near the drive heads. The XR-511R option has 750Ω internal damping resistors across each head input, further aiding the goal of short lead lengths by eliminating the need for external resistors. The XR-511R option is especially convenient when the device is mounted on the flexible cable connecting the heads, as internal damping resistors reduce layout complexity, parts counts, and mass.

The high frequency characteristics of the XR-511 lead to a certain degree of electrostatic discharge (ESD) susceptability, so static reducing precautions should be taken.

Write Mode Design Considerations

Write current, I_W, typically between 20 mA and 40 mA, is determined by a single resistor, R_{IW}.

$$R_{IW} = \frac{2500}{I_W}$$

where I_W is in mA and R_{IW} is in ohms.

Device power dissipation is reduced by a resistor, R_{CT}, connecting V_{DD2} to the +12 V supply. Some of the center tap driver voltage is then dropped across the resistor.

With the nominal 12 V supply, R_{CT}, is calculated as

$$R_{CT} = 130 \left(\frac{55}{I_W}\right)$$

where R_{CT} is in ohms and I_W is in milliamperes.

Internal dissipation reduction is primarily a consideration with high write current levels and small surface mount packages. All XR-511 packages are suitable for continuous operation under worst case conditions without requiring R_{CT}. If R_{CT} is not used, V_{DD2} is directly connected to V_{DD1}.

Write Unsafe Indicator (W.U.S.)

Write unsafe (W.U.S.) pulls high whenever one or more of six write error conditions exists. Four conditions; open head, open center tap, no write current and write data transition rate too low are detected with a differential capacitor charge/discharge circuit. Device unselected and read mode digital conditions also force W.U.S. high.

After removal of the fault condition, two negative write data transitions are required to clear W.U.S. This output is for indication only, intended for signaling a controller, and does not directly impede device operation. A pull-up resistor of from 2 kΩ to 10 kΩ is necessary for operation of this open collector output.

Power Monitor Considerations

A power monitor circuit protects data integrity by preventing erroneous writing during power up and low voltage periods. The power monitor disables write current when V_{CC} is below about 4 V and/or V_{DD1} is below about 9 V. Hysteresis avoids unwanted toggling about the thresholds. At V_{CC} and V_{DD1} levels above these thresholds, operation is fully controllable.

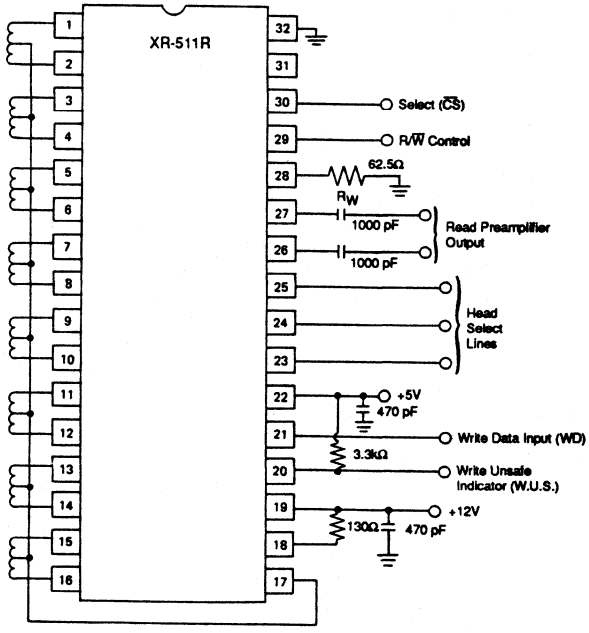
Device operation at standard voltages (V_{CC} = 5 V ± 10%, V_{DD1} = 12 V ± 10%) is not affected in any way and is fully specified.

Read mode operation is not affected by the power monitor circuitry.

Read Mode Design Considerations

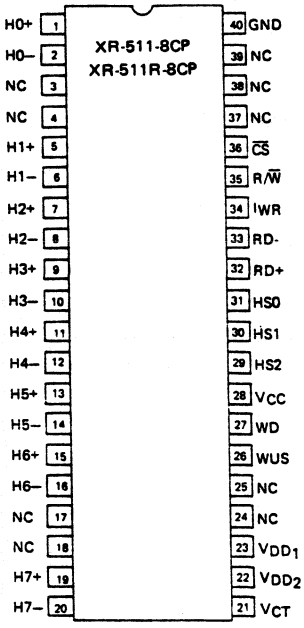
The read amp has a fully differential input and output and provides approximately 100 V/V gain. Its 60 MHz bandwidth and low noise characteristics (**1.0nV/** $\sqrt{Hz}$ typical) provide substantial margins in most drives. The output should be AC coupled to delete the approximately 5.5 V output common mode voltage. Best results are obtained by limiting load capacitance to 20 pF and load current to 100 μA.

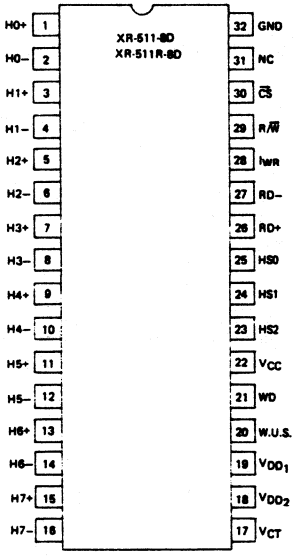
The XR-511 read preamplifier is specially designed to minimize output common mode voltage changes between write mode and read mode, thus reducing switching transients that slow write to read recovery time. DC shifts are typically held under **500** mV from the 5.5 V nominal bias level.

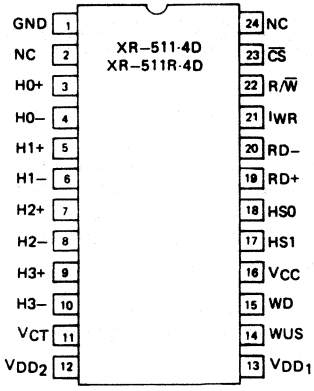


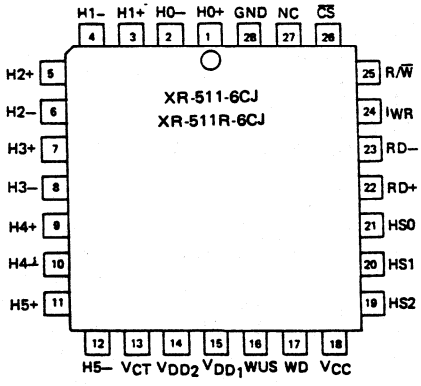
XR 511R Typical Application Circuit

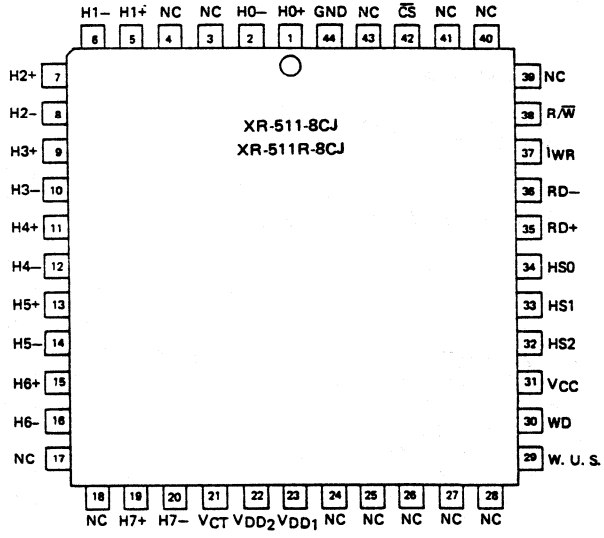
NOTE: Non 'R' Versions Require External Damping Resistors











XR-511-6CP/511R-6CP/511-6D/511R-6D 28 Pin Package Pinout shown on front page.

Hard Disk Pulse Detector

GENERAL DESCRIPTION

The XR-541 is a disk drive pulse detector designed for use with RLL and MFM coding schemes. Signals from the read/write preamplifier are qualified by an amplitude verifying gating threshold before constant width pulses are output.

The XR-541 is available in 24 Pin Plastic DIP, JEDEC S.O., and 28 Pin PLCC packages. It employs +5V and +12V supplies.

FEATURES

RLL and MFM Decoding
High Performance AGC Preamplifier
Adjustable Detection Threshold
Wide Dynamic Range
Compatible with Embedded Servo
Separate Analog and Digital Grounds
TTL Level Output and Control
Replaces SSI541 Read Data Processor

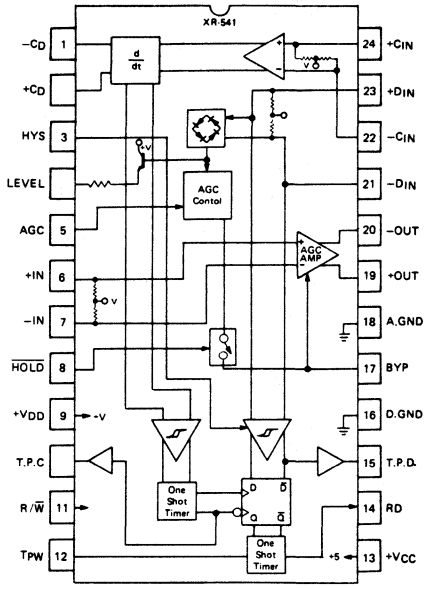
APPLICATIONS

Winchester Disk Drives
Removable Cartridge Disk Drives

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	
V_{CC}	6.5V
V_{DD}	14.0V
Storage Temperature	-65°C to150°C
Operating Junction Temperature	150°C
Power Dissipation	
24 Pin Plastic DIP	1W
Derate Above 25°C	8mW/°C
24 Pin JEDEC S.O.	1W
Derate Above 25°C	8mW/°C
28 Pin PLCC	1W
Derate Above 25°C	8mW/°C
TTL Input Voltage	-0.3V to 5.5V
Differential Input Signal	+/-3.3V

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Package	Operating Temperature
XR-541-1CP	24 Pin DIP/1nS	0°C to 70°C
XR-541-1CJ	28 Pin PLCC/1nS	0°C to 70°C
XR-541-1D	24 Pin S.O./1nS	0°C to 70°C
XR-541-3CP	24 Pin DIP/3nS	0°C to 70°C
XR-541-3CJ	28 Pin PLCC/3nS	0°C to 70°C
XR-541-3D	24 Pin S.O./3nS	0°C to 70°C

SYSTEM DESCRIPTION

Signal from the disk head preamplifier are A.C. coupled into the XR-541. A low pass filter may be employed here to reduce system bandwidth and noise. The input amplifier is AGC controlled, allowing reliable operation with signal levels ranging from 20 mV to 660 mV p-p. A low pass filter removes unwanted components as the signal enters the differentiator and level detection threshold circuitry. Only when the signal rises above this user adjustable threshold is the output one-shot timer enabled.

Detection threshold is set by the voltage on the HYS Pin. Test points are provided for alignment of the delays from the clock input and the gating flip-flop. Dual grounds reduce coupling between the digital sections and the low level signal inputs.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°, V_{CC} = 5V, V_{DD} = 12V, R/$\overline{W}$ = High (>2.0V). Unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{CC}	Supply Current		4	14	mA	V_{CC} = 5.5V
I_{DD}	Supply Current		50	70	mA	V_{DD} = 13.2V
P_D	Power Dissipation		600	730	mW	
	DIGITAL SIGNALS					
V_{IL}	Input "Low" Voltage			0.8	V	
V_{IH}	Input "High" Voltage	2.0			V	
I_{IL}	Input "Low" Current	-0.4			mA	V_{IL} = 0.4V
I_{IH}	Input "High" Current			100	µA	V_{IH} = 2.4V
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 4mA $\overline{RD}$ Output
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = -0.4mA $\overline{RD}$ Output
	AGC AMPLIFIER					
A_{Vmin}	Minimum Gain		0.1	4	V/V	Differential V_{OUT} from 1.0V
A_{Vmax}	Maximum Gain	83	250		V/V	to 2.5Vp-p
R_{IN}	Differential Input Resistance		5		kΩ	
C_{IN}	Differential Input Capacitance			10	pF	
Z_{IN}	Common Mode Input Impedance		1.8		kΩ	R/$\overline{W}$ ≥ 2.4V Both Sides
			250	500	Ω	R/$\overline{W}$ ≤ 0.8V Both Sides
e_{ni}	Input Noise Voltage			30	nV/$\sqrt{Hz}$	Av = maximum: 15 MHz bandwidth
BW	Preamplifier Bandwidth	30	60		MHz	Av = maximum: -3dB point
CMRR	Common Mode Rejection Ratio	40	60		dB	V_{IN} = 100mVp-p at 5 MHz. Av = Max.
PSRR	Power Supply Rejection Ratio	30	40		dB	ΔV_{CC} or ΔV_{DD} = 100mV Vp-p at 5 MHz. Av = Max
Vout	Output Voltage Swing	3.0	6		Vp-p	R_L ≥600Ω Differential. V_{AGC} = 5.5V
Iout	Output Current Swing	±3.2	±4		mA	
R_O	Output Resistance			32	Ω	
C_O	Output Capacitance			15	pF	
$\frac{V_{DIN}}{V_{AGC}}$	V(DIN+) - V(DIN-) Voltage Swing -vs-V_{AGC}	370	480	560	mV_{p-p}/V	V_{IN} From 30mVp-p to 550mVp-p V(DIN+) - V(DIN-) From 500Vp-p to 1.5Vp-p
$\frac{\Delta V_{DIN}}{V_{AGC}}$	V(DIN+) - V(DIN-) Change		1	8	%	VAGC = constant. V_{CC} ±10%, V_{DD} ±10%. T_A From 0°C to 70°C.
I_{AGC}	AGC Fast Charge Current	1.3	1.6	2.0	mA	V(DIN+) - V(DIN-) = 1.6V
I_{AGC}	AGC Slow Charge Current	140	180	220	µA	V(DIN+) - V(DIN-) = 1.6V. VAGC
	Fast to Slow Attack Switching Point		1.25		—	$\frac{V_{DIN}\ (Initial)}{V_{DIN}\ (Final)}$
	AGC Capacitor Discharge Current		4.5		µA	Operate (HOLD="High") V_{DIN}=0
		-200	—	200	nA	Hold (HOLD="Low") V_{DIN}=0
t_A	AGC Attack Time		4		µS	Note 1.
t_D	AGC Decay Time		50		µS	Note 2.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
	WINDOW THRESHOLD COMPARATOR					
R_{IN}	Differential Input Resistance	5		11	kΩ	
C_{IN}	Differential Input Capacitance			6	pF	
Z_{IN}	Common Mode Input Impedance		2		kΩ	V_{HYS} = 0V. $R_{(DIN+ \text{ to } DIN-)} \leq 1.5k\Omega$
V_{OS}	Threshold Comparator Offset Voltage	-10		10	mV	
	Peak Window Threshold Voltage -vs- V_{HYS}	0.16	0.22	0.25	V/V	$V_{(DIN)}$ Referred. V_{HYS} From 1V to 3V.
I_{HYS}	HYS Pin Input Current	-20		0	µA	V_{HYS} From 1V to 3V.
V_{LEVEL}	V_{LEVEL} -vs- V_{DIN}	1.5	2.0	2.5	V/Vp-p	V_{DIN} From0.6V to 1.3V p-p 10kΩ Load to Ground
I_{LEVEL}	LEVEL Maximum Output Current	3.0			mA	
$R_{O(LEVEL)}$	LEVEL Output Resistance		180		Ω	I_{LEVEL} = 500mA
V_{OLD}	Test Point "D" Output Low Voltage	V_{DD} -4		V_{DD} -2.8	V	$\lvert I_{OL} \rvert \leq$ 500mA
V_{OHD}	Test Point D Output High Voltage	V_{DD} -2.5		V_{DD} -1.8	V	$\lvert I_{OH} \rvert \leq$ 500mA
	DIFFERENTIATOR					
R_{IN}	Differential Input Resistance	5.8		11	kΩ	$\lvert V_{CIN} \rvert$ = 100mVp-p at 2.5 MHz
C_{IN}	Differential Input Capacitance			6	pF	$\lvert V_{CIN} \rvert$ = 100mVp-p at 2.5 MHz
A_{VD}	Differentiator Preamp Gain	1.7	1.8	2.2	V/V	V_{DIF}/V_{CIN}: R_{DIF} = 2kΩ
Z_{IN}	Common Mode Input Impedance		2		kΩ	
V_{OS}	Differentiator Offset Voltage	-10		10	mV	Capacitive Differentiator Network
I_D	Differentiator Drive Current	±1.3			mA	
V_{OLc}	Test Point "C" Output Low Voltage		V_{DD}-3		V	$\lvert I_{OL} \rvert \leq$ 500mA
Vo_c	Test Point "C" Output		400		mVp-p	I_{OL} , $\lvert I_{OH} \rvert \leq$ 500mA
t_c	Test Point "C" Pulse Width		30		nS	$\lvert I_{OH} \rvert \leq$ 500mA
	CONTROL TIMING					
T_{W-R}	Write to Read Transition Time	1.2	2	3.0	µS	Transition to High R_{IN}.
T_{R-W}	Read to Write Transition Time		0.25	1.0	µS	
T_{R-H}	Read to Hold Transition Time			1.0	µS	
	DYNAMIC DATA CHARACTERISTICS Additional Test Conditions: V_{CIN}, V_{DIN} = 1.0Vp.p 2.5MHz Sine Wave, V_{HYS} = 1.8V, C_D = 65pF, R_D = 100Ω, C_{pw} =60pF, $\overline{RD}$ is loaded with 4kΩ to $+V_{CC}$ & 10pF to GND. Refer to Figure 2 , Figure 3 and Figure 4					
T_{D1}	D Flip-Flop Set Up Time	0			nS	Delay from V_{DIN} Passing threshold to V_{DIF} Peaking
T_{D3}	Propagation Delay		65	110	nS	Delay from V_{DIN} = V_{CIN} Peaking to $\overline{RD}$ out.
PP	Pulse Pairing			1	nS	XR-541-1 (Note 3)
				3	nS	XR-541-3 (Note 3)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
T_{PW}	Output Data Pulse Width Accuracy	-15		15	%	Error from T_{PW} = 0.67 C_{PW}: C_{PW} from 50pF to 200pF
T_r	Output Rise Time		7	14	nS	To V_{OH} = 2.4V
T_f	Output Fall Time		6	18	nS	To V_{OL} = 0.4V

NOTE 1: Time from Write to Read transition to V_{OUT} reaching 110% of Final value using 400mVp-p 2.5 MHz sine wave.
(See Figure 1A, Figure 1B.)

NOTE 2: Time from Vin dropping from 300mVp-p to 150mVp-p to V_{OUT} recovering within 90% of final value using 2.5 MHz sine wave.
(See Figure1C, Figure 1D)

NOTE 3: Pulse Pairing is defined as: $\frac{1}{2}\left(\frac{Tpp1 - Tpp2}{Tpp1 + Tpp2}\right)$
as shown in Figure 3.
Circuit is as shown in Figure 4. $V_{CIN} = V_{DIN}$ = 1Vp-p 2.5 MHz sine wave.

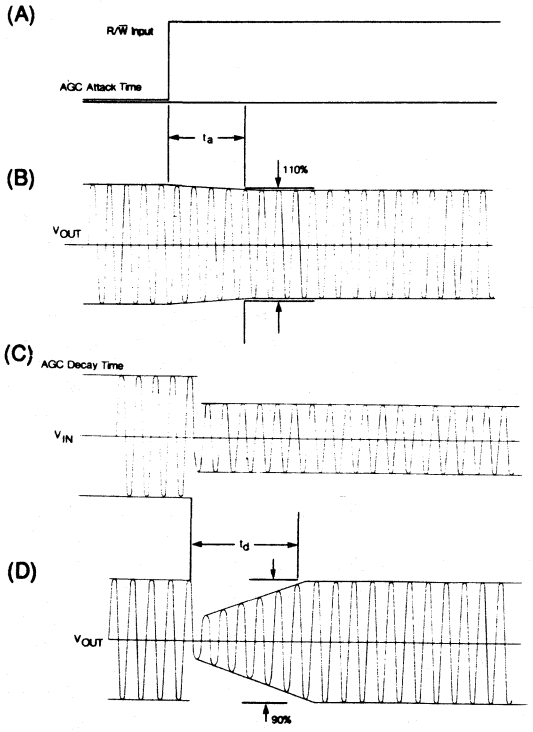


Figure 1. XR-541 AGC Characteristics
(A) R/$\overline{W}$ Control Input
(B) AGC Attack Time
(C) Stepped Input Test Signal
(D) AGC Decay Time

XR-541 Pin Description (28 Pin PLCC)

Pin	Symbol	Description
1,2	$-C_D$, $+C_D$	**Differentiator Network Terminals.**
3	HYS	**Window Gating Hysteresis.** Window gating comparator level is adjusted by this pin.
5	Level	**AGC Amplifier Level Output.** Rectified Analog signal is output for closing the AGC loop.
6	AGC	**AGC Charge Current Input.** Determines if AGC bypass capacitor is charging at the fast rate, slow rate, or is discharging.
7, 8	+IN, -IN	**AGC Preamplifier Input.** Signal input from external read preamplifier.
9	HOLD	**AGC Gain Hold.** When low, AGC Amplifier Gain is held constant.
10	V_{DD}	**+12V Supply.**
11	T.P.C.	**Test Point for monitoring "Clock" path.**
12	R/$\overline{W}$	**Read/Write Control.** A TTL low places the device in standby mode.

13	T_{PW}	**One Shot Timing Select.** Output pulse time is set using a capacitor to +VCC.
15	V_{CC}	**+5V Supply.**
16	$\overline{RD}$	**Read Data Output.** Active low digital output.
18	T.P.D.	**Test Point for monitoring "Data" path.**
19	D.GND	**Digital Ground.**
20	BYP	**AGC Control Pin.** A capacitor to ground sets AGC time constants.
21	A. GND	**Analog Ground.**
22, 23	+OUT, -OUT	**AGC Amplifier Output.**
24, 27	$-D_{IN}$, $+D_{IN}$	**"Data" path Input.**
26, 28	$-C_{IN}$, $+C_{IN}$	**"Clock" path Input.**

CIRCUIT OPERATION

Standby/Write Mode

During Data Write operations ($R/\overline{W}$ low), the XR-541 AGC input impedance is lowered to reduce the time constant caused by the input coupling capacitors, which limits the speed of Write to Read transitions. The AGC is reset to maximum gain, and digital circuitry is disabled.

Read Mode

AGC

The analog head signal is A.C. coupled from the head preamplifier to the AGC inputs. The signal is amplified and its dynamic range is compressed. Nominal peak output voltage is user-determinable by applying a voltage to the AGC Pin, according to the relationship:

$$V_{AGCOUT}\ (p\text{-}p) = 0.48\ V_{AGC}$$

Where V_{AGCOUT} is the peak to peak pre-amplifier output voltage and V_{AGC} is the DC control voltage on the AGC pin.

For most applications, a peak to peak output voltage of 2 volts is ideal.

AGC gain is held constant between pulses by the capacitor on the BYP Pin. Two rates of current charge this capacitor depending on its relative amplitude. A high level, 1.8mA, provides rapid attack characteristics needed for fast Write to Read recovery time. A low level, 180µA, allows slower gain tracking adjustment and reduces third order harmonic generation.

Preamplifier output is passed through a multiple order Bessel lowpass filter and applied to the Clock and Data inputs. For some applications, different delays are required for the Clock and Data inputs. For this reason, the XR-541 separates these inputs; many applications do not need separate timing and Clock Inputs and Data Inputs are directly connected. Internal path delays are carefully matched.

Hold

In the "Hold" mode, (Hold = low) no current charges C_{BYP}. The constant voltage on C_{BYP} keeps the amplifier gain constant at its present valve. This feature is intended to facilitate embedded servo applications, where fixed gain is essential for amplitude comparison used in head positioning.

Data Path

Preamplified signal output from the filter is applied to the $+D_{IN}/-D_{IN}$ terminals to allow amplitude qualification of the signal and AGC loop closure. When this input amplitude exceeds the hysteresis threshold, the D flip-flop data inputs are toggled.

These inputs will not change state again until the signal changes direction and crosses the hysteresis threshold on the opposite side of "zero". See figures 2a, 2d. Hysteresis comparator output is buffered and appears at T.P. D. for testing or evaluation purposes.

Clock Path

Preamplifies signal output from the filter is applied to the $+C_{IN}/-C_{IN}$ terminals to determine precise data peak timing. The clock path consists of a differentiator, a zero crossing comparator, and a one-shot timer.

The differentiator phase shifts the incoming waveform, converting data peaks into zero crossings. A capacitor, C_D- nominally 20pF to 150pF, determines the amount of phase shift. Although a phase shift of 90° across all input frequencies would be ideal, this implies an infinite bandwidth. Noise considerations usually dictate adding a resistor, and occasionally an inductor, to limit the

differentiator noise bandwidth. With a series RLC network, the differentiator transfer function becomes:

$$A_V = \frac{-2000\ C_S}{LCs^2 + (R + R_1)\ Cs + 1}$$

where $s = j\omega$ and $R_1 = 92\Omega$ (internal impedance of the differentiator).

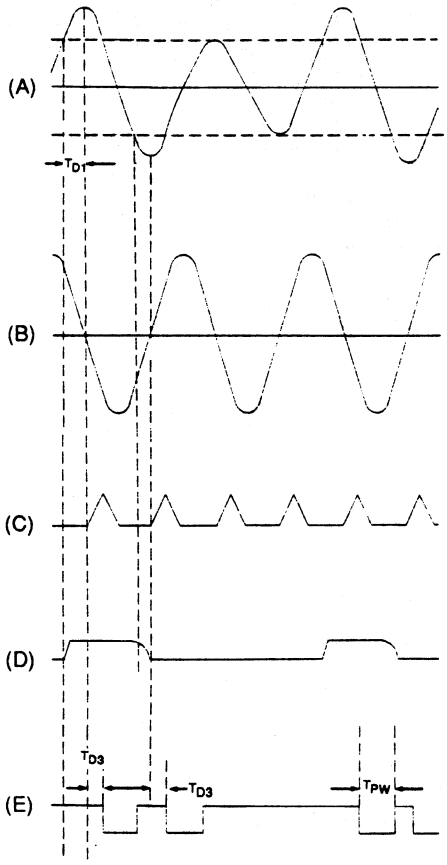


Figure 2. XR-541 Timing Diagram

(A). AGC Amplifier Output (also V_{CIN} & V_{DIN}) showing ±window comparator thresholds.
(B). Differentiator Circuit waveform (V_{CD}).
(C). Test Point "C" Output. Flip-flop clock input.
(D). Test Point "D" Output. Flip-flop D input.
(E). $\overline{RD}$ Output.

Differentiator output is applied to a zero crossing comparator. This comparator fires a bi-directionally triggered one-shot timer whose output is used as the clock of the D flip-flop. Buffered one-shot output appears at T.P. C. for alignment purposes.

Data Output

After the signal is time and amplitude qualified, the D flip-flop toggles. This fires a one shot timer which outputs a constant width active low digital data pulse, $\overline{RD}$. The period of this pulse is programmed by a capacitor, Cpw, from pin Tpw to $+V_{CC}$ and is proportioned to this capacitor by the formula:

$$Tpw = 0.67\ Cpw$$

Where Tpw is in nS and Cpw is in pF. Recommended Cpw values range from 50pF to 200 pf.

The active low $\overline{RD}$ output has a fan out of 1 TTL gate.

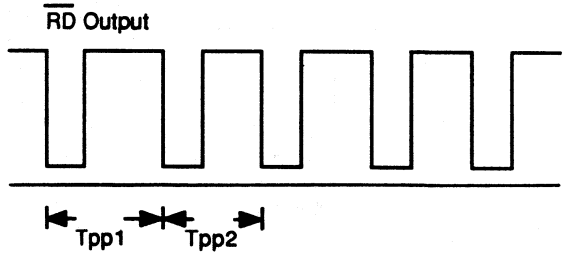


Figure 3. Pulse Pairing Definition

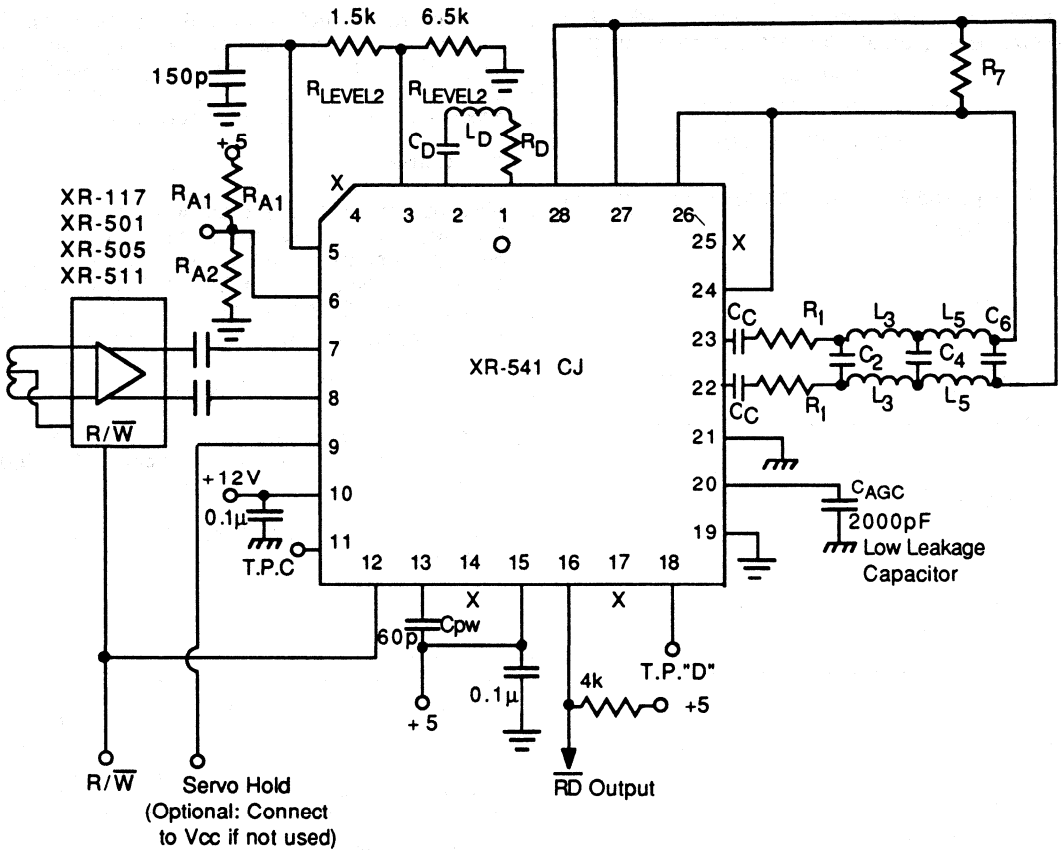
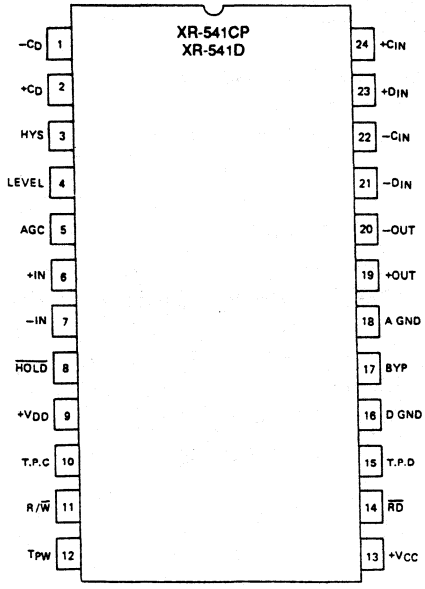
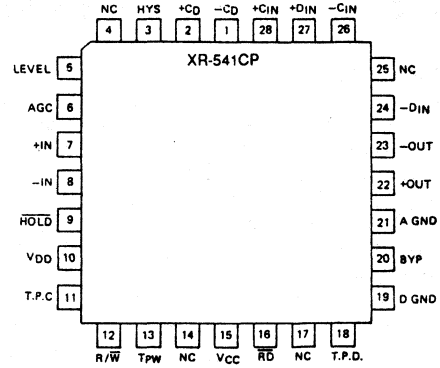


Figure 4. XR-541 Application Circuit





XR-541CJ (PLCC) Pinout

4

XR-532 RLL (2,7) Data Separator

General Description

The XR-532 is high speed, low power, single +5V supply data separator for disk drive applications. Data Synchronization and RLL (2,7) encoding and decoding are provided. The XR-532, combined with an Exar Read/Write Amplifier and Pulse detector, provides a complete Read/Write electronics channel for magnetic storage systems.

The XR-532 is manufactured with a high performance BiCMOS process, providing high speed, accurate timing, and low power consumption. It operates with a single +5V power supply and is available in a 28 pin PLCC package.

Features

Low Noise, Low Jitter Data Synchronizer
High Speed RLL (2,7) ENDEC
Low Power Operation
Easily Adapted to Zoned Recording Applications
Hard or Soft Sector Compatible
Single +5V Supply
Advanced BiCMOS Technology

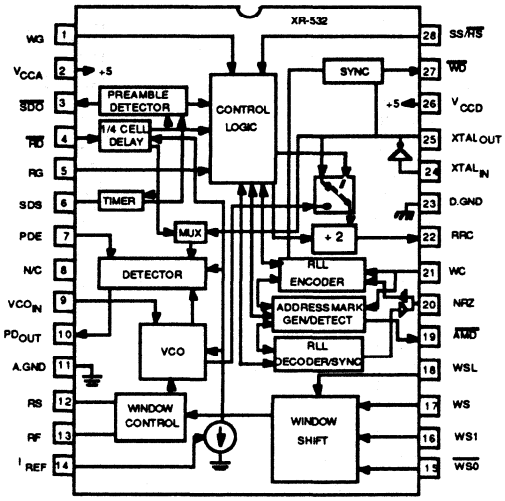
Applications

SCSI Bus Hard Disk Drive
ESDI Bus Hard Disk Drive

Absolute Maximum Ratings

V_{CCA},V_{CCD}	7V
Digital Inputs	-0.3V to V_{CCD} +0.3V
Junction Temperature	150°C
Storage Temperature	-65°C to 150°C

Functional Block Diagram



XR-532 FUNCTIONAL BLOCK DIAGRAM

Ordering Information

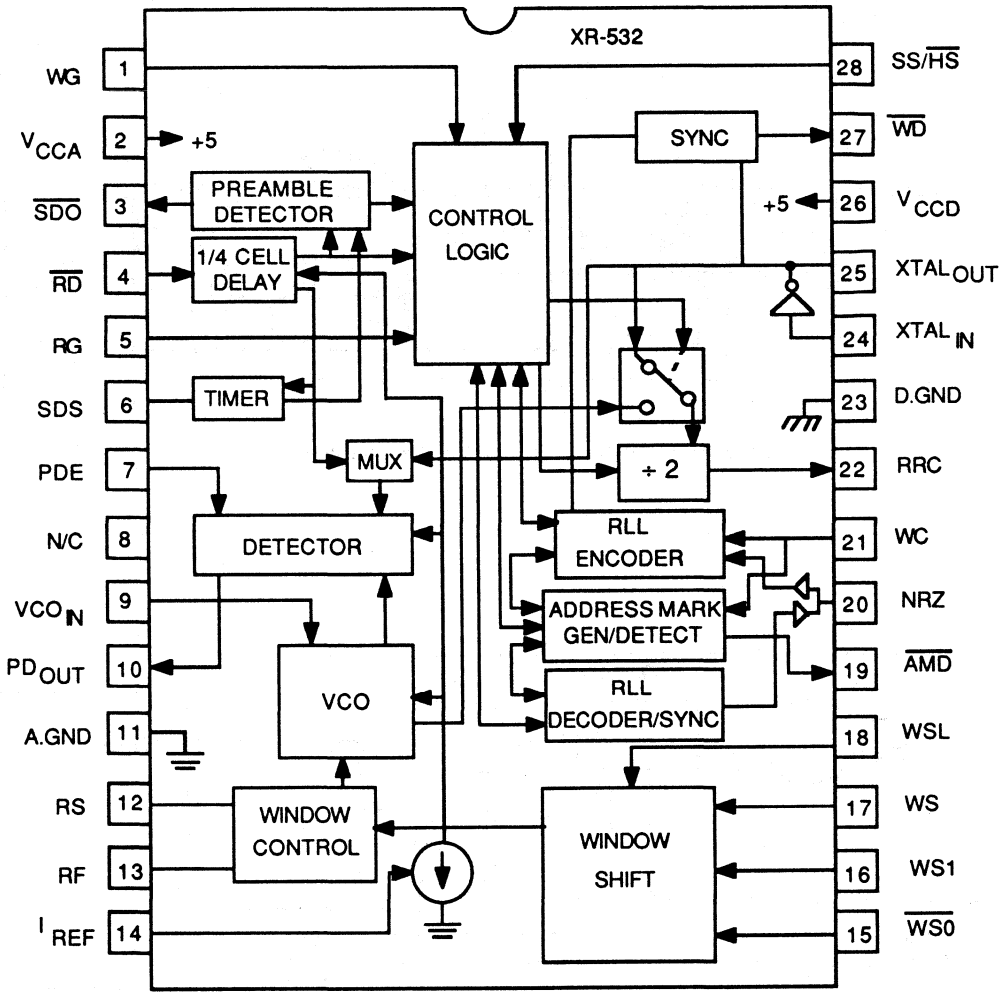
Part Number	Package	Ordering Temperature
XR-532CJ	28 Pin PLCC	0°C to 70°C

System Description

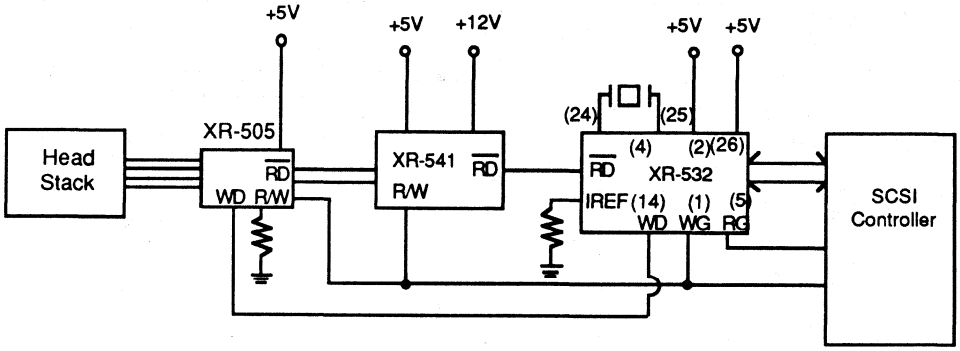
The XR-532 is a 20Mb/sec RLL (2,7) Data Synchronizer and ENDEC implemented in a state-of-the-art BiCMOS process. This no compromise process allows independant optimization of the linear VCO and charge pump in high performance bipolar technology, while using fine geometry, low power CMOS for the numerous logic functions. The resulting device is faster than similar bipolar-only versions while dissipating far less power. Only about 150mW of power is used during read operations.

Either hard sector or soft sector operation is allowed.

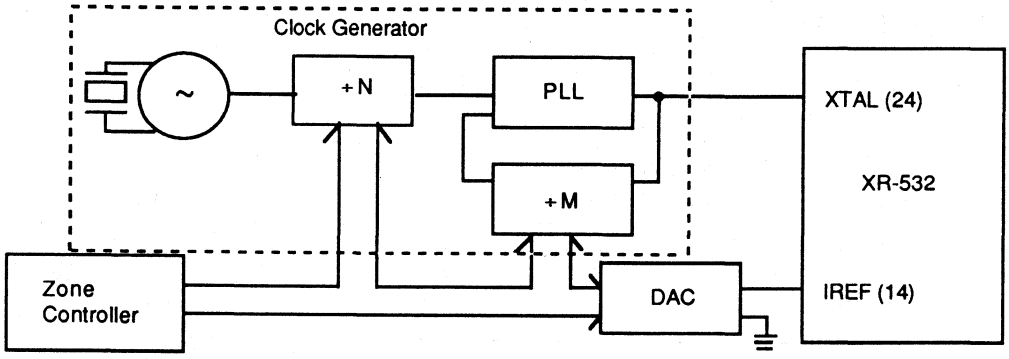
The XR-532 data rate is adjusted with a single resistor. All necessary internal timings will track each other as this resistor value is changed, accommodating zoned recording applications.



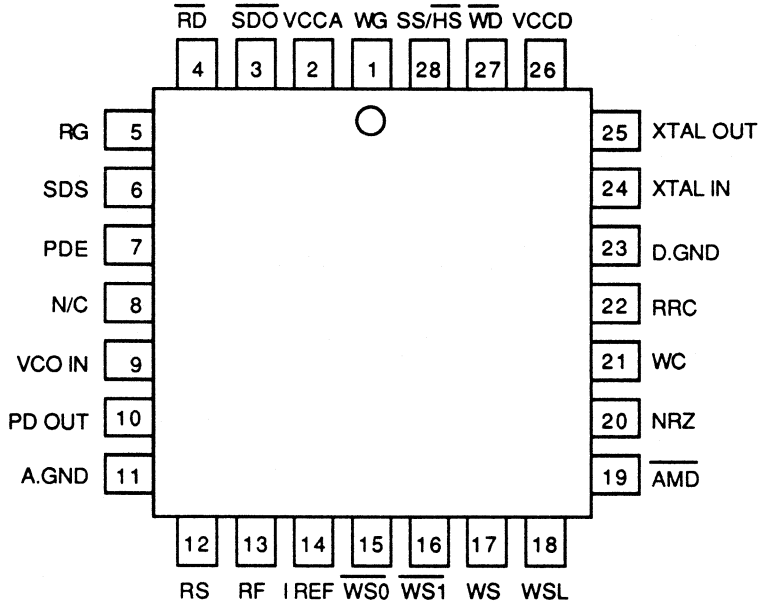
XR-532 FUNCTIONAL BLOCK DIAGRAM



Simple SCSI Disk Drive Read/Write channel with the XR-532



Zoned Recording Implementation


RD 4
SDO 3
VCCA 2
WG 1
SS/HS 28
WD 27
VCCD 26
RG 5
SDS 6
PDE 7
N/C 8
VCO IN 9
PD OUT 10
A.GND 11
25 XTAL OUT
24 XTAL IN
23 D.GND
22 RRC
21 WC
20 NRZ
19 AMD
12 RS
13 RF
14 I REF
15 WS0
16 WS1
17 WS
18 WSL

XR-532

EXAR ...the analog plus™ company

FSK Modulator/Demodulator

GENERAL DESCRIPTION

The XR-210 is a highly versatile monolithic phase-locked loop system, especially designed for data communications. It is particularly well suited for FSK modulation/demodulation (MODEM) applications, frequency synthesis, tracking filters, and tone decoding. The XR-210 operates over a power supply range of 5V to 26V, and over a frequency band of 0.5 Hz to 20 MHz. The circuit can accommodate analog signals between 300 μV and 3V, and can interface with conventional DTL, TTL, and ECL logic families.

FEATURES

Wide Frequency Range	0.5 Hz to 20 MHz
Wide Supply Voltage Range	5V to 26V
Digital Programming Capability	
RS-232C Compatible Demodulator Output	
DTL, TTL and ECL Logic Compatibility on Inputs	
Wide Dynamic Range	300 μV to 3V
ON-OFF Keying & Sweep Capability	
Wide Tracking Range	±1% to ±50%
Good Temperature Stability	200 ppm/°C
High-Current Logic Output	50 mA
Independent "Mark" and "Space" Frequency Adjustment	
VCO Duty Cycle Control	

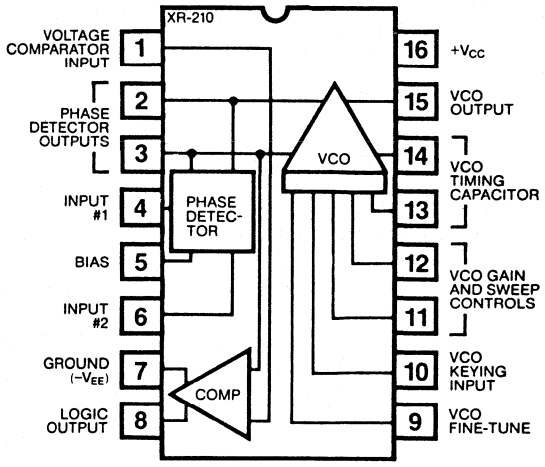
APPLICATIONS

Data Synchronization
Signal Conditioning
FSK Generation
Tone Decoding
Frequency Synthesis
FSK Demodulation
Tracking Filter
FM Detection
FM and Sweep Generation
Wideband Discrimination

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 Volts
Power Dissipation	750 mW
Derate Above +25°C	6.0 mW/°C
Storage Temperature	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-210M	Ceramic	−55°C to +125°C
XR-210CN	Ceramic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-210 is made up of a stable wide-range voltage-controlled oscillator (VCO), exclusive OR gate type phase detector, and an analog voltage comparator. The VCO, which produces a square wave as an output, is either used in conjunction with the phase detector to form a phase-locked loop (PLL) for FSK demodulation and tone detection or as a generator in FSK modulation schemes. The phase detector when used in the PLL configuration produces a differentional output voltage with a 6 KΩ output impedance, which when capacitively loaded forms a single pole loop filter. The voltage comparator is used to sense the phase detector output and produces the output in the FSK demodulation connection.

XR-210

ELECTRICAL CHARACTERISTICS

Test Conditions: V^+ = 12V (single supply), T_A = +25°C, Test circuit of Figure 1 with C_0 = 0.02 μF, S_1, S_2, S_5 closed, S_3, S_4, S_6, S_7 open, unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL CHARACTERISTICS						
V_{CC}	Supply Voltage					
	Single Supply	5		26	V dc	See Figure 1
	Split Supply	±2.5		±13	V dc	See Figure 2
I_{CC}	Supply Current	9	12	16	mA	See Figure 1, S_2 open
f_{UL}	Upper Frequency Limit	15	20		MHz	See Figure 1, S_1 open, S_4 closed
f_{LL}	Lowest Practical Operating Frequency		0.5		Hz	C_O = 500 μF non polarized
VCO SECTION						
	Stability					
T_C	Temperature		200	500	ppm/°C	f = 10 kHz, $V^+ \geq$ 10V, 0 < T_T < 70 ° C *
PSR	Power Supply		0.05	0.5	%/V	10V < V^+ < 24V
f_{SW}	Sweep Range	5:1	8:1			S_3 closed, S_4 open, 0 < V_S < 6V See Figure 5, V^+ = 12V
V_O	Output Voltage Swing	1.5	2.5		V p-p	S_5 open
DC	Duty Cycle Asymmetry		±1	±3	%	S_5 open
T_R	Rise Time		20		ns	10 pF to ground at Pin 15, S_5 open
T_F	Fall Time		40		ns	10 pF to ground at Pin 15, S_5 open
PHASE DETECTOR SECTION						
K_D	Conversion Gain		2		V/rad	V_{in} > 50 mV rms, see Figure 8
Z_O	Output Impedance		6		kΩ	Measured looking into Pin 2 or 3
V_{OOS}	Output Offset Voltage		35	150	mV	Measured across Pin 1 and 3, V_{in} = 0, S_5 open
VOLTAGE COMPARATOR SECTION						
A_{VOL}	Open Loop Voltage Gain	66	80		dB	f = 20 Hz
Z_{IN}	Input Impedance	0.5	2		MΩ	Measured looking into Pin 1
V_{OS}	Input Offset Voltage		1		mV	
I_B	Input Bias Current		80		nA	
CMRR	Common Mode Rejection		90		dB	
LOGIC OUTPUT SECTION						
SR	Slew Rate		15		V/μsec	R_L = 3 kΩ, C_L = 10 pF, S_2 closed
I_{OL}	"1" Output Leakage Current		0.02	10	μA	V_O = +24V
V_{OL}	"0" Output Voltage		0.2	0.4	V	I_L = 10 mA
I_{SINK}	Current Sink Capability	30	50		mA	$V_O \leq$ 1V

* These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

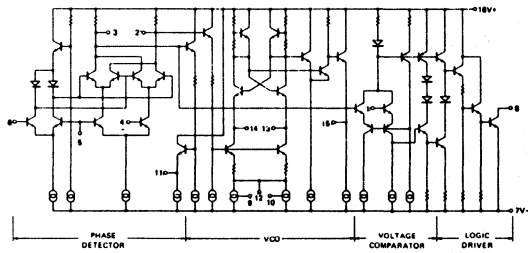
PRINCIPLES OF OPERATION

Description of Controls

Phase-Detector Inputs (Pin 4 and 6):
One input to the phase detector is used as the signal input; the remaining input should be ac coupled to the VCO output (Pin 15), to complete the PLL (see Figure 1). For split supply operation, these inputs are biased from ground as shown in Figure 2.

Phase-Detector Bias (Pin 5):
This terminal should be dc biased as shown in Figures 1 and 2, and ac grounded with a bypass capacitor. The

EQUIVALENT SCHEMATIC DIAGRAM



bias resistor in series with this pin should be half the value as those in series with Pin 4 and 6.

Phase-Detector Outputs (Pin 2 and 3):
The low-frequency (or dc) voltage across these pins corresponds to the phase difference between the two signals at the phase-detector inputs (Pin 4 and 6). These differential phase-detector outputs are internally connected to the VCO control terminals. Pin 3 is also internally connected to the reference input of the voltage comparator section.

In normal use, the low-pass loop-filter capacitor, C_1, is connected between Pin 2 and 3. The 6 kΩ impedances of the two outputs add to 12 kΩ in the single-pole RC low-pass loop filter. Pin 2 is externally connected to the voltage comparator input (Pin 1) through an RC low-pass filter.

Frequency-Keying Input (Pin 10):
The VCO frequency can be varied between two discrete frequencies, f_1 and f_2, by connecting an external resistor, R_X, to this terminal. Referring to Figure 6, the VCO frequency is proportional to the sum of currents, I_1 and I_2, through the transistors, T_1 and T_2, on the monolithic chip. These transistors are biased from a fixed internal reference. The current, I_1, is set internally, and is partially controllable by the fine-tune adjustment, R_T. The current, I_2, is set by the external resistor, R_X, connected between Pin 10 and Pin 7. For any C_O setting, the VCO frequency, f_2, with R_X connected to Pin 10, can be expressed as:

$$f_2 = f_1 \left(1 + \frac{0.3}{R_X}\right) \text{ Hz}$$

where f_1 is the frequency with Pin 10 open-circuited, and R_X is in kΩ. Note that f_2 can be fine-tuned to a desired value by the proper choice of R_X.

VCO Sweep Input (Pin 12):
The VCO frequency can be swept over a broad range by applying an analog sweep voltage, V_S to Pin 12 (see Figure 5). The impedance level looking into the sweep input is approximately 50Ω. Therefore, for sweep applications, a current limiting resistor, R_S, should be connected in series with this terminal. Typical sweep characteristics of the circuit are shown in Figure 5. The VCO temperature dependence is minimal when the sweep input is not used, and should be left open-circuited.

CAUTION: For safe operation of the circuit, the maximum current, I_S, drawn from the sweep terminal should be limited to 5 mA or less, under all operating conditions.

VCO Conversion Gain (Pin 11):
The VCO voltage-to-frequency conversion gain, K_O, is inversely proportional to the value of the external gain-control resistor, R_O, connected across Pin 11 and 12.

Fine Tune Control (Pin 9):
For a given choice of timing capacitor, C_O, the VCO frequency can be further fine-adjusted to a desired frequency, f_1, by means of a trimmer resistor, R_T, connected from Pin 9 to Pin 7, as shown in Figure 6. The fine tuned VCO frequency, f_1, is related to R_T as:

$$f_1 \approx \frac{220}{C_0}\left(1 + \frac{0.1}{R_T}\right) \text{ Hz}$$

where C_O is in μF, and R_T is in kΩ.

VCO Timing Capacitor (Pin 13 and 14):
The VCO free-running frequency, f_o, is inversely proportional to the timing capacitor, C_O, connected between Pin 13 and 14. With Pin 9 and 10 open-circuited, the VCO frequency is related to C_O as:

$$f_0 \approx \frac{220}{C_0} \text{ Hz}$$

where C_O is in μF.

VCO Output (Pin 15):
The VCO produces approximately a 2.5V p-p square wave output signal at this pin. The dc output level is approximately 2 volts below V_{CC}. This pin should be connected to Pin 7 through a 10 kΩ resistor to increase the output current drive capability. For high-voltage operation (V_{CC} > 20V), a 20 kΩ resistor is recommended. It is also advisable to connect a 500Ω resistor in series with this output, for short-circuit protection. This output can drive a 10kΩ or larger load.

Using the frequency-keying control, the VCO frequency can also be stepped in a binary manner by applying a logic signal to Pin 10, as shown in Figure 6. For high-level logic inputs, the transistor, T_2, is turned off, R_X is effectively switched out of the circuit, and the VCO frequency is shifted from f_2 to f_1.

Voltage Comparator Input (Pin 1):
This pin provides the signal input to the voltage comparator section. The comparator section is normally used for post-demodulation slicing and pulse shaping. Normally, Pin 1 is connected to Pin 2 through a 15K external resistor, as shown in Figures 1 and 2. The input impedance level at this pin is approximately 2 MΩ.

Logic Driver Output (Pin 8):
This pin provides a binary logic output corresponding to the polarity of the input signal, at the voltage comparator inputs. It is a open-collector type stage with high-current sinking capability.

Definition of Terms

Phase-Detector Gain, K_d:
K_d is the output voltage from the phase detector per radian of phase difference at the phase-detector inputs (Pin 4 and 6). K_d is proportional to the input signal for low-level inputs (≤25 mV rms), and is constant at high-input levels (see Figure 8).

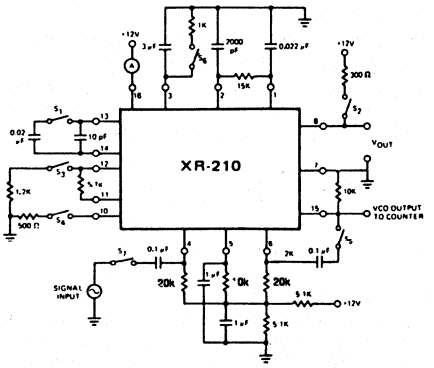


Figure 1. Test Circuits for Single Supply Operation

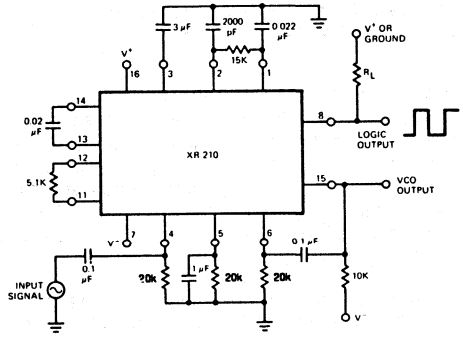


Figure 2. Test Circuit for Split Supply Operation

VCO Conversion Gain, K_O:

$$K_O \approx \frac{700}{C_O R_O} \quad \text{(radians/sec)/volt}$$

where C_O is in μF and R_O is in kΩ. For most applications, recommended values for R_O range from 1 kΩ to 10 kΩ.

When the XR-210 is connected as a PLL, its lock range can be controlled by varying the VCO gain control resistor, R_O, across Pin 11 and 12. For input signals greater than 30 mV rms, the PLL loop-gain is independent of signal amplitude, but is inversely proportional to R_O. Figure 7 shows the dependence of lock range, $\pm\Delta f_L$, on R_O.

Lock Range ($\Delta\omega_L$):
The range of frequencies in the vicinity of f_o over which the PLL can maintain lock with an input signal. If saturation or limiting does not occur, the lock range is equal to the loop gain; i.e., $\Delta\omega_L = K_T = K_d K_O$.

Capture Range ($\Delta\omega_C$):
The band of frequencies in the vicinity of f_o where the PLL can establish or acquire lock with an input signal. It is also known as the acquisition range. It is always smaller than the lock range, and is related to the low-pass filter bandwidth. It can be approximated by a parametric equation of the form:

$$\Delta\omega_C \approx \Delta\omega_L \, |F(j\Delta\omega_C)|$$

where $|F(j\Delta\omega_C)|$ is the low-pass filter magnitude response at $\omega = \Delta\omega_C$. For a simple lag filter, it can be expressed as:

$$\Delta\omega_C \approx \sqrt{\frac{\Delta\omega_L}{T_1}}$$

APPLICATIONS INFORMATION

FSK Demodulation

Figure 3 shows a generalized circuit connection for FSK demodulation. The circuit is connected as a PLL

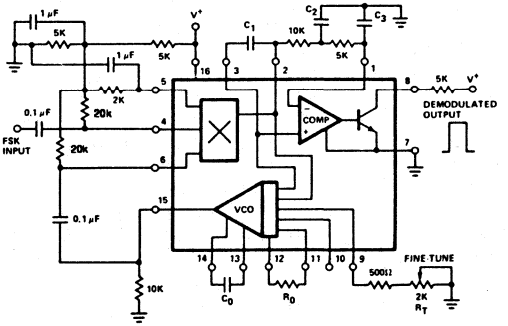


Figure 3. Circuit Connection for FSK Demodulation (Single Supply)

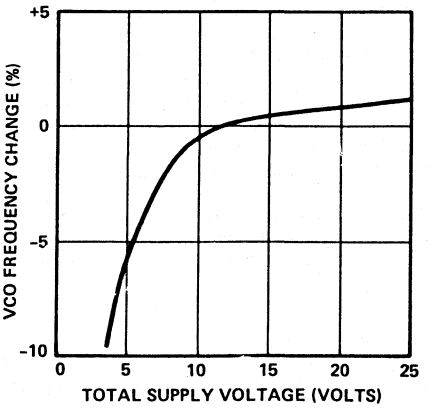
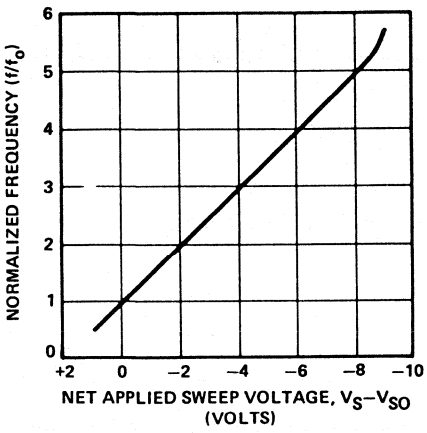
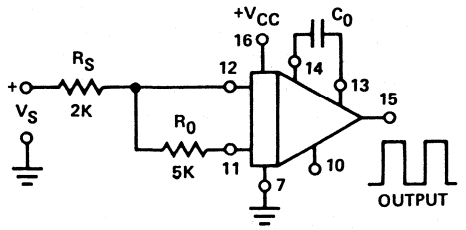


Figure 4. VCO Frequency Variation as a Function of Supply Voltage





(NOTE: $V_{SO} \approx V_{CC} - 5V$ = Open Circuit Voltage at pin 12)

Figure 5. Frequency Sweep Characteristics as a Function of Net Applied Sweep Voltage (Pin 10 Open)

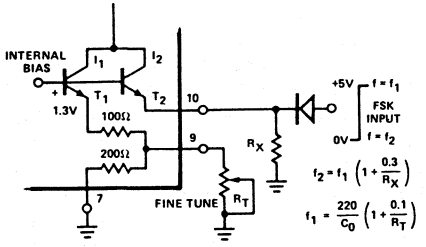


Figure 6. VCO Fine-Tune (Pin 9) and Frequency-Keying (Pin 10) Controls

system, by ac coupling the VCO output (Pin 15) to Pin 6. The FSK input is applied to Pin 4. When the input frequency is shifted, corresponding to a data bit, the polarity of the dc voltage across the phase-detector outputs (Pin 2 and 3) is reversed. The voltage comparator and the logic driver section convert this dc level shift to a binary pulse. The capacitor, C_1, serves as the PLL loop filter, and C_2 and C_3 as post-detection filters. The timing capacitor, C_O, and fine-tune adjustments are used to set the VCO frequency, f_o, midway between the mark

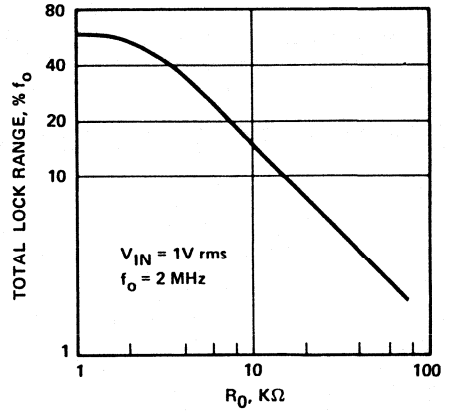


Figure 7. Total Lock Range, $\pm\Delta f_L$, versus VCO Gain Control Resistor, R_0

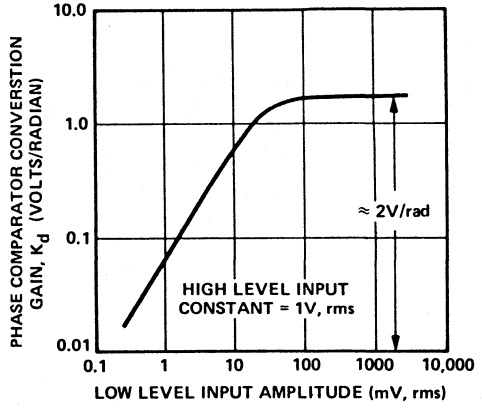


Figure 8. Phase Detector Conversion Gain, K_d, versus Input Amplitude

and space frequencies of the input signal. Typical component values for 300 baud (103-type) and 1200 baud (202-type) MODEM applications are listed below:

OPERATING CONDITIONS	TYPICAL COMPONENT VALUES
300 Baud	
Low Band: f_1 = 1070 Hz	R_0 = 5.1 kΩ, C_0 = 0.22 μF
f_2 = 1270 Hz	$C_1 = C_2$ = 0.047 μF, C_3 = 0.033 μF
High Band: f_1 = 2025 Hz	R_0 = 8.2 kΩ, C_0 = 0.1 μF
f_2 = 2225 Hz	$C_1 = C_2 = C_3$ = 0.033 μF
1200 Baud	
f_1 = 1200 Hz	C_1 = 0.033 μF, C_3 = 0.02 μF
f_2 = 2200 Hz	C_2 = 0.01 μF

Monolithic Phase-Locked Loop

The XR-215 is a highly versatile monolithic phase-locked loop (PLL) system designed for a wide variety of applications in both analog and digital communication systems. It is especially well suited for FM or FSK demodulation, frequency synthesis and tracking filter applications. The XR-215 can operate over a large choice of power supply voltages ranging from 5 V to 26 V and a wide frequency band of 0.5 Hz to 35 MHz. It can accommodate analog signals between 300 microvolts and 3 volts and can interface with conventional DTL, TTL, and ECL logic families.

FEATURES

Wide Frequency Range: 0.5 Hz to 35 MHz
Wide Supply Voltage Range: 5V to 26V
Digital Programming Capability
DTL, TTL and ECL Logic Compatibility on Inputs
Wide Dynamic Range: 300μV to 3V, nominally
ON-OFF Keying and Sweep Capability
Wide Tracking Range: Adjustable from ±1% to ±50%
High-Quality FM Detection: Distortion 0.15%
Signal/Noise 65dB

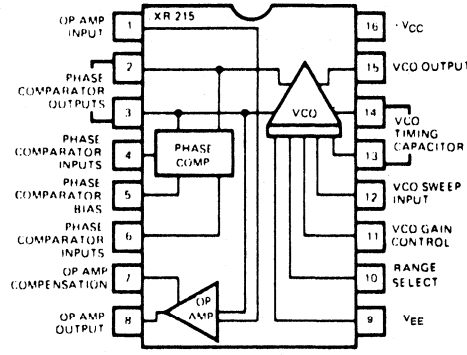
APPLICATIONS

FM Demodulation
Frequency Synthesis
FSK Coding/Decoding (MODEM)
Tracking Filters
Signal Conditioning
Tone Decoding
Data Synchronization
Telemetry Coding/Decoding
FM, FSK and Sweep Generation
Crystal-Controlled Clock Recovery
Wideband Frequency Discrimination
Voltage-to-Frequency Conversion

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 volts
Power Dissipation (Package Limitation)	
Ceramic	750mW
Derate above 25°C	5mW/°C
SO-16	500mW
Derate above + 25°C	4mW/°C
Temperature	
Storage	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-215CN	Ceramic	0°C to 70°C
XR-215MD	Japanese Dimension SO-16	0°C to 70°C

SYSTEM DESCRIPTION

The XR-215 monolithic PLL system consists of a balanced phase comparator, a highly stable voltage-controlled oscillator (VCO) and a high speed operational amplifier. The phase comparator outputs are internally connected to the VCO inputs and to the noninverting input of the operational amplifier. A self-contained PLL System is formed by simply AC coupling the VCO output to either of the phase comparator inputs and adding a low-pass filter to the phase comparator output terminals.

The VCO section has frequency sweep, on-off keying, sync, and digital programming capabilities. Its frequency is highly stable and is determined by a single external capacitor. The operational amplifier can be used for audio preamplification in FM detector applications or as a high speed sense amplifier (or comparator) in FSK demodulation.

ELECTRICAL CHARACTERISTICS

Test Conditions: V^+ = 12V (single supply), T_A = 25°C, Test Circuit of Figure 2 with C_0 = 100 pF, (silver-mica) S_1, S_2, S_5, closed, S_3, S_4 open unless otherwise specified.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
I—GENERAL CHARACTERISTICS					
SUPPLY VOLTAGE					
Single Supply	5		26	V dc	See Figure 2
Split Supply	±2.5		±13	V dc	See Figure 3
Supply Current	8	11	15	mA	See Figure 2
Upper Frequency Limit	20	35		MHz	See Figure 2, S_1 open, S_4 closed
Lowest Practical Operating Frequency		0.5		Hz	C_0 = 500 µF (non-polarized)
VCO SECTION:					
Stability:					
Temperature		250	600	ppm/°C	See Figure 6, 0°C ≤ T_T < 70°C *
Power Supply		0.1		%/V	V+ > 10V
Sweep Range	5:1	8:1			S_3 closed, S_4 open, $0 < V_S < 6V$
					See Figure 9, C_0 = 2000 pF
Output Voltage Swing	1.5	2.5		V_{p-p}	S_5 open
Rise Time		20		ns	
Fall Time		30		ns	10 pF to ground at Pin 15
PHASE COMPARATOR SECTION:					
Conversion Gain		2		V/rad	V_{in} > 50 mV rms (See characteristic curves)
Output Impedance		6		kΩ	Measured looking into Pins 2 or 3
Output Offset Voltage		20	100	mV	Measured across Pins 2 and 3 V_{in} = 0, S_5 open
OP AMP SECTION:					
Open Loop Voltage Gain	66	80		dB	S_2 open
Slew Rate		2.5		V/µ sec	A_V = 1
Input Impedance	0.5	2		MΩ	
Output Impedance		2		kΩ	
Output Swing	7	10		V_{p-p}	R_L = 30 kΩ from Pin 8 to ground
Input Offset Voltage		1		mV	
Input Bias Current		80		nA	
Common Mode Rejection		90		dB	
II—SPECIAL APPLICATIONS					
A) FM Demodulation					
Test Conditions: Test circuit of Figure 4, V^+ = 12V, input signal = 10.7 MHz FM with Δf = 75 kHz, f_{mod} = 1 kHz.					
Detection Threshold		0.8	3	mV rms	50Ω source
Demodulated Output Amplitude		500		mV rms	Measured at Pin 8
Distortion (THD)		0.15	0.5	%	
AM Rejection		40		dB	V_{in} = 10 mV rms, 30% AM
Output Signal/Noise		65		dB	
B) Tracking Filter					
Test Conditions: Test circuit of Figure 5, V^+ = 12V, f_o = 1 MHz, V_{in} = 100 mV rms, 50Ω source.					
Tracking Range (% of f_o)		±50			See Figures 5 and 25
Discriminator Output $\frac{\Delta V_{out}}{\Delta f/f_o}$		50		mV/%	Adjustable — See applications information

* Guaranteed, but not tested.

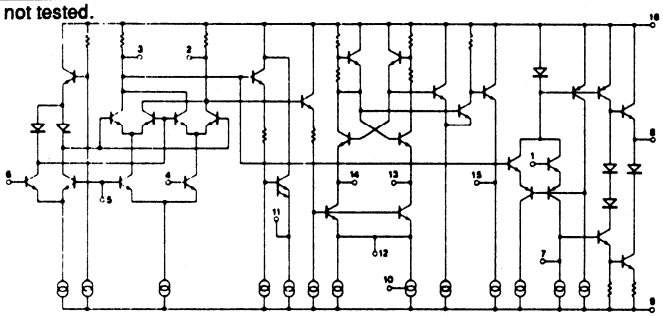


Figure 1. Equivalent Schematic Diagram

DESCRIPTION OF CIRCUIT CONTROLS

PHASE COMPARATOR INPUTS (PINS 4 AND 6)

One input to the phase comparator is used as the signal input; the remaining input should be ac coupled to the VCO output (pin 15) to complete the PLL (see Figure 2). For split supply operation, these inputs are biased from ground as shown in Figure 3. For single supply operation, a resistive bias string similar to that shown in Figure 2 should be used to set the bias level at approximately $V_{CC}/2$. The dc bias current at these terminals is nominally 8 μA.

PHASE COMPARATOR BIAS (PIN 5)

This terminal should be dc biased as shown in Figures 2 and 3, and ac grounded with a bypass capacitor.

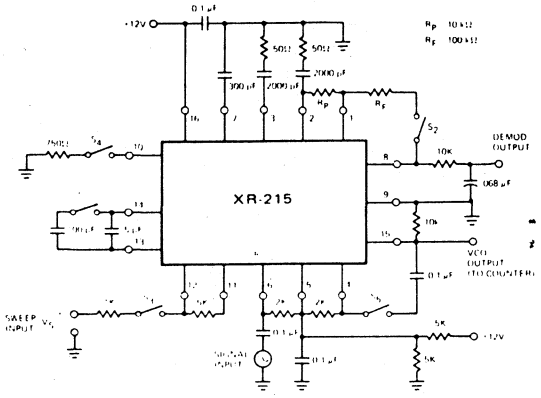


Figure 2. Test Circuit For Single Supply Operation

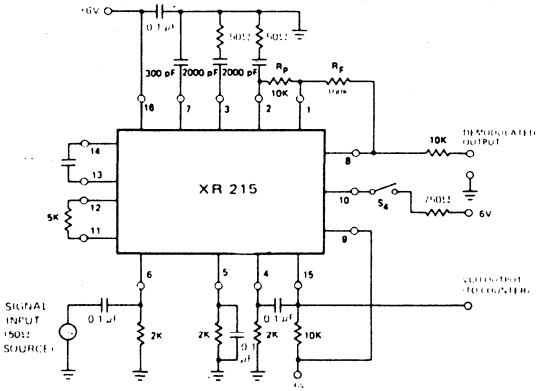


Figure 3. Test Circuit For Split-Supply Operation

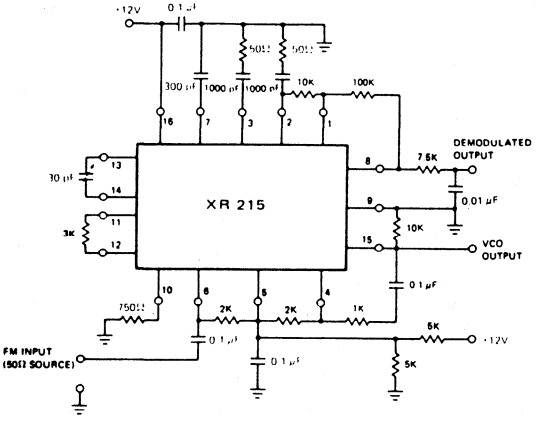


Figure 4. Test Circuit For FM Demodulation

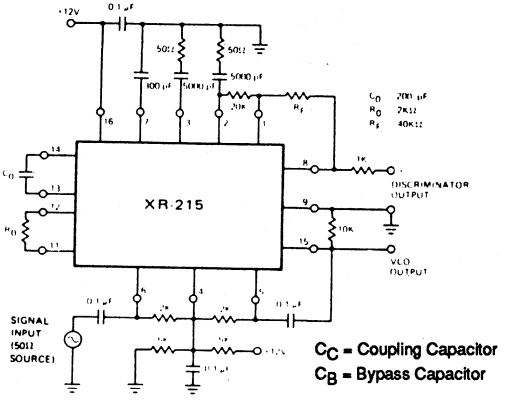


Figure 5. Test Circuit For Tracking Filter

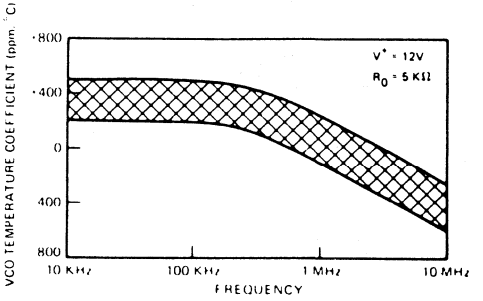


Figure 6. Typical VCO Temperature Coefficient Range as a Function of Operating Frequency (pin 10 open)

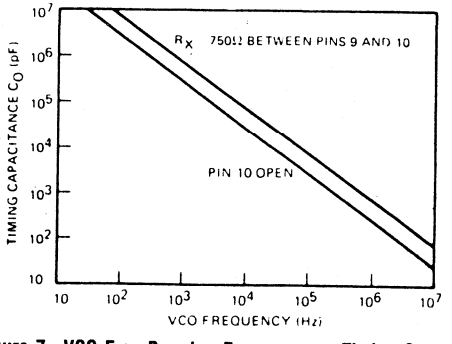


Figure 7. VCO Free Running Frequency vs Timing Capacitor

PHASE COMPARATOR OUTPUTS (PINS 2 AND 3)

The low frequency (or dc) voltage across these pins corresponds to the phase difference between the two signals at the phase comparator inputs (pins 4 and 6). The phase comparator outputs are internally connected to the VCO control terminals (see Figure 1). One of the outputs (pin 3) is internally connected to the *non-inverting* input of the operational amplifier. The low-pass filter is achieved by connecting an RC network to the phase comparator outputs as shown in Figure 14.

VCO TIMING CAPACITOR (PINS 13 AND 14)

The VCO free-running frequency, f_o, is inversely proportional to timing capacitor C_0 connected between pins 13 and 14. (See Figure 7).

VCO OUTPUT (PIN 15)

The VCO produces approximately a 2.5 V_{p-p} output signal at this pin. The dc output level is approximately 2 volts below V_{CC}. This pin should be connected to pin 9 through a 10 kΩ resistor to increase the output current drive capability. For high voltage operation (V_{CC} >

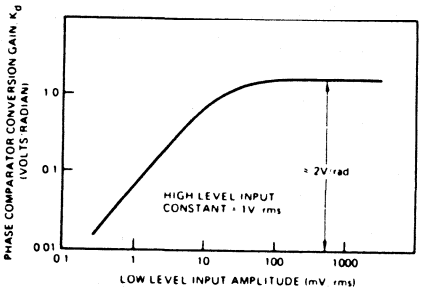


Figure 8. Phase Comparator Conversion Gain, K_d, versus Input Amplitude

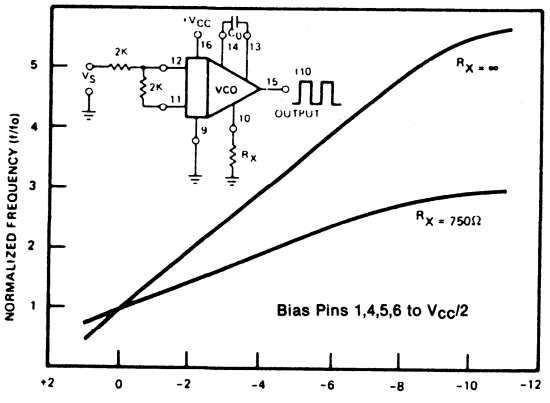


Figure 9. Typical Frequency Sweep Characteristics as a Function of Applied Sweep Voltage

(Note: $V_{SO} \approx V_{CC}$ - 5V = Open Circuit Voltage at pin 12)

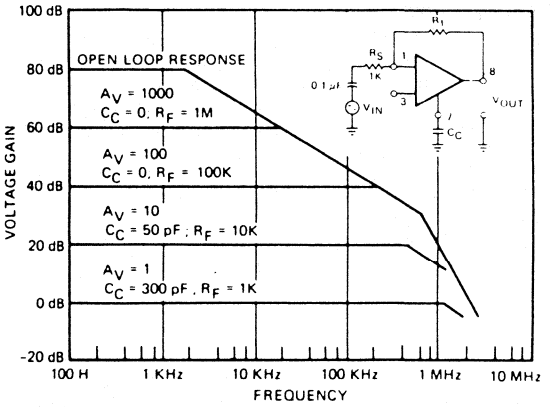


Figure 10. XR-215 Op Amp Frequency Response

20V), a 20 kΩ resistor is recommended. It is also advisable to connect a 500Ω resistor in series with this output for short circuit protection.

VCO SWEEP INPUT (PIN 12)

The VCO Frequency can be swept over a broad range by applying an analog sweep voltage, V_S, to pin 12 (see Figure 9). The impedance level looking into the sweep input is approximately 50Ω. Therefore, for sweep applications, a current limiting resistor, R_S, should be connected in series with this terminal. Typical sweep characteristics of the circuit are shown in Figure 9. The VCO temperature dependence is minimum when the sweep input is not used.

CAUTION: For safe operation of the circuit, the maximum current, I_S, drawn from the sweep terminal should be limited to 5 mA or less under all operating conditions.

ON-OFF KEYING: With pin 10 open circuited, the VCO can be keyed off by applying a positive voltage pulse to the sweep input terminal. With R_S = 2 kΩ, oscillations will stop if the applied potential at pin 12 is raised 3 volts above its open-circuit value. When sweep, sync, or on-off keying functions are not used, R_S should be left open circuited.

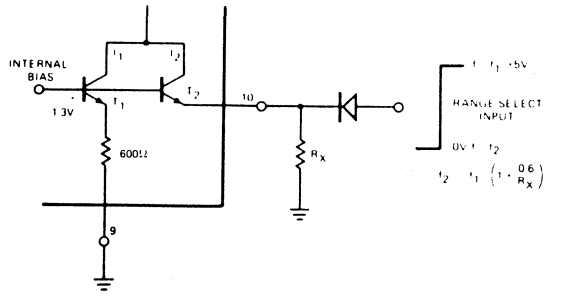


Figure 11. Explanation of VCO Range-Select Controls

RANGE-SELECT (PIN 10)

The frequency range of the XR-215 can be extended by connecting an external resistor, R_X, between pins 9 and 10. With reference to Figure 11, the operation of the range-select terminal can be explained as follows: The VCO frequency is proportional to the sum of currents I_1 and I_2 through transistors T_1 and T_2 on the monolithic chip. These transistors are biased from a fixed internal reference. The current I_1 is set internally, whereas I_2 is set by the external resistor R_X. Thus, at any C_0 setting, the VCO frequency can be expressed as:

$$f_o = f_1 \left(1 + \frac{0.6}{R_X}\right)$$

where f_1 is the frequency with pin 10 open circuited and R_X is in kΩ. External resistor R_X ($\approx$ 750Ω) is recommended for operation at frequencies in excess of 5 MHz.

The range select terminal can also be used for fine tuning the VCO frequency, by varying the value of R_X. Similarly, the VCO frequency can be changed in discrete steps by switching in different values of R_X between pins 9 and 10.

DIGITAL PROGRAMMING

Using the range select control, the VCO frequency can be stepped in a binary manner, by applying a logic signal to pin 10, as shown in Figure 11. For high level logic inputs, transistor T_2 is turned off, and R_X is effectively switched out of the circuit. Using the digital programming capability, the XR-215 can be time-multiplexed between two separate input frequencies, as shown in Figures 18 and 19.

AMPLIFIER INPUT (PIN 1)

This pin provides the inverting input for the operational amplifier section. Normally it is connected to pin 2 through a 10 kΩ external resistor (see Figure 2 or 3).

AMPLIFIER OUTPUT (PIN 8)

This pin is used as the output terminal for FM or FSK demodulation. The amplifier gain is determined by the external feedback resistor, R_F, connected between pins 1 and 8. Frequency response characteristics of the amplifier section are shown in Figure 10.

AMPLIFIER COMPENSATION (PIN 7)

The operational amplifier can be compensated by a single 300 pF capacitor from pin 7 to ground. (See Figure 10).

BASIC PHASE-LOCKED LOOP OPERATION

PRINCIPLE OF OPERATION

The phase-locked loop (PLL) is a unique and versatile circuit technique which provides frequency selective tuning and filtering without the need for coils or inductors. As shown in Figure 12, the PLL is a feedback system comprised of three basic functional blocks: phase comparator, low-pass filter and voltage-controlled oscillator (VCO). The basic principle of operation of a PLL can be briefly explained as follows: with no input signal applied to the system, the error voltage V_d, is equal to zero. The VCO operates at a set frequency, f_o, which is known as the "free-running" frequency. If an input signal is applied to the system, the phase comparator compares the phase and frequency of the input signal with the VCO frequency and generates an error voltage, $V_e(t)$, that is related to the phase and frequency difference between the two signals. This error voltage is then filtered and applied to the control terminal of the VCO. If the input frequency, f_s, is sufficiently close to f_o, the feedback nature of the PLL causes the VCO to synchronize or "lock" with the incoming signal. Once in lock, the VCO frequency is identical to the input signal, except for a finite phase difference.

A LINEARIZED MODEL FOR PLL

When the PLL is in lock, it can be approximated by the linear feedback system shown in Figure 13. ϕ_S and ϕ_O are the respective phase angles associated with the input signal and the VCO output, F(s) is the low-pass filter response in frequency domain, and K_d and K_O are the conversion gains associated with the phase comparator and VCO sections of the PLL.

DEFINITION OF XR-215 PARAMETERS FOR PLL APPLICATIONS

VCO FREE-RUNNING FREQUENCY, f_0

The VCO frequency with no input signal. It is determined by selection of C_0 across pins 13 and 14 and can be increased by connecting an external resistor R_X between pins 9 and 10. It can be approximated as:

$$f_o = \frac{200}{C_0}\left(1 + \frac{0.6}{R_X}\right)$$

where C_0 is in μF and R_X is in kΩ. (See Figure 7).

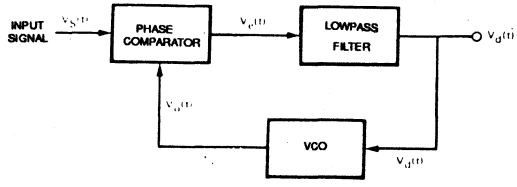


Figure 12. Block Diagram of a Phase-Locked Loop

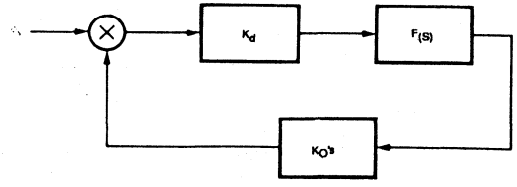


Figure 13. Linearized Model of a PLL as a Negative Feedback System

PHASE COMPARATOR GAIN K_d

The output voltage from the phase comparator per radian of phase difference at the phase comparator inputs (pins 4 **and 6). The units are volts/radions.**

VCO CONVERSION GAIN K_0

The VCO voltage-to-frequency conversion gain is determined by the choice of timing capacitor C_0 and gain control resistor, R_0 connected externally across pins 11 and 12. It can be expressed as

$$K_o \approx \frac{700}{C_0 R_0} \text{ (radians/sec)/volt}$$

where C_0 is in μF and R_0 is in kΩ. For most applications, recommended values for R_0 range from 1 kΩ to 10 kΩ.

LOCK RANGE ($\Delta\omega_L$)

The range of frequencies in the vicinity of f_o, over which the PLL can maintain lock with an input signal. It is also known as the "tracking" or "holding" range. If saturation or limiting does not occur, the lock range is equal to the loop gain, i.e. $\Delta\omega_L = K_T = K_d K_o$.

CAPTURE RANGE ($\Delta\omega_C$)

The band of frequencies in the vicinity of f_o where the PLL can establish or acquire lock with an input signal. It is also known as the "acquisition" range. It is always smaller than the lock range and is related to the low-pass filter bandwidth. It can be approximated by a parametric equation of the form:

$$\Delta\omega_C \approx \Delta\omega_L |F(j\Delta\omega_C)|$$

where $|F(j\Delta\omega_C|$ is the low-pass filter magnitude response at $\omega = \Delta\omega_C$. For a simple lag filter, it can be expressed as:

$$\Delta\omega_C \approx \sqrt{\frac{\Delta\omega_L}{T_1}}$$

where T_1 is the filter time constant.

AMPLIFIER GAIN A_V

The voltage gain of the amplifier section is determined by feedback resistors R_F and R_P between pins (8,1) and 2,1) respectively. (See Figures 2 and 3). It is given by:

$$A_V = \frac{-R_F}{R_1 + R_P}$$

where R_1 is the 6 kΩ internal impedance at pin 2, and R_p is the external resistor between pins 1 and 2.

LOW-PASS FILTER

The low-pass filter section is formed by connecting an external capacitor or RC network across terminals 2

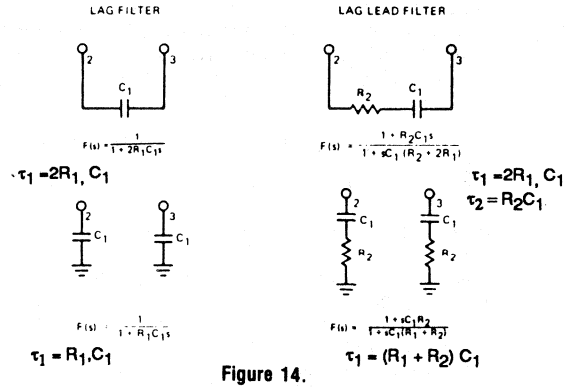


Figure 14.

and 3. The low-pass filter components can be connected either between pins 2 and 3 or, from each pin to ground. Typical filter configurations and corresponding filter transfer functions are shown in Figure 14 where **R_1 (6kΩ) is the internal impedance at pins 2 and 3. It should be noted that the rejection of the low pass filter decreases above 2mHz when the capacitor is tied from Pin 2 to 3.**

5

APPLICATIONS INFORMATION

FM DEMODULATION

Figure 15 shows the external circuit connections to the XR-215 for frequency-selective FM demodulation. The choice of C_0 is determined by the FM carrier frequency (see Figure 7). The low-pass filter capacitor C_1 is determined by the selectivity requirements. For carrier frequencies of 1 to 10 MHz, C_1 is in the range of 10 C_0 to 30 C_0. The feedback resistor R_F can be used as a "volume-control" adjustment to set the amplitude of the demodulated output. The demodulated output amplitude is proportional to the FM deviation and to resistors R_0 and R_F. For $\pm 1\%$ FM deviation it can be approximated as:

$$V_{OUT} \approx R_0 R_F \left(1 + \frac{0.6}{R_X}\right) \text{ mV, rms}$$

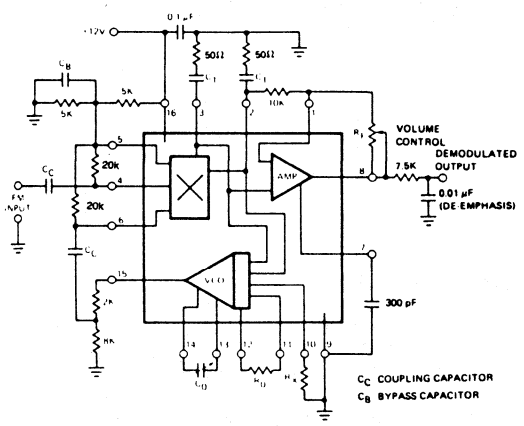


Figure 15. Circuit Connection for FM Demodulation

The damping factor can be calculated by using

$$\zeta = 1/2 \left(\frac{K_0 K_d}{\tau 1}\right)^{1/2} \cdot \tau_2 + \left(\frac{1}{K_0 K_d}\right)$$

where all resistors are in kΩ and R_X is the range extension resistor connected across pins 9 and 10. For circuit operation below 5 MHz, R_X can be open circuited. For operation above 5 MHz, $R_X \approx 750\Omega$ is recommended.

Typical output signal/noise ratio and harmonic distortion are shown in Figures 16 and 17 as a function of FM deviation, for the component values shown in Figure 4.

MULTI-CHANNEL DEMODULATION

The ac digital programming capability of the XR-215 allows a single circuit be time-shared or multiplexed between two information channels, and thereby selectively demodulate two separate carrier frequencies. Figure 18 shows a practical circuit configuration for time-multiplexing the XR-215 between two FM channels, at 1 MHz and 1.1 MHz respectively. The channel-select logic signal is applied to pin 10, as shown in Figure 18 with both input channels simultaneously present at the PLL input (pin 4). Figure 19 shows the demodulated output as a function of the channel-select pulse where the two inputs have sinusoidal and triangular FM modulation respectively.

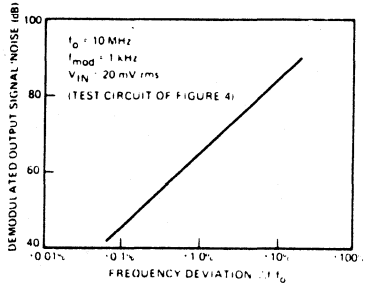


Figure 16. Output Signal/Noise Ratio as a Function of FM Deviation

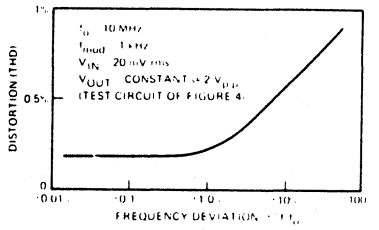


Figure 17. Output Distortion as a Function of FM Deviation

FSK DEMODULATION

Figure 20 contains a typical circuit connection for FSK demodulation. When the input frequency is shifted, corresponding to a data bit, the dc voltage at the phase comparator outputs (pins 2 and 3) also reverses polarity. The operational amplifier section is connected as a comparator, and converts the dc level shift to a binary output pulse. One of the phase comparator outputs (pin

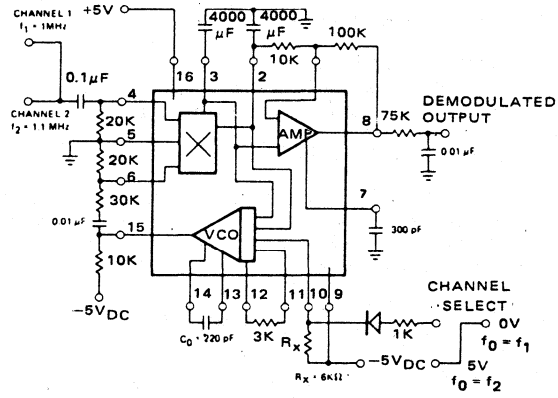


Figure 18. Time-Multiplexing XR-215 Between Two Simultaneous FM Channels

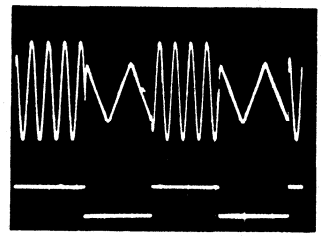


Figure 19. Demodulated Output Waveforms for Time-Multiplexed Operation

Top: Demodulated Output
Sinewave - Channel 1
Triangle Wave - Channel 2

Bottom: Channel Select Pulse

3) is ac grounded and serves as the bias reference for the operational amplifier section. Capacitor C_1 serves as the PLL loop filter, and C_2 and C_3 as post-detection filters. Range select resistor, R_X, can be used as a fine-tune adjustment to set the VCO frequency.

Typical component values for 300 baud and 1200 baud operation are listed below:

OPERATING CONDITIONS	TYPICAL COMPONENT VALUES
300 Baud	
Low Band: f_1 = 1070 Hz	R_0 = 5 kΩ, C_0 = 0.17 μF
f_2 = 1270 Hz	$C_1 = C_2$ = 0.047 μF, C_3 = 0.033 μF
High Band: f_1 = 2025 Hz	R_0 = 8 kΩ, C_0 = 0.1 μF
f_2 = 2225 Hz	$C_1 = C_2 = C_3$ = 0.033 μF
1200 Baud	R_0 = 2 kΩ, C_0 = 0.12 μF
f_1 = 1200 Hz f_2 = 2200 Hz	$C_1 = C_3$ = 0.003 μF, C_2 = 0.01 μF

Note that for 300 Baud operation the circuit can be time-multiplexed between high and low bands by switching the external resistor R_X in and out of the circuit with a control signal, as shown in Figure 11.

FSK GENERATION

The digital programming capability of the XR-215 can be used for FSK generation. A typical circuit connection for this application is shown in Figure 21. The VCO frequency can be shifted between the mark (f_2) and space (f_1) frequencies by applying a logic pulse to pin 10. The circuit can provide two separate FSK outputs: a low level (2.5 V_{p-p}) output at pin 15 or a high amplitude (10 V_{p-p}) output at pin 8. The output at each of these terminals is a symmetrical squarewave with a typical second harmonic content of less than 0.3%.

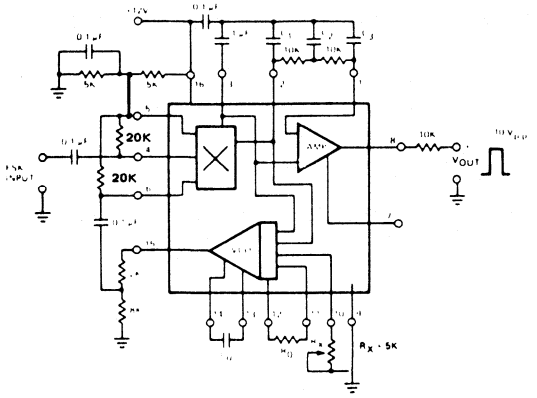


Figure 20. Circuit Connection for FSK Demodulation

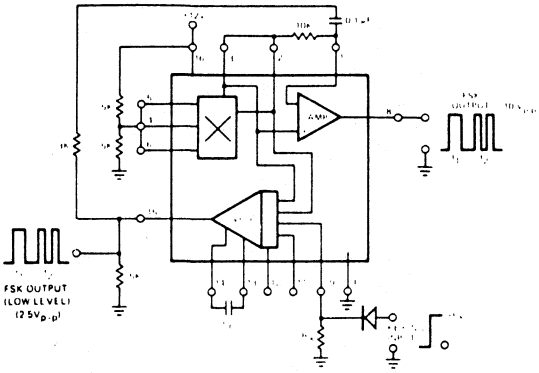


Figure 21. Circuit Connection For FSK Generation

FREQUENCY SYNTHESIS

In frequency synthesis applications, a programmable counter or divide-by-N circuit is connected between the VCO output (pin 15) and one of the phase detector inputs (pins 4 or 6), as shown in Figure 22. The principle of operation of the circuit can be briefly explained as

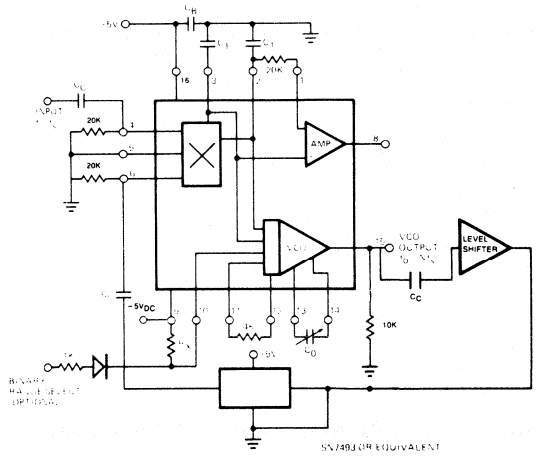


Figure 22. Circuit Connection For Frequency Synthesis

follows: The counter divides down the oscillator frequency by the programmable divider modulus, N. Thus, when the entire system is phase-locked to an input signal at frequency, f_S, the oscillator output at pin 15 is at a frequency (Nf_S), where N is the divider modulus. By proper choice of the divider modulus, a large number of discrete frequencies can be synthesized from a given reference frequency. The low-pass filter capacitor C_1 is normally chosen to provide a cut-off frequency equal to 0.1% to 2% of the signal frequency, f_S.

The circuit was designed to operate with commercially available monolithic programmable counter circuits using TTL logic, such as MC4016, SN5493 or equivalent. The digital or analog tuning characteristics of the VCO can be used to extend the available range of frequencies of the system, for a given setting of the timing capacitor C_0.

Typical input and output waveforms for N = 16 operation with f_S = 100 kHz and f_0 = 1.6 MHz are shown in Figure 23.

TRACKING FILTER/DISCRIMINATOR

The wide tracking range of the XR-215 allows the system to track an input signal over a 3:1 frequency range,

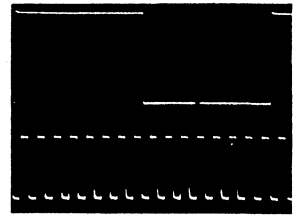


Figure 23. Typical Input/Output Waveforms For N = 16
Top: Input (100 kHz)
Bottom: VCO Output (1.6 MHz)
Vertical Scale 1 V/cm

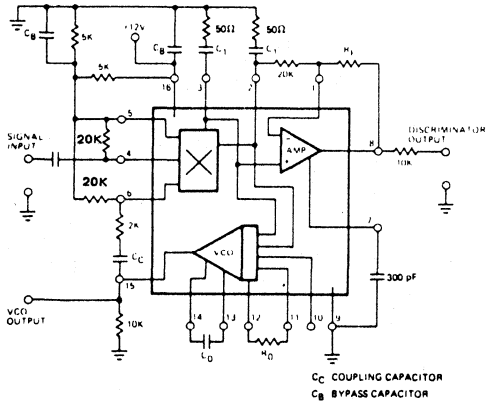


Figure 24. Circuit Connection For Tracking Filter Applications

centered about the VCO free running frequency. The tracking range is maximum when the binary range-select (pin 10) is open circuited. The circuit connections for this application are shown in Figure 24. Typical tracking range for a given input signal amplitude is shown in Figure 25. Recommended values of external components are: 1 kΩ < R_0 < 4 kΩ and 30 C_0 < C_1 < 300 C_0 where the timing capacitor C_0 is determined by the center frequency requirements (see Figure 7).

The phase-comparator output voltage is a linear measure of the VCO frequency deviation from its free-running value. The amplifier section, therefore, can be used to provide a filtered and amplified version of the loop error voltage. In this case, the dc output level at pin 15 can be adjusted to be directly proportional to the difference between the VCO free-running frequency, f_0, and the input signal, f_S. The entire system can operate as a "linear discriminator" or analog "frequency-meter" over a 3:1 change of input frequency. The discriminator gain can be adjusted by proper choice of R_0 or R_F. For the test circuit of Figure 24, the discriminator output is approximately (0.7 R_0R_F) mV per % of frequency deviation where R_0 and R_F are in kΩ. Output non-linearity is typically less than 1% for frequency deviations up to ±15%. Figure 27 shows the normalized output characteristics as a function of input frequency, with R_0 = 2 kΩ and R_F = 36 kΩ.

CRYSTAL-CONTROLLED PLL

The XR-215 can be operated as a crystal-controlled phase-locked loop by replacing the timing capacitor with a crystal. A circuit connection for this application is shown in Figure 27. Normally a small tuning capacitor (≈ 30 pF) is required in series with the

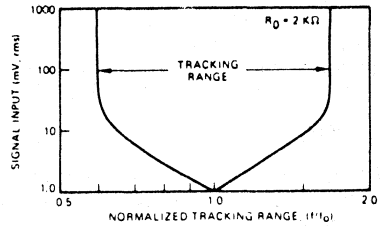


Figure 25. Tracking Range vs Input Amplitude (Pin 10 Open Circuited)

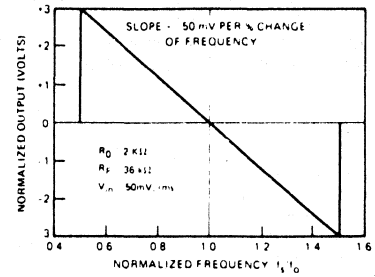


Figure 26. Typical Discriminator Output Characteristics For Tracking Filter Applications

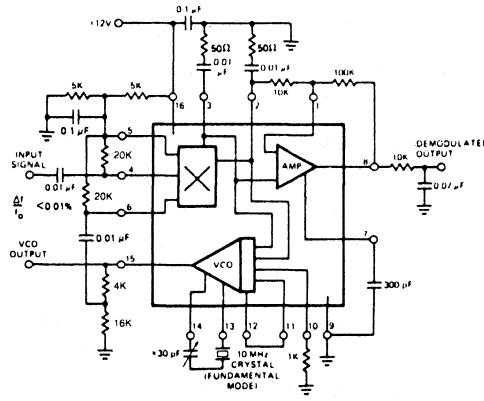


Figure 27. Typical Circuit Connection for Crystal-Controlled Clock Recovery.

crystal to set the crystal frequency. For this application the crystal should be operated in its fundamental mode. Typical pull-in range of the circuits is ±1 kHz at 10 MHz. There is some distortion on the demodulated output.

FSK Demodulator/Tone Decoder

GENERAL DESCRIPTION

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications applications. It is particularly suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL, and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power supply provides ration metric operation for low system performance variations with power supply changes.

The XR-2211 is available in 14 pin DIP ceramic or plastic packages specified for commercial or military temperature ranges.

FEATURES

Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20 V
HCMOS / TTL / Logic Compatibility	
FSK Demodulation, with Carrier Detection	
Wide Dynamic Range	2 mV to 3 V rms
Adjustable Tracking Range (±1% to ±80%)	
Excellent Temp. Stability	20 ppm/°C, typ.

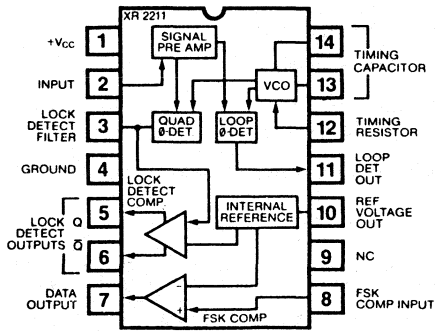
APPLICATIONS

FSK Demodulation
Data Synchronization
Tone Decoding
FM Detection
Carrier Detection

ABSOLUTE MAXIMUM RATINGS

Power Supply	20V
Input Signal Level	3V rms
Power Dissipation	900 mW
Ceramic Package	750 mW
Derate Above T_A = +25°C	8mW°C
Plastic Package	800 mW
Derate Above T_A = +25°C	60 mW/°C
JEDEC SO and Japanese SO	390 mW
Derate Above T_A = +25°C	5 mW/°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2211M	Ceramic	−55°C to +125°C
XR-2211CN	Ceramic	0°C to +70°C
XR-2211CP	Plastic	0°C to +70°C
XR-2211N	Ceramic	−40°C to +85°C
XR-2211P	Plastic	−40°C to +85°C
XR-2211CD	JEDEC SO-14	0°C to 70°C
XR-2211MD	Japanese SO-14	0°C to 70°C

SYSTEM DESCRIPTION

The output of the phase detector produces sum and difference frequencies of the input and the VCO (internally connected). When in lock, these frequencies are $f_{IN} + f_{VCO}$ (2 times f_{IN} when in lock) and $f_{IN} - f_{VCO}$ (0HZ when lock). By adding a capacitor to the phase detector output, the 2 times f_{IN} component is reduced, leaving a DC voltage that represents the phase difference between the two frequencies. This closes the loop and allows the VCO to track the input frequency.

The other sections of the XR-2211 act to: determine if the VCO is driven above or below the center frequency (FSK comparator); produced both active high and active low outputs to indicate when the main PLL is in lock (quadrature phase detector and lock detector comparator).

XR-2211

ELECTRICAL CHARACTERISTICS

Test Conditions: $V+ = 12V$, $T_A = +25°C$, $R_O = 30\ K\Omega$, $C_O = 0.033\ \mu F$.

PARAMETER	XR-2211/2211M			XR-2211C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL								
Supply Voltage	4.5		20	4.5		20	V	
Supply Current		4	7		5	9	mA	$R_0 \geq 10\ k\Omega$. See Fig. 4
OSCILLATOR SECTION								
Frequency Accuracy		±1	±3		±1		%	Deviation from $f_0 = 1/R_0C_0$
Frequency Stability								$R_1 = 1/2$
Temperature		±20	±50		±20		ppm/°C	* See Figure. 8
Power Supply		0.05	0.5		0.05		%/V	$V^+ = 12 \pm 1V$. See Fig. 7.
		0.2			0.2		%/V	$V^+ 5 \pm 0.5V$. See Fig. 7.
Upper Frequency Limit	100	300			300		kHz	$R_0 = 8.2\ k\Omega$, $C_0 = 400\ pF$
Lowest Practical								
Operating Frequency			0.01		0.01		Hz	$R_0 = 2\ M\Omega$, $C_0 = 50\ \mu F$
Timing Resistor, R_0								See Fig. 5.
Operating Range	5		2000	5		2000	kΩ	
Recommended Range	15		100	15		100	kΩ	See Figs. 7 and 8.
LOOP PHASE DETECTOR SECTION								
Peak Output Current	±150	±200	±300	±100	±200	±300	μA	Measured at Pin 11.
Output Offset Current		±1			±2		μA	
Output Impedance		1			1		MΩ	
Maximum Swing	±4	±5		±4	±5		V	Referenced to Pin 10.
QUADRATURE PHASE DETECTOR								Measured at Pin 3.
Peak Output Current	100	150			150		μA	
Output Impedance		1			1		MΩ	
Maximum Swing		11			11		V pp	
INPUT PREAMP SECTION								Measured at Pin 2.
Input Impedance		20			20		kΩ	
Input Signal								
Voltage Required to								
Cause Limiting		2	10		2		mV rms	
VOLTAGE COMPARATOR SECTIONS								
Input Impedance		2			2		MΩ	Measured at Pins 3 and 8.
Input Bias Current		100			100		nA	
Voltage Gain	55	70		55	70		dB	$R_L = 5.1\ k\Omega$
Output Voltage Low		300			300		mV	$I_C = 3\ mA$
Output Leakage Current		0.01			0.01		μA	$V_O = 20V$
INTERNAL REFERENCE								
Voltage Level	4.9	5.3	5.7	4.75	5.3	5.85	V	Measured at Pin 10.
Output Impedance		100			100		Ω	AC Small Signal
Maximum Source Current		80			80		μA	

* These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

PRINCIPLES OF OPERATION

Signal Input (Pin 2): Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20 KΩ. Recommended input signal level is in the range of 10 mV rms to 3V rms.

Quadrature Phase Detector Output (Pin 3): This is the high impedance output of quadrature phase detector and is internally connected to the input of lock detect voltage comparator. In tone detection applications, Pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 2) to eliminate the chatter at lock detect outputs. If the tone detect section is not used, Pin 3 can be left open circuited.

Lock Detect Output, Q (Pin 5): The output at Pin 5 is at "high" state when the PLL is out of lock and goes to "low" or conducting state when the PLL is locked. It is an open collector type output and requires a pull-up resistor, R_L, to V+ for proper operation. At "low" state, it can sink up to 5 mA of load current.

Lock Detect Complement, $\overline{Q}$ (Pin 6): The output at Pin 6 is the logic complement of the lock detect output at Pin 5. This output is also an open collector type stage which can sink 5 mA of load current at low or "on" state.

FSK Data Output (Pin 7): This output is an open collector logic stage which requires a pull-up resistor, R_L, to V+ for proper operation. It can sink 5 mA of load current. When decoding FSK signals, FSK data output is at "high" or "off" state for low input frequency, and at "low" or "on" state for high input frequency. If no input signal is present, the logic state at Pin 7 is indeterminate.

FSK Comparator Input (Pin 8): This is the high impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase detector output (Pin 11). This data filter is formed by R_F and C_F of Figure 2. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at Pin 10.

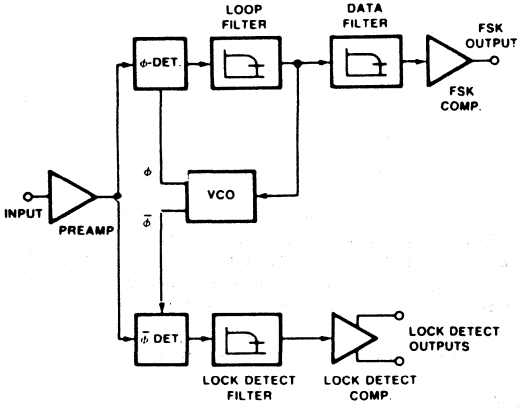


Figure 1. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211

Reference Voltage, V_R (Pin 10): This pin is internally biased at the reference voltage level, V_R: $V_R = V+/2 - 650$ mV. The dc voltage level at this pin forms an internal reference for the voltage levels at Pins 5, 8, 11 and 12. Pin 10 *must* be bypassed to ground with a 0.1 μF capacitor for proper operation of the circuit.

Loop Phase Detector Output (Pin 11): This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R_1 and C_1 connected to Pin 11 (see Figure 2). With no input signal, or with no phase error within the PLL, the dc level at Pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

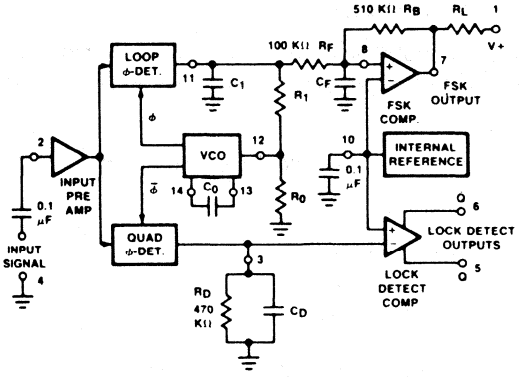


Figure 2. Generalized Circuit Connection for FSK and Tone Detection

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. The VCO free-running frequency, f_0, is:

$$f_0 = \frac{1}{R_0 C_0} \text{ Hz}$$

where C_0 is the timing capacitor across Pins 13 and 14. For optimum temperature stability, R_0 must be in the range of 10 KΩ to 100 KΩ see Figure 8).

This terminal is a low impedance point, and is internally biased at a dc level equal to V_R. The maximum timing current drawn from Pin 12 must be limited to ≤3 mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (see Figure 5). C_0 must be nonpolar, and in the range of 200 pF to 10 μF.

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at Pin 12 (see Figure 9).

VCO Free-Running Frequency, f_0: XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. For set-up or adjustment

purposes, the VCO free-running frequency can be tuned by using the generalized circuit in Figure 2, and applying an alternating bit pattern of O's and I's at known mark and space frequencies. By adjusting R_O, the VCO can then be tuned to obtain a 50% duty cycle on the FKS output (pin 7). This sill ensure that the VCO f_o value is accurately referenced to the mark and space frequencies.

DESIGN EQUATIONS

(See Figure 2 for definition of components.)

1. VCO Center Frequency, f_0:

   $f_0 = 1/R_0C_0$ Hz

2. Internal Reference Voltage, V_R (measured at Pin 10):

   $V_R = V+/2 - 650$ mV

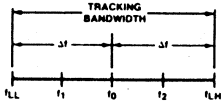
3. Loop Low-Pass Filter Time Constant, τ:

   $\tau = R_1C_1$

4. Loop Damping, ζ:

   $$\zeta = 1/4\sqrt{\frac{C_0}{C_1}}$$

5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$:
   $\Delta f/f_0 = R_0/R_1$



6. FSK Data Filter Time Constant, τF:
   $\tau F = R_FC_F$

7. Loop Phase Detector Conversion Gain, $K\phi$: ($K\phi$ is the differential dc voltage across Pins 10 and 11, per unit of phase error at phase detector input):

   $K\phi = 02V_R/\pi$ volts/radian

8. VCO Conversion gain, K_0: (K_0 is the amount of change in VCO frequency, per unit of dc voltage change at Pin 11):

   $K_0 = -1/V_RC_0R_1$ Hz/volt

9. Total Loop Gain, K_T:

   $K_T = 2\pi K\phi K_0 = 4/C_0R_1$ rad/sec/volt

10. Peak Phase Detector Current I_A:

    $I_A = V_R$ (volts)/25 mA

APPLICATIONS INFORMATION

FSK DECODING:

Figure 9 shows the basic circuit connection for FSK decoding. With reference to Figures 2 and 9, the functions of external components are defined as follows: R_0 and C_0 set the PLL center frequency, R_1 sets the system bandwidth, and C1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one-pole post-detection filter for the FSK data output. The resistor R_B (= 510 KΩ) from Pin 7 to Pin 8 introduces positive feedback across the FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bands are given in Table 1.

Design Instructions:

The circuit of Figure 9 can be tailored for any FSK decoding application by the choice of five key circuit components: R_0, R_1, C_0, C_1 and C_F. For a given set of FSK mark and space frequencies, f_1 and f_2, these parameters can be calculated as follows:

a) Calculate PLL center frequency, f_0:

$$f_O = \frac{f_1 + f_2}{2}$$

b) Choose value of timing resistor R_0, to be in the range of 10 KΩ to 100 KΩ. This choice is arbitrary.

The recommended value is $R_0 \equiv 20$ KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

c) Calculate value of C_0 from design equation (1) or from Figure 6:

$C_0 = 1/R_0f_0$

d) Calculate R_1 to give a Δf equal to the mark space deviation:

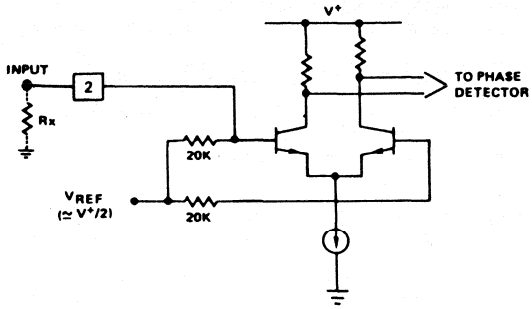
$R_1 = R_0[f_0/(f_1 - f_2)]$

e) Calculate C_1 to set loop damping. (See design equation No. 4.):

Normally, $\zeta \approx 1/2$ is recommended.

Then: $C_1 = C_0/4$ for $\zeta = 1/2$

f) The input to the XR-2211 may sometimes be to sensitive to noise conditions on the input line. Figure 3 illustrates a method of de-sensitizing the XR-2211 from such noisy line conditions by the use of a resistor, R_X, connected from pin 2 to ground. The value of R_X is chosen by the equation and the desired minimum signal threshold level.



$$V_{IN\ MINIMUM\ (PEAK)} \simeq V^+ \left[\frac{10K}{R_X + 20K}\right] \pm 2.8\ mV$$

Figure 3. Desensitizing Input Stage

g) Calculate Data Filter Capacitance, C_F:

For R_F = 100 KΩ, R_B = 510 KΩ, the recommended value of C_F is:

$C_F \approx 3/(\text{Baud Rate})\ \mu F$

Note: All calculated component values except R_0 can be rounded to the nearest standard value, and R_0 can be varied to fine-tune center frequency, through a series potentiometer, R_X. (See Figure 9.)

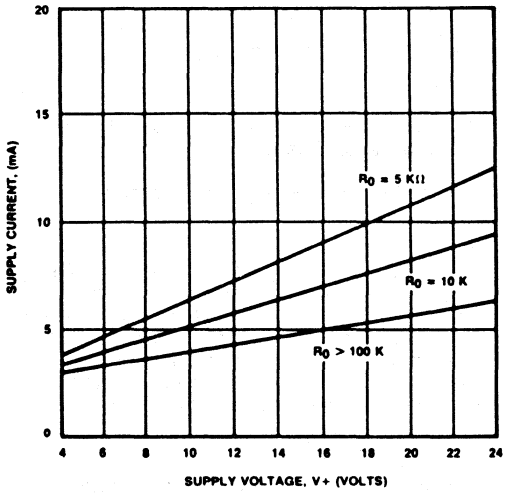


Figure 4. Typical Supply Current vs V^+ (Logic Outputs Open Circuited)

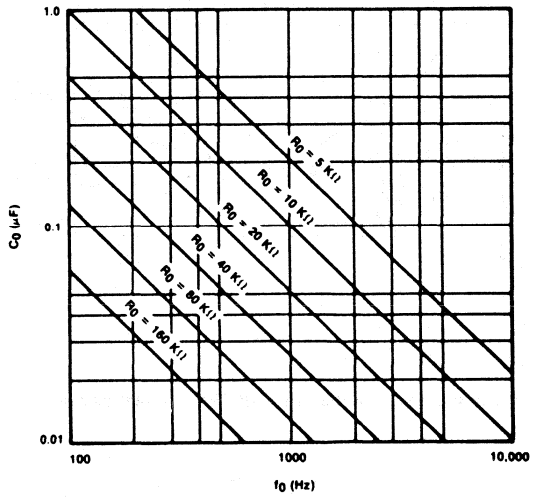


Figure 5. VCO Frequency vs Timing Resistor

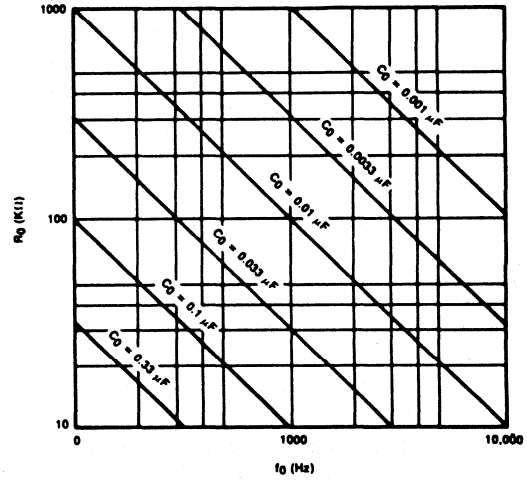


Figure 6. VCO Frequency vs Timing Capacitor

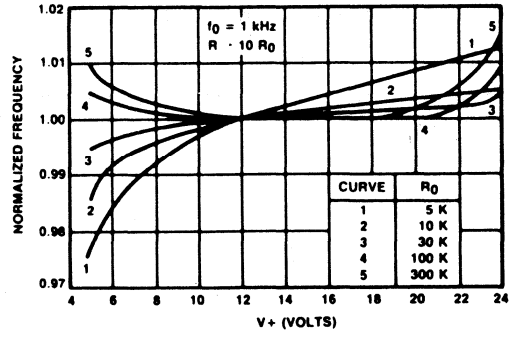


Figure 7. Typical f_0 vs Power Supply Characteristics

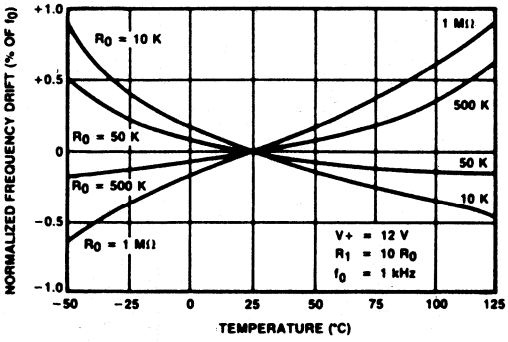


Figure 8. Typical Center Frequency Drift vs Temperature

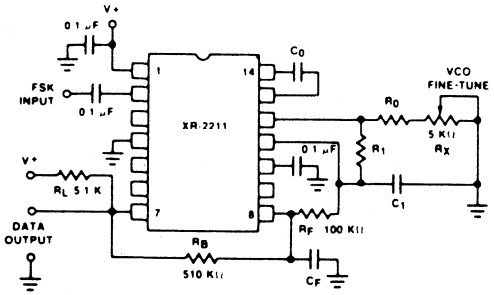


Figure 9. Circuit Connection for FSK Decoding

Design Example:

75 Baud FSK demodulator with mark space frequencies of 1110/1170 Hz:

Step 1: Calculate f_0: f_0 (1110 + 1170) (1/2) = 1140 Hz

Step 2: Choose R_0 - 20 KΩ (18 KΩ fixed resistor in series with 5 KΩ potentiometer)

Step 3: Calculate C_0 from Figure 6: C_0 = 0.044 μF

Step 4: Calculate R_1: R_1 = R_0 (1140/60)= 380 KΩ

Step 5: Calculate C_1: C_1 = C_0/4 = 0.011 μF

Note: All values except R_0 can be rounded to *nearest* standard value.

Table 1. Recommended Component Values for Commonly Used FSK Bands. (See Circuit of Figure 9.)

FSK BAND	COMPONENT VALUES
300 Baud f_1 = 1070 Hz F_2 = 1270 Hz	C_O = 0.039 μF C_F = 0.005 μF C_1 = 0.01 μF R_O = 18 KΩ R_1 = 100 KΩ
300 Baud f_1 = 2025 Hz f_2 = 2225 Hz	C_O = 0.022 μF C_F = 0.005 μF C_1 = 0.0047 μF R_O = 18 KΩ R_1 = 200 KΩ
1200 Baud f_1 = 1200 Hz f_2 = 2200 Hz	C_O = 0.027 μF C_F = 0.0022 μF C_1 = 0.01 μF R_O = 18 KΩ R_1 = 30 KΩ

FSK DECODING WITH CARRIER DETECT:

The lock detect section of XR-2211 can be used as a carrier detect option, for FSK decoding. The recommended circuit connection for this application is shown in Figure 10. The open collector lock detect output, Pin 6, is shorted to data output (Pin 7). Thus, data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL and the Pin 6 output goes "high," to enable the data output.

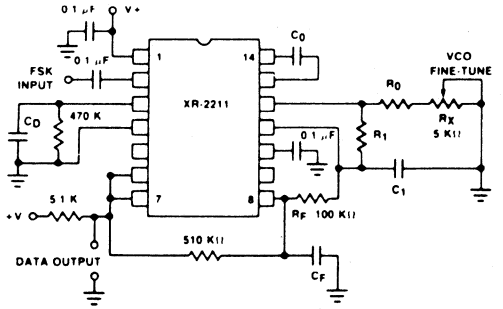


Figure 10. External Connectors for FSK Demodulation with Carrier Detect Capability

Note: Data Output is "Low" When No Carrier is Present.

The minimum value of the lock detect filter capacitance C_D is inversely proportional to the capture range, ± Δf_C. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C_1. For most applications, $\Delta f_C > \Delta f/2$. For R_D = 470 KΩ, the approximate minimum value of C_D can be determined by:

C_D (μF) ≥ 16/capture range in Hz.

With values of C_D that are too small, chatter can be observed on the lock detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock detect output.

TONE DETECTION:

Figure 11 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\overline{Q}$ at Pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5 mA of load current.

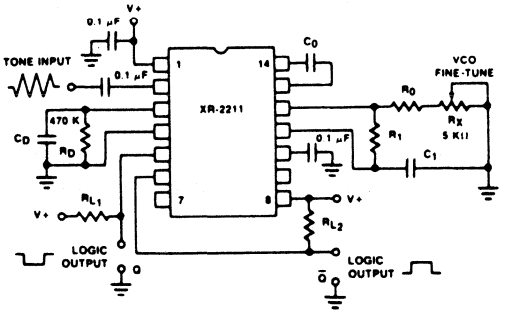


Figure 11. Circuit Connection for Tone Detection

Both logic outputs at Pins 5 and 6 are open collector type stages, and require external pull-up resistors R_{L1} and R_{L2}, as shown in Figure 11.

With reference to Figures 2 and 11, the functions of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency; R_1 sets the detection bandwidth; C_1 sets the low pass-loop filter time constant and the loop damping factor. R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\overline{Q}$ logic outputs.

Design Instructions:

The circuit of Figure 11 can be optimized for any tone detection application by the choice of the 5 key circuit components: R_0, R_1, C_0, C_1 and C_D. For a given input, the tone frequency, f_S, these parameters are calculated as follows:

a) Choose R_0 to be in the range of 15 KΩ to 100 KΩ. This choice is arbitrary.

b) Calculate C_0 to set center frequency, f_0 equal to f_S (see Figure 6): $C_0 = 1/R_0 f_S$

c) Calculate R_1 to set bandwidth $\pm\Delta f$ (see design equation No. 5):

$$R_1 = R_0(f_0/\Delta f)$$

Note: The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$.

d) Calculate value of C_1 for a given loop damping factor;

$$C_1 = C_0/16\,\zeta^2$$

Normally $\zeta \approx 1/2$ is optimum for most tone detector applications, giving $C_1 = 0.25\,C_0$.

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

e) Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with R_D = 470 KΩ, C_D must be:

$$C_D(\mu F) \geq (16/\text{capture range in Hz})$$

Increasing C_D slows down the logic output response time.

Design Examples:

Tone detector with a detection band of 1 kHz ± 20 Hz:

a) Choose R_0 = 20 KΩ (18 KΩ in series with 5 KΩ potentiometer).

b) Choose C_0 for f_0 = 1 kHz (from Figure 6): C_0 = 0.05 μF.

c) Calculate R_1: $R_1 = (R_0)\,(1000/20)$ = 1 MΩ.

d) Calculate C_1: for ζ = 1/2, C_1 = 0.25, C_0 = 0.013 μF.

e) Calculate C_D: C_D = 16/38 = 0.42 μF.

f) Fine-tune center frequency with 5 KΩ potentiometer, R_X.

LINEAR FM DETECTION:

XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this application is shown in Figure 12. The demodulated output is taken from the loop phase detector output (Pin 11), through a post-detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at Pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 12.

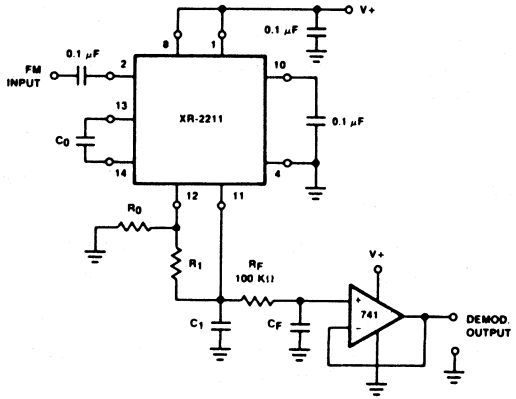


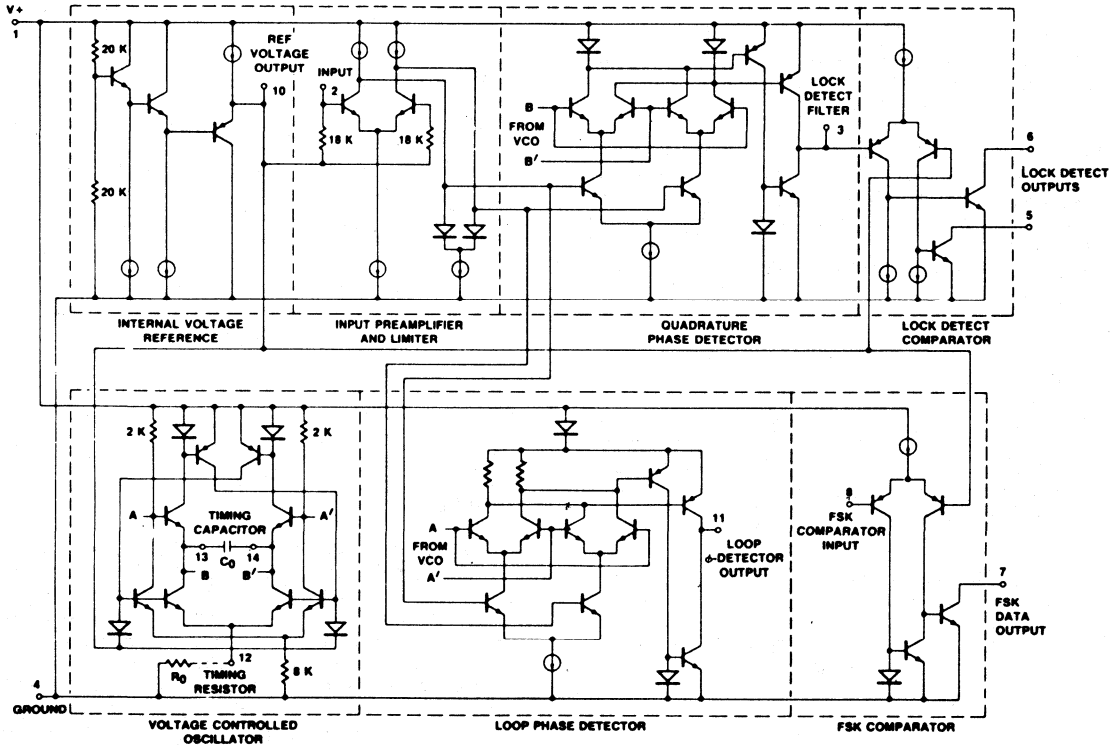
Figure 12. Linear FM Detector Using XR-2211 and an External Op Amp. (See Section on Design Equation for Component Values.)

The FM detector gain, i.e., the output voltage change per unit of FM deviation can be given as:

$$V_{out} = R_1 V_R/100 R_0 \text{ Volts/\% deviation}$$

where V_R is the internal reference voltage ($V_R = V+/2 - 650$ mV). For the choice of external components R_1, R_0, C_D, C_1 and C_F, see section on design equations.

EQUIVALENT SCHEMATIC DIAGRAM



Precision Phase-Locked Loop

GENERAL DESCRIPTION

The XR-2212 is an ultra-stable monolithic phase-locked loop (PLL) system especially designed for data communications and control system applications. Its on board reference and uncommitted operational amplifier, together with a typical temperature stability of better than 20 ppm/°C, make it ideally suited for frequency synthesis, FM detection, and tracking filter applications. The wide input dynamic range, large operating voltage range, large frequency range, and HCMOS and TTL compatibility contribute to the usefullness and wide applicability of this device.

FEATURES

Quadrature VCO Outputs	
Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20V
TTL/HCMOS Compatible	(V_{CC} = 5VDC)
Wide Dynamic Range	2 mV to 3 Vrms
Adjustable Tracking Range (±1% to ±80%)	
Excellent Temp. Stability	20 ppm/°C, Typ.

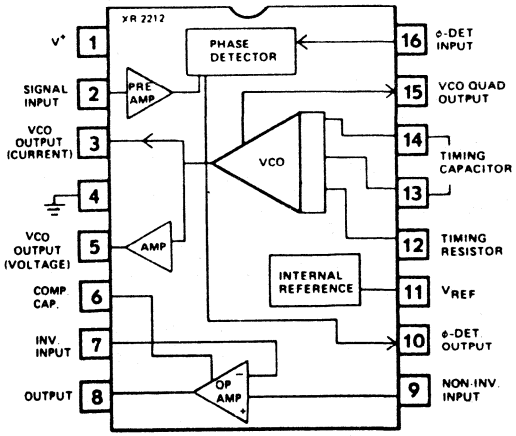
APPLICATIONS

Frequency Synthesis
Data Synchronization
FM Detection
Tracking Filters
FSK Demodulation

ABSOLUTE MAXIMUM RATINGS

Power Supply	18V
Input Signal Level	3 Vrms
Power Dissipation	
Ceramic Package:	750 mW
Derate Above T_A = +25°C	6 mW/°C
Plastic Package:	625 mW
Derate Above T_A = +25°C	5 mW/°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2212M	Ceramic	−55°C to +125°C
XR2212CN	Ceramic	0°C to +70°C
XR-2212CP	Plastic	0°C to +70°C
XR-2212N	Ceramic	−40°C to +85°C
XR-2212P	Plastic	−40°C to +85°C

SYSTEM DESCRIPTION

The XR-2212 is a complete PLL system with buffered inputs and outputs, an internal reference, and an uncommited op amp. Two VCO outputs are pinned out; one sources current, the other sources voltage. This enables operation as a frequency synthesizer using an external programmable divider. The op amp section can be used as an audio preamplifier for FM detection or as a high speed sense amplifier (comparator) for FSK demodulation. The center frequency, bandwidth, and tracking range of the PLL are controlled independantly by external components. The PLL output is directly by compatible with CMOS, HCMOS and TTL logic families as well as microprocessor peripheral systems.

The precision PLL system operates over a supply voltage range of 4.5 V to 20 V, a frequency range of 0.01 Hz to 300 kHz, and accepts input signals in the range of 2 mV to 3 Vrms. Temperature stability of the VCO is typically better than 20 ppm/ C, with the optimum timing resistor value.

XR-2212

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +12V$, $T_A = +25°C$, $R_0 = 30\ k\Omega$, $C_0 = 0.033\ \mu F$, unless otherwise specified. See Figure 2 for component designation.

PARAMETERS	XR-2212/2212M			XR-2212C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL								
Supply Voltage	4.5		15	4.5		15	V	
Supply Current		6	10		6	12	mA	$R_0 \geq 10\ K\Omega$. See Fig. 4
OSCILLATOR SECTION								
Frequency Accuracy		±1	±3		±1		%	Deviation from $f_0 = 1/R_0C_0$
Frequency Stability								$R_1 = \infty$
Temperature		±20	±50		±20		ppm/°C	See Fig. 8.*
Power Supply		0.05	0.5		0.05		%/V	$V^+ = 12 \pm 1$ V. See Fig. 7.
		.2			.2		%/V	$V^+ = 5 \pm 0.5$ V. See Fig. 7.
Upper Frequency Limit	100	300			300		kHz	$R_0 = 8.2\ K\Omega$, $C_0 = 400\ pF$
Lowest Practical								
Operating Frequency			0.01		0.01		Hz	$R_0 = 2\ M\Omega$, $C_0 = 50\ \mu F$
Timing Resistor, R_0								See Fig. 5.
Operating Range	5		2000	5		2000	KΩ	
Recommended Range	15		100	15		100	KΩ	See Fig. 7 and 8.
OSCILLATOR OUTPUTS								
Voltage Output								Measured at Pin 5.
Positive Swing, V_{OH}		11			11		V	
Negative Swing, V_{OL}		.4	.8		.5		V	
Current Sink Capability		1			1		mA	
Current Output								Measured at Pin 3.
Peak Current Swing	100	150			150		μA	
Output Impedance		1			1		MΩ	
Quadrature Output								Measured at Pin 15.
Output Swing		0.6			0.6		V	
DC Level		0.3			0.3		V	Referenced to Pin 11.
Output Impedance		3			3		KΩ	
LOOP PHASE DETECTOR SECTION								Measured at Pin 10.
Peak Output Current	±150	±200	±300	±100	±200	±300	μA	
Output Offset Current		±1			±2		μA	
Output Impedance		1			1		MΩ	
Maximum Swing	±4	±5		±4	±5		V	Referenced to Pin 11.
INPUT PREAMP SECTION								Measured at Pin 2.
Input Impedance		20			20		KΩ	
Input Signal to Cause Limiting		2	10		2		mVrms	
OP AMP SECTION								
Voltage Gain	55	70		55	70		dB	$R_L = 5.1\ K\Omega$, $R_F = \infty$
Input Bias Current		0.1	1		0.1	1	μA	
Offset Voltage		±5	±20		±5	±20	mV	
Slew Rate		2			2		V/μsec	
INTERNAL REFERENCE								Measured at Pin 11.
Voltage Level	4.9	5.3	5.7	4.75	5.3	5.85	V	
Output Impedance		100			100		Ω	AC Small Signal
Maximum Source Current		80			80		μA	

* For XR-2212P and XR-2212N, the parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production

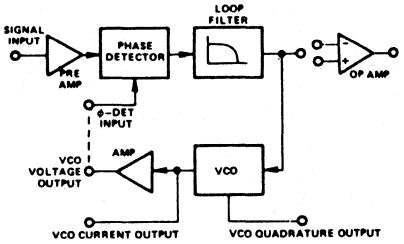


Figure 1. Functional Block Diagram of XR-2212 Precision PLL System

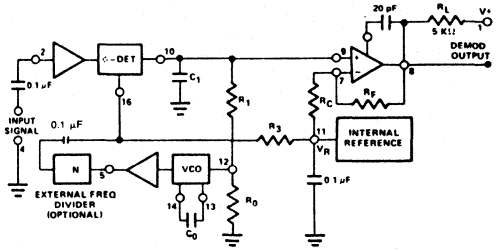


Figure 2. Generalized Circuit Connection for FM Detection, Signal Tracking or Frequency Synthesis

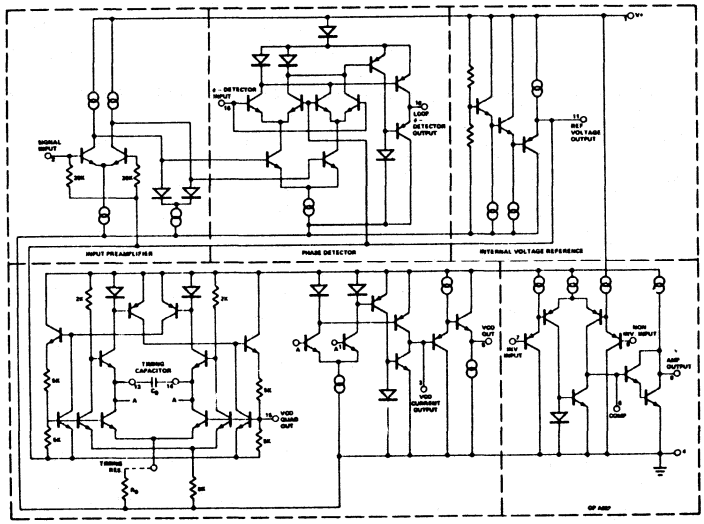


Figure 3. Simplified Circuit Schematic of XR-2212

TYPICAL CHARACTERISTICS

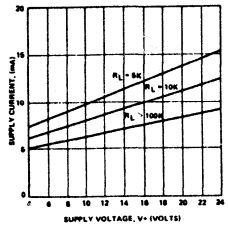


Figure 4. Typical Supply Current vs V+ (Logic Outputs Open Circuited)

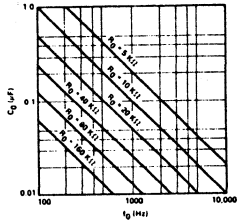


Figure 5. VCO Frequency vs Timing Resistor

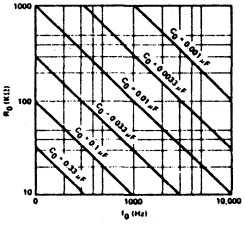


Figure 6. VCO Frequency vs Timing Capacitor

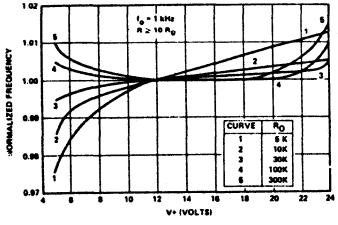


Figure 7. Typical f_0 vs Power Supply Characteristics

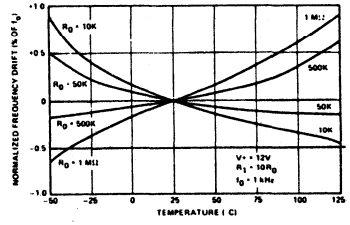


Figure 8. Typical Center Frequency Drift vs Temperature

DESCRIPTION OF CIRCUIT CONTROLS

Signal Input (Pin 2): Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20 KΩ. Recommended input signal level is in the range of 10 mV to 5V peak-to-peak. If desired , the input can be de-sensitized by adding R_X to pin 2 to V_{EE} (pin 4). The formula is V_{IN} =

$$V+\left[\frac{10K}{R_X+20K}\right]\pm 2.8mV$$

VCO Current Output (Pin 3): This is a high impedance (MΩ) current output terminal which can provide ±100 μA drive capability with a voltage swing equal to V+. This output can directly interface with CMOS or NMOS logic families.

VCO Voltage Output (Pin 5): This terminal provides a low-impedance (≈ 50Ω) buffered output for the VCO. It can directly interface with low-power Schottley TTL. For interfacing with standard TTL circuits, a 750Ω pull-down resistor from pin 5 to ground is required. For operation of the PLL without an external divider, pin 5 can be dc coupled to pin 16.

Op Amp Compensation (Pin 6): The op amp section is frequency compensated by connecting an external capacitor from pin 6 to the amplifier output (pin 8). For unity-gain compensation a 20 pF capacitor is recommended.

Op Amp Inputs (Pins 7 and 9): These are the inverting and the non-inverting inputs for the op amp section. The common-mode range of the op amp inputs is from +1V to (V+ − 1.5) volts.

Op Amp Output (Pin 8): The op amp output is an open-collector type gain stage and requires a pull-up resistor, R_L, to V+ for proper operation. For most applications, the recommended value of R_L is in 5 kΩ to 10 kΩ range.

Phase Detector Output (Pin 10): This terminal provides a high-impedance output for the loop phase-detector. The PLL loop filter is formed by R_1 and C_1 connected to Pin 10 (see Figure 2). With no input signal, or with no phase-error within the PLL, the dc level at Pin 10 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to ±V_R.

Reference Voltage, V_R (Pin 11): This pin is internally biased at the reference voltage level, V_R:V_R = V+/2—650 mV. The dc voltage level at this pin forms an internal reference for the voltage levels at pins 10, 12 and 16. Pin 1 *must* be bypassed to ground with a 0.1 μF capacitor, for proper operation of the circuit.

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. For optimum temperature stability, R_0 must be in the range of 10 KΩ to 100 KΩ (see Figure 8).

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at Pin 12 (see Figure 10).

This terminal is a low-impedance point, and is internally biased at a dc level equal to V_R. The maximum timing current drawn from Pin 12 must be limited to ≤3 mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (see Figure 5). C_0 must be nonpolar, and in the range of 200 pF to 10 μF.

VCO Quadrature Output (Pin 15): The low-level (≈0.6 Vpp) output at this pin is at quadrature phase (i.e. 90° phase-offset) with the other VCO outputs at pins 3 and 5. The dc level at pin 15 is approximately 300 mV above V_R. The quadrature output can be used with an external multiplier as a "lock detect" circuit. In order not to degrade oscillator performance, the output at pin 15 must be buffered with an external high-impedance low-capacitance amplifier. When not in use, pin 15 should be left open-circuited.

Phase Detector Input (Pin 16): Voltage output of the VCO (pin 5) or the output of an external frequency divider is connected to this pin. The dc level of the sensing threshold for the phase detector is referenced to V_R. If the signal is capacitively coupled to pin 16, then this pin must be biased from pin 11, through an external resistor, R_B (R_B ≈ 10 KΩ). The peak voltage swing applied to pin 16 *must not* exceed (V+ − 1.5) volts.

PHASE-LOCKED LOOP PARAMETERS:

Transfer Characteristics:

Figure 9 shows the basic frequency to voltage characteristics of XR-2212. With no input signal present, filtered phase detector output voltage is approximately equal to the internal reference voltage, V_R, at pin 11. The PLL can track an input signal over its tracking bandwidth, shown in the figure. The frequencies f_{TL} and f_{TH} represent the lower and the upper edge of the tracking range, f_0 represents the VCO center frequency.

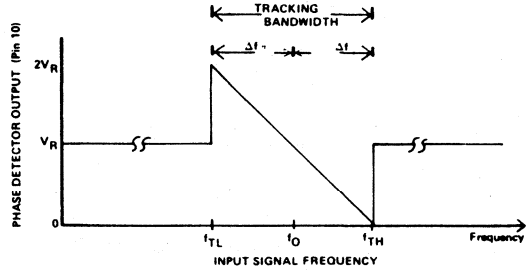


Figure 9. Phase Detector Output Voltage (Pin 10) as a Function of Input Signal Frequency. Note: Output Voltage is Referenced to Internal Reference Voltage V_R at Pin 11

Design Equations:

(See Figure 2 and Figure 9 for definition of components.)

1. VCO Center Frequency, f_0: $f_0 = 1/R_0C_0$ Hz

2. Internal Reference Voltage, V_R (measured at Pin 11)

   $V_R = V+/2 - 650$ mV

3. Loop Low-Pass Filter Time Constant, τ: $\tau = R_1C_1$

4. Loop Damping, ζ: $\zeta = 0.25\sqrt{\frac{NC_0}{C_1}}$

   where N is the external frequency divider modular (See 2). If no divider is used, N = 1.

5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$: $\Delta f/f_0 = R_0/R_1$

6. Phase Detector Conversion Gain, K_ϕ: (K_ϕ is the differential dc voltage across Pins 10 and 11, per unit of phase error at phase-detector input) $K_\phi = -2V_R/\pi$ volts/radian

7. VCO Conversion Gain, K_0: (K_0 is the amount of change in VCO frequency, per unit of dc voltage change at Pin 10. It is the reciprocal of the slope of conversion characteristics shown in Figure 9). $K_0 = -1/V_RC_0R_1$ Hz/volt

8. Total Loop Gain, K_T:

   $K_T = 2\pi K_\phi K_0 = 4/C_0R_1$ rad/sec/volt

9. Peak Phase-Detector Current, I_A; available at pin 10.

   $I_A = V_R$ (volts)/25 mA

APPLICATION INFORMATION

FM DEMODULATION:

XR-2212 can be used as a linear FM demodulator for both narrow-band and wide-band FM signals. The generalized circuit connection for this application is shown in Figure 10, where the VCO output (pin 5) is directly connected to the phase detector input (pin 16). The demodulated signal is obtained at phase detector output (pin 10). In the circuit connection of Figure 10, the op amp section of XR-2212 is used as a buffer amplifier to provide both additional voltage amplification as well as current drive capability. Thus, the demodulated output signal available at the op amp output (pin 8) is fully buffered from the rest of the circuit.

In the circuit of Figure 10, R_0C_0 set the VCO center frequency, R_1 sets the tracking bandwidth, C_1 sets the low-pass filter time constant. Op amp feedback resistors R_F and R_C set the voltage gain of the amplifier section.

Design Instructions:

The circuit of Figure 10 can be tailored to any FM demodulation application by a choice of the external components R_0, R_1, R_C, R_F, C_0 and C_1. For a given FM center frequency and frequency deviation, the choice of these components can be calculated as follows, using the design equations and definitions given on page 1-34, 1-35 and 1-36.

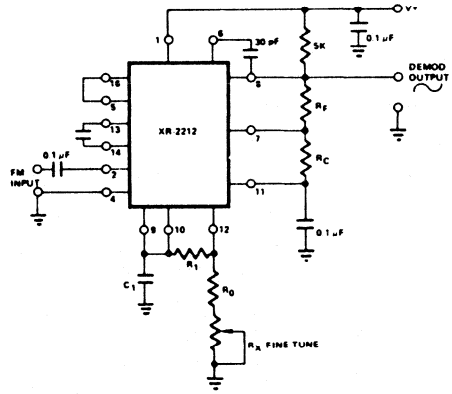


Figure 10. Circuit Connection for FM Demodulation

a) Choose VCO center frequency f_0 to be the same as FM carrier frequency.

b) Choose value of timing resistor R_0, to be in the range of 10 KΩ to 100 KΩ. This choice is arbitrary. The recommended value is $R_0 \cong 20$ KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

c) Calculate value of C_0 from design equation (1) or from Figure 6:

$$C_0 = 1/R_0f_0$$

d) Choose R_1 to determine the tracking bandwidth, Δf (see design equation 5). The tracking bandwidth, Δf, should be set significantly wider than the maximum input FM signal deviation, Δf_{SM}. Assuming the tracking bandwidth to be "N" times larger than Δf_{SM}, one can re-unite design equation 5 as:

$$\frac{\Delta f}{f_0} = \frac{R_0}{R_1} = N\frac{\Delta f_{SM}}{f_0}$$

Table I lists recommended values of N, for various values of the maximum deviation of the input FM signal.

% Deviation of FM Signal ($\Delta f_{SM}/f_0$)	Recommended value of Bandwidth Ratio, N ($N = \Delta f/\Delta f_{SM}$)
1% or less	10
1 to 3%	5
1 to 5%	4
5 to 10%	3
10 to 30%	2
30 to 50%	1.5

TABLE I

Recommended values of bandwidth ratio, N, for various values of FM signal frequency deviation. (Note: N is the ratio of tracking bandwidth Δf to max. signal frequency deviation, Δf_{SM}).

e) Calculate C_1 to set loop damping (see design equation 4). Normally, $\zeta = 1/2$ is recommended. Then, $C_1 = C_0/4$ for $\zeta = 1/2$. Otherwise ζ is calculated by

$$\zeta = \frac{1}{2\sqrt{K_D K_O \cdot 2 \cdot \pi \cdot 1 \times 10^6 \cdot C}} \frac{\text{sec}}{\text{sec}}$$

f) Calculate R_C and R_F to set peak output signal amplitude. Output signal amplitude, V_{out}, is given as:

$$V_{out} = \left(\frac{\Delta f_{SM}}{f_0}\right)\left(V_R\right)\left(\frac{R_1}{R_0}\right)\left[\frac{R_C + R_F}{R_C}\right]$$

In most applications, $R_F = 100\ K\Omega$ is recommended; then R_C, can be calculated from the above equation to give desired output swing. The output amplifier can also be used as a unity-gain voltage follower, by open circuiting R_C (i.e., $R_C = \infty$).

Note: All calculated component values except R_0 can be rounded-off to the nearest standard value, and R_0 can be varied to fine-tune center frequency, through a series potentiometer, R_X. (See Figure 10.)

Design Example:

Demodulator for FM signal with 67 kHz carrier frequency with ±5 kHz frequency deviation. Supply voltage is +12V and required peak output swing is ±4 volts.

Step a) f_0 is chosen as 67 kHz.

Step b) Choose $R_0 = 20\ K\Omega$ (18 KΩ fixed resistor in series with 5 KΩ potentiometer).

Step c) Calculate C_0; from design Eq. (1).

$C_0 = 746$ pF

Step d) Calculate R_1. For given FM deviation, $\Delta f_{SM}/f_0 = 0.0746$, and $N = 3$ from Table I.

Then:

$R_0/R_1 = (3)(0.0746) = 0.224$

or:

$R_1 = 89.3\ K\Omega$.

Step e) Calculate $C_1 = (C_0/4) = 186$ pF.

Step f) Calculate R_C and R_F to get ±4 volts peak output swing: Let $R_F = 100\ K\Omega$. Then,

$R_C = 80.6\ K\Omega$.

Note: All values except R_0 can be rounded-off to nearest standard value.

FREQUENCY SYNTHESIS

Figure 11 shows the generalized circuit connection for frequency synthesis. In this application an external frequency divider is connected between the VCO output (pin 5) and the phase-detector input (pin 16). When the circuit is in lock, the two signals going into the phase-detector are at the same frequency, or $f_S = f_1/N$ where N is the modulus of the external frequency divider. Conversely, the VCO output frequency, f_1 is equal to Nf_S.

In the circuit configuration of Figure 11, the external timing components, R_0 and C_0, set the VCO free-running frequency; R_1 sets the tracking bandwidth and C1 sets the loop damping, i.e., the low-pass filter time constant (see design equations).

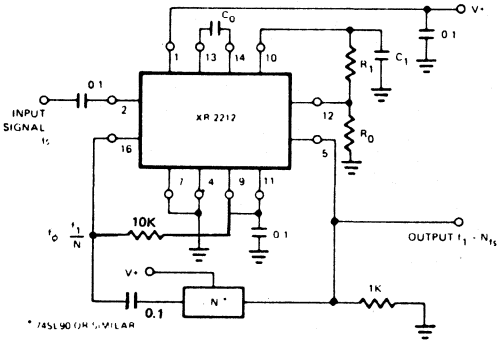


Figure 11. Circuit Connection for Frequency Synthesizer

The total tracking range of the PLL (see Figure 9), should be chosen to accommodate the lowest and the highest frequency, f_{max} and f_{min}, to be synthesized. A recommended choice for most applications is to choose a tracking half-bandwidth Δf, such that:

$$\Delta f \approx f_{max} - f_{min}.$$

If a fixed output frequency is desired, i.e. N and f_S are fixed, then a ±10% tracking bandwidth is recommended. Excessively large tracking bandwidth may cause the PLL to lock on the harmonics of the input signals; and the small tracking range increases the "lock-up" or acquisition time.

If a variable input frequency and a variable counter modulus N is used, then the maximum and the minimum values of output frequency will be:

$$f_{max} = N_{max}\,(f_S)_{max} \text{ and } f_{min} = N_{min}\,(f_S)_{min}.$$

Design Instructions:

For a given performance requirement, the circuit of Figure 11 can be optimized as follows:

a) Choose center frequency, f_0, to be equal to the output frequency to be synthesized. If a range of output frequencies is desired, set f_0 to be at mid-point of the desired range.

b) Choose timing resistor R_0 to be in the range of 15 KΩ to 100 KΩ. This choice is arbitrary. R_0 can be fine tuned with a series potentiometer, R_X.

c) Choose timing capacitor, C_0 from Figure 6 or Equation 1.

d) Calculate R_1 to set tracking bandwidth (see Figure 9, and design equation 5). If a range of output frequencies are desired, set R_1 to get:

$$\Delta f = f_{max} - f_{min}.$$

If a single fixed output frequency is desired, set R_1 to get:

$$\Delta f = 0.1\ f_0.$$

e) Calculate C_1 to obtain desired loop damping. (See design equation 4). For most applications, $\zeta = 1/2$ is recommended, thus:

$$C_1 = NC_0/4$$

Note: All component values except R_0 can be rounded-off to nearest standard value.

5

Monolithic Tone Decoder

GENERAL DESCRIPTION

The XR-567 is a monolithic phase-locked loop system designed for general purpose tone and frequency decoding. The circuit operates over a wide frequency band of 0.01 Hz to 500 kHz and contains a logic compatible output which can sink up to 100 milliamps of load current. The bandwidth, center frequency, and output delay are independently determined by the selection of four external components.

The circuit consists of a phase detector, low-pass filter, and current-controlled oscillator which comprise the basic phase-locked loop; plus an additional low-pass filter and quadrature detector that enables the system to distinguish between the presence or absence of an input signal at the center frequency.

FEATURES

Bandwidth adjustable from 0 to 14%.
Logic compatible output with 100 mA current sinking capability
High stable center frequency.
Center frequency adjustable from 0.01 Hz to 500 kHz
Inherent immunity to false signals
High rejection of out-of-band signals and noise
Frequency range adjustable over 20:1 range by external resistor.

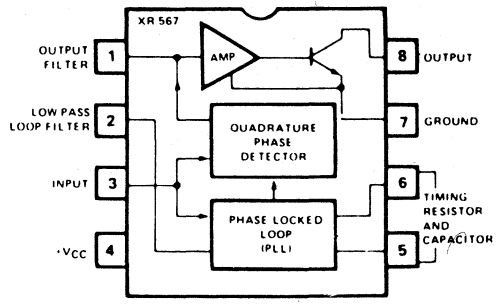
APPLICATIONS

Touch-Tone® Decoding
Sequential Tone Decoding
Communications Paging
Ultrasonic Remote-Control
Telemetry Decoding

ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
SO-8	220 mW
Derate Above +25°C	2.5 mW/°C
Temperature	
Storage	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-567M	Ceramic	−55°C to +125°C
XR-567CN	Ceramic	0°C to +70°C
XR-567CP	Plastic	0°C to +70°C
XR-567MD	Japanese SOIC	0°C to +70°C

SYSTEM DESCRIPTION

The XR-567 monolithic tone decoder consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection on in-band signals. The device has a normally high open collector output capable of sinking 100 mA.

The input signal is applied to Pin 3 (20 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6 and can typically reach 500 kHz. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; bandwidth and skew are also dependant upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 4 is $+V_{CC}$ (4.75 to 9V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is open collector output, pulling low when an in-band signal triggers the device.

In applications requiring two or more 567-type devices, consider the XR-2567 dual tone decoder. Where center frequency accuracy and drift are critical, compare the XR-567A. Investigate employing the XR-L567 in low power circuits.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V. T_A = 25°C, unless otherwise specified. Test circuit of Figure 2.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
GENERAL					
Supply Voltage Range	4.75		9.0	V dc	
Supply Current					
Quiescent XR-567M		6	8	mA	R_L = 20kΩ
XR-567C		7	10	mA	R_L = 20 kΩ
Activated XR-567M		11	13	mA	R_L = 20 kΩ
XR-567C		12	15	mA	R_L = 20 kΩ
Output Voltage			15	V	
Negative Voltage at Input			−10	V	
Positive Voltage at Input			V_{CC} + 0.5	V	
CENTER FREQUENCY					
Highest Center Frequency	100	500		kHz	
Center Frequency Stability					
Temperature T_A = 25°C		35		ppm/°C	See Figure 9
0°C < T_T < 70°C *		±60		ppm/°C	See Figure 9
-55 < T_T < +125°C *		±140		ppm/°C	See Figure 9
Supply Voltage					
XR-567M		0.5	1.0	%/V	f_o = 100 kHz
XR-567C		0.7	2.0	%/V	f_o = 100 kHz
DETECTION BANDWIDTH					
Largest Detection Bandwidth					
XR-567M	12	14	16	% of f_o	f_o = 100 kHz
XR-567C	10	14	18	% of f_o	f_o = 100 kHz
Largest Detection Bandwidth Skew					
XR-567M		1	2	% of f_o	
XR-567C		2	3	% of f_o	
Largest Detection Bandwidth Variation					
Temperature		±0.1		%/°C	V_{in} = 300 mV rms
Supply Voltage		±2		%/V	V_{in} = 300 mV rms
INPUT					
Input Resistance		20		kΩ	
Smallest Detectable Input Voltage		20	25	mV rms	I_L = 100 mA, f_i = f_o
Largest No-Output Input Voltage	10	15		mV rms	I_L = 100 mA, f_i = f_o
Greatest Simultaneous Outband Signal to Inband Signal Ratio		+6		dB	
Minimum Input Signal to Wideband Noise Ratio		−6		dB	B_n = 140 kHz
OUTPUT					
Output Saturation Voltage		0.2	0.4	V	I_L = 30 mA, V_{in} = 25 mV rms
		0.6	1.0	V	I_L = 100 mA, V_{in} = 25 mV rms
Output Leakage Current		0.01	25	μA	
Fastest ON-OFF Cycling Rate		f_o/20			
Output Rise Time		150		ns	R_L = 50Ω
Output Fall Time		30		ns	R_L = 50Ω

*These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

5

DEFINITION OF XR-567 PARAMETERS

CENTER FREQUENCY f_o

f_o is the free-running frequency of the current-controlled oscillator with no input signal. It is determined by resistor R_1 between pins 5 and 6, and capacitor C_1 from pin 6 to ground f_o can be approximated by

$$f_o \approx \frac{1}{R_1 C_1}$$

where R_1 is in ohms and C_1 is in farads.

DETECTION BANDWIDTH (BW)

The *detection bandwidth* is the frequency range centered about f_o, within which an input signal larger than the threshold voltage (typically 20 mV rms) will cause a logic zero state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass bandwidth filter. The bandwidth of the filter, as a percent of f_o, can be determined by the approximation

$$BW = 1070 \sqrt{\frac{V_i}{f_o C_2}}$$

where V_i is the input signal in volts, rms, and C_2 is the capacitance at pin 2 in μF.

LARGEST DETECTION BANDWIDTH

The *largest detection bandwidth* is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

DETECTION BAND SKEW

The *detection band skew* is a measure of how accurately the largest detection band is centered about the center frequency, f_o. It is defined as $(f_{max} + f_{min} - 2 f_o)/f_o$, where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. If necessary, the detection band skew can be reduced to zero by an optional centering adjustment. (See Optional Controls).

DESCRIPTION OF CIRCUIT CONTROLS

OUTPUT FILTER — C_3 (Pin 1)

Capacitor C_3 connected from pin 1 to ground forms a simple low-pass *post detection* filter to eliminate spurious outputs due to out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3 C_3$, where R_3 (4.7 kΩ) is the internal impedance at pin 1.

The precise value of C_3 is not critical for most applications. To eliminate the possibility of false triggering by spurious signals, it is recommended that C_3 be $\geq 2 C_2$, where C_2 is the loop filter capacitance at pin 2.

If the value of C_3 becomes too large, the *turn-on* or *turn-off* time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, the delay may be desirable as a means of suppressing spurious outputs. Conversely, if the value of C_3 is too small, the beat rate at the output of the quadrature detector (see Functional Block Diagram) may cause a false logic level change at the output. (Pin 8)

The average voltage (during lock) at pin 1 is a function of the inband input amplitude in accordance with the given transfer characteristic.

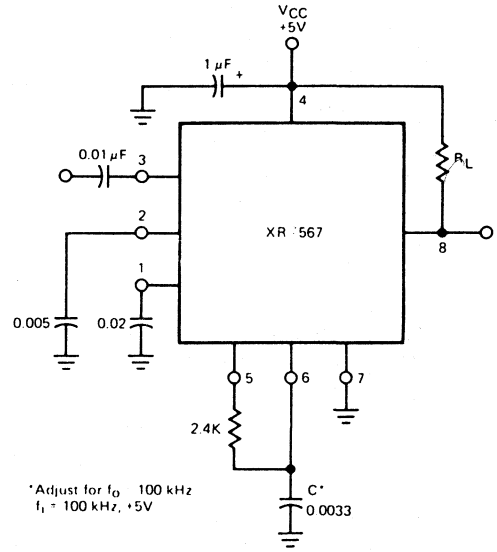


Figure 2. XR-567 Test Circuit

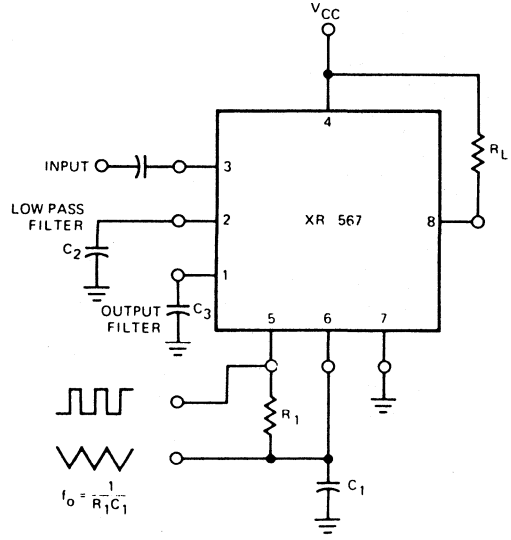


Figure 3. XR-567 Connection Diagram

TYPICAL CHARACTERISTIC CURVES

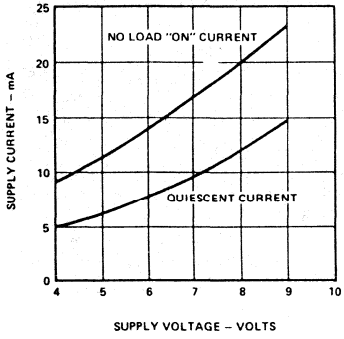


Figure 4. Supply Current Versus Supply Voltage

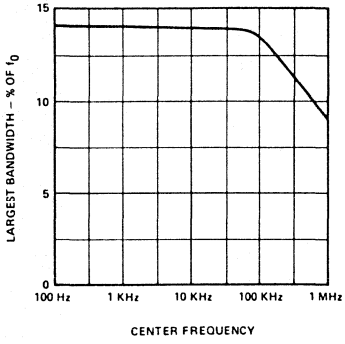


Figure 5. Largest Detection Bandwidth Versus Operating Frequency

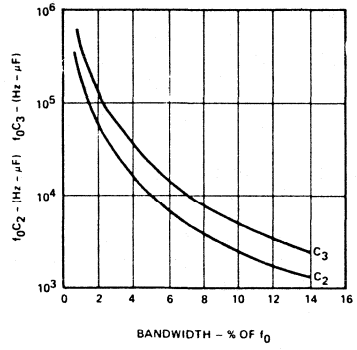


Figure 6. Detection Bandwidth as a Function of C_2 and C_3

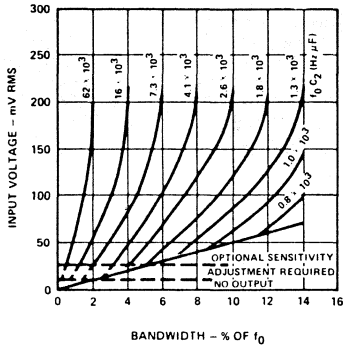


Figure 7. Bandwidth Versus Input Signal Amplitude (C_2 in μF)

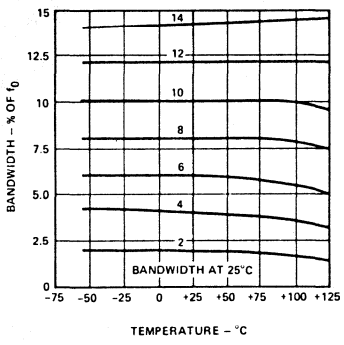


Figure 8. Bandwidth Variation with Temperature

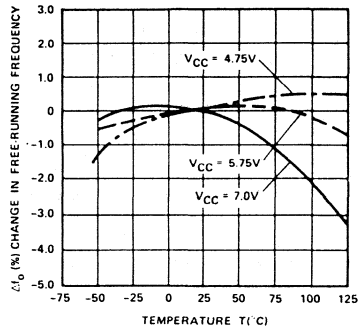


Figure 9. Frequency Drift with Temperature

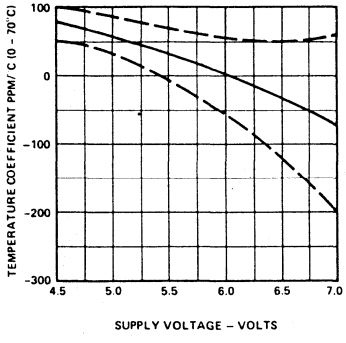


Figure 10. Temperature Coefficient of Center Frequency (Mean and S.D.)

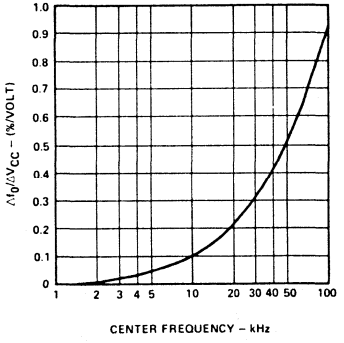


Figure 11. Power Supply Dependence of Center Frequency

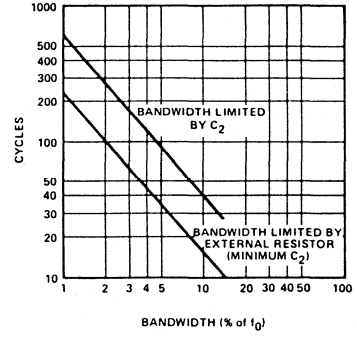


Figure 12. Greatest Number of Cycles Before Output

LOOP FILTER — C_2 (Pin 2)

Capacitor C_2 connected from pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the XR-567. The filter time constant is given by $T_2 = R_2C_2$, where R_2 (10 kΩ) is the impedance at pin 2.

The selection of C_2 is determined by the detection bandwidth requirements, as shown in Figure 6. For additional information see section on "Definition of XR-567 Parameters".

The voltage at pin 2, the phase detector output, is a linear function of frequency over the range of 0.95 to 1.05 f_o, with a slope of approximately 20 mV/% frequency deviation.

INPUT (Pin 3)

The input signal is applied to pin 3 through a coupling capacitor. This terminal is internally biased at a dc level 2 volts above ground, and has an input impedance level of approximately 20 kΩ.

TIMING RESISTOR R_1 AND CAPACITOR C_1 (Pins 5 and 6)

The center frequency of the decoder is set by resistor R_1 between pins 5 and 6, and capacitor C_1 from pin 6 to ground, as shown in Figure 3.

Pin 5 is the oscillator squarewave output which has a magnitude of approximately V_{CC} – 1.4V and an average dc level of $V_{CC}/2$. A 1 kΩ load may be driven from this point. The voltage at pin 6 is an exponential triangle waveform with a peak-to-peak amplitude of 1 volt and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to pin 6 to avoid disturbing the temperature stability or duty cycle of the oscillator.

LOGIC OUTPUT (Pin 8)

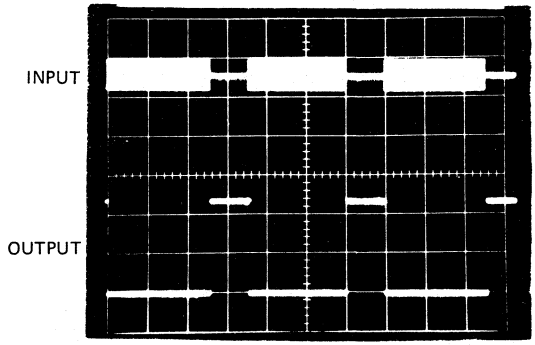
Terminal 8 provides a binary logic output when an input signal is present within the pass-band of the decoder. The logic output is an uncommitted, "base-collector" power transistor capable of switching high current loads. The current level at the output is determined by an external load resistor, R_L, connected from pin 8 to the positive supply.

When an in-band signal is present, the output transistor at pin 8 saturates with a collector voltage less than 1 volt (typically 0.6V) at full rated current of 100 mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V+, higher than the V_{CC} supply. For safe operation, V+ ≤ 20 volts.

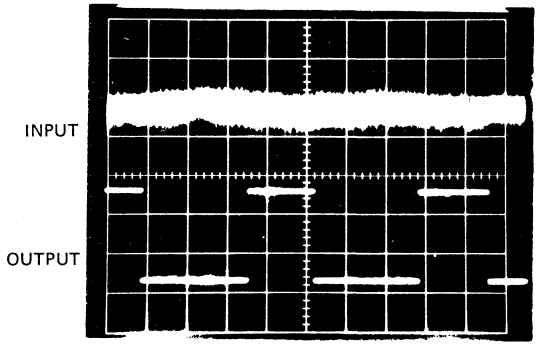
OPERATING INSTRUCTIONS

SELECTION OF EXTERNAL COMPONENTS

A typical connection diagram for the XR-567 is shown in Figure 3. For most applications, the following procedure will be sufficient for determination of the external components R_1, C_1, C_2, and C_3.



Response to 100 mV rms tone burst.
R_L = 100 ohms.



Response to same input tone burst with wideband noise.
$\frac{S}{N}$ = −6 dB R_L = 100 ohms

Noise Bandwidth = 140 Hz

Figure 13. Typical Response

1. R_1 and C_1 should be selected for the desired center frequency by the expression $f_o \approx 1/R_1C_1$. For optimum temperature stability, R_1 should be selected such that 2kΩ ≤ R_1 ≤ 20 kΩ, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.

2. Low-pass capacitor, C_2, can be determined from the Bandwidth versus Input Signal Amplitude graph of Figure 7. One approach is to select an area of operation from the graph, and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_oC_2 product can be found to give the desired bandwidth. Constant bandwidth operation requires V_i > 200 mV rms. Then, as noted on the graph, bandwidth will be controlled solely by the f_oC_2 product.

3. Capacitor C_3 sets the ·nd edge of the low-pass filter which attenuates frequencies outside of the detection band and thereby eliminates spurious outputs. If C_3 is too small, frequencies adjacent to the detection band may switch the output stage off and on at the beat frequency, or the output may pulse off and on during the turn-on transient. A typical minimum value of C_3 is 2 C_2.

Conversely, if C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage across C_3 passes the threshold value.

PRINCIPLE OF OPERATION

The XR-567 is a frequency selective tone decoder system based on the phase-locked loop (PLL) principle. The system is comprised of a phase-locked loop, a quadrature AM detector, a voltage comparator, and an output logic driver. The four sections are internally interconnected as shown in Figure 1.

When an input tone is present within the pass-band of the circuit, the PLL synchronizes or "locks" on the input signal. The quadrature detector serves as a lock indicator: when the PLL is locked on an input signal, the dc voltage at the output of the detector is shifted. This dc level shift is then converted to an output logic pulse by the amplifier and logic driver. The logic driver is a "bare collector" transistor stage capable of switching 100 mA loads.

The logic output at pin 8 is normally in a "high" state, until a tone that is within the capture range of the decoder is present at the input. When the decoder is locked on an input signal, the logic output at pin 8 goes to a "low" state.

The center frequency of the detector is set by the free-running frequency of the current-controlled oscillator in the PLL. This free-running frequency, f_o, is determined by the selection of R_1 and C_1 connected to pins 5 and 6, as shown in Figure 3. The detection bandwidth is determined by the size of the PLL filter capacitor, C_2; and the output response speed is controlled by the output filter capacitor, C_3.

OPTIONAL CONTROLS

PROGRAMMING

Varying the value of resistor R_1 and/or capacitor C_1 will change the center frequency. The value of R_1 can be changed either mechanically or by solid state switches. Additional C_1 capacitors can be added by grounding them through saturated npn transistors.

SPEED OF RESPONSE

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transient becomes greater. Thus maximum operating speed is obtained when the value of capacitor C_2 is minimum. At the instant an input signal is applied its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C_2 and C_3, in microfarads, which allow the maximum operating speeds for various center frequencies. The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o},\ C_3 = \frac{260}{f_o}\ \mu F$$

In situations where minimum turn-off time is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Figure 14 can be used to bring the quiescent C_3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

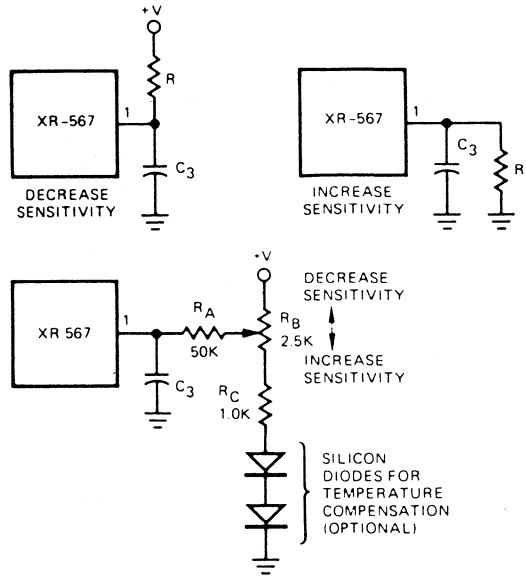


Figure 14. Optional Sensitivity Connections

CHATTER

When the value of C_3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, logic may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input (pin 1) or, by increasing the size of capacitor C_3. Generally, the feedback method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Figure 15. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

SKEW ADJUSTMENT

The circuits shown in Figure 16 can be used to change the position of the detection band (capture range) with-

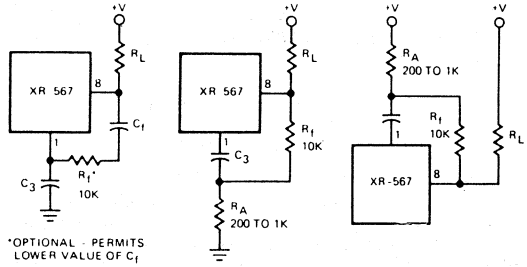


Figure 15. Methods of Reducing Chatter

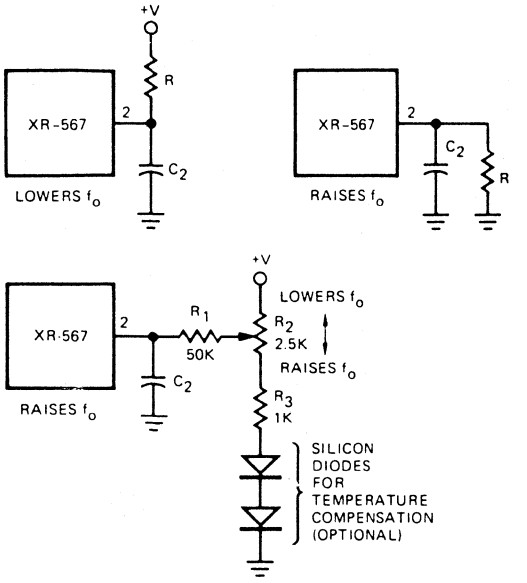


Figure 16. Connections to Reposition Detection Band

in the largest detection band (or lock range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only. Since R_3 also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

OUTPUT LATCHING

In order to latch the output of the XR-567 "on" after a signal is received, it is necessary to include a feedback resistor around the output stage, between pin 8 and pin 1, as shown in Figure 17. Pin 1 is pulled up to unlatch the output stage.

BANDWIDTH REDUCTION

The bandwidth of the XR-567 can be reduced by either increasing capacitor C_2 or reducing the loop gain. Increasing C_2 may be an undesirable solution since this will also reduce the damping of the loop and thus slow the circuit response time.

Figure 18 shows the proper method of reducing the loop gain for reduced bandwidth. This technique will improve damping and permit faster performance under narrow band operation. The reduced impedance level at pin 2 will require a larger value of C_2 for a given cut-off frequency.

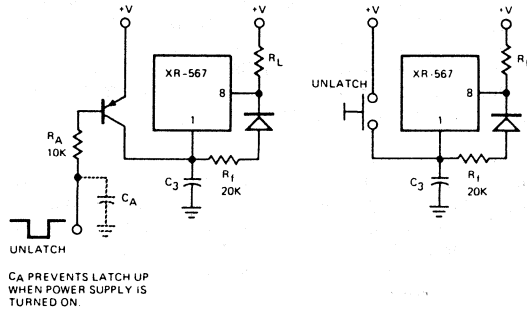


Figure 17. Output Latching

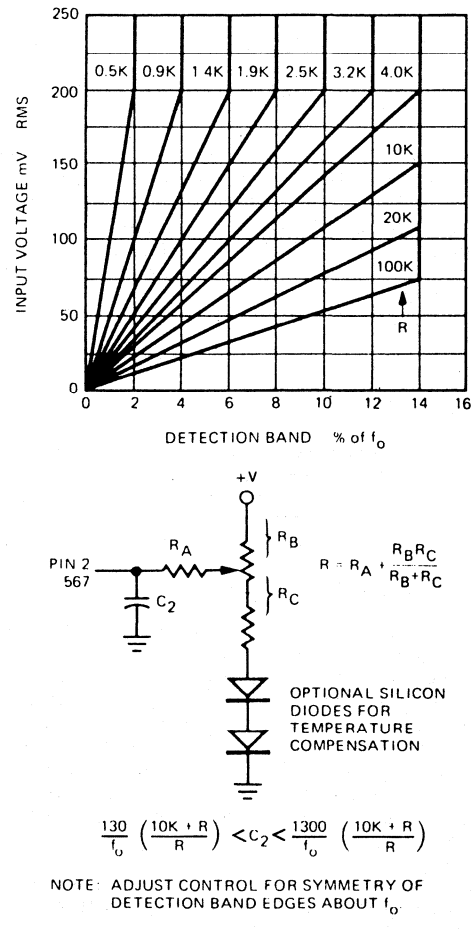


Figure 18. Bandwidth Reduction

PRECAUTIONS

1. The XR-567 will lock on signals near $(2n + 1)\ f_o$ and produce an output for signals near $(4n + 1)\ f_o$, for n = 0,1,2 - etc. Signals at 5 f_o and 9 f_o can cause an unwanted output and should, therefore, be attenuated before reaching the input of the circuit.

2. Operating the XR-567 in a reduced bandwidth mode of operation at input levels less than 200 mV rms results in maximum immunity to noise and out-band signals. Decreased loop damping, however, causes the worst-case lock-up time to increase, as shown by the graph of Figure 12.

3. Bandwidth variations due to changes in the in-band signal amplitude can be eliminated by operating the XR-567 in the high input level mode, above 200 mV. The input stage is then limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. In addition, the limited input stage will create in-band components from subharmonic signals so that the circuit components from subharmonic signals so that the circuit becomes sensitive to signals at $f_o/3$, $f_o/5$ etc.

4. Care should be exercised in lead routing and lead lengths should be kept as short as possible. Power supply leads should be properly bypassed close to the integrated circuit and grounding paths should be carefully determined to avoid ground loops and undesirable voltage variations. In addition, circuits requiring heavy load currents should be provided by a separate power supply, or filter capacitors increased to minimize supply voltage variations.

ADDITIONAL APPLICATIONS

DUAL TIME CONSTANT TONE DECODER

For some applications it is important to have a tone decoder with narrow bandwidth and fast response time. This can be accomplished by the dual time constant tone decoder circuit shown in Figure 19. The circuit has two low-pass loop filter capacitors, C_2 and C'_2. With no input signal present, the output at pin 8 is high, transistor Q_1 is off, and C'_2 is switched out of the circuit. Thus the loop low-pass filter is comprised of C_2, which can be kept as small as possible for minimum response time.

When an in-band signal is detected, the output at pin 8 will go low, Q_1 will turn on, and capacitor C'_2 will be switched in parallel with capacitor C_2. The low-pass filter capacitance will then be $C_2 + C'_2$. The value of C'_2 can be quite large in order to achieve narrow bandwidth. Notice that during the time that no input signal is being received, the bandwidth is determined by capacitor C_2.

NARROW BAND FM DEMODULATOR WITH CARRIER DETECT

For FM demodulation applications where the bandwidth is less than 10% of the carrier frequency, an XR-567

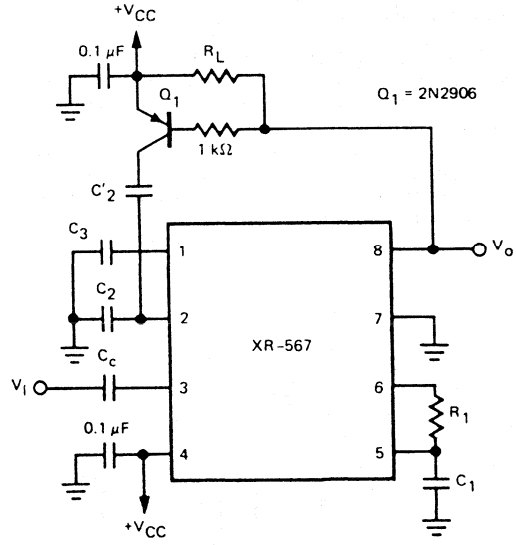


Figure 19. Dual Time Constant Tone Decoder

can be used to detect the presence of the carrier signal. The output of the XR-567 is used to turn off the FM demodulator when no carrier is present, thus acting as a squelch. In the circuit shown, an XR-215 FM demodulator is used because of its wide dynamic range, high signal/noise ratio and low distortion. The XR-567 will detect the presence of a carrier at frequencies up to 500 kHz.

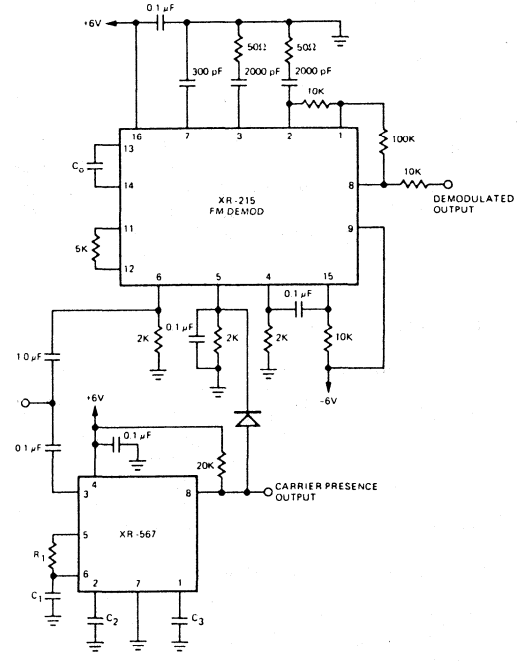


Figure 20. Narrow Band FM Demodulator with Carrier Detect

DUAL TONE DECODER

In dual tone communication systems, information is transmitted by the simultaneous presence of two separate tones at the input. In such applications two XR-567 units can be connected in parallel, as shown in Figure 21 to form a dual tone decoder. The resistor and capacitor values of each decoder are selected to provide the desired center frequencies and bandwidth requirements. **Due to capacitor and device variation, it is not possible to use a fixed R_1 value in production applications.**

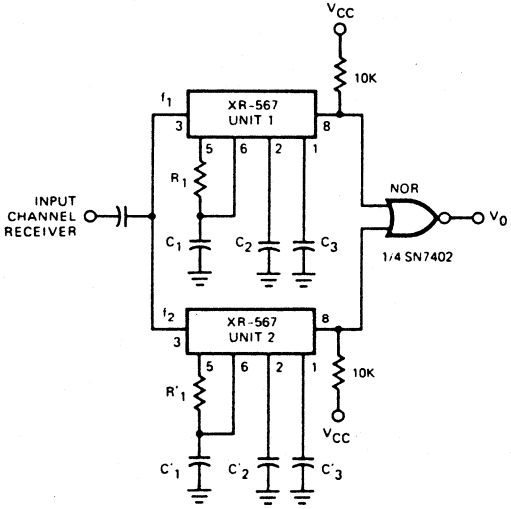


Figure 21. Dual Tone Decoder

PRECISION OSCILLATOR

The current-controlled oscillator (CCO) section of the XR-567 provides two basic output waveforms as shown in Figure 22. The squarewave is obtained from pin 5, and the exponential ramp from pin 6. The relative phase relationships of the waveforms are also provided in the figure. In addition to being used as a general purpose oscillator or clock generator, the CCO can also be used for any of the following special purpose oscillator applications:

1. **High-Current Oscillator**

   The oscillator output of the XR-567 can be amplified using the output amplifier and high-current logic output available at pin 8. In this manner, the circuit can switch 100 mA load currents without sacrificing oscillator stability. A recommended circuit connection for this application is shown in Figure 23. The oscillator frequency can be modulated over ±6% in frequency by applying a control voltage to pin 2.

2. **Oscillator with Quadrature Outputs**

   Using the circuit connection of Figure 24 the XR-567 can function as a precision oscillator with two separate squarewave outputs (at pins 5 and 8, respectively) that are at nearly quadrature phase with each other. Due to the internal biasing arrangement the actual phase shift between the two outputs is typically 80°

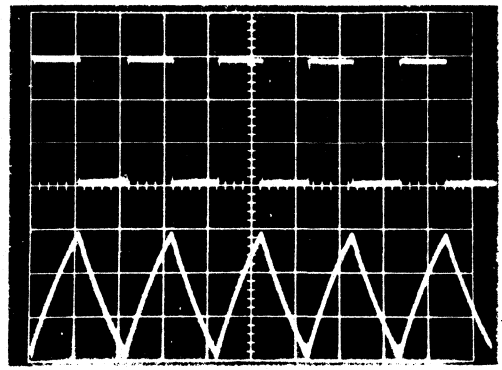


Figure 22. Oscillator Output Waveform Available From CCO Section.
Top: Square Wave Output at Pin 5:
Amplitude = (V+ −1.4V), pp.,
Avg. Value = V+/2
Bottom: Exponential Triangle Wave at Pin 6:
Amplitude = 1V pp., Avg. Value = V+/2

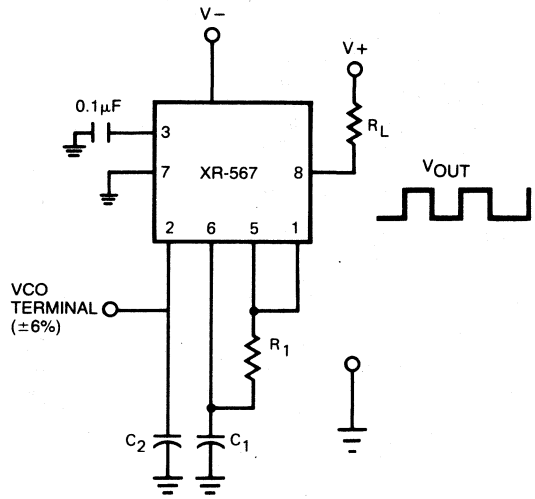


Figure 23. Precision Oscillator to Switch 100 mA Loads

3. **Oscillator with Frequency Doubled Output**

   The CCO frequency can be doubled by applying a portion of the squarewave output at pin 5 back to the input at pin 3, as shown in Figure 25. In this manner, the quadrature detector functions as a frequency doubler and produces an output of 2 f_o at pin 8.

FSK DECODING

XR-567 can be used as a low speed FSK demodulator. In this application the center frequency is set to one of

the input frequencies, and the bandwidth is adjusted to leave the second frequency outside the detection band. When the input signal is frequency keyed between the *in-band* signal and the *out-band* signal, the logic state of the output at pin 8 is reversed. Figure 26 shows the FSK input ($f_2 = 3\ f_1$) and the demodulated output signals, with $f_o = f_2 = 1$ kHz. The circuit can handle data rates up to $f_o/10$ baud.

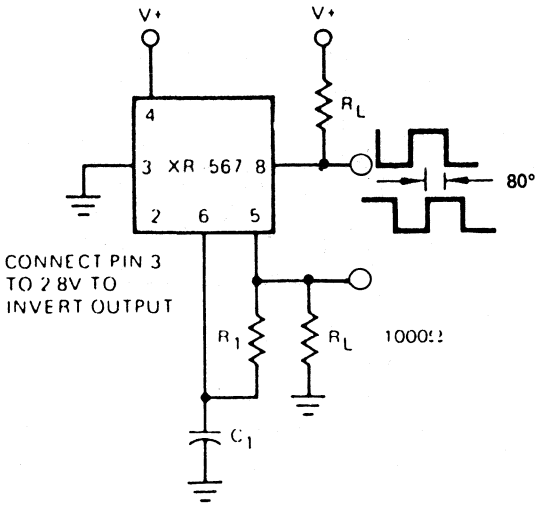


Figure 24. Oscillator with Quadrature Output

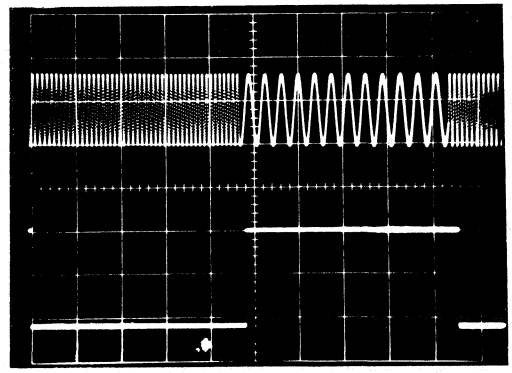
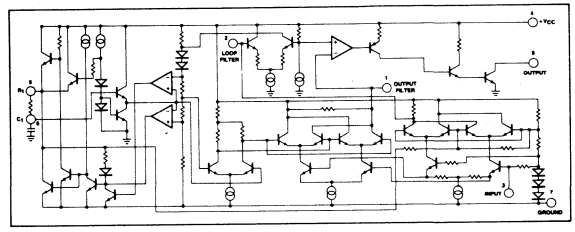


Figure 26. Input and Output Waveforms for FSK Decoding
Top: Input FSK Signal ($f_2 = 3f_1$)
Bottom: Demodulated Output



EQUIVALENT SCHEMATIC DIAGRAM

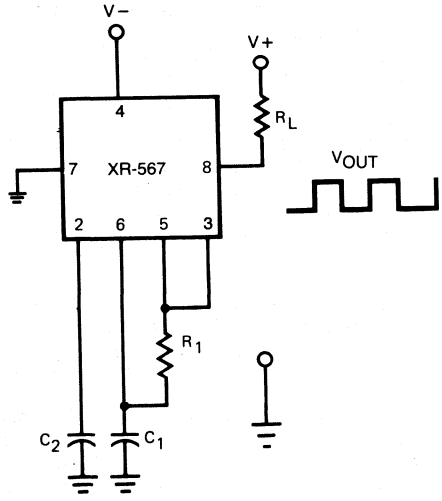


Figure 25. Oscillator with Double Frequency Output

Precision Tone Decoder

GENERAL DESCRIPTION

The XR-567A provides all the necessary circuitry for constructing a variety of tone detectors and frequency decoders. Phase-locked loop circuit techniques are used to provide operation from 0.01 Hz tp 500 kHz. The circuit also features an input preamp, a high-current logic output, and programmable output delay.

The XR-567A, available in an 8-Pin DIL package, is designed to offer improved frequency accuracy and drift characteristics over the standard industry 567. These changes offer improved overall circuit performance, while reducing initial circuit adjustments.

FEATURES

Programmable Detection Bandwidth	0% to 14%
Logic Output	100 mA
Wide Center Frequency Range	0.01 Hz to 500 kHz
High Rejection of Out-of-Band Signals and Noise	
Pin for Pin Replacement for Standard 567	
Inherent immunity to out-of-band signals & noise	

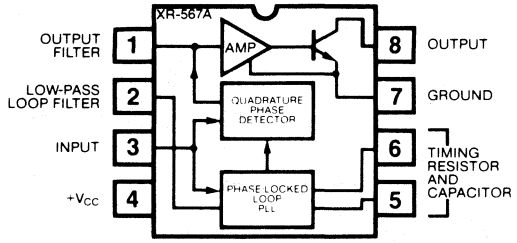
APPLICATIONS

Tone Detection
Touch-Tone® Decoding
Communications Paging
Ultrasonic Remote Control
Precision Oscillator
Wireless Intercom
Carrier-Tone Transceiver
FSK Demodulation
Dual Time Constant Tone Detector

ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate above 25°C	2.5 mW/°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-567AM	Ceramic	−55°C to +125°C
XR-567ACN	Ceramic	0°C to +70°C
XR-567ACP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-567A is an improved version of the popular 567 tone decoder. Center frequency accuracy is guaranteed by design modifications and testing to 5%, and is typically better than 2%. Temperature drift of the center frequency is also improved. Thus, in most applications, no trimming is required.

The XR-567A monolithic tone decoder consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. The device has a normally high open collector output capable of sinking 100 mA.

The input signal is applied to Pin 3 (20 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6 and can typically reach 500 kHz. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; bandwidth and skew are also dependant upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 4 is $+V_{CC}$ (4.75 to 9V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is open collector output, pulling low when an in band signal triggers the device.

XR-567A

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V. T_A = 25° C, unless otherwise specified.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
GENERAL					
Supply Voltage Range	4.75		9.0	Vdc	
Supply Current					
Quiescent XR-567AM		6	8	mA	R_L = 20 kΩ
Quiescent XR-567AC		7	10	mA	R_L = 20 kΩ
Activated XR-567AM		11	13	mA	R_L = 20 kΩ
Activated XR-567AC		12	15	mA	R_L = 20 kΩ
Output Voltage			15	V	
Negative Voltage at Input			−10	V	
Positive Voltage at Input			V_{CC} +0.5	V	
CENTER FREQUENCY					
Highest Center Frequency	100	500		kHz	
Center Frequency Stability					
Temperature T_A = 25°C		35		ppm/°C	
0 < T_T < 70°C		±60		ppm/°C	not tested in production
−55 < T_T < +125°C		±120		ppm/°C	
Supply Voltage					
XR-567AM		0.5	1.0	%/V	f_o = 100 kHz
XR-567AC		0.7	2.0	%/V	f_o = 100 kHz
Initial Accuracy		±2.0	±5.0	%	f_o = 80 kHz
Center Frequency		1.06			nominal multiple of f_0 from $f = \frac{1}{RC}$ is recommended
DETECTION BANDWIDTH					
Largest Detection Bandwidth					
XR-567AM	12	14	16	% of f_o	f_o = 100 kHz V_{IN} = 300 μVrms
XR-567AC	10	14	18	% of f_o	f_o = 100 kHz V_{IN} = 300 μVrms
Largest Detection Bandwidth Skew					
XR-567AM		1	2	% of f_o	
XR-567AC		2	3	% of f_o	
Largest Detection Bandwidth Variation					
Temperature		±0.1		%/°C	V_{in} = 300 mV rms
Supply Voltage		±1	±2	%/V	V_{in} = 300 mV rms
INPUT					
Input Resistance		20		kΩ	
Smallest Detectable Input Voltage		20	25	mV rms	I_L = 100 mA, $f_i = f_o$
Largest No-Output Input Voltage	10	15		mV rms	I_L = 100 mA, $f_i = f_o$
Greatest Simultaneous Outband Signal to Inband Signal Ratio		+6		dB	
Minimum Input Signal to Wideband Noise Ratio		−6		dB	B_n = 140 kHz
OUTPUT					
Output Saturation Voltage		0.2	0.4	V	I_L = 30 mA, V_{in} = 25 mV rms
		0.6	1.0	V	I_L = 100 mA, V_{in} = 25 mV rms
Output Leakage Current		0.01	25	μA	
Fastest ON/OFF Cycling Rate		$f_o/20$			
Output Rise Time		150		ns	R_L = 50Ω
Output Fall Time		30		ns	R_L = 50Ω

Note: Center Frequency Calculation differs from standard XR-567 devices as indicated.

5

Micropower Tone Decoder

GENERAL DESCRIPTION

The XR-L567 is a micropower phase-locked loop (PLL) circuit designed for general purpose tone and frequency decoding. In applications requiring very low power dissipation, the XR-L567 can replace the popular 567-type decoder with only minor component value changes. The XR-L567 offers approximately 1/10th the power dissipation of the conventional 567-type tone decoder, without sacrificing its key features such as the oscillator stability, frequency selectivity, and detection threshold. Typical quiescent power dissipation is less than 4 mW at 5 volts. It operates over a wide frequency band of 0.01 Hz to 60 kHz and contains a logic compatible output which can sink up to 10 milliamps of load current. The bandwidth, center frequency, and output delay are independently determined by the selection of four external components.

FEATURES

Very Low Power Dissipation (≈4 mW at 5V).
Bandwidth Adjustable from 0 to 14%.
Logic Compatible Output with 10 mA Current Sinking Capability.
Highly Stable Center Frequency.
Center Frequency Adjustable from 0.01 Hz to 60 kHz.
Inherent Immunity to False Signals.
High Rejection of Out-of-Band Signals and Noise.
Frequency Range Adjustable Over 20:1 Range by External Resistor.

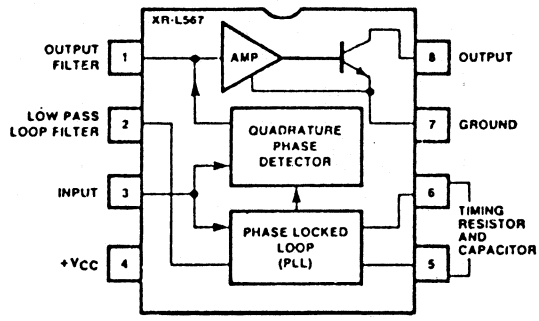
APPLICATIONS

Battery-Operated Tone Detection
Touch-Tone® Decoding
Sequential Tone Decoding
Communications Paging
Ultrasonic Remote-Control
Telemetry Decoding

ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate Above +25°C	2.5 mW/°C
SO-8	220mW
Storage Temperature	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-L567M	Ceramic	-55°C to + 125°C
XR-L567CN	Ceramic	0°C to + 70°C
XR-L567CP	Plastic	0°C to + 70°C
XR-L567MD	Japanese SOIC	0°C to + 70°C

SYSTEM DESCRIPTION

The XR-L567 monolithic circuit consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. The device has a normally high open collector output.

The input signal is applied to Pin 3 (100 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; band-width and skew are also dependant upon the circuitry here. Pin 4 is $+V_{CC}$ (4.75 to 8V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is the open collector output, pulling low when an in-band signal triggers the device.

The XR-L567 is pin-for-pin compatible with the standard XR-567-type decoder. Internal resistors have been scaled up by a factor of ten, thereby reducing power dissipation and allowing use of smaller capacitors for the same applications compared to the standard part. This scaling also lowers maximum device center frequency and load current sinking capabilities.

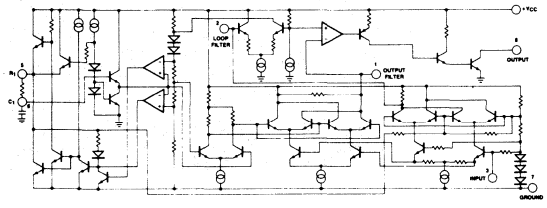
XR-L567

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V. T_A = 25°C, unless otherwise specified. Test Circuit of Figure 1.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
General					
Supply Voltage Range	4.75		8.0	V	
Supply Current					
Quiescent		0.6	1.0	mA	R_L = 20 kΩ
Activated		0.8	1.4	mA	R_L = 20 kΩ
Center Frequency					
Highest Center Frequency	10	60		kHz	
Center Frequency Drift					
Temperature T_A = 25°C		−35		ppm/°C	See Figures 10 and 11
0 < T_A < 70°C		−150		ppm/°C	See Figures 10 and 11
Supply Voltage		0.5	3.0	%/V	f_o = 10 kHz, V_{CC} = 5.25 ± 0.5V
Detection Bandwidth					
Largest Detection Bandwidth	10	14	18	% of f_o	f_o = 10 kHz
Largest Detection Bandwidth Skew		2	3	% of f_o	See Figure 13 for Definition
Largest Detection Bandwidth Variation					
Temperature		±0.1		%/°C	V_{in} = 300 mV rms
Supply Voltage		±2		%/V	V_{in} = 300 mV rms
Inputs					
Input Resistance		100		kΩ	
Smallest Detectable Input Voltage		20	25	mV rms	I_L = 10 mA, f_i = f_o
Largest No-Output Input Voltage	10	15		mV rms	I_L = 10 mA, f_i = f_o
Greatest Simultaneous Outband Signal to Inband Signal Ratio		+6		dB	
Minimum Input Signal to Wideband Noise Ratio		−6		dB	B_n = 140 kHz
Outputs					
Output Saturation Voltage		0.2	0.4	V	I_L = 2 mA, V_{in} = 25 mV rms
		0.3	0.6	V	I_L = 10 mA, V_{in} = 25 mV rms
Output Leakage Current		0.01	25	μA	
Fastest On/Off Cycling Rate		f_o/20			
Output Rise Time		150		ns	R_L = 1 kΩ
Output Fall Time		30		ns	R_L = 1 kΩ

EQUIVALENT SCHEMATIC DIAGRAM



PRINCIPLES OF OPERATION

The XR-L567 is a frequency selective tone decoder system based on the phase-locked loop (PLL) principle. The system is comprised of a phase-locked loop, a quadrature am detector, a voltage comparator, and an output logic driver.

When an input tone is present within the pass-band of the circuit, the PLL synchronizes or "locks" on the input signal. The quadrature detector serves as a lock indicator: when the PLL is locked on an input signal, the dc voltage at the output of the detector is shifted. This dc level shift is then converted to an output logic pulse by the amplifier and logic driver. The logic output at Pin 8 is an "open-collector" NPN transistor stage capable of switching 10 mA current loads.

The logic output at Pin 8 is normally in a "high" state, until a tone that is within the capture range of the decoder is present at the input. When the decoder is locked on an input signal, the logic output at Pin 8 goes to a "low" state.

Figure 3 shows the typical output response of the circuit for a tone-burst applied to the input, within the detection band.

The center frequency of the detector is set by the free-running frequency of the current-controlled oscillator in the PLL. This free-running frequency, f_o, is determined by the selection of R_1 and C_1 connected to Pins 5 and 6, as shown in Figure 2. The detection bandwidth is determined by the size of the PLL filter capacitor, C_2 (see Figure 10); and the output response speed is controlled by the output filter capacitor, C_3.

DEFINITION OF DEVICE PARAMETERS

Center Frequency f_o

f_o is the free-running frequency of the current-controlled oscillator with no input signal. It is determined by resistor R_1 between Pins 5 and 6, and capacitor C_1 from Pin 6 to ground. f_o can be approximated by

$$f_o \approx \frac{1}{R_1 C_1} \text{ Hz}$$

where R_1 is in ohms and C_1 is in farads.

Detection Bandwidth (BW)

The largest *detection bandwidth* is the frequency range centered about f_o, within which an input signal larger than the threshold voltage (typically 20 mV rms) will cause a logic zero state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass loop filter at Pin 2. Typical dependence of detection bandwidth on the filter capacitance and the input signal amplitude is shown in Figures 10 and 11, or may be calculated by the approximation

$$BW\ (\%) \approx 338 \sqrt{\frac{V_i\ (RMS)}{f_o(Hz) \cdot C_2\ (\mu F)}}$$

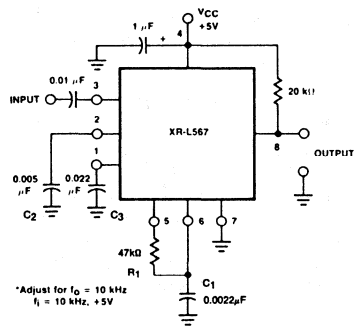


Figure 1. XR-L567 Test Circuit

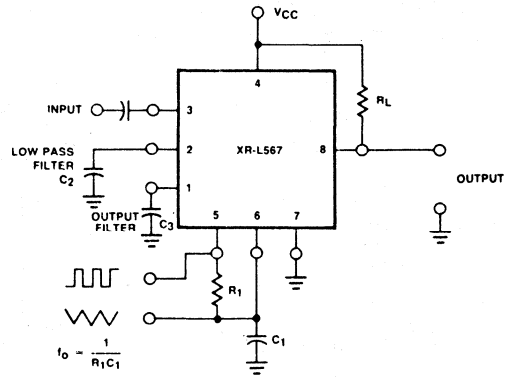


Figure 2. XR-L567 Generalized Connection Diagram

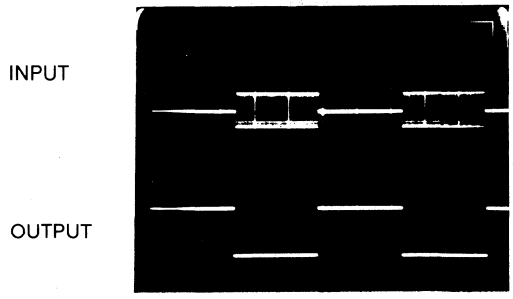
Largest Detection Bandwidth

The largest detection bandwidth is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero stage at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

Detection Band Skew

The *detection band skew* is a measure of how accurately the largest detection band is centered about the center frequency, f_o. This parameter is graphically illustrated in Figure 4. In the figure, f_{min} and f_{max} correspond to the lower and the upper ends of the largest detection band, and f_1 corresponds to the apparent center of the detection band, and is defined as the arithmetic average of f_{min} and f_{max} and f_o is the free-running frequency of the XR-L567 oscillator section. The bandwidth skew, Δf_x, is the difference between these frequencies. Normalized to f_o, this bandwidth skew can be expressed as:

$$\text{Bandwidth Skew} = \frac{\Delta f_x}{f_o} = \frac{(f_{max} + f_{min} - 2f_o)}{2f_o}$$



Response to 100 mV rms tone burst.
R_L = 1K ohms

Figure 3. Typical Output Response to 100 mV Input Tone-Burst

If necessary, the detection band skew can be reduced to zero by an optional centering adjustment. (See Optional Controls.)

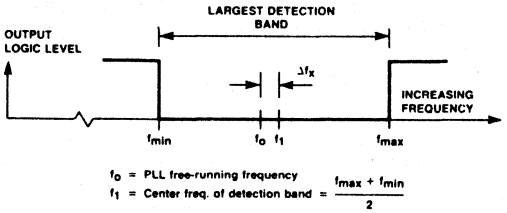


Figure 4. Definition of Bandwidth Skew

DESCRIPTION OF CIRCUIT CONTROLS

Input (Pin 3)

The input signal is applied to Pin 3 through a coupling capacitor. This terminal is internally biased at a dc level 2 volts above ground, and has an input impedance level of approximately 100 kΩ.

Timing Resistor R_1 and Capacitor C_1 (Pins 5 and 6)

The center frequency of the decoder is set by resistor R_1 between Pins 5 and 6, and capacitor C_1 from Pin 6 to ground, as shown in Figure 2.

Pin 5 is the oscillator squarewave output which has a magnitude of approximately V_{CC} – 1.4V and an average dc level of $V_{CC}/2$. A 5 kΩ load may be driven from this point. The voltage at Pin 6 is an exponential triangle waveform with a peak-to-peak amplitude of ≈ (V_{CC} – 1.3)/3.5 volts and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to Pin 6 to avoid disturbing the temperature stability or duty cycle of the oscillator.

Loop Filter—C_2 (Pin 2)

Capacitor C_2 connected from Pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the XR-L567. The filter time constant is given by $T_2 = R_2C_2$, where R_2 (100 kΩ) is the impedance at Pin 2.

The selection of C_2 is determined by the detection bandwidth requirements, as shown in Figure 10. For additional information see section on "Definition of Device Parameters."

The voltage at Pin 2, the phase detector output, is a linear function of frequency over the range of 0.95 f_o to 1.05 f_o, with a slope of approximately 20 mV/% frequency deviation.

Output Filter—C_3 (Pin 1)

Capacitor C_3 connected from Pin 1 to ground forms a simple low-pass post *detection* filter to eliminate spurious outputs due to out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3C_3$, where R_3 (47 kΩ) is the internal impedance at Pin 1.

If the value of C_3 becomes too large, the *turn-on* or *turn-off* time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, the delay may be desirable as a means of suppressing spurious outputs. Conversely, if the value of C_3 is too small, the beat rate at the output of the quadrature detector may cause a false logic level change at the output (Pin 8).

The average voltage (during lock) at Pin 1 is a function of the in-band input amplitude in accordance with the given transfer characteristic.

Logic Output (Pin 8)

Terminal 8 provides a binary logic output when an input signal is present within the pass-band of the decoder. The logic output is an uncommitted, open-collector power transistor capable of switching high current loads. The current level at the output is determined by an external load resistor, R_L, connected from Pin 8 to the positive supply.

When an in-band signal is present the output transistor at Pin 8 saturates with a collector voltage of less than 0.6V at full rated output current of 10 mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V+, higher than the V_{CC} supply. For safe operation, V+ ≤15 volts.

OPERATING INSTRUCTIONS

Selection of External Components

A typical connection diagram for the XR-L567 is shown in Figure 2. For most applications, the following procedure will be sufficient for determination of the external components R_1, C_1, C_2, and C_3.

1. R_1 and C_1 should be selected for the desired center frequency by the expression $f_o \approx 1/R_1C1$. For optimum temperature stability, R_1 should be selected such that 20 kΩ ≤ R_1 ≤ 200 kΩ, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.

2. Low-pass capacitor, C_2, can be determined from the Bandwidth versus Input Signal Amplitude graph of Figure 10. One approach is to select an area of operation from the graph, and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_oC_2 product can be found to give the desired bandwidth. Constant bandwidth operation requires V_i > 200 mV rms. Then, as noted on the graph, bandwidth will be controlled solely by the f_oC_2 product.

3. Capacitor C_3 sets the band edge of the low-pass filter which attenuates frequencies outside of the detection band and thereby eliminates spurious outputs. If C_3 is too small, frequencies adjacent to the

detection band may switch the output stage off and on at the beat frequency, or the output may pulse off and on during the turn-on transient. A typical minimum value for C_3 is 2 C_2.

Conversely, if C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage across C_3 passes the threshold value.

Precautions

1. The XR-L567 will lock on signals near (2n + 1) f_o and produce an output for signals near (4n + 1) f_o, for n = 0,1,2—etc. Signals at 5 f_o and 9 f_o can cause an unwanted output and should, therefore, be attenuated before reaching the input of the circuit.

2. Operating the XR-L567 in a reduced bandwidth mode of operation at input levels less than 200 mV rms results in maximum immunity to noise and outband signals. Decreased loop damping, however, causes the worst-case lock-up time to increase, as shown by the graph of Figure 13.

3. Bandwidth variations due to changes in the in-band signal amplitude can be eliminated by operating the XR-L567 in the high input level mode, above 200 mV. The input stage is then limiting, however, so that outband signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. In addition, the limited input stage will create in-band components from subharmonic signals so that the circuit becomes sensitive to signals at $f_o/3$, $f_o/5$ etc.

4. Care should be exercised in lead routing and lead lengths should be kept as short as possible. Power supply leads should be properly bypassed close to the integrated circuit and grounding paths should be carefully determined to avoid ground loops and undesirable voltage variations. In addition, circuits requiring heavy load currents should be provided by a separate power supply, or filter capacitors increased to minimize supply voltage variations.

OPTIONAL CONTROLS

Programming

Varying the value of resistor R_1 and/or capacitor C_1 will change the center frequency. The value of R_1 can be changed either mechanically or by solid state switches. Additional C_1 capacitors can be added by grounding them through saturated npn transistors.

Speed of Response

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transients becomes greater. Thus maximum operating speed is obtained when the value of capacitor C_2 is minimum. At the instant an input signal is applied, its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C_2 and C_3, in microfarads, which allow the maximum operating speeds for various center frequencies where f_o is Hz.

$$C_2 = \frac{13}{f_o}, C_3 = \frac{26}{f_o} \mu F$$

The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_o/10$ baud. In situations where minimum turn-off is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Figure 5 can be used to bring the quiescent C_3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

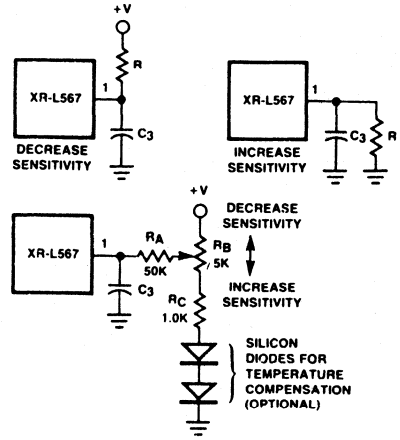


Figure 5. Adjustable Sensitivity Connections

Chatter

When the value of C_3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, logic may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input (Pin 1) or, by increasing the size of capacitor C_3. Generally, the feedback method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Figure 6. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

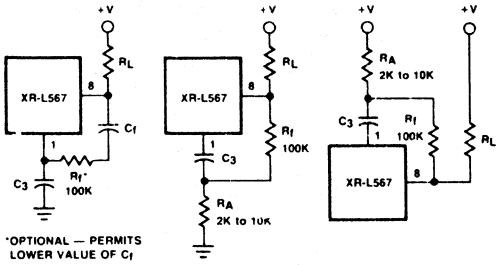


Figure 6. Methods of Reducing Chatter

Skew Adjustment

The circuits shown in Figure 7 can be used to change the position of the detection band (capture range) within the largest detection band (lock range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only. Since R_3 also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

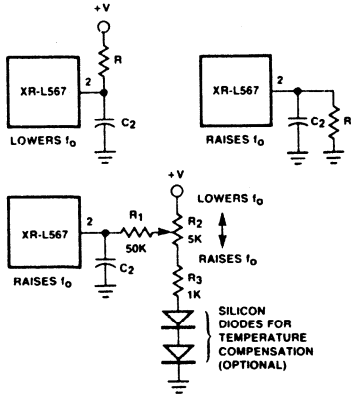


Figure 7. Detection Band Skew Adjustment

CHARACTERISTIC CURVES

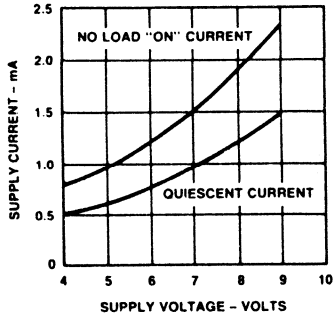


Figure 8. Supply Current Versus Supply Voltage

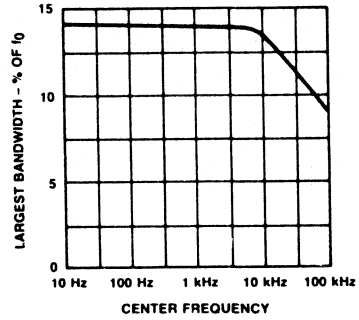


Figure 9. Largest Detection Bandwidth Versus Operating Frequency

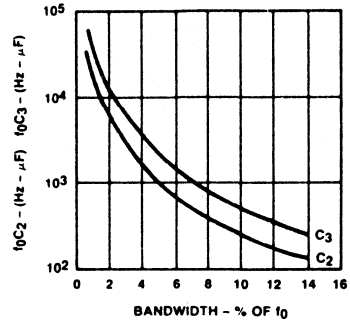


Figure 10. Detection Bandwidth as a Function of C_2 and C_3

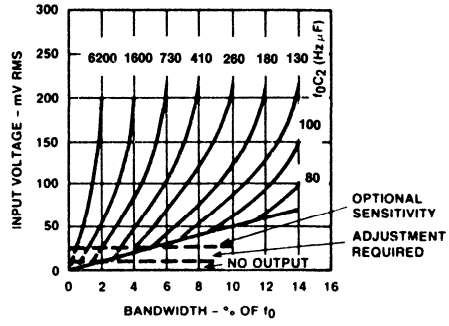


Figure 11. Bandwidth Versus Input Signal Amplitude (C_2 in μF)

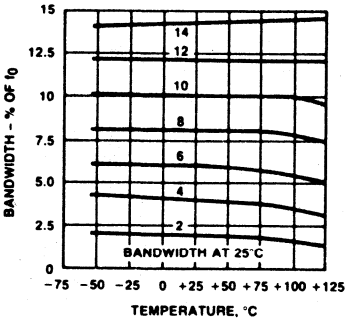


Figure 12. Bandwidth Variation With Temperature

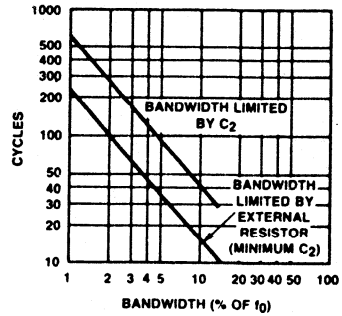


Figure 13. Greatest Number of Cycles Before Output

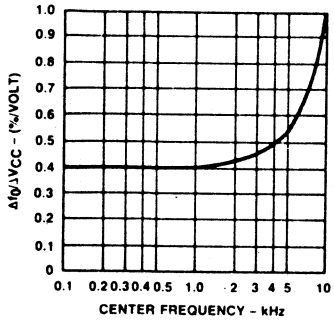


Figure 14. Power Supply Dependence of Center Frequency

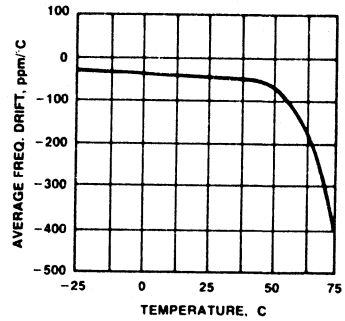


Figure 15. Typical Center Frequency Drift With Temperature (V^+ = 5V, R_1 = 80 kΩ, f_0 = 1 kHz)

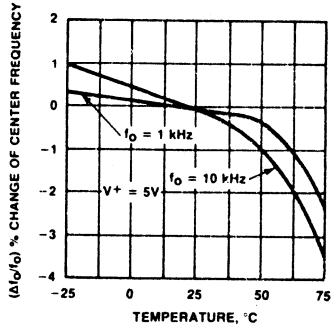


Figure 16. Typical Frequency Drift as a Function of Temperature

Dual Monolithic Tone Decoder

GENERAL DESCRIPTION

The XR-2567 is a dual monolithic tone decoder of the 567-type that is ideally suited for tone or frequency decoding in multiple-tone communication systems. Each decoder of the XR-2567 can be used independently or both sections can be interconnected for dual operation. The matching and temperature tracking characteristics between decoders on this monolithic chip are superior to those available from two separate tone decoder packages.

The XR-2567 operates over a frequency range of 0.01 Hz to 500 kHz. Supply voltages can vary from 4.5V to 12V, with internal voltage regulation provided for supplies between 7V and 12V. Each decoder consists of a phase-locked loop (PLL), a quadrature AM detector, a voltage comparator, and a logic compatible output that can sink more than 100 mA of load current.

The center frequency of each decoder is set by an external resistor and capacitor which determine the free-running frequency of each PLL. When an input tone is present within the passband of the circuit, the PLL "locks" on the input signal. The logic output, which is normally "high", then switches to a "low" state during this "lock" condition.

FEATURES

Replaces two 567-type decoders
Excellent temperature tracking between decoders
Bandwidth adjustable from 0 to 14%
Logic compatible outputs with 100 mA sink capability
Center frequency matching (1% typ.)
Center frequency adjustable from 0.01 Hz to 500 kHz
Inherent immunity to false triggering
Frequency range adjustable over 20:1 range by external resistor.

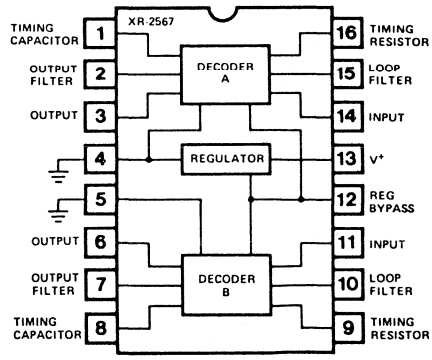
APPLICATIONS

Touch-Tone® Decoding
Sequential Tone Decoding
Dual-Tone Decoding/ Encoding
Communications Paging
Ultrasonic Remote-Control and Monitoring
Full-Duplex Carrier-Tone Transceiver
Wireless Intercom
Dual Precision Oscillator
FSK Generation and Detection

ABSOLUTE MAXIMUM RATINGS

Power Supply	
With Internal Regulator	14V
Without Regulator (Pins 12 and 13 shorted)	10V
Power Dissipation	
Ceramic Package	750 mW
Derate Above +25°C	6 mW/°C
Plastic Package	625 mW/°C
Derate Above +25°C	5.5 mW/°C
Storage Temperature	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



5

ORDERING INFORMATION

Part Number	Package	Temperature Range
XR-2567M	Ceramic	-55°C to 125°C
XR-2567CN	Ceramic	0°C to +70°C
XR-2567CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2567 dual monolithic tone decoder consists of two independant 567-type circuits and an on board voltage regulator. Each decoder has a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. Both devices have normally high open collector outputs capable of sinking 100 mA.

The input signal is applied to Pin 14 (device A) or Pin 11 (device B), both with 20 kΩ nominal input resistance. Free running frequency is controlled by an RC network at Pins 1 and 16 (device A) or Pins 8 and 9 (device B). A capacitor on Pin 2 (A), or Pin 7 (B) serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 15 (A), or Pin 10 (B); bandwidth and skew are also dependant upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 13 is $+V_{CC}$ (4.75 to 12V nominal, 14V maximum); Pin 7 is ground; and Pin 3 (A) or Pin 6 (B) is the open collector output, pulling low when an in-band signal triggers the device.

Voltage supplies below 7V necessitate bypassing the internal regulator. This is accomplished by shorting Pin 12 to V_{CC}; for supplies over 7V, a bypass capacitor of at least 1 μF should AC ground Pin 12.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V, T_A = 25° C, unless otherwise specified. Test circuit of Figure 2, S_1 closed unless otherwise specified.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
GENERAL					
Supply Voltage Range					
Without Regulator	4.75		7	V_{dc}	See Figure 5, S_1 closed.
With Internal Regulator	6.5		12	V_{dc}	See Figure 5, S_1 open.
Supply Current (both decoders)					See Figure 7, 8
Quiescent XR-2567M		12	16	mA	R_L = 20 kΩ
XR-2567C		14	20	mA	R_L = 20 kΩ
Activated XR-2567M		22	26	mA	R_L = 20 kΩ
XR-2567C		24	30	mA	R_L = 20 kΩ
Output Voltage			15	V	
Negative Voltage at Input			−10	V	
Positive Voltage at Input			V_{CC} + 0.5	V	
CENTER FREQUENCY (each decoder section)					
Highest Center Frequency	100	500		kHz	
Center Frequency Stability					
Temperature T_A = 25°C		35		ppm/°C	See Figure 14
0°C < T_T < 70°C *		±60		ppm/°C	See Figure 14
-55° < T_T < +125°C *		±140		ppm/°C	See Figure 14
Supply Voltage					
Without Regulator					
XR-2567M		0.5	1.0	%/V	f_o = 100 kHz
XR-2567C		0.7	2.0	%/V	f_o = 100 kHz
With Internal Regulator					
XR-2567M		0.05		%/V	f_o = 100 kHz, V_{CC} = 9V
XR-2567C		0.1		%/V	f_o = 100 kHz, V_{CC} = 9V
DETECTION BANDWIDTH (each decoder section)					
Largest Detection Bandwidth					
XR-2567M	12	14	16	% of f_o	f_o = 100 kHz
XR-2567C	10	14	18	% of f_o	f_o = 100 kHz
Largest Detection Bandwidth Skew					
XR-2567M		1	2	% of f_o	
XR-2567C		1	3	% of f_o	
Largest Detection Bandwidth Variation					
Temperature		±0.1		%/°C	V_{in} = 300 mV rms
Supply Voltage		±2		%/V	V_{in} = 300 mV rms
INPUT (each decoder section)					
Input Resistance		20		kΩ	
Smallest Detectable Input Voltage		20	25	mV rms	I_L = 100 mA, f_i = f_o
Largest No-Output Input Voltage	10	15		mV rms	I_L = 100 mA, f_i = f_o
Greatest Simultaneous Outband Signal to Inband Signal Ratio		+6		dB	
Minimum Input Signal to Wideband Noise Ratio		−6		dB	Noise BW = 140 kHz
OUTPUT (each decoder section)					
Output Saturation Voltage		0.2	0.4	V	I_L = 30 mA, V_{in} = 25 mV rms
		0.6	1.0	V	I_L = 100 mA, V_{in} = 25 mV rms
Output Leakage Current		0.01	25	μA	
Fastest ON-OFF Cycling Rate		f_o/20			
Output Rise Time		150		ns	R_L = 50Ω
Output Fall Time		30		ns	R_L = 50Ω
MATCHING CHARACTERISTICS					
Center Frequency Matching		1		%	f_o = 10 kHz
Temperature Drift Matching		±20		ppm/°C	0°C<T_A<70°C
		±50		ppm/°C	−55°C<T_A<125°C

* These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

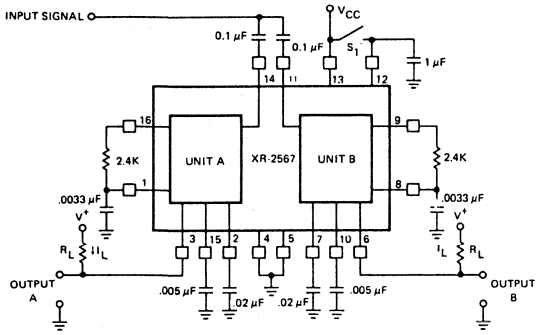
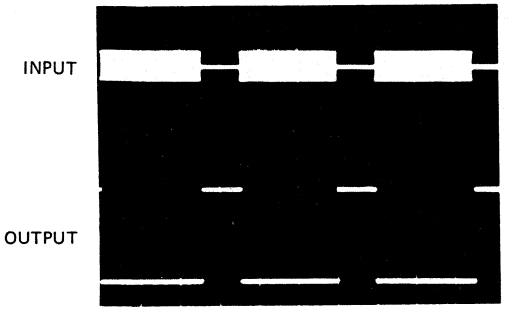


Figure 2. Test Circuit



Response to 100 mV rms tone burst.
R_L = 100 ohms.

Figure 3. XR-2567 Typical Response

DEFINITIONS OF XR-2567 PARAMETERS

f_o is the *free-running frequency* of the current-controlled oscillator of the PLL with no input signal. It is determined by resistor R_1 and capacitor C_1; f_o can be approximated by

$$f_o \approx \frac{1}{R_1 C_1} \text{ Hz}$$

where R_1 is in ohms and C_1 is in farads.

The *detection bandwidth* is the frequency range centered about f_o, within which an input signal larger than the threshold voltage (typically 20 mV rms) will cause a "logic zero" state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass bandwidth filter. The bandwidth of the filter, as a percent of f_o, can be determined by the approximation

$$BW \approx 1070 \sqrt{\frac{V_i}{f_o C_2}}$$

where V_i is the input signal in volts, rms, and C_2 is the capacitance in μF at Pins 10 or 15.

The *largest detection bandwidth* is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

The *detection band skew* is a measure of how accurately the largest detection band is centered about the center frequency, f_o. It is defined as $(f_{max} + f_{min} - 2f_o)/f_o$, where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. If necessary, the detection band skew can be reduced to zero by an optional centering adjustment. (See Optional Controls.)

DESCRIPTION OF CIRCUIT CONTROLS

INPUT (Pins 11 and 14)

The input signal is applied to Pins 14 and/or 11 through a coupling capacitor, C_C. These terminals are internally biased at a dc level 2 volts above ground and they have an input impedance level of approximately 20 kΩ.

TIMING RESISTOR R_1 AND CAPACITOR C_1 (Pins 1, 8, 9, and 16)

The center frequency, f_o, of each decoder section is set by a resistor R_1 and a capacitor C_1. R_{1A} is connected between Pins 1 and 16 in decoder section A, and R_{1B} between Pins 8 and 9 of decoder section B. C_{1A} is connected from Pin 1 to ground, and C_{1B} from Pin 8 to ground, as shown in Figure 4. R_1 and C_1 should be selected for the desired center frequency by the expression $f_o \approx 1/R_1C_1$. For optimum temperature stability, R_1 should be selected such that 2 kΩ ≤ R_1 ≤ 20 kΩ, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.

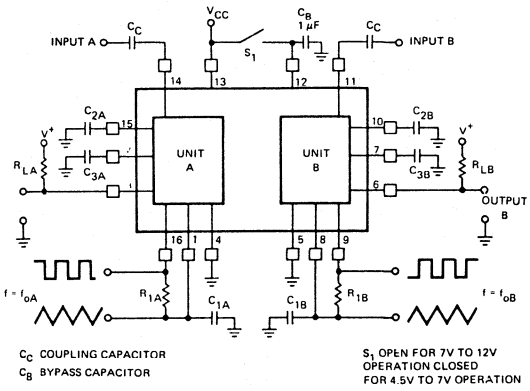


Figure 4. Circuit Connection Diagram

For decoder section A, the oscillator output can be obtained at either Pin 1 or 16. Pin 16 is the oscillator squarewave output which has a magnitude of approximately V_{CC} – 1.4V and an average dc level of $V_{CC}/2$. A 1 kΩ load may be driven from this point. The voltage at

TYPICAL CHARACTERISTICS

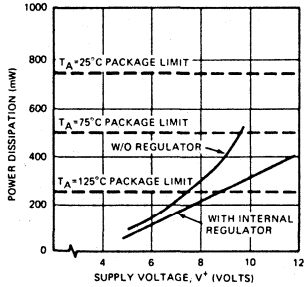


Figure 5. Internal Power Dissipation vs. Supply Voltage. Both Units Activated, R_L = 20 k

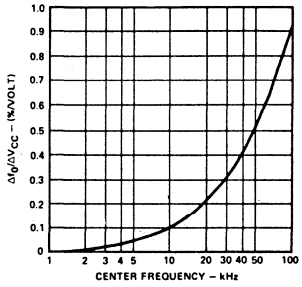


Figure 6. Power Supply Dependence of Center Frequency

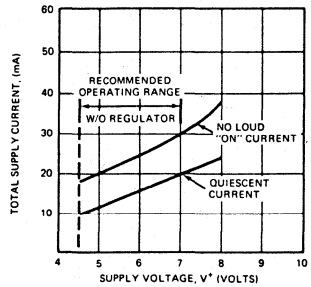


Figure 7. Total Supply Current vs. Supply Voltage for Operation Without Internal Regulator (Pins 12 and 13 Shorted)

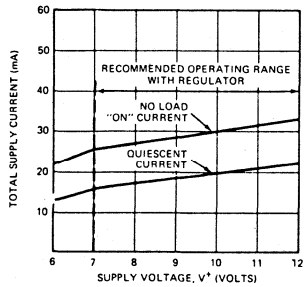


Figure 8. Total Supply Current vs. Supply Voltage for Operation with Internal Regulator (Pins 12 and 13 Not Connected)

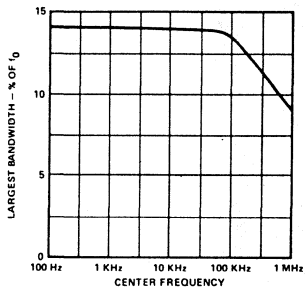


Figure 9. Largest Detection Bandwidth

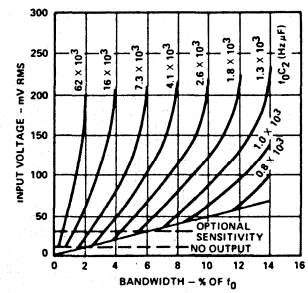


Figure 10. Bandwidth vs. Input Signal Amplitude (C_2 in μF)

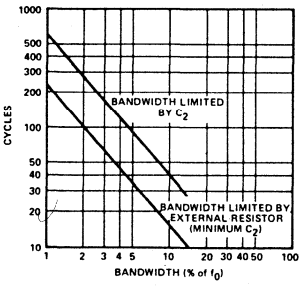


Figure 11. Greatest Number of Cycles Before Output

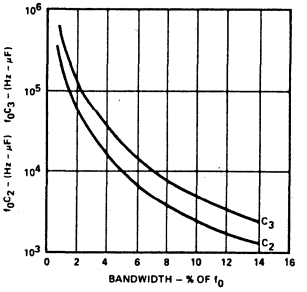


Figure 12. Detection Bandwidth as a Function of C_2 and C_3

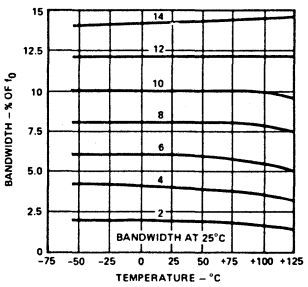


Figure 13. Bandwidth Variation With Temperature

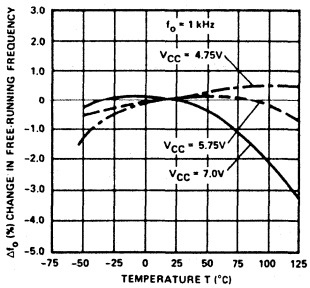


Figure 14. Frequency Drift With Temperature

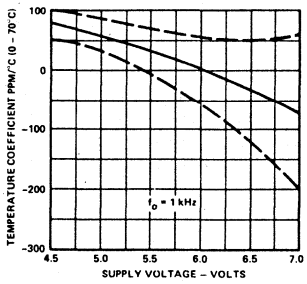


Figure 15. Temperature Coefficient of Center Frequency (Mean and S.D.)

pin 1 is an exponential triangle waveform with a peak-to-peak amplitude of 1 volt and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to Pin 1 to avoid disturbing the temperature stability or duty cycle of the oscillator. For section B, Pin 9 is the squarewave output and Pin 8 the exponential triangle waveform output.

LOOP FILTER, C_2 (Pins 10 and 15)

Capacitors C_{2A} and C_{2B} connected from Pins 15 and 10 to ground are the single-pole, low-pass filters for the PLL portion of decoder sections A and B. The filter time constant is given by $T_2 = R_2C_2$, where R_2 (10 kΩ) is the impedance at Pins 10 or 15. The selection of C_2 is determined by the detection bandwidth requirements and input signal amplitude as shown in Figures 10 and 12. One approach is to select an area of operation from the graph and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_oC_2 product can be found to give the desired bandwidth. Constant bandwidth operation requires $V_i > 200$ mV rms. Then, as noted in Figure 10, bandwidth will be controlled solely by the f_oC_2 product. (For additional information, see Optional Controls Section, "Speed of Response" and "Bandwidth Reduction".)

Pins 10 and 15 correspond to the PLL phase detector outputs of sections A and B, respectively. The voltage level at these pins is a linear function of frequency over the range of 0.95 to 1.05 f_o, with a slope of approximately 20 mV/% frequency deviation.

OUTPUT FILTER, C_3 (Pins 2 and 7)

Capacitors C_{3A} and C_{3B} connected from Pins 2 and 7 to ground form low-pass post detection filters for sections A and B respectively. The function of the post detection filter is to eliminate spurious outputs caused by out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3C_3$, where R_3 (4.7 k) is the internal impedance at Pins 2 or 7.

The precise value of C_3 is not critical for most applications. To eliminate the possibility of false triggering by spurious signals, a minimum value for C_3 is $2C_2$, where C_2 is the loop filter capacitance for the corresponding decoder section. If C_3 is smaller than $2C_2$, then frequencies adjacent to the detection band may switch the output stage "off" and "on" at the beat frequency, or the output may pulse "off" and "on" during the turn-on transient.

If the value of C_3 becomes too large, the turn-on or turn-off time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, this delay may be desirable as a means of suppressing spurious outputs. (For additional information, see Optional Controls Section, "Speed of Response" and "Chatter".)

LOGIC OUTPUT (Pins 3 and 6)

Output terminals 3 and 6 provide a binary logic output when an input signal tone is present within the detection-band of each respective decoder section. The logic outputs are uncommitted "bare-collector" power transistors capable of switching high current loads. The current level at the output is determined by an external load resistor, R_L, connected from V_{CC} to Pins 3 or 6.

When an in-band signal is present, the output transistor at Pins 3 or 6 saturates with a collector voltage less than 1 volt (typically 0.6V) at full rated current of 100 mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V+ higher than the V_{CC} supply. For safe operation, V+ ≤ 15 volts.

REGULATOR BY-PASS (Pin 12)

This pin corresponds to the output of the voltage regulator section. For circuit operation with a supply voltage greater than 7V, Pin 12 should be ac grounded with a bypass capacitor ≥ 1 μF. For circuit operation over a supply voltage range of 4.5 to 7V, the voltage regulator section is not required; Pin 12 should be shorted to V_{CC}.

GROUND TERMINALS (Pins 4 and 5)

To eliminate parasitic interaction, each decoder section has a separate ground terminal. The internal regulator shares a common ground with decoder section A (Pin 4).

Independent ground terminals also allow additional flexibility for split supply operation. Pin 4 can be used as V−, and Pin 5 as ground, as shown in Figure 16. When the circuit is operated with split supplies, the positive supply should always be >6V, and the dc potential across Pins 13 and 14 should not exceed 15 volts.

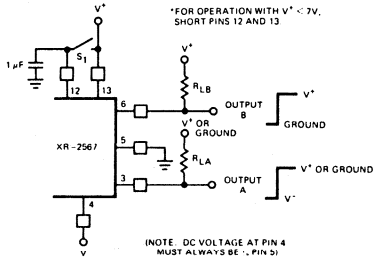


Figure 16. Split-Supply Operation Using Independent Ground Terminals of Units A and B. Unit A Operates Between V+ and V−; Unit B Operates Between V+ and Ground

OPTIONAL CONTROLS

SPEED OF RESPONSE

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transient becomes greater. Thus, maximum operating speed is obtained when the value of capacitor C_2 is minimum. At the instant an input signal is applied, its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C_2 and C_3, in microfarads, which allow the maximum operating speeds for various center frequencies. The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o}, C_3 = \frac{260}{f_o}$$

In situations where minimum turn-off time is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Figure 17 can be used to bring the quiescent C_3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

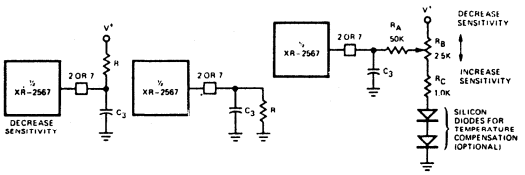


Figure 17. Optional Connections for Sensitivity Control

CHATTER

When the value of C_3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, "logic" may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input or, by increasing the size of capacitor C_3. Generally, the feedback method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Figure 18. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

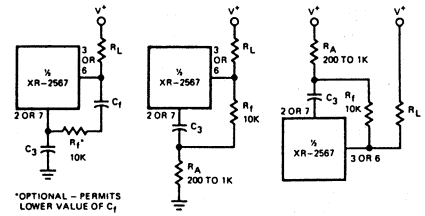


Figure 18. Methods of Reducing Chatter

SKEW ADJUSTMENT

The circuits shown in Figure 19 can be used to change the position of the detection band (capture range) within the largest detection band (or lock range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only. Since R_3 also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

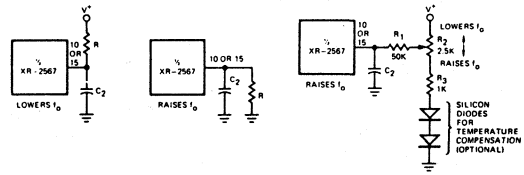


Figure 19. Connections to Reposition Detection Band

OUTPUT LATCHING

After a signal is received, the output of either decoder section can be latched "on" by connecting a 20 kΩ resistor and diode from the "output" terminal to the "output filter" terminal as shown in Figure 20. The output stage can be unlatched by raising the voltage level at the output filter terminal.

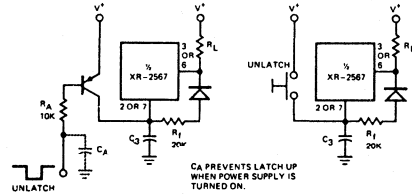
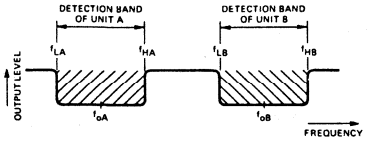


Figure 20. Output Latching

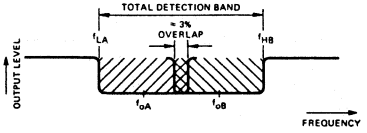
POSITIONING OF DETECTION BANDS

Figure 21 defines the respective band-edge and band-center frequencies for sections A and B of the dual tone decoder.

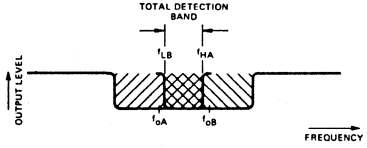
Frequencies f_L and F_H with appropriate subscripts refer to the low and the high band-edge frequencies for decoder sections A and B, and f_o is the center frequency.



(a) Independent Detection of Two Separate Tones



(b) Addition of Detection Bandwidth for Wide-Band Detection



(c) Subtraction of Bandwidths for Narrow-Band Detection

Figure 21. Positioning of Detection Bands

The two sections can be interconnected to form a single tone detector with an overall detection bandwidth equal to the sum or the difference of the detection bands for the two individual detector sections. For example, if the individual decoder sections are interconnected as shown in Figure 25, then the total detection bandwidth would be approximately equal to the sum of the respective bandwidths as shown in Figure 21(b). Similarly, if the decoders are interconnected as shown in Figure 23, then the overall detection band would be equal to the difference, or the overlap, between the respective bandwidths as shown in Figure 21(c).

BANDWIDTH REDUCTION

The bandwidth of each decoder can be reduced by either increasing the loop filter capacitor C_2 or reducing the loop gain. Increasing C_2 may be an undesirable solution since this will also reduce the damping of the loop and thus slow the circuit response time.

Figure 22 shows the proper method of reducing the loop gain for reduced bandwidth. This technique will improve damping and permit faster performance under narrow band operation. Bandwidth reduction can also be obtained by subtracting overlapping bandwidths of the two decoder sections (see Figures 21(c) and 23).

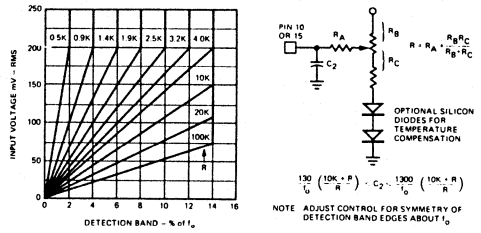


Figure 22. Bandwidth Reduction

APPLICATIONS

DUAL-TONE DETECTION

In most dual-tone detection systems, the decoder output is required to change state only when *both* input tones are present simultaneously. This can be implemented by setting the detection bandwidth of each of the XR-2567 decoder sections to cover one of the input tones; and then connecting the respective outputs through a NOR gate, as shown in Figure 23. In this case, the output of the NOR gate will be "high" only when both input tones are present simultaneously. Due to capacitor and device variation, it is not possible to use a fixed R1 value in production applications.

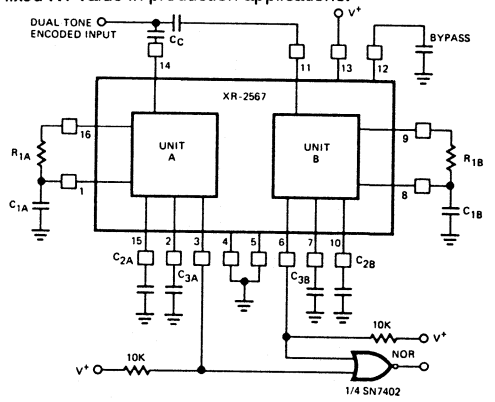


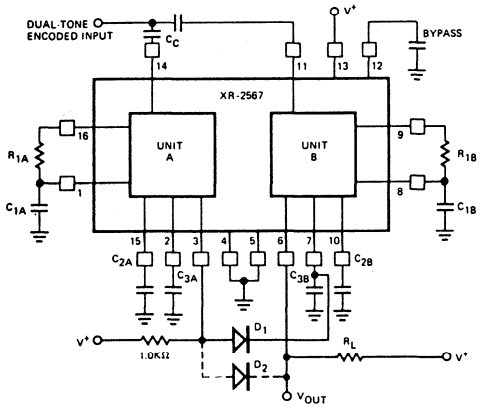
Figure 23. Connection for Decoding Dual-Tone Encoded Input Signals

Figure 24 shows additional circuit configurations which can be used for decoding multiple-tone input signals. In Figure 24(a), the output of Unit A is connected to the output filter (Pin 7) of Unit B through the diode D_1. *If no input tone is present within the detection-band of Unit A,* then its output (pin 3) is "high", which keeps diode D_1 conducting and "disables" Unit B by keeping its output (pin 6) "high". *If an input tone is present within the detection-band of Unit A,* Pin 3 is low, diode D_1 is reverse biased, and decoder B is no longer disabled. If under these conditions an input signal is present within the detection-band of Unit B, then its output at Pin 6 would be "low". Thus, the output at Pin 6 is "low" only

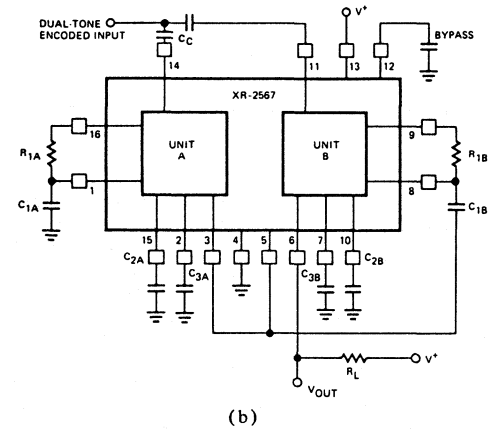
when input tones within the detection-band of A and B are present simultaneously.

The dual-tone decoder circuit of Figure 24(b) makes use of the split-ground feature of the XR-2567. The output terminal of Unit A is used as a "switch" in series with the ground terminal (Pin 5) of Unit B. If the input tone A is not present, Pin 3 is at its high-impedance state, and the ground terminal of Unit B is open-circuited. When the input tone A is present, Pin 3 goes to a low-impedance state and Unit B is activated. In this manner, the output of Unit B will be "low" *only* when both tones A and B are present.

In the circuit connection of Figure 24(b), Unit B does not draw any current until it is activated. Therefore, its power dissipation in a stand-by condition is lower than other dual-tone decoder configurations. However, due to finite series resistance between Pin 3 and ground when Unit B is activated, the output current sink capability is limited to ≤ 10 mA.



(a)



(b)

Figure 24. Additional Dual-Tone Decoding Circuits

SEQUENTIAL TONE DECODING

Dual-tone decoder circuits can also be used for sequential tone decoding where one tone must be present before the other for the circuit to operate. This can be achieved by making the output filter capacitance, C_3, of one of the sections large with respect to the other. For example, in the circuits of Figures 24(a) and 24(b), if C_{3A} is chosen to be much larger than C_{3B} ($C_{3A} \geq C_{3B}$), then Unit A will remain "on" and activate B for a finite time duration after tone A is terminated. Thus, the circuit will be able to detect the two tones only if they are present sequentially, with tone A preceding tone B.

The circuit of Figure 24(a) can also be modified for sequential tone decoding by addition of a diode, D_2, between pins 3 and 6. Once activated by Unit A, Unit B will stay "on" as long as tone B is present, even though tone A may terminate. Once tone B disappears, the circuit is reset to its original state and would require tone A to be present for activation.

HIGH-SPEED NARROW-BAND TONE DECODER

The circuit of Figure 23 can be used as a narrow-band tone decoder by overlapping the detection bands of Units A and B (see Figure 21(c)). The output of the NOR gate will be high only when an input signal is present within the overlapping portions of the detection band. To maintain uniform response within the pass-band, the input signal amplitude should be ≥ 80 mV rms. For minimum response time, PPL filter capacitors C_{2A} and C_{2B} should be:

$$C_{2A} = C_{2B} \cong \frac{130}{f_o\ (Hz)}\ \mu F$$

Under this condition, the worst-case output delay is ≈10 to 14 cycles of the input tone.

The practical matching and tracking tolerances of individual units limit the minimum bandwidth to ≈4% of f_o.

WIDE-BAND TONE DECODER

Figure 25 is a circuit configuration for increasing the detection bandwidth of the XR-2567 by combining the respective bandwidths of individual decoder sections. If the detection bands of each section are located adjacent to each other as shown in Figure 21(b), and if the two outputs (pins 3 and 6) are shorted together, then the resulting bandwidth is the sum of individual bandwidths. In this manner, the total detection bandwidth can be increased to 24% of center frequency. To maintain uniform response throughout the pass band, the input signal level should be ≥80 mV, rms, and the respective pass-bands of each section should have ≈3% overlap at center frequency.

TONE TRANSCEIVER

The XR-2567 can be used as a full-duplex tone transceiver by using one section of the unit as a tone detector and the remaining section as a tone generator. Since both sections operate independently, the circuit

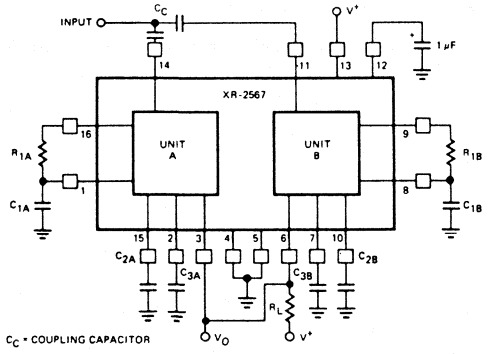


Figure 25. Wide-Band Tone Detection

can transmit and receive simultaneously. A recommended circuit connection for transceiver applications is shown in Figure 26. In this case, Unit A is utilized as the receiver, and Unit B is used as the transmitter. The transmitter section can be keyed "on" and "off" by applying a pulse to pin 8 through a disconnect diode D_1. The oscillator section of Unit B will be keyed "off" when the keying logic level at pin 8 is at a "low" state.

The output of the transmitter section (Unit B) can also be frequency modulated over a +6% deviation range by applying a modulation signal to pin 10.

HIGH CURRENT OSCILLATOR

The oscillator output of each section of XR-2567 can be amplified using the high current logic driver sections of the circuit. In this manner, each section of the circuit can switch 100 mA loads, without sacrificing oscillator stability. A recommended circuit connection for this application is shown in Figure 27. The oscillator frequency can be modulated over ±6% of f_O by applying a control voltage to pins 15 or 10.

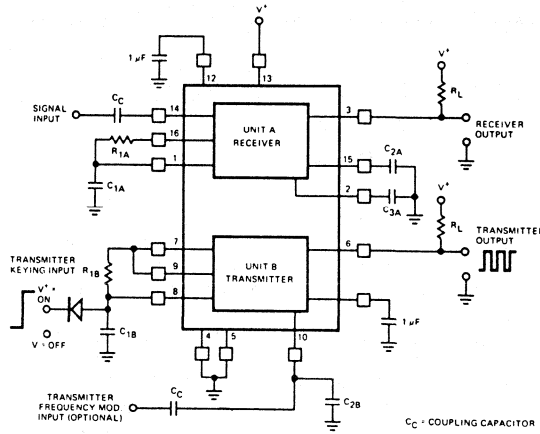


Figure 26. Tone Transceiver

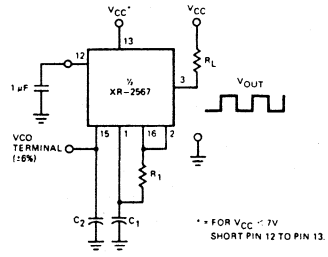


Figure 27. Precision Oscillator with High Current Output Capability

Operational Multiplier

GENERAL DESCRIPTION

The XR-2208 operational multiplier combines a four-quadrant analog multiplier (or modulator), a high frequency buffer amplifier, and an operational amplifier in a monolithic circuit that is ideally suited for both analog computation and communications signal processing application. As shown in the functional block diagram, for maximum versatility the multiplier and operational amplifier sections are not internally connected. They can be interconnected, with a minimum number of external components, to perform arithmetic computation, such as multiplication, division, square-root extraction. The operational amplifier can also function as a pre-amplifier for low-level input signals, or as a post detection amplifier for synchronous demodulator applications. For signal processing, the high frequency buffer amplifier output is available at pin 15. This multiplier/buffer amplifier combination extends the small signal 3-db bandwidth to 8-MHz and the transconductance bandwidth to 100 MHz.

The XR-2208 operates over a wide range of supply voltages, ±4.5V to ±16V. Current and voltage levels are internally regulated to provide excellent power supply rejection and temperature stability. The XR-2208 operates over a 0°C to 70°C temperature range. The XR-2208M is specified for operation over the military temperature range of −55°C to +125°C.

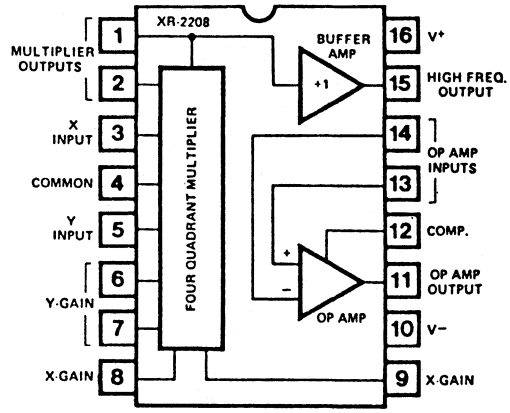
FEATURES

Maximum Versatility
  Independent Multiplier, Op Amp, and Buffer
Excellent Linearity (0.3% typ.)
Wide Bandwidth
  3 dB B.W.—8 MHz typ.
  3° Phase Shift B.W.—1.2 MHz typ.
  Transconductance B.W.—100 MHz typ.
Simplified Offset Adjustments
Wide Supply Voltage Range (±4.5V to ±16V)

APPLICATIONS

Analog Computation
  Multiplication
  Division
  Squaring
  Square-Root
Signal Processing
  AM Generation
  Frequency Doubling
  Frequency Translation
  Synchronous AM Detection
  Triangle-to-Sinewave Converter
  AGC Amplifier
  Phase Detector
Phase-Locked Loop (PLL) Applications
  Motor Speed Control
  Precision PLL
  Carrier Detection
  Phase-Locked AM Demodulation

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply V+	+18 Volts
V−	−18 Volts
Power Dissipation	
Ceramic Package	750mW
Derate above +25°C	6mW/°C
Plastic Package	625 mW
Derate above +25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2208M	Ceramic	−55°C to +125°C
XR-2208N	Ceramic	0°C to +70°C
XR-2208P	Plastic	0°C to +70°C
XR-2208CN	Ceramic	0°C to +70°C
XR-2208CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2208 operational multiplier contains a four-quadrant multiplier with a buffer amplifier for one of the differential outputs for applications requiring high frequency applications. The inputs have a dynamic response of 4 MHz (8 MHz for the X input) and a transconductance bandwidth of 100 MHz for phase detector applications. The fully independent operational amplifier features high gain and a large common mode rejection ratio (90 dB). The device can be powered by voltages from 4.5 VDC to 16 VDC.

ELECTRICAL CHARACTERISTICS

Test Conditions: Supply Voltage = ±15V, T_A = 25°C, unless otherwise specified.

PARAMETERS	XR-2208/ XR-2208M MIN	XR-2208/ XR-2208M TYP	XR-2208/ XR-2208M MAX	XR-2208C MIN	XR-2208C TYP	XR-2208C MAX	UNITS	FIGURES	CONDITIONS
I. GENERAL									
Supply Voltage	±4.5		±16	±4.5		±16	Vdc		See Figure 11
Supply Current		4	7		5	8	mA	2	Measured at Pin 16
II. MULTIPLIER SECTION									
Non-linearity									No external offset trim
(Output Error									
in % of Full Scale)		0.3	0.5		0.5	1.0	%	3	V_y = ±10V, −10V < V_x < +10V
		0.3	0.5		0.5	1.0	%		V_x = ±10V, −10V < V_y < +10V
		0.7	1.0		0.8		%		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1)
									f = 50 Hz
Feedthrough									
a) With Offset Adj.									
X-input		45	80		70	120	mVp-p		V_x = 20 Vp-p V_y = 0
Y-input		60	100		90	150	mVp-p		V_y = 20 Vp-p, V_x = 0
b) No Offset Adj.									
X-input		120			200		mVp-p		V_x = 20 Vp-p, V_x = 0
Y-input		120			200		mVp-p		V_y = 20 Vp-p, V_x = 0
Temperature Coefficient of Scale Factor		±0.07			±0.07		%/°C		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1)
Input Bias Current									
X, Y input		2	6		3	8	μA	2	I_3,I_5 of Figure 2
Common input		4	12		6	16	μA	2	I_4 of Figure 2
Input Resistance	0.5	1.0			1.0		MΩ	2	Measured looking into Pin 3 or Pin 5
Output Offset Voltage		50	80		80	140	mV	2	Measured across Pins 1 and 2
Avg. Temp. Drift		0.5			0.5		mV/°C		$T_{LOW} \le T_A \le T_{HIGH}$
Dynamic Response								5	See Definition Section
3-dB Bandwidth									
X-input	6	8		6	8		MHz		
Y-input	3	4		3	4		MHz		
3° Phase-Shift Bandwdith		1.2			1.2		MHz		
1% Absolute Error Bandwidth		30			30		kHz		
Transconductance Bandwidth		100			100		MHz		
Output Impedance		6			6		kΩ		Measured looking into Pins 1 or 2
III. BUFFER AMPLIFIER									
Output Impedance		200			200		Ω	4	Measured looking into Pin 15
Gain		1.0			1.0				
IV. OPERATIONAL AMPLIFIER									
Input Offset Voltage		1	3		2	6	mV	6	R_S < 50Ω
Temperature Coefficient of Input Offset Voltage		6	20		9	30	μV/°C		$T_{LOW} \le T_A \le T_{HIGH}$
Input Offset Current		4	75		10	100	nA	6	$I_{B1} - I_{B2}$
Input Bias Current		30	200		50	300	nA	6	$\frac{I_{B1} + I_{B2}}{2}$
Voltage Gain	70	75		70	75		dB	6	$R_L \ge 2K$, V_o = ±10V, f = 20 Hz
Differential Input Resistance	0.5	3			3		MΩ	6	
Output Voltage Swing	±10	±12		±10	±12		V		$R_L \ge 2K$, $T_{LOW} \le T_A \le T_{HIGH}$
Input Common	+12	+14		+12	+14				
Mode Range	−10	−12		−10	−12		V	6	
Common Mode Rejection	70	90		70	90		dB	6	f = 20 Hz
Output Resistance		2			2		kΩ	6	
Output Short	**50**	**10**	**30**		**10**		**mA**	**5**	**Positive**
Circuit Current	**-30**	**-10**	**65**		**-10**		**mA**	**5**	**Negative**
Slew Rate		0.5			0.5		V/μs	7	Gain = 1, $R_L \ge 2K$ $C_L \le 100$ pF C_C = 20 pF
Power Supply Sensitivity		30			30		μV/V	6	$R_S \le 10K$

Note 1: T_{LOW} = −55°C, T_{HIGH} = +125°C for XR-2208M T_{LOW} = 0°C, T_{HIGH} = +70°C for XR-2208/XR-2208C

CAUTION: *When using only the op amp or only the multiplier section of the XR-2208, the input terminals to the unused section must be grounded. Thus, when using the multiplier section alone, ground pins 13 and 14; when using the op amp section alone, ground pins 3, 4 and 5.*

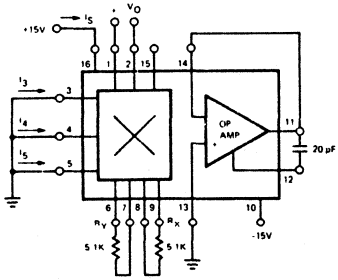


Figure 1. Test Circuit for Quiescent Supply Current, Multiplier Input Bias and Output Offset Voltage.

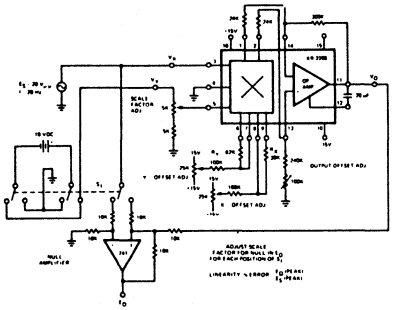


Figure 2. Linearity Test Circuit

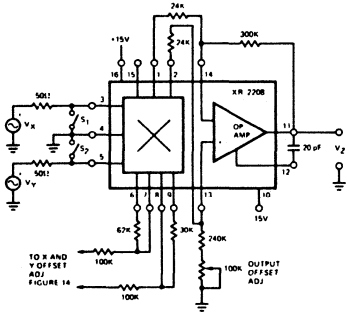


Figure 3. Test Circuit for Feedthrough Measurement. X-Input Feedthrough = V_Z with S_1, open, S_2 closed. Y-Input Feedthrough = V_Z with S_1, closed, S_2 open.

DEFINITION OF MULTIPLIER TERMS

NONLINEARITY: Nonlinearity is the maximum deviation of the output voltage from a straight-line transfer function. It is measured separately for the X and Y inputs and is specified as (%) of full scale output.

FEEDTHROUGH: The amount of peak-to-peak output voltage present with one input grounded and a specified peak-to-peak input applied to the other input. Feedthrough is a function of multiplier offsets and can be minimized by offset adjustment (see Figure 13).

OFFSET VOLTAGES: A four-quadrant analog multiplier has three separate offsets: the X and Y input offsets and the output offset. The transfer function of a practical multiplier with scale factor K can be written as:

$$V_Z = K[(V_X + \phi_X)(V_y + \phi_y)] + \phi_O$$

where ϕ_X and ϕ_y are the offset voltages associated with the respective inputs, ϕ_O is the offset voltage of the output, V_Z is the multiplier output, V_X and V_y are the multiplier inputs. As shown in Figures 13 and 14, each of these offset voltages can be nulled to zero by external adjustments.

SCALE FACTOR, K: The constant of proportionality that relates the multiplier output to the X and Y inputs. If the offset terms are neglected, the multiplier output, V_Z, is related to the X and Y inputs as $V_Z = K(V_X \cdot V_y)$. The scale factor K has the dimensions of $(volts)^{-1}$ and can be adjusted externally.

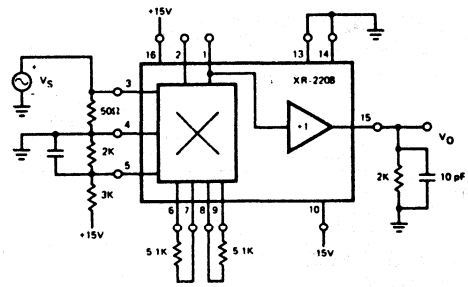


Figure 4. Test Circuit for Multiplier Small-Signal Bandwidth for X-Input (For Y-Input, reverse connections between Pin 3 and 5).

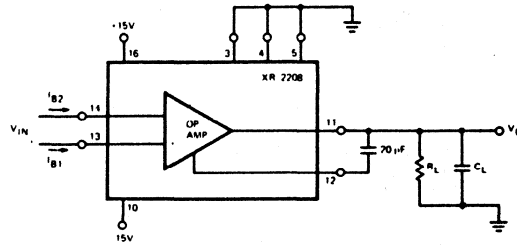


Figure 5. Test Circuit for Op Amp DC Parameters

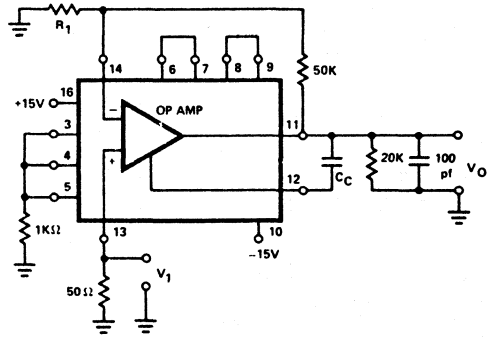


Figure 6. Op Amp AC Test Circuit

TYPICAL CHARACTERISTIC CURVES

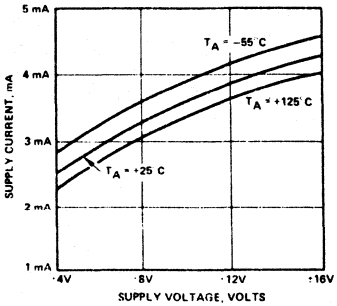


Figure 7. Supply Current vs Supply Voltage

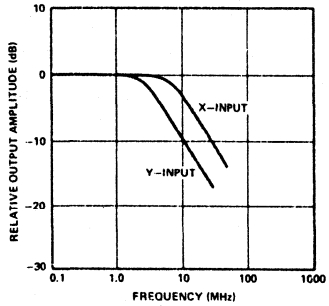


Figure 8. Small-Signal Frequency Response for the Multiplier Section. (Output Measured at Pin 15—See Fig. 4).

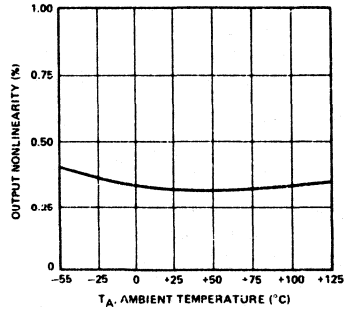


Figure 9. Temperature Dependence of Output Nonlinearity for X or Y Inputs (See Figure 2).

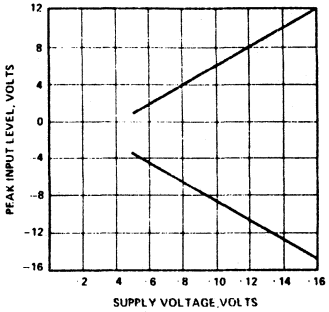


Figure 10. Multiplier Input Dynamic Range vs Power Supply

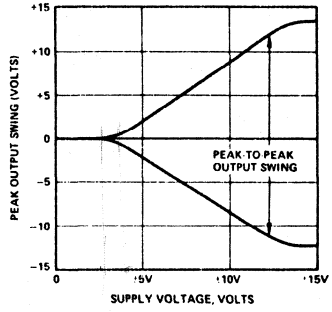


Figure 11. Op Amp Output Swing vs Power Supply

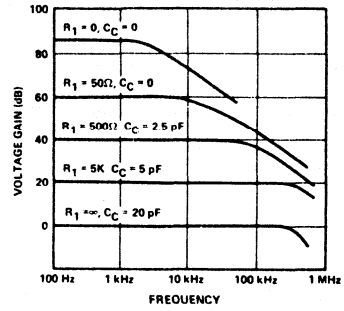


Figure 12. Op Amp Frequency Response

In most arithmetic applications the multiplier and op amp sections of the XR-2208 are interconnected as shown in Figure 14. In such applications, over-all scale factor K can be written as:

$$K = (K_m)(K_a) = \left(\frac{V_o}{V_x V_y}\right)\left(\frac{V_z}{V_o}\right)$$

where K_m is the gain constant of the multiplier section, and K_a is the gain of the op amp stage in Figure 14, V_o is the multiplier output across pins 1 and 2, and V_z is the op amp output at pin 11. With reference to Figure 14, these gain constants can be expressed as:

$$K_m \simeq \frac{25}{R_x R_y}(\text{volts})^{-1}; \quad K_a \simeq \frac{R_f}{6 + R_i}$$

where all resistors are in kΩ.

Thus, overall scale factor K can be adjusted by varying R_x, R_y, R_f. For fine adjustment of the scale factor, K, an additional potentiometer can be included into the circuit, as shown in Figure 14.

INPUT DYNAMIC RANGE: The maximum peak signal which can be applied to the X or Y inputs for a given supply voltage without impairing linearity. (See Figure 10).

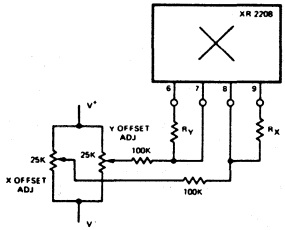


Figure 13. Offset Adjustment

MULTIPLIER BANDWIDTH: Depending on the particular application, a different definition of "multiplier bandwidth" may be used. The most commonly accepted definitions are:

a) *3-dB Bandwidth:* Frequency where the multiplier output is 3-dB below its low frequency (f = 20 Hz) level.

b) *3° Phase Shift Bandwidth:* Frequency where the net phase shift across the multiplier is equal to 3°.

c) *1% Absolute Error Bandwidth:* Frequency where the phase vector error between the actual and ideal output vectors is equal to 1%. This frequency is reached when the net phase shift across the multiplier is equal to 0.01 radian or 0.57°.

d) *Transconductance Bandwidth:* Frequency where the transconductance of the multiplier drops 3-dB below its low frequency value. This bandwidth defines the frequency range of operation for phase-detector and synchronous AM detector applications.

DESCRIPTION OF CIRCUIT CONTROLS

MULTIPLIER INPUTS (PINS 3, 4, AND 5)

The X and Y inputs to the multiplier are applied to pins 3 and 5 respectively. The third input (pin 4) is common to both X and Y portions of the multiplier, and in most applications serves as a "reference" or ground terminal. The typical bias current at the multiplier inputs is 3 μA for the X- and Y- inputs and 6 μA for the "common" terminal. In circuit applications such as "synchronous AM detection" or "frequency doubling" where the same input signal is applied to both X and Y inputs, pin 4 can be used as the input terminal since it is common to both X and Y sections of the multiplier.

MULTIPLIER OUTPUTS (PINS 1 AND 2)

The differential output voltage, V_O, across these terminals is proportional to the linear product of voltages V_X and V_Y applied to the inputs. V_O can be expressed as:

$$V_O \approx \left(\frac{25}{R_X R_Y}\right)\left(V_X V_Y\right)$$

where all voltages are in volts and the resistors are in kΩ. R_X and R_Y are the gain control resistors for X and Y sections of the multiplier.

The common-mode dc potential at the multiplier outputs is approximately 3 volts below the positive supply. One of the multiplier outputs (pin 1) is internally connected to the unity-gain buffer amplifier input for high-frequency applications.

In most analog computation operations, such as multiplication, division, etc., pins 1 and 2 are dc coupled to the op amp inputs (pins 13 and 14). The final output, V_Z, is then obtained from the op amp output at pin 11, as shown in Figure 14.

X AND Y GAIN ADJUST (PINS 6, 7, 8, 9)

The gains of the X and Y sections of the multiplier are inversely proportional to resistors R_X and R_Y connected across the respective gain terminals. The multiplier conversion gain, K_m, can be expressed as:

$$K_m = \frac{25}{R_X R_Y} \quad (\text{volts})^{-1}$$

where R_X and R_Y are in kΩ.

X AND Y OFFSET ADJUST (PINS 7 AND 8)

Two of the gain-control terminals, pins 7 and 8, are also used for adjusting X and Y offsets. Figure 13 shows the typical adjustment circuitry which can be connected to these pins to null-out input offsets.

OP AMP INPUTS (PINS 13 AND 14)

Pin 13 is the non-inverting and pin 14 the inverting inputs for the op amp section. In most multiplier applications, these terminals are connected to the multiplier outputs (pins 1 and 2). **Note: When the op amp section is not used, these terminals should be grounded.**

OP AMP COMPENSATION (PIN 12)

The op amp section can be compensated for unconditional stability with a 20 pF capacitor connected between pin 12 and pin 11. For op amp voltage gains greater than unity, this compensation capacitance can be reduced to improve slew rate and small signal bandwidth as shown in Figure 12.

OP AMP OUTPUT (PIN 11)

This terminal serves as the output for the op amp section. It is internally protected against accidental short circuit conditions, and can sink or source 10 mA of current into a resistive load. In most multiplier applications, pin 11 is the actual XR-2208 output, with the op amp inputs being connected to the multiplier outputs.

BUFFER AMPLIFIER OUTPUT (PIN 15)

The buffer amp is internally connected to the multiplier section. The buffer amp has unity voltage gain, and provides a low-impedance output at pin 15 for the multiplier section. The buffer amp is particularly useful for high frequency operation since it minimizes the capacitive loading effects at the multiplier outputs.

The buffer amplifier is activated by connecting a load resistor, R_1, from pin 15 to ground. When it is not used, pin 15 can be left open circuited. However, since the buffer amplifier output is a low impedance point, reasonable care should be taken to avoid burnout due to accidental short circuits. The maximum dc current drawn from pin 15 should be limited to 10 mA. The dc voltage at pin 15 is typically 4.5 volts below V+.

APPLICATIONS INFORMATION

PART I: ARITHMETIC OPERATIONS

Multiplication

For most multiplication applications, the multiplier and op amp sections are interconnected as shown in Figure 15 to provide a single-ended analog output with a wide dynamic range. The circuit of Figure 14 provides a linear output swing of 10V for maximum input signals of 10V, with a scale factor K = 0.1. The trimming procedure for the circuit is as follows:

1. Apply OV to both inputs and adjust the output offset to OV using the output offset control.

2. Apply 20V p-p at 50 Hz to the X-input and OV to the Y-input. Trim the Y-offset adjust for minimum peak-to-peak output.

3. Apply 20V p-p to the Y-input and OV to the X-input. Trim X-offset adjust for minimum peak-to-peak output.

4. Repeat step 1.

5. Apply +10V to both inputs and adjust scale factor for V_O = +10V. This step may be repeated with different amplitudes and polarities of input voltages to optimize accuracy over the entire range of input voltages, or over any specific portion of input voltage range.

Squaring Circuit

The recommended circuit connection for squaring applications is shown in Figure 15. This circuit is the same as the basic multiplier circuit with both inputs tied together, except only one input offset adjustment is necessary. Trimming procedure for the squaring circuit is as follows:

1. Apply 0 volts to the input and adjust the output offset to zero.

2. Apply 1.0V to the input and adjust the Y-offset until V_O = 0.10V.

3. Apply 10V to the input and adjust the scale factor until V_O = +10V.

4. Apply −10V to the input and check that V_O = +10V. If not, repeat steps 1 through 3. Some compromise may be necessary in scale factor adjustments given in steps 3 and 4.

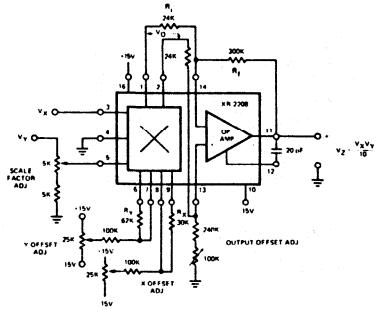


Figure 14. Multiplication Circuit

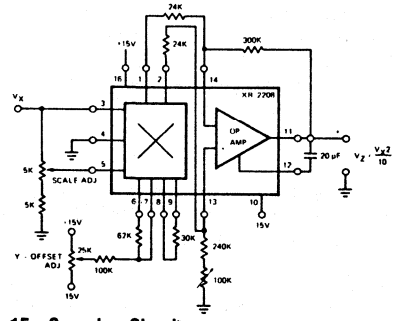


Figure 15. Squaring Circuit

Dividing Circuit

Recommended circuit connection for performing analog division is shown in Figure 16. This circuit uses the multiplier in the feedback path of the op amp. For the circuit shown, $V_O = +10\ V_Z/V_X$ where $V_X < 0$ and V_Z can have either sign. Positive values of V_X are not allowed, since this will reverse the polarity of the feedback loop, causing positive feedback and latchup.

This latchup mode is nondestructive to the XR-2208, and is common to all analog division circuits. The divide circuit is trimmed as follows:

1. Apply V_Z = 0 and trim the output offset adjustment for constant output voltage as V_X is varied from −1V to −10V.

2. Keeping V_Z = 0, and applying V_X = −10V, trim the Y-offset adjust until V_O = 0.

3. Let $V_Z = V_X$ and/or $V_Z = -V_X$ and trim the X-offset adjustment for constant output voltage as V_X is varied from −1V to −10V.

4. Repeat steps 1 and 2 if step 3 required a large initial adjustment.

5. Keeping $V_Z = V_X$, adjust the scale factor trim for V_O = −10V as V_X is varied from −1V to −10V.

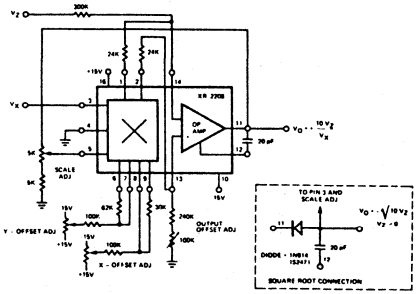


Figure 16. Dividing Circuit

Square Root Circuit

This is essentially the dividing circuit with the X input tied to the output. Thus, the voltage on the Z input is divided by the output voltage, i.e. the output is proportional to the square root of the input. A diode is included in series with the output to prevent a latchup condition which would result if V_Z were allowed to go negative. The square root circuit may be trimmed as a divider by disconnecting the X-input from the output, keeping $V_Z > 0$ and $V_X < 0$. The square root circuit may also be trimmed in the closed-loop mode by the following procedure:

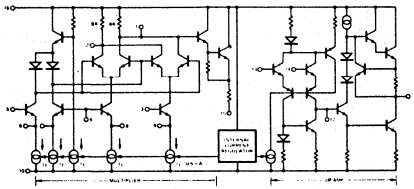
1. Apply V_Z = +0.10V and trim the output offset adjust for V_O = −0.316V.

2. Apply V_Z = +0.9V and trim the X-offset adjust for V_O = −3.0V.

3. Apply $V_Z = +10V$ and trim the scale factor adjust for $V_O = -10V$.

4. Repeat steps 1 through 3 until desired accuracy is achieved.

EQUIVALENT SCHEMATIC DIAGRAM



PART II: SIGNAL PROCESSING

AM GENERATION

Figure 17 is the recommended circuit connection for generating double side-band (DSB) or suppressed carrier AM signals. Modulation and carrier inputs are applied to the X and Y inputs respectively. The carrier level at the output can be adjusted by the dc voltage applied to pin 3. For suppressed carrier operation, the carrier feedthrough can be further reduced by using the X and Y offset adjustments. In this application, the unity-gain buffer amplifier section will provide a low impedance output if desired. If the buffer amp is not used, pin 15 should be open circuited to reduce power dissipation.

Typical carrier suppression without offset adjustment is 40 dB for frequencies up to 1 MHz, and 30 dB for frequencies up to 10 MHz. For low frequency applications ($f < 10$ kHz), carrier suppression can be reduced to 60 dB by using the offset adjustment controls.

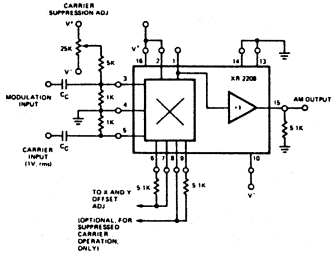


Figure 17. AM Generation

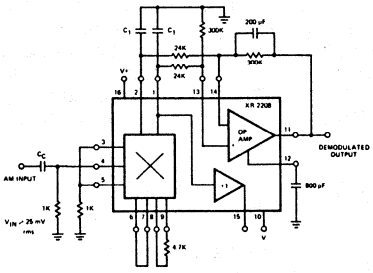


Figure 18. Synchronous AM Detector.

SYNCHRONOUS AM DETECTION

Figure 18 is a typical circuit connection for synchronous AM detection for carrier frequencies up to 100 MHz. The AM input signal is applied to the multiplier "common" terminal (pin 4). The Y-gain terminals are shorted, and this section of the multiplier serves as a "limiter" for input signals ≥ 50 mVrms; the X-section of the multiplier operates in its linear mode. The low-pass filter capacitors, C_1, at pins 1 and 2 are used to filter the carrier feedthrough. If desired, the op amp section can be used as an audio preamplifier to increase the demodulated output amplitude.

TRIANGLE-TO-SINEWAVE CONVERSION

A triangular input can be converted into a low distortion (THD < 1%) sinusoidal output with the XR-2208. A recommended connection for this application is shown in Figure 19. The triangle input signal is applied to the X-input (pin 3). The multiplier section rounds off the peaks of this input and converts it to a low distortion sine wave. For the component values shown in Figure 19, the recommended input signal level at pin 3 is ≃ 300 mV pp in order to obtain a 2V pp sine wave output at pin 15. This waveform can be further amplified using the op amp section to provide high level (10V pp), low distortion output at pin 11.

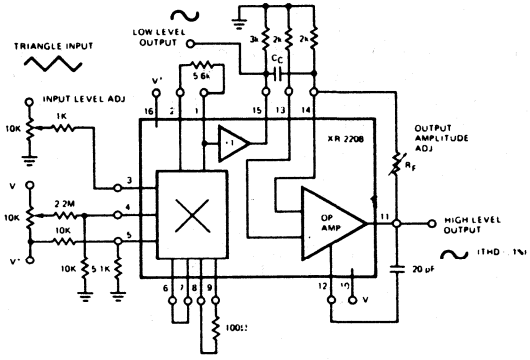


Figure 19. Triangle-to-Sine Converter

PHASE DETECTION

The multiplier section can be used as a phase detector. A recommended circuit connection is shown in Figure 20. The reference input is applied to pin 5, and the input signal whose phase is to be detected is applied to pin 3. The differential dc voltage, V_ϕ, at the multiplier outputs (pins 1 and 2) is related to the phase difference, ϕ, between the two input signals, V_1 and V_2, as:

$$V_\phi = K_d \cos \phi$$

where K_d is the phase detector conversion gain. For input signals ≥ 50 mV rms, K_d is ≈2V/radian and is independent of signal amplitude. For lower input amplitudes, K_d decreases linearly with the decreasing input level. The capacitors C_1 at pins 1 and 2 provide a low-pass filter with a time constant $T_1 = R_1 C_1$, where $R_1 = 6$ kΩ is the internal impedance level at these pins.

If needed, the phase conversion gain can be increased by using the op amp section of the XR-2208 to further amplify the output voltage, V_{ϕ}. The XR-2208 is suitable for phase detection for input frequencies up to 100 MHz. Pins 1 and 2 are normally tied to an operational amplifier placed in a difference amplifier configuration.

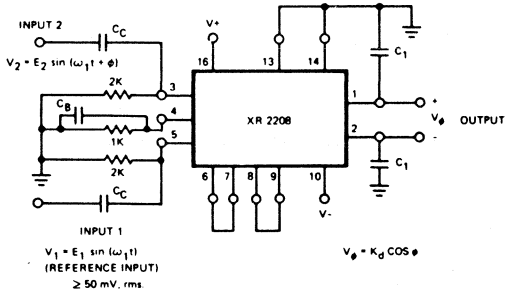


Figure 20. Phase-Detector Circuit

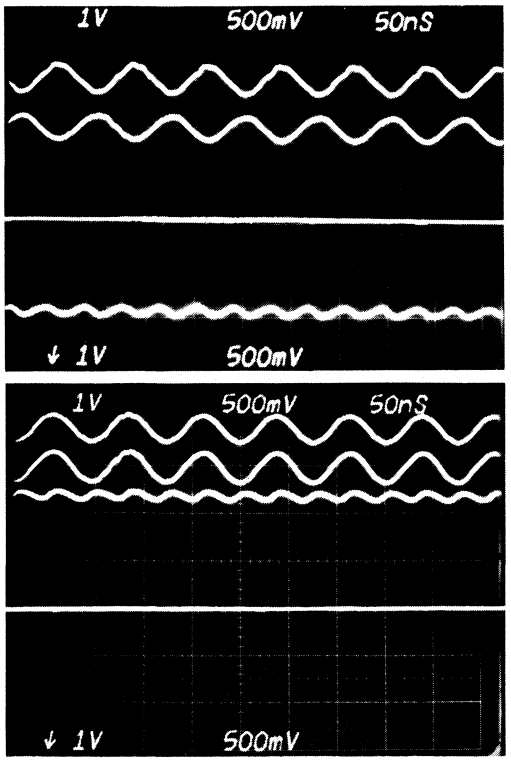


Figure 21. Shows the summed output of the phase detector circuit with pin 1 applied to the inverting input of oscilloscope; pin 2 applied to the noninverting input of oscilloscope.
C_1 = 12pF, f_{INPUT} = 12 MHz, ø = 180°, V_0 = −2.5 V_{DC}, (a)
ø = 0°, (b) V_0 = +2.5 V_{DC}.

PART III: PHASE-LOCKED LOOP APPLICATIONS

MOTOR SPEED CONTROL

A motor speed control where the frequency of the motor is "phase-locked" to the input reference frequency, f_r, is shown in Figure 22. The multiplier section of the XR-2208 is used as a phase-comparator, comparing the phase of the tachometer output signal with the phase of the reference input. The resulting error voltage across pins 1 and 2 is low-pass filtered by capacitors C_1 and amplified by the op amp section. This error signal is then applied to the motor field-winding to phase-lock the motor speed to the input reference frequency.

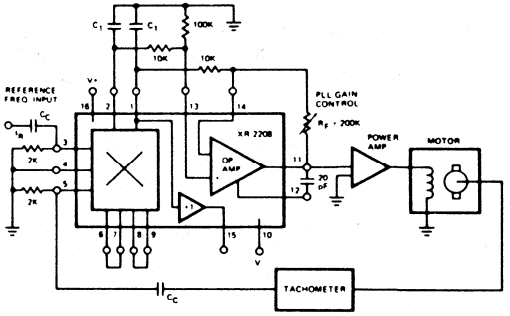


Figure 22. Motor Speed Control Circuit

PRECISION PLL

A precision phase-locked loop may be constructed using an XR-2207 voltage controlled oscillator and an XR-2208. (See Figure 23.) Due to the excellent temperature stability and wide sweep range of the XR-2207 this PLL circuit exhibits especially good stability of center frequency and wide lock range. In this application the XR-2208 serves as a phase comparator and level shifter. Resistor R_L adjusts the loop gain of the PLL, thus varying the lock range. Tracking range may be varied from about 1.5:1 up to 12:1. For large values of R_L, temperature stability of center frequency is better than 30 ppm/°C.

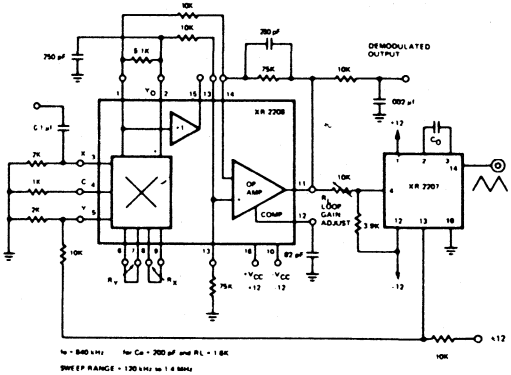


Figure 23. Precision PLL

PHASE-LOCKED AM AND CARRIER DETECTION

The XR-2208 can be used as a "quadrature detector" in conjunction with monolithic PLL circuits to perform phase-locked AM demodulation and for carrier-level detection. Figure 24 shows a recommended circuit connection for such applications. The XR-210 or XR-215 monolithic PLL circuits can be adjusted to lock on the desired input AM signal and re-generate the unmodulated carrier. This carrier frequency appears across the timing capacitor, C_O, of the PLL and is used as the "reference input" to the XR-2208 multiplier. The AM signal is applied simultaneously to the PLL input and to the XR-2208 multiplier input (pin 3), as shown in Figure 24.

The demodulated signal is then low-pass filtered by capacitor C_1 at the multiplier output, and can be amplified further to the desired audio level by using the op amp section of the XR-2208.

In the carrier detector applications, the op amp is used as a voltage comparator and produces a "high" or "low" level logic signal at the op amp output when the input carrier level reaches a detection threshold level set by an external potentiometer. The output from the carrier detector can then be used to enable the "logic-output" stage of the XR-210 FSK modem.

The phase-locked AM or carrier detector system of Figure 23 shows a high degree of frequency selectivity, as determined by the monolithic PLL "capture" bandwidth.

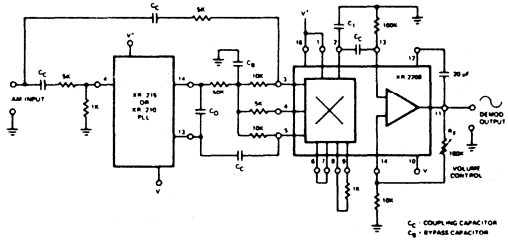


Figure 24. Phase-Locked AM Demodulation or Carrier Detection

Monolithic Multiplier/Detector

GENERAL DESCRIPTION

The XR-2228 is a monolithic multiplier/detector circuit especially designed for interfacing with integrated phase-locked loop (PLL) circuits, to perform synchronous AM detection and triangle-to-sinewave conversion. It combines a four-quadrant analog multiplier (or modulator) and a high-gain operational amplifier in a single monolithic circuit.

As shown in the equivalent schematic diagram, the four-quadrant multiplier section is designed with fully differential X- and Y-inputs and differential outputs. For maximum versatility, the multiplier and the operational amplifier sections are not internally connected. The operational amplifier can also function as a pre-amplifier for low-level input signals, or as a post-detection amplifier for synchronous demodulation, phase-detection or for sine-shaper applications.

FEATURES

Independent Multiplier and Op Amp Sections
Differential X and Y Inputs
Interfaces with all PLL and VCO Circuits
Wide Common Mode Range
Wide Transconductance Bandwidth (100 MHz, Typ.)
Wide Supply Voltage Range (±4.5V to ±16V)

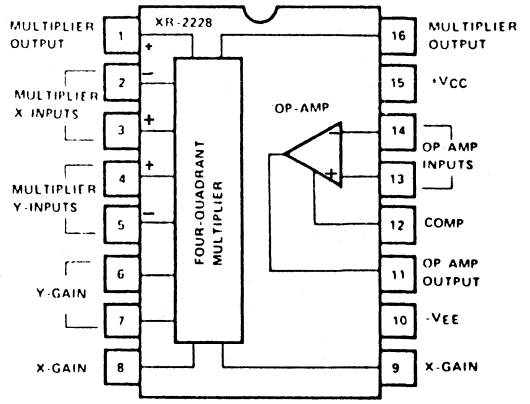
APPLICATIONS

Phase-Locked Loop Design
Phase Detection
Synchronous AM Detection
AM Generation
Triangle-to-Sinewave Conversion
Frequency Translation

ABSOLUTE MAXIMUM RATINGS

Power Supply	±18 Volts
Power Dissipation	
Ceramic Package	750 mW
Derate above +25°C	6 mW/°C
Plastic Package	625 mW
Derate above +25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2228CN	Ceramic	0°C to +70°C
XR-2228CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2228 multiplier/detector contains a four quadrant multiplier and a fully independent operational amplifier. The four quadrant multiplier has fully differential X and Y inputs and outputs. Both inputs have 3 MHz dynamic response and 100 MHz transconductance bandwidth. The operational amplifier features high gain and a large common mode range. The device is powered by 4.5V to 16V split supplies.

For higher frequency applications, consider the XR-2208.

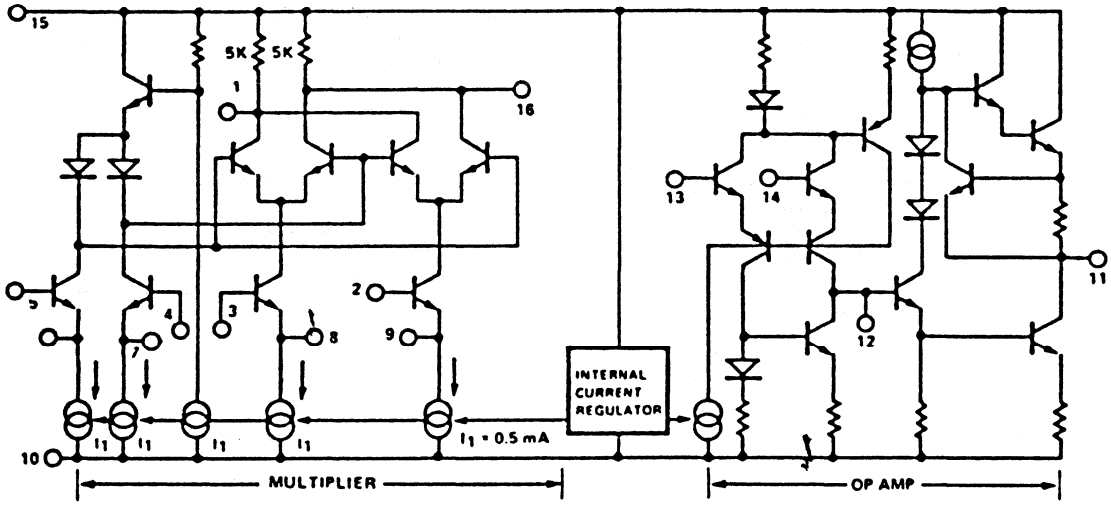
ELECTRICAL CHARACTERISTICS

Test Conditions: Supply Voltage = ±15V, T_A = 25°C, unless otherwise specified.

PARAMETERS	XR-2228C MIN	XR-2228C TYP	XR-2228C MAX	UNITS	FIGURES	CONDITIONS
I. GENERAL						
Supply Voltage	±4.5		±16	V dc		See Figure 11
Supply Current		5	8	mA	1	Measured at Pin 15
II. MULTIPLIER/MODULATOR SECTION						
Non-linearity						No external offset trim
(Output Error in % of Full Scale)		0.5	1.0	%	2	V_y = ±10V, −10V < V_x < +10V
		0.5	1.0	%		V_x = ±10V, −10V < V_y < +10V
		0.8		%		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1) f = 50 Hz
Feedthrough						
a. With Offset Adj.						
X-input		70	120	mVp-p	3	V_x = 20 Vp-p V_y = 0
Y-input		90	150	mVp-p		V_y = 20 Vp-p, V_x = 0
b. No Offset Adj.						
X-input		200		mVp-p		V_x = 20 Vp-p, V_x = 0
Y-input		200		mVp-p		V_y = 20 Vp-p, V_x = 0
Temperature Coefficient of Scale Factor		±0.07		%/°C		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1)
Input Bias Current						
X or Y inputs		3	8	μA	1	Measured at Pins 2, 3, 4 or 5.
Input Resistance		1.0		MΩ	2	Measured at Pins 2, 3, 4 or 5.
Output Offset Voltage		80	140	mV	2	Measured across Pins 1 and 16
Avg. Temp. Drift		0.5		mV/°C		$T_{LOW} \le T_A \le T_{HIGH}$
Dynamic Response					4	See definition section, and Note 1
3-dB Bandwidth						
X-input	1	3		MHz		
Y-input	1	3		MHz		
3° Phase-Shift Bandwidth		1		MHz		
1% Absolute Error Bandwidth		30		kHz		
Transconductance Bandwidth		100		MHz		
Output Impedance		5		kΩ		Measured looking into Pins 1 or 16
III. OPERATIONAL AMPLIFIER SECTION						
Input Offset Voltage		2	6	mV	5	R_S < 50Ω
Temp. Coef. of Input Offset Voltage		9	30	μV/°C		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1)
Input Offset Current		10	100	nA	5	$I_{B1} - I_{B2}$
Input Bias Current		50	300	nA	5	$\frac{I_{B1} + I_{B2}}{2}$
Voltage Gain	70	75		dB	5	$R_L \ge 2K$, V_O = ±10V, f = 20 Hz
Differential Input Resistance		3		MΩ	5	
Output Voltage Swing	±10	±12		V		$R_L \ge 2K$, $T_{LOW} \le T_A \le T_{HIGH}$
Input Common Mode Range	+12 −10	+14 −12		V	5	
Common Mode Rejection	70	90		dB	5	f = 20 Hz
Output Resistance		2		kΩ	5	
Slew Rate		0.5		V/μs	5	Gain = 1, $R_L \ge 2K$, $C_L \le 100$ pF C_C = 20 pF
Power Supply Sensitivity		30		μV/V	5	$R_S \le 10K$

Note 1: T_{LOW} = 0°C, T_{HIGH} = +70°C for XR-2228C; not tested in production

CAUTION: *When using only the op amp or only the multiplier section of the XR-2228, the input terminals to the unused section must be grounded. Thus, when using the multiplier section alone, ground pins 13 and 14; when using the op amp section alone, ground pins 2, 3, 4 and 5.*



EQUIVALENT SCHEMATIC DIAGRAM

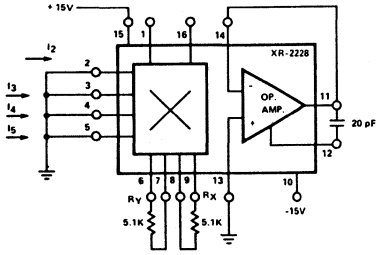


Figure 1. Test Circuit for Quiescent Supply Current, Multiplier Input Bias and Output Offset Voltage

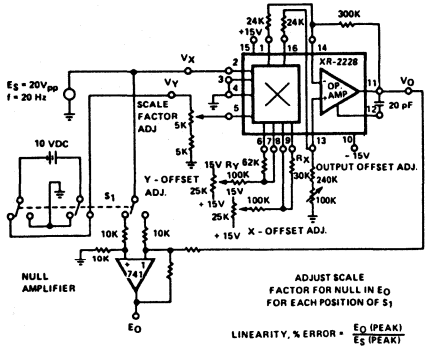


Figure 2. Linearity Test Circuit

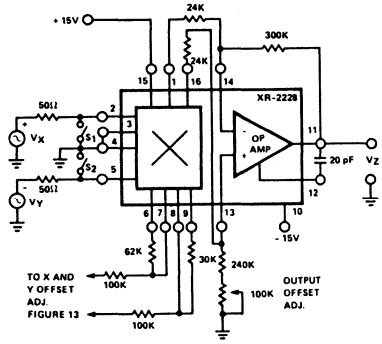


Figure 3. Test Circuit for Feedthrough Measurement. X-Input Feedthrough = V_Z with S_1, open S_2 closed. Y-Input Feedthrough = V_Z with S_1 closed, S_2 open.

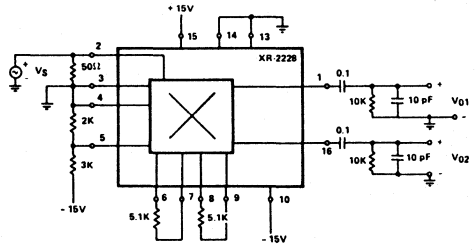


Figure 4. Test Circuit for Multiplier Small-Signal Bandwidth for X-Input (For Y-Input, reverse connections between Pins 2 and 5)

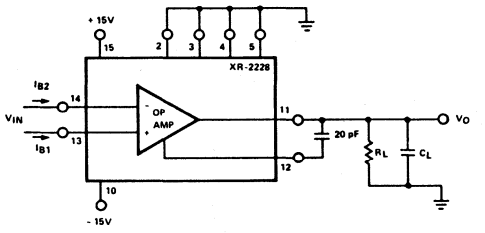


Figure 5. Test Circuit for Op Amp DC Parameters

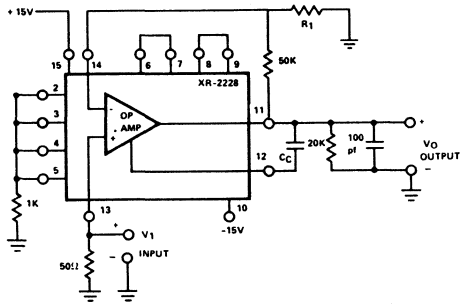


Figure 6. Op Amp AC Test Circuit

DEFINITION OF MULTIPLIER TERMS

NONLINEARITY: Nonlinearity is the maximum deviation of the output voltage from a straight-line transfer function. It is measured separately for the X and Y inputs and is specified as (%) of full scale output.

FEEDTHROUGH: The amount of peak-to-peak output voltage present with one input grounded and a specified peak-to-peak input applied to the other input. Feedthrough is a function of multiplier offsets and can be minimized by offset adjustment (see Figure 13).

OFFSET VOLTAGES: A four-quadrant analog multiplier has three separate offsets: the X and Y input offsets and the output offset. The transfer function of a practical multiplier with scale factor K can be written as:

$$V_Z = K[(V_X + \phi_X)(V_y + \phi_y)] + \phi_O$$

where ϕ_X and ϕ_y are the offset voltages associated with the respective inputs, ϕ_O is the offset voltage of the output. V_Z is the multiplier output, V_X and V_y are the multiplier inputs. As shown in Figures 13 and 14, each of these offset voltages can be nulled to zero by external adjustments.

TYPICAL CHARACTERISTICS CURVES

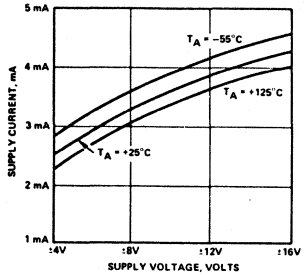


Figure 7. Supply Current vs Supply Voltage

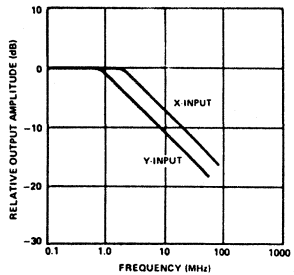


Figure 8. Small-Signal Frequency Response for the Multiplier Section. (Output Measured at Pin 16—See Fig. 4)

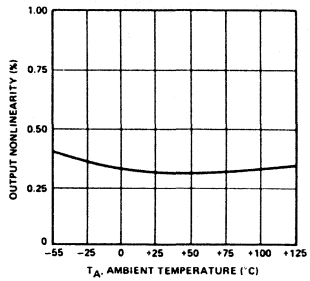


Figure 9. Temperature Dependence of Output Nonlinearity for X or Y Inputs (See Figure 2)

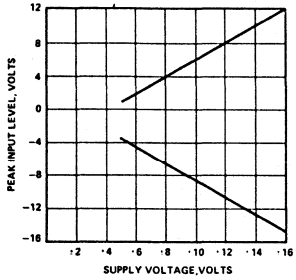


Figure 10. Multiplier Input Dynamic Range vs Power Supply

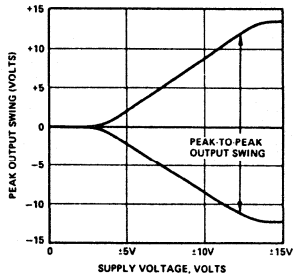


Figure 11. Op Amp output Swing vs Power Supply

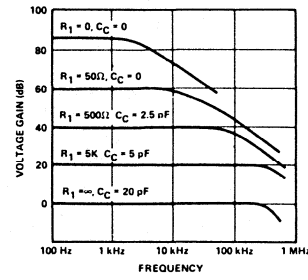


Figure 12. Op Amp Frequency Response

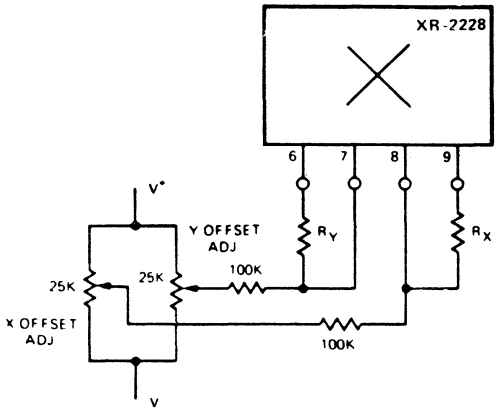


Figure 13. Offset Adjustment

where ϕ_X and ϕ_Y are the offset voltages associated with the respective inputs, ϕ_O is the offset voltage of the output. V_Z is the multiplier output, V_X and V_Y are the multiplier inputs. As shown in Figures 13 and 14, each of these offset voltages can be nulled to zero by external adjustments.

SCALE FACTOR, K: The constant of proportionality that relates the multiplier output to the X and Y inputs. If the offset terms are neglected, the multiplier output, V_Z, is related to the X and Y inputs as $V_Z = K(V_X \cdot V_Y)$. The scale factor K has the dimensions of $(\text{volts})^{-1}$ and can be adjusted externally.

In most arithmetic applications the multiplier and op amp sections of the XR-2228 are interconnected as shown in Figure 14. In such applications, over-all scale factor K can be written as:

$$K = (K_m)(K_a) = \left(\frac{V_O}{V_X Y_X}\right)\left(\frac{V_Z}{V_O}\right)$$

where K_m is the gain constant of the multiplier section, and K_a is the gain of the op amp stage in Figure 14. V_O is the multiplier output across pins 1 and 16, and V_Z is the op amp output at pin 11. With reference to Figure 14, the gain constants can be expressed as:

$$K_m \simeq \frac{25}{R_X R_Y}\,(\text{volts})^{-1}; \quad K_a \simeq \frac{R_f}{6 + R_i}$$

where all resistors are in kilo-ohms.

Thus, overall scale factor K can be adjusted by varying R_X, R_Y, R_f. For fine adjustment of the scale factor, K, an additional potentiometer can be included into the circuit, as shown in Figure 14.

INPUT DYNAMIC RANGE: The maximum peak signal which can be applied to the X or Y inputs for a given supply voltage without impairing linearity. (See Figure 10).

MULTIPLIER BANDWIDTH: Depending on the particular application, a different definition of "multiplier bandwidth" may be used. The most commonly accepted definitions are:

a) *3-dB Bandwidth*: Frequency where the multiplier output is 3-dB below its low frequency (f = 20 Hz) level.

b) *3° Phase Shift Bandwidth*: Frequency where the net phase shift across the multiplier is equal to 3°.

c) *1% Absolute Error Bandwidth*: Frequency where the phase vector error between the actual and ideal output vectors is equal to 1%. This frequency is reached when the net phase shift across the multiplier is equal to 0.01 radian or 0.57°.

d) *Transconductance Bandwidth*: Frequency where the transconductance of the multiplier drops 3-dB below its low frequency value. This bandwidth defines the frequency range of operation for phase-detector and synchronous AM detector applications.

DESCRIPTION OF CIRCUIT CONTROLS

MULTIPLIER INPUTS (PINS 2, 3, 4 AND 5): These four terminals provide the differential inputs to the X- and Y-sections of the multiplier, respectively. The output will be a linear product of the two voltages, V_X and V_Y, applied differentially across pins (2,3) and (4,5). Typical input bias current at the multiplier inputs is approximately 3 μA, for each of the four inputs. In circuit applications requiring single-ended, rather than differential, input signals, pins 3 and 4 can be shorted together and connected to a common bias point.

MULTIPLIER OUTPUTS (PINS 1 AND 16): The differential output voltage, V_O, across these terminals is proportional to the linear product of voltages V_x and V_y applied to the inputs. V_O can be expressed as:

$$V_O \approx \left(\frac{25}{R_X R_Y}\right)(V_X V_Y)$$

where all voltages are in volts and the resistors are in kΩ. R_X and R_Y are the gain control resistors for X and Y sections of the multiplier.

The common-mode dc potential at the multiplier outputs is approximately 3 volts below the positive supply.

In most analog computation operations, such as multiplication, division, etc., pins 1 and 16 are dc coupled to the op amp inputs (pins 13 and 14). The final output, V_Z, is then obtained from the op amp output at pin 11, as shown in Figures 14 and 15.

X AND Y GAIN ADJUST (PINS 6, 7, 8, 9): The gains of the X and Y sections of the multiplier are inversely proportional to resistors R_X and R_Y connected across the respective gain terminals. The multiplier conversion gain, K_m, can be expressed as:

$$K_m \cong \frac{25}{R_X R_Y}\ (\text{volts})^{-1}$$

where R_X and R_Y are in kΩ.

X AND Y OFFSET ADJUST (PINS 7 AND 8): Two of the gain-control terminals, pins 7 and 8, are also used for adjusting X and Y offsets. Figure 13 shows the typical adjustment circuitry which can be connected to these pins to null-out input offsets.

OP AMP INPUTS (PINS 13 AND 14): Pin 13 is the noninverting and pin 14 the inverting inputs for the op amp section. In most multiplier applications, these terminals are connected to the multiplier outputs (pins 1 and 16). **Note: When the op amp section is not used, these terminals should be grounded.**

OP AMP COMPENSATION (PIN 12): The op amp section can be compensated for unconditional stability with a 20 pF capacitor connected between pin 12 and pin 11. For op amp voltage gains greater than unity, this compensation capacitance can be reduced to improve slew rate and small signal bandwidth as shown in Figure 12.

OP AMP OUTPUT (PIN 11): This terminal serves as the output for the op amp section. It is internally protected against accidental short circuit conditions, and can sink or source 10 mA of current into a resistive load. In most multiplier applications, pin 11 is the actual XR-2228 output, with the op amp inputs being connected to the multiplier outputs.

APPLICATIONS INFORMATION

PART I: ARITHMETIC OPERATIONS

MULTIPLICATION

For most multiplication applications, the multiplier and op amp sections are interconnected as shown in Figure 14 to provide a single-ended analog output with a wide dynamic range. The circuit of Figure 14 provides a linear output swing of 10V for maximum input signals of 10V, with a scale factor K = 0.1. The trimming procedure for the circuit is as follows:

1. Apply 0V to both inputs and adjust the output offset to 0V using the output offset control.

2. Apply 20V p-p at 50 Hz to the X-input and 0V to the Y-input. Trim the Y-offset adjust for minimum peak-to-peak output.

3. Apply 20V p-p to the Y-input and 0V to the X-input. Trim X-offset adjust for minimum peak-to-peak output.

4. Repeat step 1.

5. Apply +10V to both inputs and adjust scale factor for V_O = +10V. This step may be repeated with different amplitudes and polarities of input voltages to optimize accuracy over the entire range of input voltages, or over any specific portion of input voltage range.

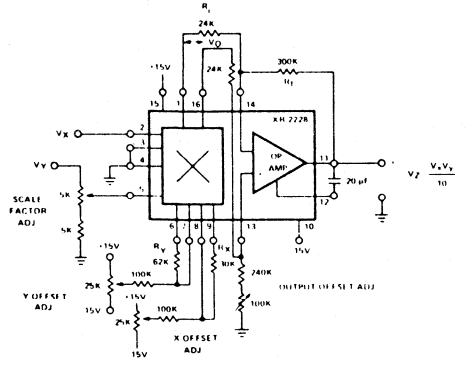


Figure 14. Multiplication Circuit

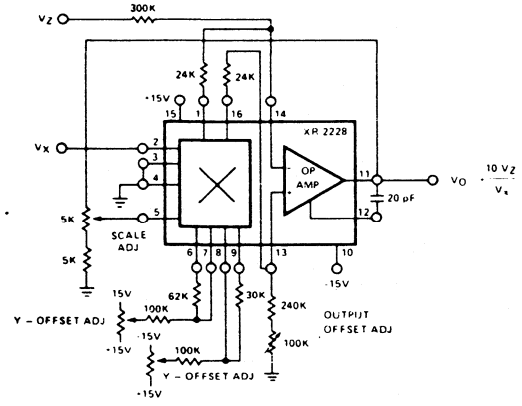


Figure 15. Dividing Circuit

DIVIDING CIRCUIT

Recommended circuit connection for performing analog division is shown in Figure 15. This circuit uses the multiplier in the feedback path of the op amp. For the circuit shown, $V_O = +10\ V_Z/V_X$ where $V_X < 0$ and V_Z can have either sign. Positive values of V_X are not allowed, since this will reverse the polarity of the feedback loop, causing positive feedback and latchup.

This latchup mode is nondestructive to the XR-2228, and is common to all analog division circuits. The divider circuit is trimmed as follows:

1. Apply V_Z = 0 and trim the output offset adjustment for constant output voltage as V_X is varied from −1V to −10V.

2. Keeping V_Z = 0, and applying V_X = −10V, time the Y-offset adjust until V_O = 0.

3. Let $V_Z = V_X$ and/or $V_Z = -V_X$ and trim the X-offset adjustment for constant output voltage as V_X is varied from −1V to −10V.

4. If step 3 requires a large initial adjustment, repeat steps 1, 2 and 3.

5. Keeping $V_Z = V_X$, adjust the scale factor trim for V_O = −10V as V_X is varied from −1V to −10V.

PART II: ANALOG SIGNAL PROCESSING

PHASE DETECTION

The multiplier section of the XR-2228 can be used as a linear phase-discriminator. A recommended circuit connection for this application is shown in Figure 16. In this case, the reference input (input 1) is applied to pin 2, and the input signal whose phase is to be detected (input 2) is applied to pin 5. For input signal amplitudes ≥50 mV rms, the differential output voltage, V_O across pins 1 and 16 is directly proportional to the phase difference, ϕ, between the two input signals. It can be expressed as

$$V_O(\phi) = 5\left(\frac{2\phi}{\pi} - 1\right)$$

Where ϕ is the phase difference expressed in radians. Even though the op amp is, in this application, not used, it is necessary to bias its inputs within their common mode range. This is easily accomplished in the phase detector circuit of pin 16 by tying pins 13 and 14 to pin 3 (which puts pins 13 and 14 at half supply).

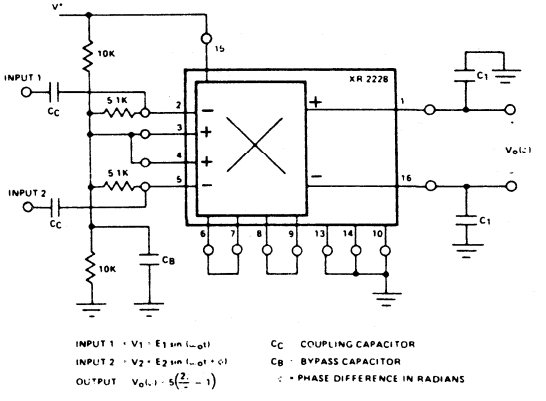


Figure 16. Phase-Detector Circuit

The capacitors C_1 at pins 1 and 16 provide a low-pass filter with a time constant $T_1 = R_1 C_1$, where $R_1 = 5$ kΩ is the international impedance level at these pins.

If needed, the phase conversion gain can be increased by using the op amp section of the XR-2228 to further amplify the output voltage, $V_O(\phi)$. The XR-2228 is suitable for phase detection of input frequencies up to 100 MHz.

SYNCHRONOUS AM DETECTION

Figure 17 is a typical circuit connection for synchronous AM detection for carrier frequencies up to 100 MHz. The AM input signal is applied to the multiplier X- and Y-input terminals (pins 3 and 4) simultaneously.

The Y-gain terminals (pins 6 and 7) are shorted, and this section of the multiplier serves as a "limiter" for input signals ≥50 mVrms; the X-section of the multiplier operates in its linear mode. The low-pass filter capacitors, C_1, and at pins 1 and 16 are used to filter the carrier feedthrough. If desired, the op amp section can be used as an audio preamplifier to increase the demodulated output amplitude.

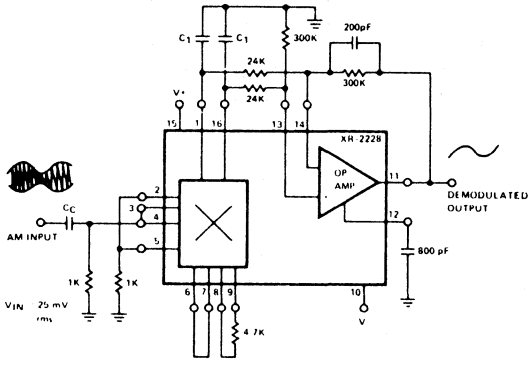


Figure 17. Synchronous AM Detector

PRECISION PHASE-LOCKED LOOP DESIGN

A precision phase-locked loop may be constructed using an XR-2209 voltage controlled oscillator and an XR-2228. (See Figure 18.) Due to the excellent temperature stability and wide sweep range of the XR-2209 this PLL circuit exhibits especially good stability of center frequency and wide lock range. In this application the XR-2228 serves as a phase comparator and level shifter. Resistor R_L adjusts the loop gain of the PLL, thus varying the lock range. Tracking range may be varied from about 1.5:1 up to 12:1. For large values of R_L, temperature stability of center frequency is better than 30 ppm/°C.

TRIANGLE-TO-SINEWAVE CONVERSION

A triangular input can be converted into a low distortion (THD < 1%) sinusoidal output with the XR-2228. A recommended connection for this application is shown in Figure 19. The triangle input signal is applied to the X-input (pin 2). The multiplier section rounds off the peaks of this input and converts it to a low distortion sine wave.

For the component values shown in Figure 19, the recommended input signal level at pin 2 is ≅300 mV pp, in order to obtain a 2V pp signal at pins 1 or 16, with R_X set at approximately 100Ω. The dc level at pin 5 can be used for adjusting the output amplitude, or providing amplitude modulation. The sensitivity of the output amplitude to the dc voltage level at pin 5 is inversely proportional to the external resistor across pins 6 and 7.

If higher amplitude output signal is required, the op amp section of XR-2228 can be used to provide additional amplification. If the op amp is not used, its inputs must be biased within common mode range to ensure proper device operation.

PHASE-LOCKED AM DETECTION

The XR-2228 can be used in conjunction with any one of the commercially available monolithic phase-locked loop (PLL) IC's to provide phase-locked AM detection. In this manner, frequency-selective detection capabilities of PLL circuits can be extended to AM signals.

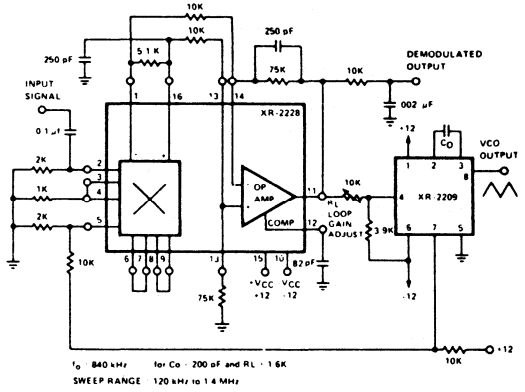


Figure 18. Precision PLL

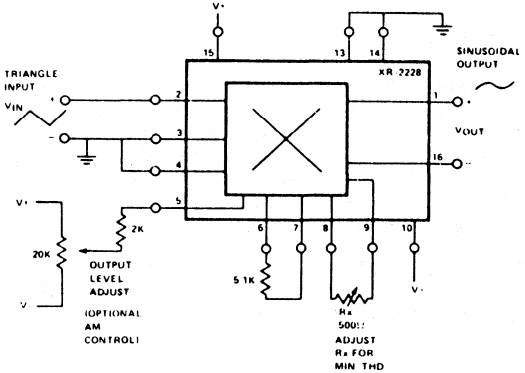


Figure 19. Triangle-to-Sinewave Converter

Figure 20 shows the circuit connection diagram for a two-chip AM and FM detection system, using the XR-215 high-frequency PLL in conjunction with the XR-2228 multiplier/detector. Because of the high-frequency capability of the XR-215, the circuit is useful as a phase-locked AM detector for carrier frequencies up to 20 MHz, and operates over a supply voltage range of 10V to 20V.

The VCO section of XR-215 does not have a separate "quadrature" output. However, this problem can be overcome by driving the XR-2228 multiplier directly from the timing capacitor terminals (pins 13 and 14) of XR-215. The Y-input of the XR-2228 is operated with maximum gain, since the Y-gain control terminals (pins 6 and 7) are shorted together. This causes the triangular waveform across the timing capacitor, C_0, to be converted to an effective "quadrature" drive.

The modulated input signal is simultaneously applied to both circuits through coupling capacitors. The phase-detector inputs of the XR-215, as well as the multiplier X-inputs of the XR-2228, are biased at approximated one-half of V_{CC}, by means of an external resistive divider.

In Figure 20, C_0 sets the VCO frequency of the XR-215. In the case of FM demodulation, R_1 and C_1 serve as the post-detection filter for the detected FM signal and R_{F1} sets the gain of the FM post-detection amplifier.

The Y-input of the XR-2228 is operated in its switching mode, with the Y-gain terminals (pins 6 and 7) shorted together. The AM and/or FM signal is simultaneously applied to both circuits through coupling capacitors; the output of the multiplier, at pin 16, is AC coupled to the op amp section of the XR-2228, which serves as the post-detection amplifier for the demodulated AM signal. In the circuit, R_X sets the amplifier demodulation gain, C_3 serves as the low-pass post-detection filter.

A detailed description of the circuit operation, and the design equations for calculating the external component values are given in Exar's Application Note AN-13, entitled "Frequency Selective AM Detection using Monolithic Phase-Locked Loops."

PHASE-LOCKED LOOP TONE DETECTION

The XR-2228 multiplier/detector can be used in conjunction with the XR-210 or the XR-215 high-frequency PLL circuits, to provide high-frequency tone or carrier-detect systems. The generalized circuit connection for such an application is given in Figure 21. The circuit, as shown, can operate with a single power supply, from 10V, to 20V, or with split supplies in the range of ±5V to ±10V. In the case of split power supplies, the resistor string biasing the input terminals of the XR-2228 is not necessary and can be eliminated by connecting node A of Figure 21 to ground.

The input signal is AC coupled, with separate coupling capacitors, both to the input of the particular PLL circuit to be used and to the X-input terminal (pin 2) of the XR-2228.

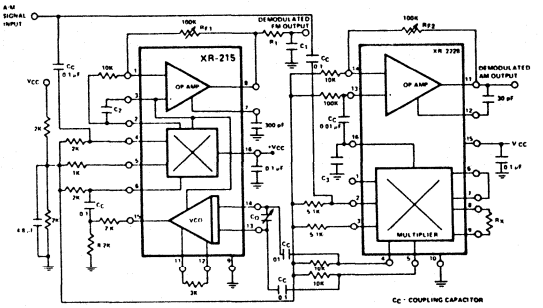


Figure 20. Phase-Locked AM Detection Using XR-215 Monolithic PLL and XR-2228 Multiplier/Detector

The Y-inputs (pins 4 and 5) are driven differentially from the VCO timing capacitor signal (available at pins 13 and 14 of the PLL IC) which is AC coupled to pins 4 and 5 of the XR-2228 multiplier input. the differential DC voltage level at the multiplier output terminals (pins 1 and 16) is offset by means of an external resistor, R_A. This initial offset causes the op amp output of the XR-2228 to settle to a known state when there is no carrier or tone signal to be detected. With the op amp input connections as shown in Figure 21, the op amp output (pin 11) would be at a "low" state when the PLL is not locked on a tone, and goes to a "high" state (i.e., near $+V_{CC}$) when the PLL circuit is "locked" on to an input tone. The output logic polarity can be reversed simply by reversing the op amp inputs.

The filter capacitor, C_A, connected across pins 1 and 16 of the multiplier outputs, serves as the post-detection low-pass filter. The value of C_A is chosen to provide a compromise between the response time and the spurious noise rejection characteristics of the circuit: increasing C_A improves the noise rejection characteristics of the circuit, but slows down the response time.

A detailed description of the principle of operation of the circuit of Figure 21 is given in Exar's Application Note AN-12 entitled: "Designing High Frequency Phase-Locked Loop Carrier-Detector Circuits".

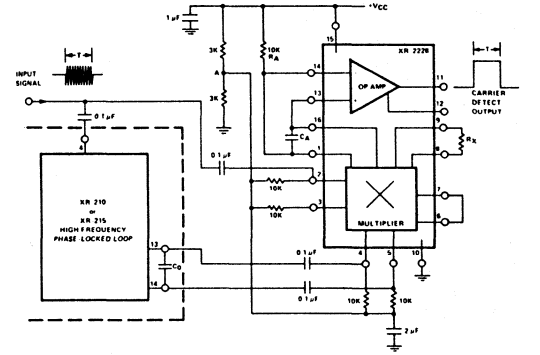


Figure 21. Recommended Circuit Connection of the XR-2228 with the XR-210 or the XR-215 High-Frequency Phase-Locked Loops for Tone or Carrier-Detector Application

Multi-Function PLL System

GENERAL DESCRIPTION

The XR-S200 integrated circuit is a highly versatile, multipurpose circuit that contains all of the essential functions of most communication system designs on a single monolithic substrate. The function contained in the XR-S200 include: 1. a four quadrant analog multiplier, 2. a high frequency voltage controlled oscillator (VCO) and 3. a high performance operational amplifier.

The three functions can be used independently, or directly interconnected in any order to perform a large number of complex circuit functions, from phase-locked loops to the generation of complex waveforms. The XR-S200 can accommodate both analog and digital signals, over a frequency range of 0.1 Hz to 30 MHz, and operate with a wide choice of power supplies extending from ±2.5 Volts ± 13 Volts.

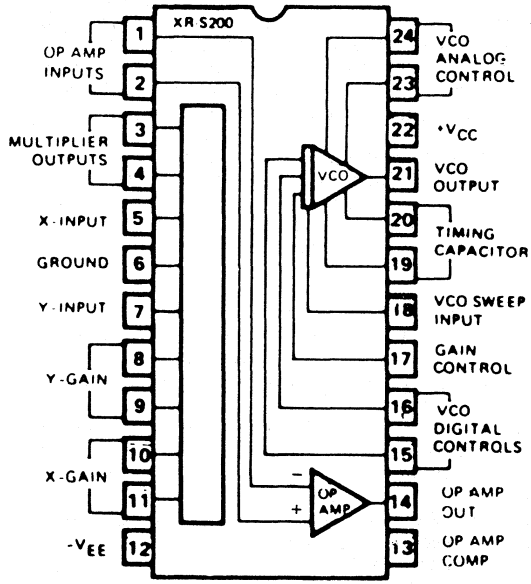
FEATURES

Wide VCO Frequency Range	0.1 Hz to 30 MHz
Wide Supply Voltage Range	±2.5 V ± 13 V
Uncommitted Inputs and Outputs for Maximum Flexibility	
Large Input Dynamic Range	

APPLICATIONS

Phase-locked loops
FM demodulation
  Narrow and wideband FM
  Commercial FM-IF
  TV sound and SCA detection
FSK detection (MODEM)
PSK demodulation
Signal conditioning
Tracking filters
Frequency synthesis
Telemetry coding/decoding
AM detection
  Quadrature detectors
  Synchronous detectors
Linear sweep & AM generation
  Suppressed carrier
  Double sideband
Tone generation/detection
Waveform generation
  Single/square/triangle/sawtooth
Analog multiplication

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply	30 Volts
Power Dissipation	900 mW
Derate above +25°C	9 mW/°C
Temperature	
Operating	0° to +70°C
Storage	−65°C to +150°C
Input Signal Level, V_S	6 V,p-p

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-S200	24 Pin Ceramic Dip	0° to +70°C

ELECTRICAL SPECIFICATIONS

T_A = 25C, VSUPPLY = ±10V, unless otherwise indicated.

PARAMETERS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
GENERAL CHARACTERISTICS						
I_{CC}	Positive Supply Current			18	mA	
I_{EE}	Negative Supply Current	-18			mA	
V_{CC}	Positive Supply Voltage Range					
	Single Supply	5	20	26	V	
	Split	2.5	10	13	V	V_{EE} = -2.5 to -13V
V_{EE}	Negative Supply Voltage Range	-13	-10	2.5	V	V_{CC} = +2.5 to + 13V
MULTIPLIER SECTION: See figure 2, $R_x = R_y$ = 15k, Pins 1, 2, 6, 23, 24 grounded.						
V_{OO}	Output Offset Voltage		±40	±120	mV	$V_x = V_y = 0$, $V_{io} = V_3 - V_4$
I_{BC}	Input Bias Current		5	15	µV	Measured at pins 5 and 7
I_{IO}	Input Offset Current		0.1	1.0	µV	Measured at pins 5 and 7
	Linearity (output error, %		1.0		%	-5 < V_x < +5, V_y = ±5V
	of full scale)		1.5		%	-5 < V_y < +5, V_x = ±5V
K_M	Scale Factor		0.1		-	$K_M = 25/R_xR_y$ (Adjustable)
R_W	Input Resistance	0.3	1.0		MΩ	f = 20HzMeasured at pins 5 and 7
B_W	3 dB Bandwidth	3	6		MHz	$C_L \leq 5$ pF
0	Phase detection B. W.	50	100		MHz	$R_x = R_y = 0$
B_W	Differential Output Swing	±4	±6		V p--p	Measured across pins 3 and 4
Z_O	Output Impedance					
	Single Ended		6		kΩ	Measured across pins 3 and 4
	Differential		12		kΩ	
OPERATIONAL AMPLIFIER SECTION: See figure 10, R_L = 20k, C_L = 550 pF.						
I_{IB}	Input Bias Current		0.08	0.5	µA	
I_{IO}	Input Offset Current		0.02	0.2	µA	
V_{IO}	Input Offset Voltage		1.0	6.0	mVdc	
	Differential Input Impedance					Open loop, f = 20 Hz
	Resistance	0.4	2.0		MΩ	
	Capacitance		1.0		pF	
CMR	Common Mode Range		±8		V	
CMRR	Common Mode Rejection	70	90		dB	f = 20 Hz
	Open Loop Voltage Gain	66	80		dB	
Z_O	Output Impedance		2		kΩ	
	Output Voltage Swing	±7	±9		V	$R_L \geq 20$ kΩ
	Power Supply Sensitivity		30		µV/V	$R_S \leq 10$ kΩ
S_R	Slew Rate		2.5		V/µsec	A_V = 1, C_L = 10 pF

5

ELECTRICAL SPECIFICATIONS

T_A = 25C, VSUPPLY = ±10V, unless otherwise indicated. (Cont.)

	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
VCO SECTION: See figure 11, R_L = 10k f_o = MHz.						
	Upper Frequency Limit	15	30		MHz	C_o = 10 pF
	Sweep Range	8:1	10:1		-	f_o = 10 kHz, See figure 14 Digital Controls Off
	Linearity (distortion for $\Delta f/f$ = 10%)		.2	1.0	%	Digital Controls Off
	Frequency Stability					V_{CC} > 8V, f_o 1 MHz
	Power Supply		0.08	0.5	%/V	Sweep Input Open
	Temperature		300	650	ppm/°C	Not tested in production
Z_{AI}	Analog Input Impedance					Measured at pins 23 and 24
	Resistance	0.1	0.5		MΩ	
	Capacitance		1.5		pF	
	Output Amplitude		3		V p--p	Squarewave
	Output Rise Time		15		ns	C_L = 10 pF, R_L = 5 kΩ
	Fall Time		30		ns	
CMR	Input Common Mode Range	+6	+8		Vdc	
		-4	-6		Vdc	

CAUTION: When using only some of the blocks within the XR-S200, the input terminals to the unused section must be grounded (for split-supply operation); or connected to an AC ground biased at V+/2 (for single supply operation).

XR-S200 ANALOG MULTIPLIER SECTION

The analog multiplier in the XR-S200 (Figure 2) provides linear four-quadrant multiplication over a broad range of input signal levels. It also serves as a balanced modulator, phase comparator, or synchronous detector. Gain is externally adjustable. Nonlinearity is less than 2% of full scale output.

TYPICAL APPLICATIONS OF MULTIPLIER SECTION

- Analog multiplication/division
- Phase detection
- Balanced modulation/demodulation
- Electronic gain control
- Synchronous detection
- Frequency doubling

ANALOG MULTIPLICATION

The XR-S200 multiplier section can be combined with the amplifier section to perform analog multiplication without the need for dc level shifting between input and output. The amplifier functions as an operational amplifier with a single-ended output at ground level when connected as shown in Figure 3.

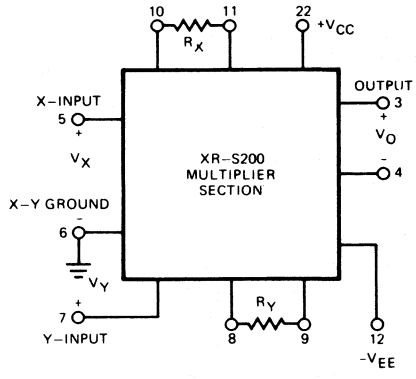


Figure 2. XR-S200 Multiplier Section

PHASE COMPARATOR

For phase comparison, a low-level reference signal is normally applied to one input and a high-level reference or carrier signal to the other input, as in Figure 4. The signal may be applied to either the X or Y input, since the response is symmetrical.

If the two inputs, $V_R(t)$ and $V_S(t)$ are at the same frequency, then the dc voltage at the output of the phase comparator can be related to the phase angle ϕ between the two signals as

$$V_\phi = K_\phi \cos\phi$$

where K_ϕ is the conversion gain in volts per radian (Figure 5). For phase comparator applications, one input is

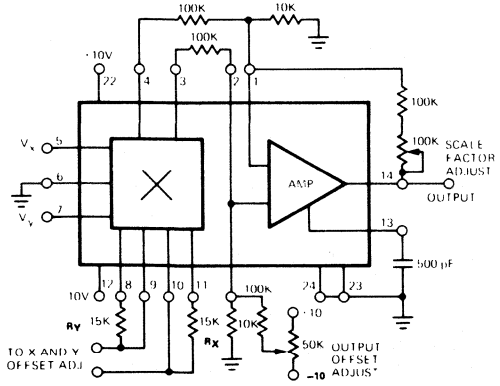


Figure 3. Analog Multiplication

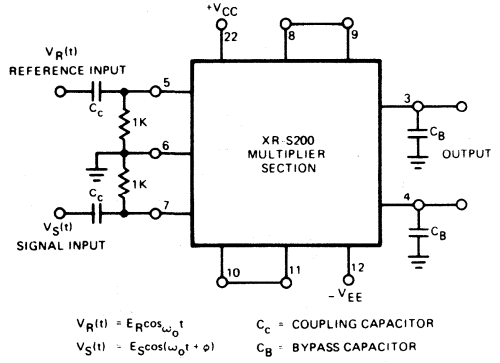


Figure 4. XR-S200 Multiplier Section as a Phase Comparator

normally a high level reference signal and the other input a low level information signal. Since the XR-S200 multiplier section offers symmetrical response with respect to the X and Y inputs, either input can be used as the carrier or signal input. For low input levels, the conversion gain is proportional to the input signal amplitude. For high level inputs, (V_S > 40 mV, rms) K_ϕ is constant and approximately equal to 2V/rad.

SUPPRESSED-CARRIER AM

The multiplier generates suppressed-carrier AM signals when connected as in Figure 6. Again, the symmetrical response allows the X or Y inputs to be used interchangeably as the carrier or modulation inputs. The X and Y offset adjustments optimize carrier suppression. Gain control resistors R_X and R_Y typically range from 1 KΩ to 10 KΩ, depending on input signal amplitudes. The values shown give approximately 60 dB carrier suppression at 500 kHz and 40 dB at 10 MHz.

DOUBLE-SIDEBAND AM GENERATION

The connection for double-sideband AM generation is shown in Figure 7. The dc offset adjustment on the modulation input terminal sets the carrier output level, while the dc offset of the carrier input governs symmetry of the output waveform. The modulation input can also be used as a linear gain control (AGC), to control amplification with respect to the carrier input signals.

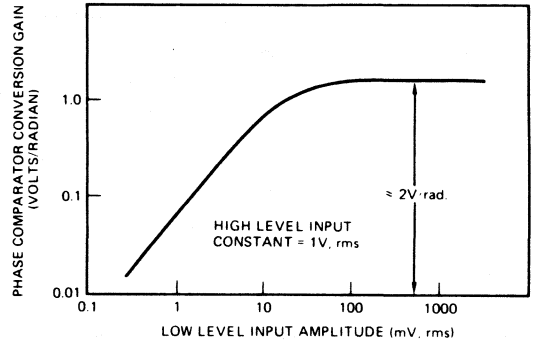


Figure 5. Phase Comparator Conversion Gain Versus Input Amplitude

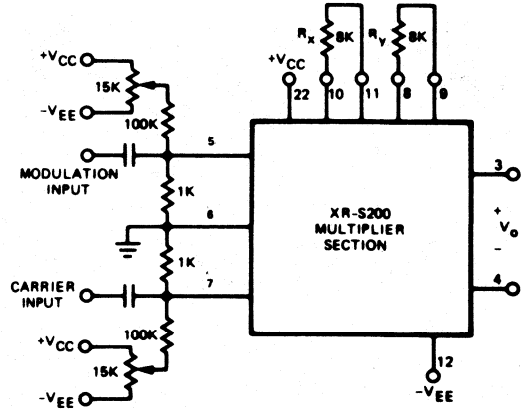


Figure 6. Suppressed Carrier Modulation Using XR-S200 Multiplier Section

FREQUENCY DOUBLING

Figure 8 shows how to double a sinusoidal input signal of frequency f_S to produce a low-distortion sinewave output of $2f_S$. Total harmonic distortion is less than 0.6% with an input of 4V, p-p, at 10 kHz and an output of 1V, p-p, at 20 kHz. The multiplier's X and Y offsets are nulled as shown to minimize the output's harmonic content.

SYNCHRONOUS AM DETECTION

A typical synchronous AM detector is shown in Figure 9. The signal is applied to the multiplier common input and the X and Y inputs are grounded. Since the Y input

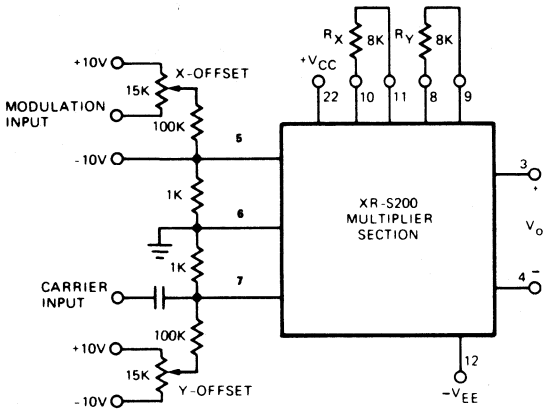


Figure 7. Double Sideband Amplitude Modulation Using XR-S200 Multiplier Section

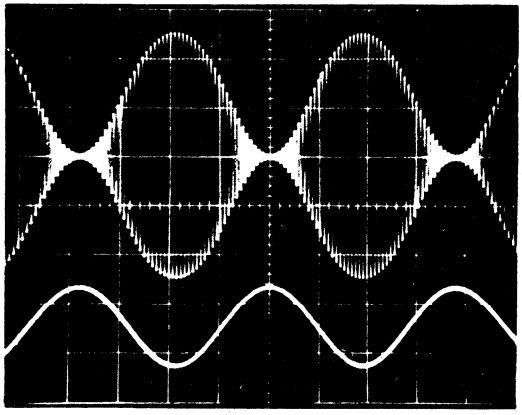


Figure 7-1. AM Modulation, 95% AM, f_c = 50 kHz, f_m = 1 kHz

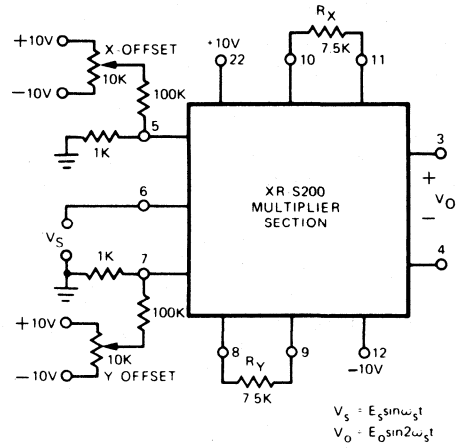


Figure 8. Multiplier Section as Frequency Doubler

operates at maximum gain with R_Y = 0, the detector gain and demodulated output linearity are determined by R_X. An R_X range of 1 KΩ to 10 KΩ is recommended for carrier amplitudes of 100 mV, p-p; or greater. The multiplier output can be low-pass filtered to obtain the demodulated output. Figure 9-1 shows the carrier and modulated waveforms for a 30% modulated input signal with a 10 MHz carrier and 1 kHz modulation.

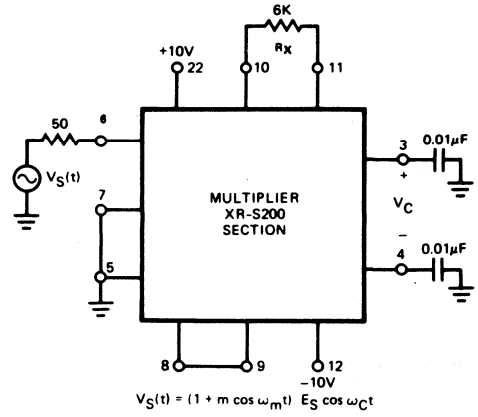


Figure 9. Synchronous AM Detector

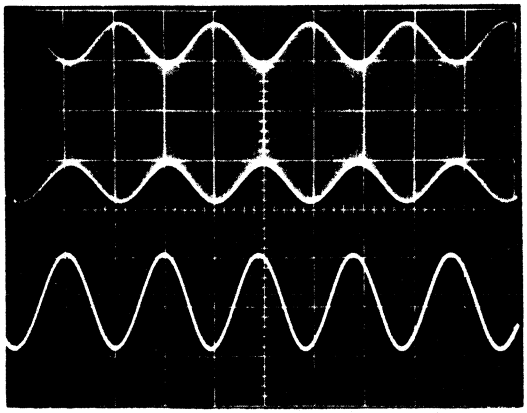


Figure 9-1. Synchronous AM Demodulation

XR-S200 AMPLIFIER SECTION

This multi-purpose function (Figure 10) can be used as a general-purpose operational amplifier, high-speed comparator, or sense amplifier. It features an input impedance of 2 megohms, high voltage gain, and a slew rate of 2.5V/microsecond. The frequency response curves for the amplifier section are also shown in Figure 10.

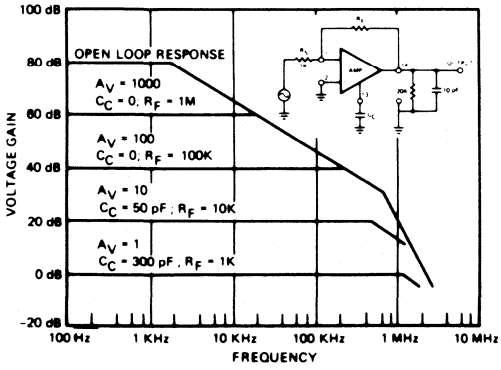


Figure 10. Amplifier Section Frequency Response

XR-S200 OSCILLATOR SECTION

The voltage-controlled oscillator section, (Figure 11) is an exceptionally versatile design capable of operating from a fraction of a cycle to in excess of 30 MHz. Frequencies can be selected and controlled by three methods, and used in various combinations for different applications:

1. External timing capacitor C_0 tunes the VCO to a center frequency between 0.1 Hz and 30 MHz. The free-running frequency is inversely proportional to C_0. (see Figure 12)

2. Two digital control inputs allow four discrete frequencies to be selected at any cer..er frequency. The digital inputs convert the logic signal voltages to internal control currents. (see Figure 13)

3. A sweep voltage, applied through a limiting resistor R_S is used for frequency sweeping, on-off keying, and synchronization of the VCO to a sync pulse. (see Figure 14)

The voltage-to-frequency conversion of the VCO section is highly linear. In addition, the conversion gain can be controlled through the analog control input. Gain is inversely proportional to R_0. When the digital controls are also used, gain decreases as the frequency is stepped up.

The VCO interfaces easily with ECL or TTL logic. It can be converted to a highly stable crystal-controlled oscillator by simply substituting a crystal in place of the timing capacitor, C_0.

Typical performance characteristics of the VCO section are shown in Figures 12, 13, and 14.

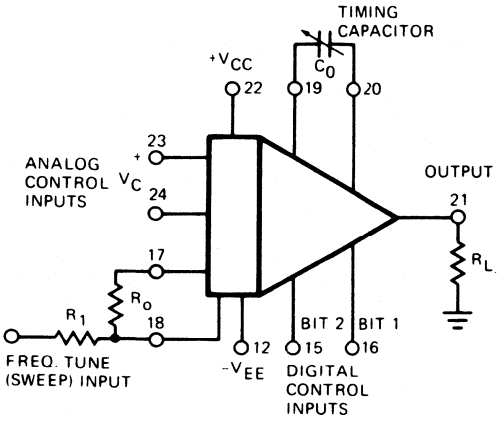


Figure 11. XR-S200 Oscillator Section

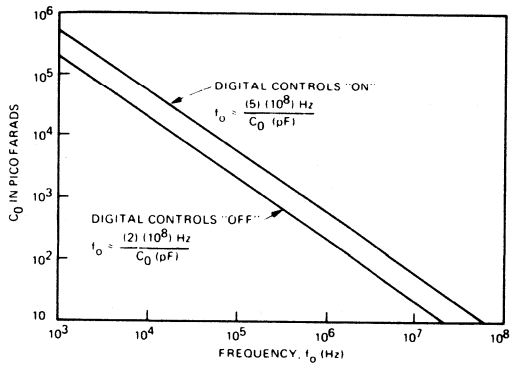


Figure 12. VCO Frequency as a Function of Timing Capacitor, C_0

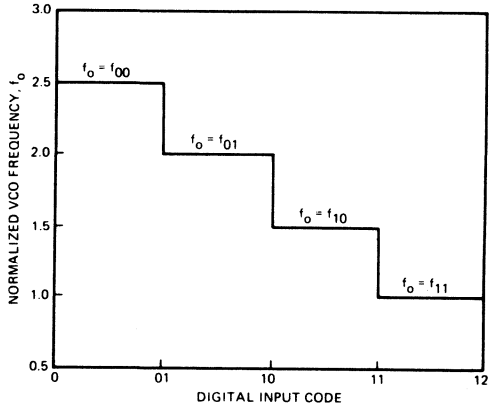


Figure 13. VCO Digital Tuning Characteristics

EXPLANATION OF VCO DIGITAL CONTROLS

The VCO frequency is proportional to the total charging current, I_T, applied to the timing capacitor. As shown in Figure 15, I_T is comprised of three separate components: I_0, I_1, and I_2, which are contributed by transistors T_0, T_1, and T_2, respectively. With pins 15 and 16 open circuited, these currents are interrelated as

$$I_0 = I_1 = 2I_2$$

Currents $I_1$and I_2 can be externally controlled through pins 16 and 15 respectively. By increasing the dc level at either of these pins, T_1 or T_2 can be turned "off" and I_1 or I_2 can be reduced to zero. With reference to Figure 15, this can be done by applying a 3 volt logic pulse to these pins, through disconnect diodes D_1 and D_2. In this manner, the VCO frequency can be stepped in four discrete intervals, over a frequency range of 2.5:1, as shown in Figure 13.

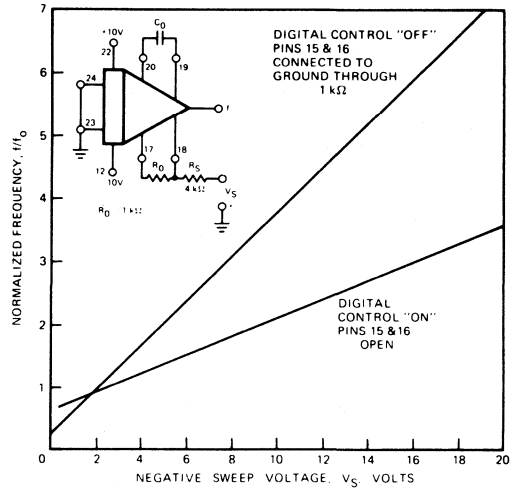


Figure 14. Voltage Sweep Characteristics

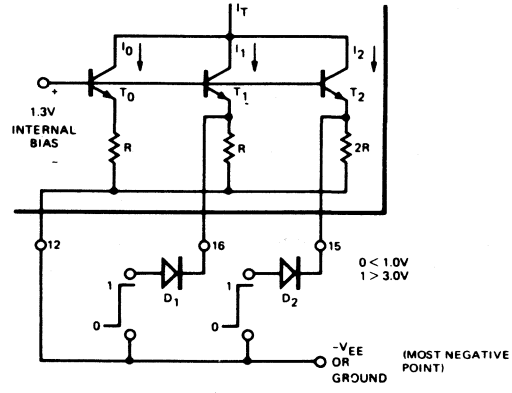


Figure 15. Explanation of VCO Digital Controls

TYPICAL APPLICATIONS OF VCO SECTION

- Voltage/frequency conversion
- Phase-locked loops
- Frequency synthesis
- Signal conditioning
- Carrier generation
- Synchronization
- Sweep and FM generator
- Crystal oscillator
- Waveform generator
- Keyed oscillator

APPLICATIONS OF THE XR-S200 SYSTEM

PHASE-LOCKED LOOP

A self-contained phase-locked loop is formed by connecting the XR-S200 as outlined in Figure 16.

In most PLL applications, the amplifier is available for functions useful outside the loop, since the phase comparator (multiplier section) and VCO provide sufficient conversion gain. In this case, the amplifier gain does not enter the PLL gain expression. Assuming unity dc gain for the filter, the PLL loop gain is $K_T = K_\phi K_0$ where K_ϕ and K_0 are the multiplier and VCO conversion gains, respectively.

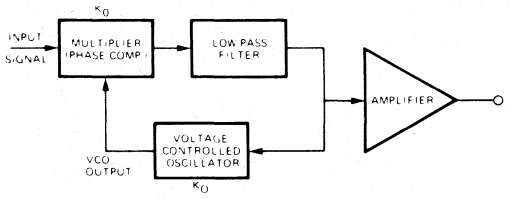


Figure 16. XR-S200 as a Phase-Locked Loop

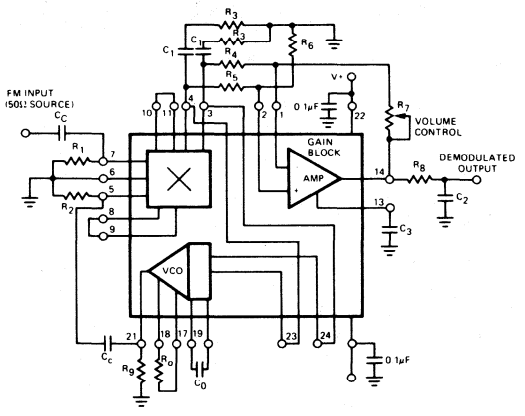


Figure 17. Circuit Connection for FM Detection

FREQUENCY-SELECTIVE FM DEMODULATION

For FM demodulation, the PLL connection is used (Figure 17.) The multiplier, with its gain terminals shorted, serves as the phase detector, and the VCO and filter govern the operating frequencies.

The gain block is used as an audio preamplifier to set the demodulated output signal level. Volume is controlled by the variable feedback resistor R_7. If R_6 equals R_7, the dc output level will be very close to ground, for circuit operation with split power supplies. C_3 is the amplifier's compensation capacitor. R_8 and C_2 set the output de-emphasis time constant T_D, which is normally 75 μsec. for commercial FM applications (f_o = 10.7 MHz).

FSK DETECTION

FSK signals are detected and demodulated with the PLL connection, as well. It is shown in Figure 18 as a monolithic MODEM suitable for Bell 103 or 202 type data sets operating at data rates to 1800 baud. An input frequency shift corresponding to a data bit causes the multiplier's dc voltage output to reverse polarity. The dc level is changed to a binary output pulse by the gain block, connected as a voltage comparator.

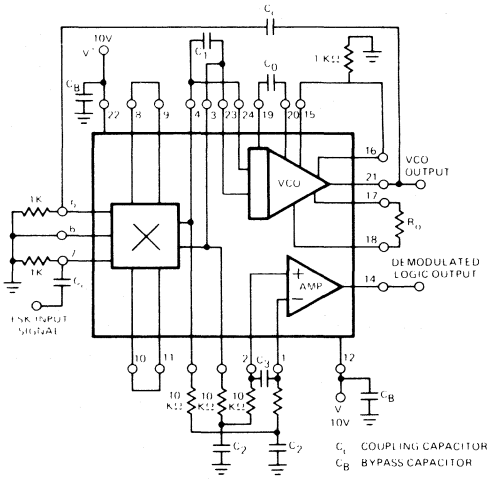


Figure 18. FSK Detection

FREQUENCY SYNTHESIZER

Frequency synthesis is performed in Figure 19 by a phase-locked loop closed with a programmable counter or digital divide-by-N circuit inserted into the feedback loop. The VCO frequency is divided by N, so that when the circuit locks to an input signal at frequency f_S, the

oscillator output is Nf_S. A large number of discrete frequencies can be synthesized from a given reference frequency by changing N.

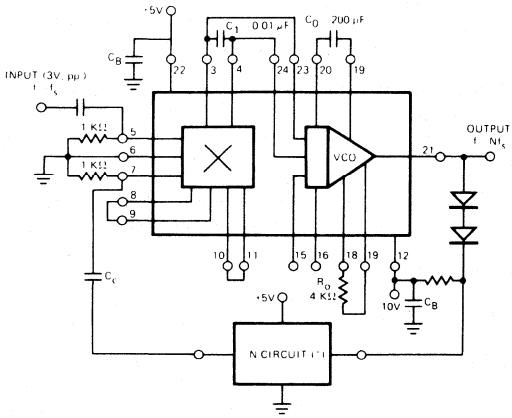


Figure 19. Frequency Synthesizer

TRACKING FILTER AND WIDEBAND DISCRIMINATOR

In tracking filter applications, the XR-S200 again forms a PLL system (Figure 20). When the PLL locks on an input signal, it functions as a "frequency-filter" and produces a filtered version of the input signal frequency at the VCO output. Since it can track the input over a broad range of frequencies around the VCO free-running frequency, it is also called a "tracking filter". The system can track input signals over a 3:1 frequency range.

WAVEFORM GENERATOR

The XR-S200 can also be interconnected to form a versatile waveform generator. The typical circuit shown in Figure 21 generates the basic periodic square (or sawtooth) waveform. The multiplier section, connected as a linear differential amplifier, convert the differential sawtooth waveform input into a triangle wave output at pins

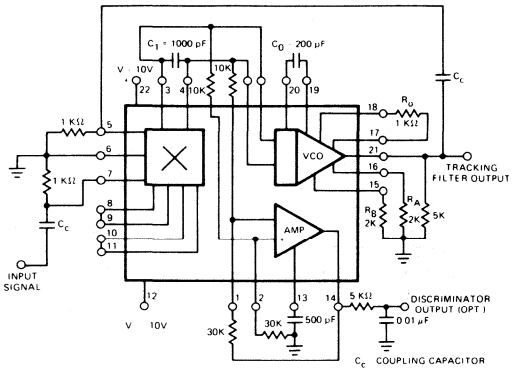


Figure 20. Recommended Circuit Connection for Tracking Filter Application (f_0 = 1 MHz)

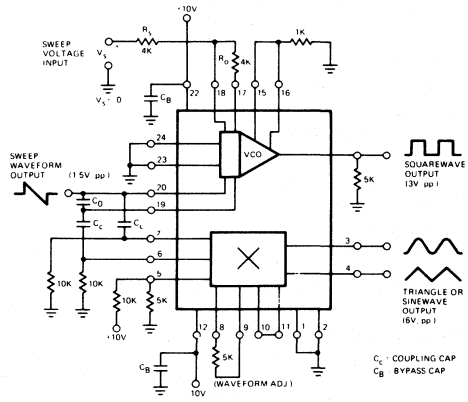


Figure 21. Waveform Generator Typical Circuit Connection Diagram

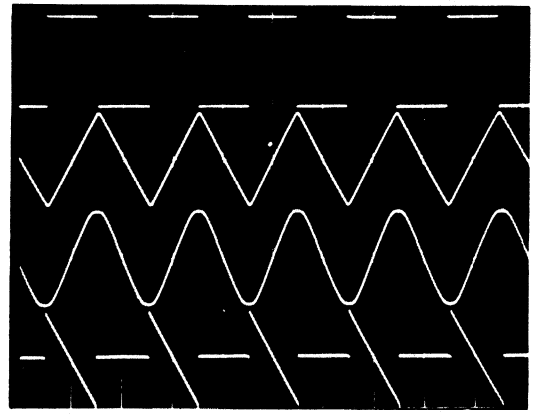


Figure 21-1. Basic Waveforms Available from XR-S200

3 and 4. The waveform adjustment pot across pins 8 and 9 can be used to round the peaks of the triangle waveform and convert it to a low distortion sinewave (THD < 2%). Terminals 3 and 4 can be used either differentially or single endedly to provide both in-phase and out-of-phase output waveforms.

The output frequency can be swept or frequency modulated by applying the proper analog control input to the circuit. For linear FM modulation with relatively small frequency deviation ($\Delta f/f < 10\%$) the modulation input can be applied across terminals 23 and 24. For large deviation sweep inputs, a negative going sweep voltage, V_S, can be applied to pin 18.

This allows the frequency to be voltage-tuned over approximately a 10:1 range in frequency. The digital control inputs (15 and 16) can be used for frequency-shift-keying (FSK) applications. They can be disabled by connecting them to ground through a current-limiting resistor.

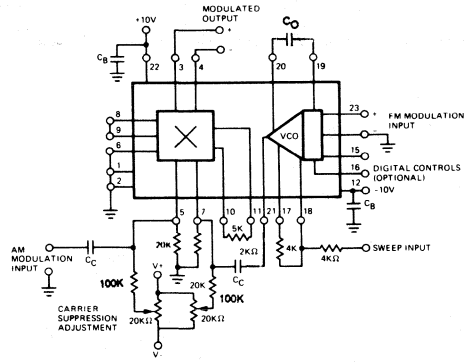


Figure 22. Circuit Connection for AM/FM AM Generator Application

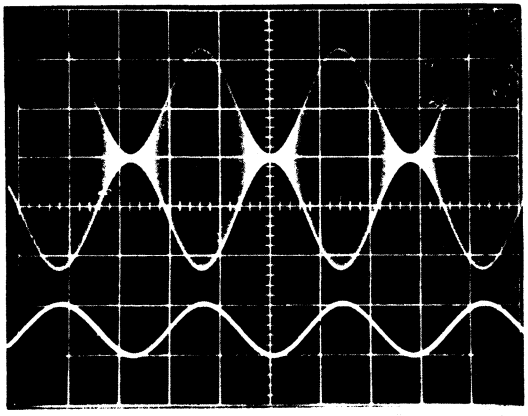


Figure 22-1. Double Sideband AM Output Waveform $f_{carrier}$ = 3.688 MHz f_{mod} = 1 kHz (90% modulation)

AM & FM SIGNAL GENERATION

The oscillator and multiplier sections can be interconnected as a general purpose radio-frequency signal generator with AM, FM and sweep capability as shown in Figure 22.

The oscillator section can be used as a voltage-tuned, variable frequency oscillator. The multiplier section introduces the amplitude modulation on the carrier signal generated by the VCO. The balanced nature of the multiplier allows suppressed carrier as well as double sideband modulation (Figures 22-1 and 22-2). Typical carrier suppression is in excess of 40 dB for frequencies up to 10 MHz.

If a timing capacitor is used, the oscillator section can provide highly linear FM or Frequency sweep. The digital control terminals of the oscillator are used for frequency-shift-keying.

The XR-S200 is not recommended for use as a crystal oscillator.

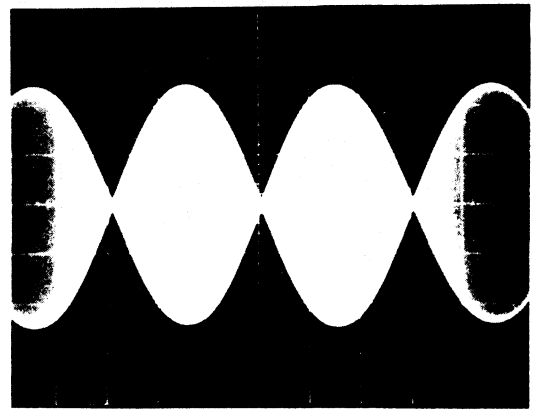
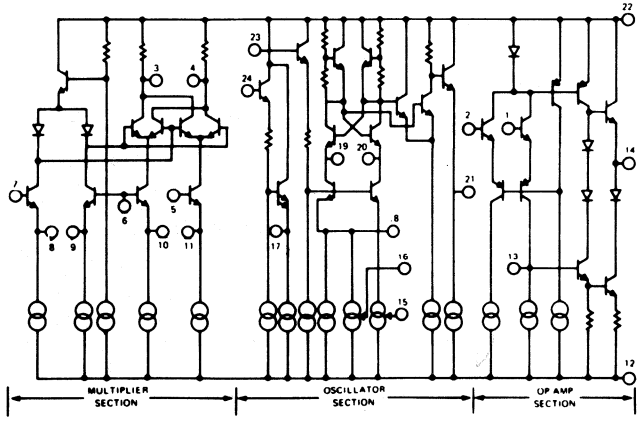


Figure 22-2. Suppressed Carrier AM Output Waveform $f_{carrier}$ = 3.688 MHz f_{mod} = 1 kHz



EQUIVALENT SCHEMATIC DIAGRAM

Monolithic Waveform Generator

GENERAL DESCRIPTION

The XR-205 is a highly versatile, monolithic waveform generator designed for diverse applications in communication and telemetry equipment, as well as in systems design and testing. It is a self-contained, totally monolithic signal generator that provides sine, square, triangle, ramp and sawtooth output waveforms, which can be both amplitude and frequency modulated.

The circuit has three separate sections: a voltage-controlled oscillator (VCO) which generates the basic periodic waveforms; a balanced modulator which provides amplitude or phase modulation; a buffer amplifier section which provides a low impedance output with high current drive capability.

FEATURES

High Frequency Operation
AM and FM Capabilities
Sine, Triangle, Square, Sawtooth, Ramp and Pulse Waveforms
Wide Supply Range 8 V to 26 V
Split Supply Capability

APPLICATIONS

Waveform Generation

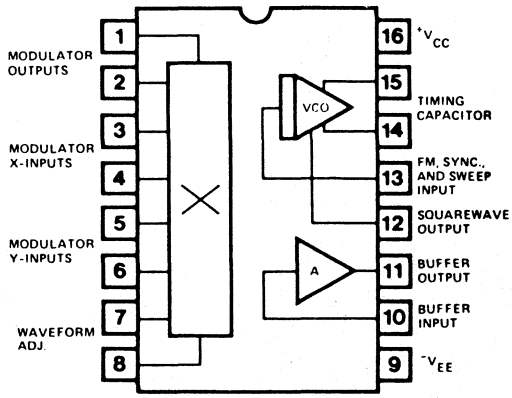
Sinewave	Sawtooth
Triangle	Ramp
Square	Pulse

AM Generation Double Sideband Suppressed Carrier
FM Generation
Sweep Generation
Tone Burst Generation
Simultaneous AM/FM
Frequency-Shift Keyed (FSK) Signal Generation
Phase-Shift Keyed (PSK) Signal Generation
On-Off Keyed Oscillation
Clock Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 Volts
Power Dissipation	750 mW
Derate above +25°C	6 mW/°C
Temperature	
Storage	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-205	Ceramic	0°C to + 70°C

SYSTEM DESCRIPTION

The XR-205 is a high frequency monolithic function generator capable of sine, square, triangle, ramp, sawtooth, and pulse waveforms with frequencies ranging to 4 MHz. Operating frequency is determined by a single capacitor and may be externally swept over a 10:1 range. Duty cycle is variable from 10% to 90%. Amplitude modulation, up to 100%, is accomplished using the modulator X inputs (Pins 3 and 4). The on board buffer amplifier features 50Ω output resistance and 20 mA output capability. The XR-205 operates with either single or split supplies.

ELECTRICAL CHARACTERISTICS

Test Conditions: Supply Voltage = 12V (single supply) T_A = 25°C, f - 10 kHz, R_L = 3 kΩ, unless otherwise specified.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
I — General Characteristics					
Supply Voltage:					
Single Supply	8		26	Vdc	See Figure 1
Split Supply	±5		±13	Vdc	See Figures 2 and 3
Supply Current	8	10	12	mA	w/o buffer amp
Frequency Stability:					
Power Supply		0.2	0.5	%/V	$\|V_{CC} - V_{EE}\| > 10V$
Temperature		300	600	ppm/°C	Sweep input open circuit
Frequency Sweep Range	7:1	10:1			See Figure 7
Output Swing:					
Single Ended	2	3		Vpp	Measured at pin 1 or 2
Differential	4	6		Vpp	Measured across 1 and 2
Output Diff. Offset Voltage		0.1	0.4	Vdc	Measured across 1 and 2
Amplitude Control Range		60		dB	Controlled by R_Q (see Figure 1)
Buffer Amplifier Output Resistance		50		ohms	R_L = 750Ω
Output Current Swing	±6	±10		mA	
II — Output Waveforms					
Sinusoidal:					
Upper Frequency Limit	2	4		MHz	Measured at Pin 11
Peak Output Swing	2	3		Vpp	S_1, S_3 closed, S_2 open
Distortion (THD)		2.5	4	%	closed S_2 open
Triangle:					
Peak Swing	2	4		Vpp	Measured at Pin 11
Non-Linearity		±1		%	S_1, S_2 open, S_3 closed
Asymmetry		±1		%	f = 10 kHz
Sawtooth:					
Peak Swing	2	3		Vpp	See Figure 1, S_2 closed;
Non-Linearity		1.5		%	S_2 and S_3 closed
Ramp:					
Peak-Swing	1	1.4		Vpp	See Figure 1, S_2 and S_3 open
Non-Linearity		1		%	pin 10 connected to pin 15
Squarewave (Low Level):					
Output Swing	0.5	0.7		Vpp	See Figure 1, S_2 and S_3 open,
Duty Cycle Asymmetry		±1	±4	%	pin 10 connected to pin12
Rise Time		20		ns	10 pF connected from pin 11
Fall Time		200		ns	to ground
Squarewave (High Level):					
Peak Swing	2	3		Vpp	See Figure 3, S_2 open
Duty Cycle Asymmetry		±1	±4	%	
Rise Time		80		ns	10 pF connected from pin 11
Fall Time		60		ns	to ground
Pulse Output:	2	3		Vpp	See Figure 3, S_2 closed
Peak Swing	2	3		Vpp	See Figure 3, S_2 closed
Rise Time		80		ns	
Fall Time		60		ns	
Duty Cycle Range		20-80		%	Adjustable (see Figure 6)
III — Modulation Characteristics (sine, triangle and squarewave):					
Amplitude Modulation:					
Double Sideband					
Modulation Range		0-100		%	See Figure 2 S3 closed
Linearity		0.5		%	for 30% modulation
Sideband Symmetry		1.0		%	
Suppressed Carrier					
Carrier Suppression		52		dB	f < 1 MHz after Rq adjustment
Frequency Modulation:					
Distortion		0.3		%	See Figure 2 (±10 frequency deviation)

5

TEST CIRCUITS

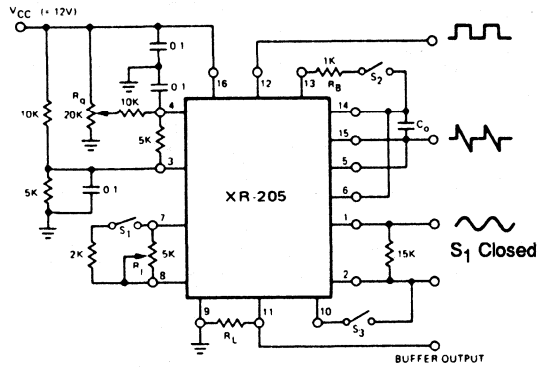


Figure 1. Test Circuit for Single-Supply Operation

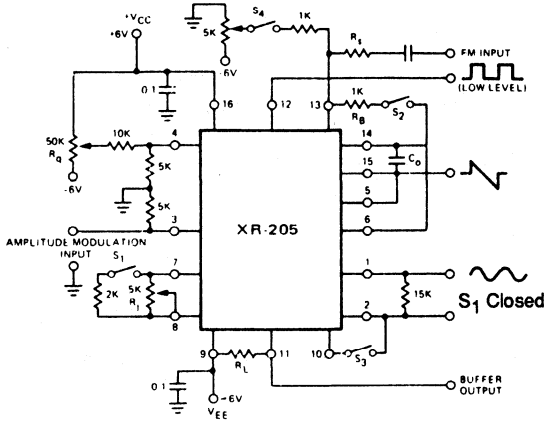


Figure 2. Test Circuit for Split-Supply Operation and AM/FM Modulation

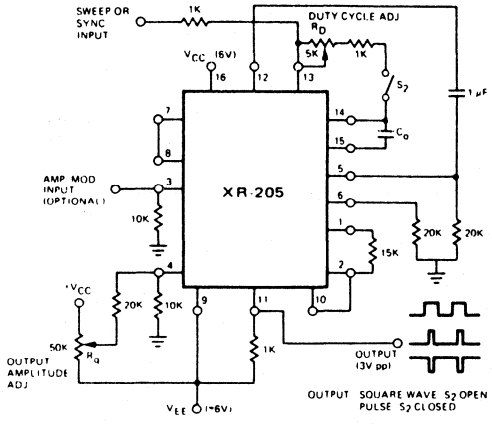


Figure 3. Test Circuit for High-Level Pulse and Squarewave Output

DESCRIPTION OF CIRCUIT CONTROLS

(Refer to functional block diagram)

TIMING CAPACITOR (PINS 14 AND 15)

The oscillator frequency is inversely proportional to the value of the timing capacitor, C_O, connected between pins 14 and 15. With the sweep input open circuited, frequecy f_O can be approximated as: $f_O = 400/C_O$ where f_O is in Hz and C_O is in microforads. (See Figure 4.)

MODULATOR Y-INPUTS (PINS 5 AND 6)

These inputs are normally connected to the oscillator outputs. For sinewave or trianglewave outputs, they are dc coupled to pins 14 and 15 (see Figure 1); for high-level squarewave or pulse output, ac coupling is used as shown in Figure 3.

MODULATOR X-INPUTS (PINS 3 AND 4)

Modulator output (at pins 1 or 2) is proportional to a dc voltage applied across these inputs - (see Figure 5). These inputs can be used for amplitude modulation or, as an output amplitude control. The phase of the output voltage is reversed if the polarity of the dc bias across pins 3 and 4 is reversed; therefore these inputs can be used for phase-shift keyed (PSK) modulation.

MODULATOR OUTPUTS (PINS 1 AND 2)

All of the high level output waveforms are obtained at these terminals. The output waveforms appear differentially between pins 1 and 2. The terminals can, therefore, be used for either in-phase or out-of-phase outputs. Normally, a 15KΩ load resistor should be connected between these terminals to prevent the output from saturating or clipping at large output voltage swings. This output has a high output impedance and should be buffered.

LOW LEVEL SQUAREWAVE OUTPUT (PIN 12)

The output at this pin is a symmetrical squarewave with 0.7V amplitude and 20 ns rise time. It can be used directly as an output waveform, or amplified to a 3 Vpp signal level using the modulator section of the XR-205 as an amplifier (see Figure 3).

SWEEP OR FM INPUT (PIN 13)

The oscillator frequency increases linearly with an increasing *negative* voltage, V_S, applied to this terminal. Normally a series resistor, R_S ($R_S \approx$ approx. 1 KΩ) is connected in series with this terminal to provide current limiting and linear voltage-to-frequency transfer characteristics. The frequency derivation (for any given modulation level) is inversely proportional to R_S. Typical sweep characteristics of the circuit are shown in Figure 7. For proper operation of the circuit with R_S = 1 KΩ, the sweep voltage, V_S, must be within range: $(V_{SO} - 6) < V_S < (V_{SO} + 1)$ where V_{SO} is the open circuit voltage at pin 13.

WAVEFORM ADJUSTMENT (PINS 7 AND 8)

The shape of the output waveform at pins 1 and 2 is controlled by a potentiometer, R_j, connected between these terminals as shown in Figure 1. For sinewave outputs at pins 1 and 2, the value of R_j is adjusted to minimize the harmonic content of the output waveform. This adjustment is independent of frequency and *needs to be done only once.* The output can be converted to a symmetrical triangle waveform by increasing the effective resistance across these terminals. This can be done without changing the potentiometer setting, by opening the switch S_2 as shown in Figures 1-3.

BUFFER INPUT AND OUTPUT (PINS 10 AND 11)

The buffer amplifier can be connected to any of the circuit outputs (pins 1, 2, 12, 14 or 15) to provide low output impedance and high current drive capability. *For proper operation of the buffer amplifier, pin 11 must be connected to the most negative potential in the circuit, with an external load resistor* R_L *(0.75 KΩ <* R_L *< 10 KΩ).* The maximum output current at this pin must not exceed 20 mA.

DUTY CYCLE ADJUSTMENT

The duty-cycle of the *output waveforms* can be adjusted by connecting a resistor R_B across pins 13 and 14, as shown in Figures 1-3. With switch S_2 open, the output waveform will be symmetrical. Duty cycle is reduced as R_B is decreased. (See Figure 6.)

ADDITIONAL GAIN CONTROL

For amplitude modulated output signals, the dc level across pins 3 and 4 is fixed by the modulation index required. In this case, the output amplitude can be controlled without effecting the modulation by connecting a potentiometer between pins 1 and 2.

ON-OFF KEYING

The oscillator can be keyed off by applying a positive voltage pulse to the sweep input terminal. With R_S = 1 KΩ, oscillations will stop if the applied potential at pin 13 is raised 3 volts above its open-circuit value.

OUTPUT WAVEFORMS

TRIANGLE OUTPUT

The circuit is connected as shown in Figures 1 or 2, with switches S_1 and S_2 open.

SINEWAVE OUTPUT

The circuit is connected as shown in Figures 1 or 2, with switch S_2 open and S_1 closed. The output waveform is adjusted for minimum harmonic distortion using trimmer resistor R_j connected across pins 7 and 8. Sinusoidal output is obtained from pins 1 or 2 (or pin 11 if the buffer amplifier is used). The amplitude of the output waveform is controlled by the differential dc voltage appearing between pins 3 and 4. This bias can be controlled by potentiometer R_Q. for a differential bias between these terminals of ±2 volts or greater, the output amplitude is maximum and equal to approximately 3 volts p-p.

SAWTOOTH OUTPUT

The circuit is connected as shown in Figures 1 or 2, with switch S_1 open and S_2 closed. Closing S_2 places resistor R_B across pins 13 and 14. This changes the duty cycle of the triangle output and converts it to a sawtooth waveform. The polarity of the sawtooth can be changed by reversing the polarity of the dc bias across pins 3 and 4. If S_1 is closed, the linear sawtooth waveform is converted to the sinusoidal sawtooth waveform of Figure 9A.

RAMP OUTPUT (FIGURE 9B)

For ramp outputs, switch S_3 of Figure 1 or 2 is opened, and pin 10 is shorted to pin 14. This results in a 1.4 volt p-p ramp output at pin 11. The duty cycle of this ramp can be controlled by connecting R_B across pins (13-14) or (13-15).

SQUAREWAVE AND PULSE OUTPUTS

For squarewave outputs, the circuit is connected as shown in Figure 3, with S_2 open. The output can be converted to a pulse by closing S_2. The duty cycle of the pulse output is controlled by potentiometer R_D. The amplitude and polarity of either the pulse or squarewave output can be controlled by potentiometer R_Q.

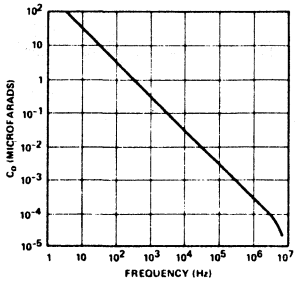


Figure 4. Frequency as a Function of C_0 Across Pins 14 and 15

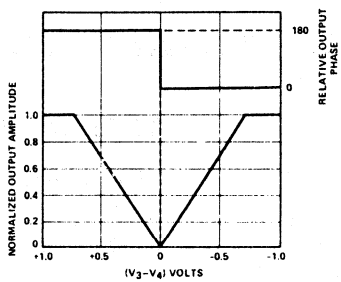


Figure 5. Modular Section Phase and Amplitude Transfer Characteristics

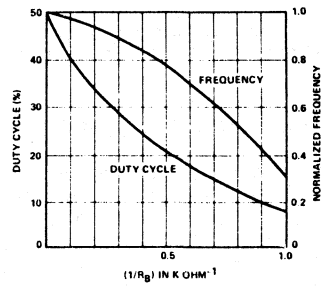


Figure 6. Duty-Cycle and Frequency Variation as a Function of Resistor R_B Connected Across Pins 13 and 14

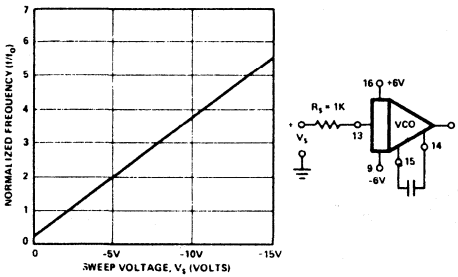


Figure 7. Normalized Frequency vs. Sweep Voltage

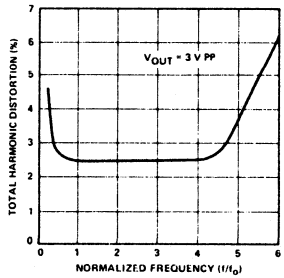


Figure 8. Sinusoidal Output Distortion as a Function of Frequency Sweep

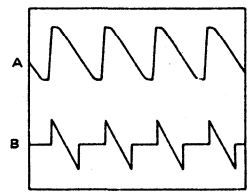
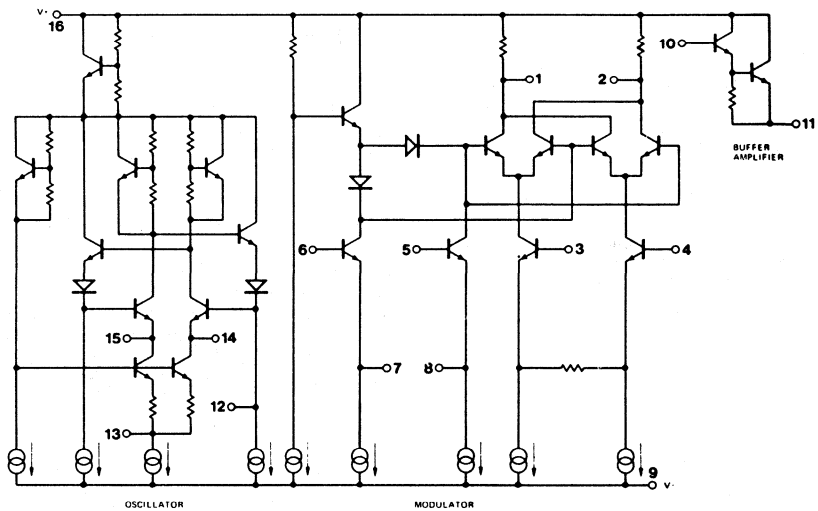


Figure 9. Sinusoidal Sawtooth and Linear Ramp Outputs



EQUIVALENT SCHEMATIC DIAGRAM

Monolithic Function Generator

GENERAL DESCRIPTION

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01 Hz to more than 1 MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage, while maintaining low distortion.

FEATURES

Low-Sine Wave Distortion	0.5%, Typical
Excellent Temperature Stability	20 ppm/°C, Typical
Wide Sweep Range	2000:1, Typical
Low-Supply Sensitivity	0.01%V, Typical
Linear Amplitude Modulation	
TTL Compatible FSK Controls	
Wide Supply Range	10V to 26V
Adjustable Duty Cycle	1% to 99%

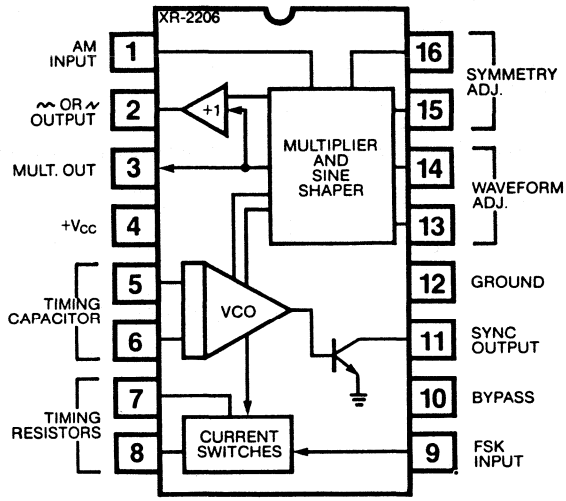
APPLICATIONS

Waveform Generation
Sweep Generation
AM/FM Generation
V/F Conversion
FSK Generation
Phase-Locked Loops (VCO)

ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation	750 mW
Derate Above 25°C	5 mW/°C
Total Timing Current	6 mA
Storage Temperature	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2206M	Ceramic	−55°C to +125°C
XR-2206N	Ceramic	0°C to +70°C
XR-2206P	Plastic	0°C to +70°C
XR-2206CN	Ceramic	0°C to +70°C
XR-2206CP	Plastic	0°C to +70°C
XR-2206D	JEDEC SOIC	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2206 is comprised of four functional blocks; a voltage-controlled oscillator (VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches.

The VCO produces an output frequency proportional to an input current, which is set by a resistor from the timing terminals to ground. With two timing pins, two discrete output frequencies can be independently produced for FSK generation applications by using the FSK input control pin. This input controls the current switches which select one of the timing resistor currents, and routes it to the VCO.

XR-2206

ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of Figure 1, $V^+ = 12V$, $T_A = 25°$, $C = 0.01\ \mu F$, $R_1 = 100\ k\Omega$, $R_2 = 10\ k\Omega$, $R_3 = 25\ k\Omega$ unless otherwise specified. S_1 open for triangle, closed for sine wave.

PARAMETERS	XR-2206M			XR-2206C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Single Supply Voltage	10		26	10		26	V	
Split-Supply Voltage	±5		±13	±5		±13	V	
Supply Current		12	17		14	20	mA	$R_1 \geq 10\ k\Omega$
OSCILLATOR SECTION								
Max. Operating Frequency	0.5	1		0.5	1		MHz	$C = 1000\ pF$, $R_1 = 1\ k\Omega$
Lowest Practical Frequency		0.01			0.01		Hz	$C = 50\ \mu F$, $R_1 = 2\ M\Omega$
Frequency Accuracy		±1	±4		±2		% of f_o	$f_o = 1/R_1C$
Temperature Stability								
Frequency		±10	±50		±20		ppm/°C	$0°C \leq T_A \leq 70°C$, $R_1 = R_2 = 20\ k\Omega$
Sine Wave Amplitude Stability		4800			4800		ppm/°C	See Note 2.
Supply Sensitivity		0.01	0.1		0.01		%/V	$V_{LOW} = 10V$, $V_{HIGH} = 20V$, $R_1 = R_2 = 20\ k\Omega$
Sweep Range	1000:1	2000:1			2000:1		$f_H = f_L$	f_H @ $R_1 = 1\ k\Omega$ f_L @ $R_1 = 2\ M\Omega$
Sweep Linearity								
10:1 Sweep		2			2		%	$f_L = 1\ kHz$, $f_H = 10\ kHz$
1000:1 Sweep		8			8		%	$f_L = 100\ kHz$, $f_H = 100\ kHz$
FM Distortion		0.1			0.1		%	±10% Deviation
Recommended Timing Components								
Timing Capacitor: C	0.001		100	0.001		100	μF	See Figure 4.
Timing Resistors: R_1 & R_2	1		2000	1		2000	k Ω	
Triangle Sine Wave Output								See Note 1, Figure 2.
Triangle Amplitude		160			160		mV/k Ω	Figure 1, S_1 Open
Sine Wave Amplitude	40	60	80		60		mV/k Ω	Figure 1, S_1 Closed
Max. Output Swing		6			6		V p-p	
Output Impedance		600			600		Ω	
Triangle Linearity		1			1		%	
Amplitude Stability		0.5			0.5		dB	For 1000:1 Sweep
Sine Wave Distortion								
Without Adjustment		2.5			2.5		%	$R_1 = 30\ k\Omega$
With Adjustment		0.4	1.0		0.5	1.5	%	See Figures 6 and 7.
Amplitude Modulation								
Input Impedance	50	100		50	100		k Ω	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
Square-Wave Output								
Amplitude		12			12		V p-p	Measured at Pin 11.
Rise Time		250			250		nsec	$C_L = 10\ pF$
Fall Time		50			50		nsec	$C_L = 10\ pF$
Saturation Voltage		0.2	0.4		0.2	0.6	V	$I_L = 2\ mA$
Leakage Current		0.1	20		0.1	100	μA	$V_{11} = 26V$
FSK Keying Level (Pin 9)	0.8	1.4	2.4	0.8	1.4	2.4	V	See section on circuit controls
Reference Bypass Voltage	2.9	3.1	3.3	2.5	3	3.5	V	Measured at Pin 10.

Note 1: Output amplitude is directly proportional to the resistance, R_3, on Pin 3. See Figure 2.
Note 2: For maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.

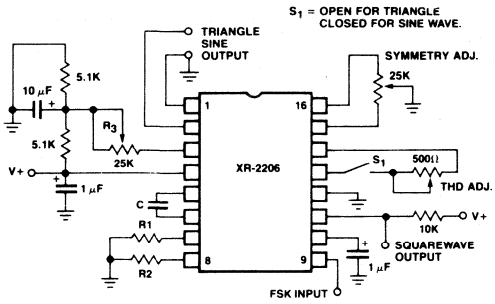


Figure 1. Basic Test Circuit.

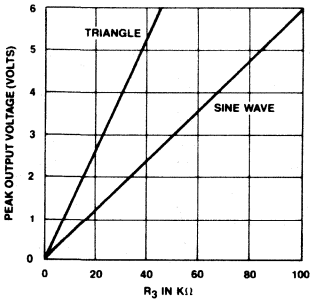


Figure 2. Output Amplitude as a Function of the Resistor, R_3, at Pin 3.

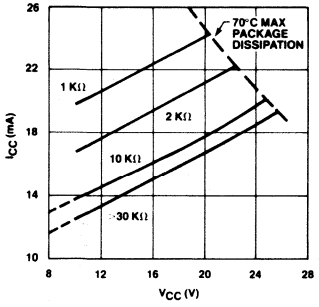


Figure 3. Supply Current versus Supply Voltage, Timing, R.

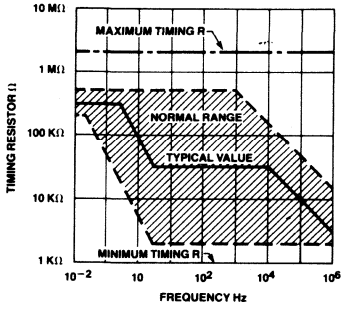


Figure 4. R versus Oscillation Frequency.

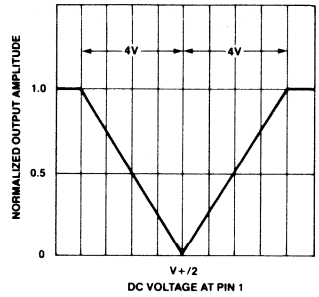


Figure 5. Normalized Output Amplitude versus DC Bias at AM Input (Pin 1).

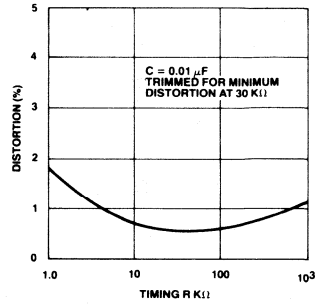


Figure 6. Trimmed Distortion versus Timing Resistor.

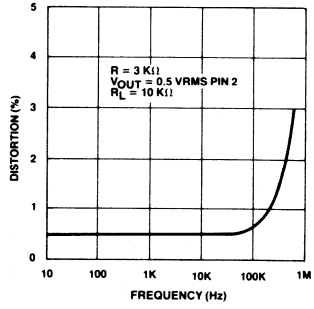


Figure 7. Sine Wave Distortion versus Operating Frequency with Timing Capacitors Varied.

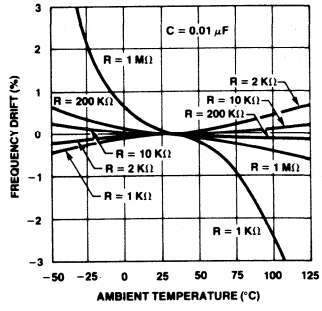


Figure 8. Frequency Drift versus Temperature.

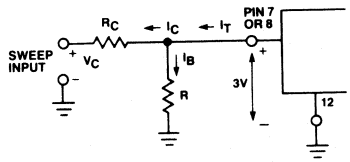


Figure 9. Circuit Connection for Frequency Sweep.

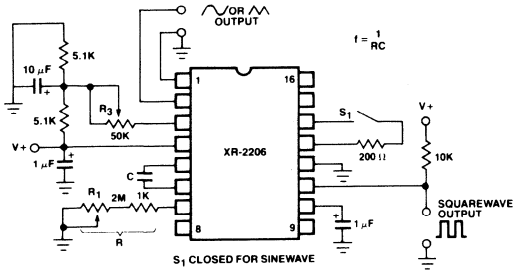


Figure 10. Circuit for Sine Wave Generation without External Adjustment. (See Figure 2 for Choice of R_3).

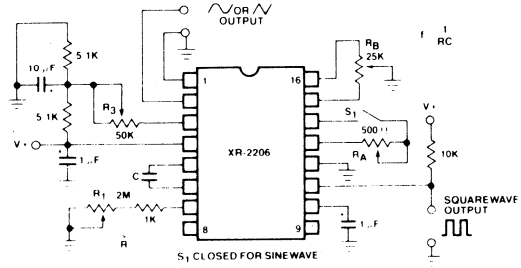


Figure 11. Circuit for Sine Wave Generation with Minimum Harmonic Distortion. (R_3 Determines Output Swing—See Figure 2.)

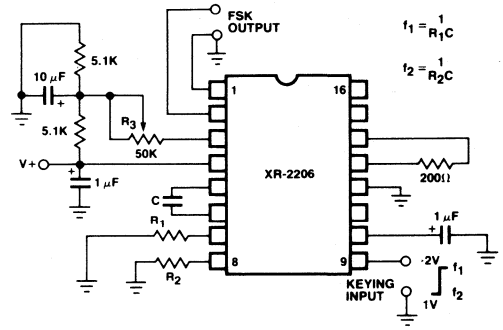


Figure 12. Sinusoidal FSK Generator.

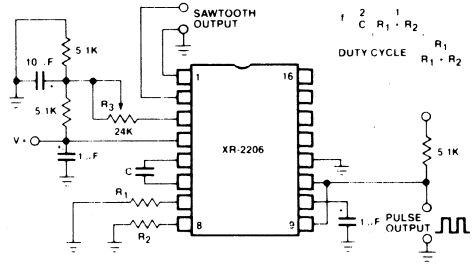


Figure 13. Circuit for Pulse and Ramp Generation.

Frequency-Shift Keying:

The XR-2206 can be operated with two separate timing resistors, R_1 and R_2, connected to the timing Pin 7 and 8, respectively, as shown in Figure 12. Depending on the polarity of the logic signal at Pin 9, either one or the other of these timing resistors is activated. If Pin 9 is open-circuited or connected to a bias voltage $\geq$2V, only R_1 is activated. Similarly, if the voltage level at Pin 9 is $\leq$1V, only R_2 is activated. Thus, the output frequency can be keyed between two levels, f_1 and f_2, as:

$$f_1 = 1/R_1C \text{ and } f_2 = 1/R_2C$$

For split-supply operation, the keying voltage at Pin 9 is referenced to V^-

Output DC Level Control:

The dc level at the output (Pin 2) is approximately the same as the dc bias at Pin 3. In Figures 10, 11 and 12, Pin 3 is biased midway between V^+ and ground, to give an output dc level of $\approx V^+/2$.

APPLICATIONS INFORMATION

Sine Wave Generation

Without External Adjustment:

Figure 10 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer, R_1 at Pin 7, provides the desired frequency tuning. The maximum output swing is greater than $V^+/2$, and the typical distortion (THD) is <2.5%. If lower sine wave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of Figure 10 can be converted to split-supply operation, simply by replacing all ground connections with V^-. For split-supply operation, R_3 can be directly connected to ground.

With External Adjustment:

The harmonic content of sinusoidal output can be reduced to $\approx$0.5% by additional adjustments as shown in Figure 11. The potentiometer, R_A, adjusts the sine-shaping resistor, and R_B provides the fine adjustment for the waveform symmetry. The adjustment procedure is as follows:

1. Set R_B at midpoint and adjust R_A for minimum distortion.
2. With R_A set as above, adjust R_B to further reduce distortion.

Triangle Wave Generation

The circuits of Figures 10 and 11 can be converted to triangle wave generation, by simply open-circuiting Pin 13 and 14 (i.e., S_1 open). Amplitude of the triangle is approximately twice the sine wave output.

FSK Generation

Figure 12 shows the circuit connection for sinusoidal FSK signal operation. Mark and space frequencies can be independently adjusted by the choice of timing resistors, R_1 and R_2; the output is phase-continuous during transitions. The keying signal is applied to Pin 9. The circuit can be converted to split-supply operation by simply replacing ground with V^-

Pulse and Ramp Generation

Figure 13 shows the circuit for pulse and ramp waveform generation. In this mode of operation, the FSK keying terminal (Pin 9) is shorted to the square-wave output (Pin 11), and the circuit automatically frequency-shift keys itself between two separate frequencies during the positive-going and negative-going output waveforms. The pulse width and duty cycle can be adjusted from 1% to 99% by the choice of R_1 and R_2. The values of R_1 and R_2 should be in the range of 1 kΩ to 2 MΩ.

PRINCIPLES OF OPERATION

5

Description of Controls

Frequency of Operation:

The frequency of oscillation, f_o, is determined by the external timing capacitor, C, across Pin 5 and 6, and by the timing resistor, R, connected to either Pin 7 or 8. The frequency is given as:

$$f_o = \frac{1}{RC} \text{ Hz}$$

and can be adjusted by varying either R or C. The recommended values of R, for a given frequency range, as shown in Figure 4. Temperature stability is optimum for 4 kΩ < R < 200 kΩ. Recommended values of C are from 1000 pF to 100 μF.

Frequency Sweep and Modulation:

Frequency of oscillation is proportional to the total timing current, I_T, drawn from Pin 7 or 8:

$$f = \frac{320\ I_T\ (\text{mA})}{C\ (\mu\text{F})} \text{ Hz}$$

Timing terminals (Pin 7 or 8) are low-impedance points, and are internally biased at +3V, with respect to Pin 12 Frequency varies linearly with I_T, over a wide range of current values, from 1 μA to 3 mA. The frequency can be controlled by applying a control voltage, V_C, to the activated timing pin as shown in Figure 9. The frequency of oscillation is related to V_C as:

$$f = \frac{1}{RC}\left(1 + \frac{R}{R_C}\left(1 - \frac{V_C}{3}\right)\right) \text{Hz}$$

where V_C is in volts. The voltage-to-frequency conversion gain, K, is given as:

$$K = \partial f / \partial V_C = -\frac{0.32}{R_C C} \text{ Hz/V}$$

CAUTION: For safety operation of the circuit, I_T should be limited to ≤ 3 mA.

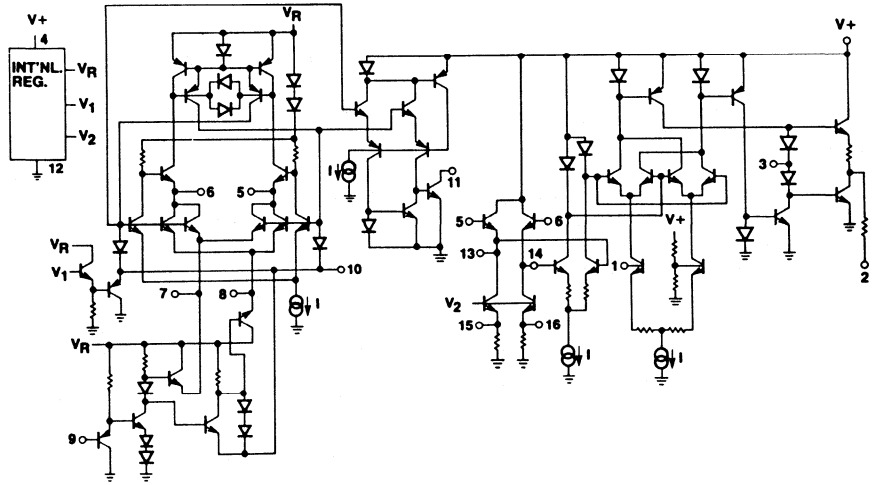
Output Amplitude:

Maximum output amplitude is inversely proportional to the external resistor, R_3, connected to Pin 3 (see Figure 2). For sine wave output, amplitude is approximately 60 mV peak per kΩ of R_3; for triangle, the peak amplitude is approximately 160 mV peak per kΩ of R_3. Thus, for example, R_3 = 50 kΩ would produce approximately ±3V sinusoidal output amplitude.

Amplitude Modulation:

Output amplitude can be modulated by applying a dc bias and a modulating signal to Pin 1. The internal impedance at Pin 1 is approximately 100 kΩ. Output amplitude varies linearly with the applied voltage at Pin 1, for values of dc bias at this pin, within ±4 volts of $V^+/2$ as shown in Figure 5. As this bias level approaches $V^+/2$, the phase of the output signal is reversed, and the amplitude goes through zero. This property is suitable for phase-shift keying and suppressed-carrier AM generation. Total dynamic range of amplitude modulation is approximately 55 dB.

CAUTION: AM control must be used in conjunction with a well-regulated supply, since the output amplitude now becomes a function of V^+.



EQUIVALENT SCHEMATIC DIAGRAM

Voltage-Controlled Oscillator

GENERAL DESCRIPTION

The XR-2207 is a monolithic voltage-controlled oscillator (VCO) integrated circuit featuring excellent frequency stability and a wide tuning range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01 Hz to 1 MHz. It is ideally suited for FM, FSK, and sweep or tone generation, as well as for phase-locked loop applications.

The XR-2207 has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 1000:1 range with an external control voltage; and the duty cycle of both the triangle and the squarewave outputs can be varied from 0.1% to 99.9% to generate stable pulse and sawtooth waveforms.

FEATURES

Excellent Temperature Stability (20 ppm/°C)
Linear Frequency Sweep
Adjustable Duty Cycle (0.1% to 99.9%)
Two or Four Level FSK Capability
Wide Sweep Range (3000:1 Typical)
Logic Compatible Input and Output Levels
Wide Supply Voltage Range (±4V to ±13V)
Low Supply Sensitivity (0.1%/V)
Wide Frequency Range (0.01 Hz to 1 MHz)
Simultaneous Triangle and Squarewave Outputs

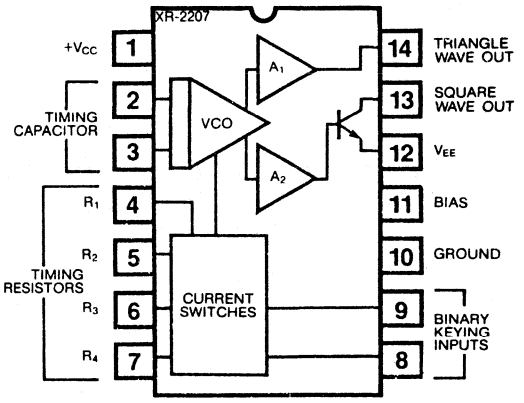
APPLICATIONS

FSK Generation
Voltage and Current-to-Frequency Conversion
Stable Phase-Locked Loop
Waveform Generation
  Triangle, Sawtooth, Pulse, Squarewave
FM and Sweep Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation (package limitation)	
Ceramic package	750 mW
Derate above +25°C	6.0 mW/°C
Plastic package	625 mW
Derate above +25°C	5 mW/°C
Storage Temperature Range	-65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR2207M	Ceramic	-55°C to +125°C
XR2207N	Ceramic	0°C to +70°C
XR2207P	Plastic	0°C to +70°C
XR2207CN	Ceramic	0°C to +70°C
XR2207CP	Plastic	0°C to +70°C
XR-2207CD	JEDEC SOL-16	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2207 utilizes four main functional blocks for frequency generation. These are a voltage controlled oscillator (VCO), four current switches which are activated by binary keying inputs, and two buffer amplifiers for triangle and squarewave outputs. The VCO is actually a current controlled oscillator which gets its input from the current switches. As the output frequency is proportional to the input current, the VCO produces four discrete output frequencies. Two binary input pins determine which timing currents are channelled to the VCO. These currents are set by resistors to ground from each of the four timing terminals.

The triangle output buffer provides a low impedance output (10Ω TYP) while the squarewave is an open-collector type. A programmable reference point allows the XR-2207 to be used in either single or slip supply configurations.

ELECTRICAL CHARACTERISTICS

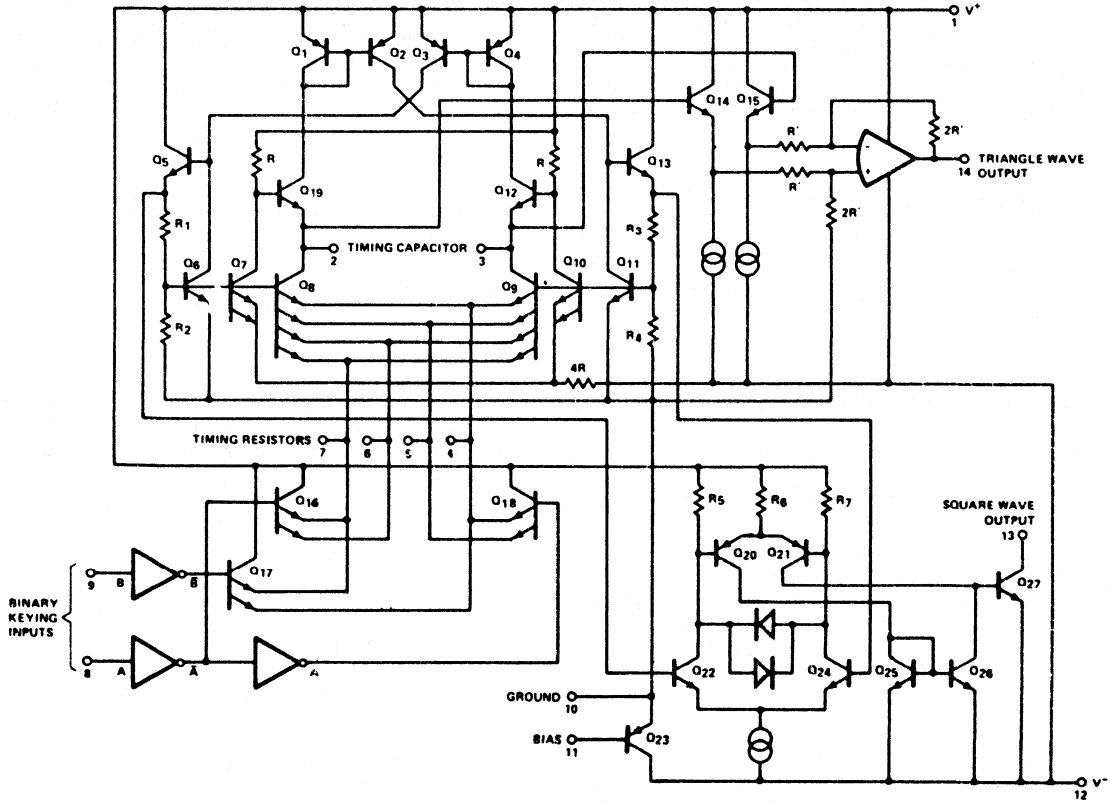
Test Conditions: Test Circuit of Figure 1, $V^+ = V^- = 6V$, $T_A = +25°C$, $C = 5000$ pF, $R_1 = R_2 = R_3 = R_4 = 20$ KΩ, $R_L = 4.7$ KΩ, Binary Inputs grounded, S_1 and S_2 closed unless otherwise specified.

PARAMETERS	XR-2207/XR-2207M			XR-2207C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage								
Single Supply	8		26	8		26	V	See Figure 3
Split Supplies	±4		±13	±4		±13	V	
Supply Current								
Single Supply		5	7		5	8	mA	Measured at pin 1, S_1 and S_2 open See Figure 2
Split Supplies								
Positive		5	7		5	8	mA	Measured at pin 1, S_1, S_2 open
Negative		4	6		4	7	mA	Measured at pin 12, S_1, S_2 open
OSCILLATOR SECTION — FREQUENCY CHARACTERISTICS								
Upper Frequency Limit	0.5	1.0		0.5	1.0		MHz	C = 500 pF, R_3 = 2 KΩ
Lowest Practical Frequency		0.01			0.01		Hz	C = 50 μF, R_3 = 2 MΩ
Frequency Accuracy		±1	±3		±1	±5	% of f_o	
Frequency Matching		0.5			0.5		% of f_o	
Frequency Stability								
Temperature		20	50		30		ppm/°C	0°C < T_A < 70°C
Power Supply		0.15			0.15		%/V	
Sweep Range	1000:1	3000:1			1000:1		f_H/f_L	R_3 = 1.5 KΩ for f_{H1} R_3 = 2 MΩ for f_L
Sweep Linearity							%	C = 5000 pF
10:1 Sweep		1	2		1.5			f_H = 10 kHz, f_L = 1 kHz
1000:1 Sweep		5			5			f_H = 100 kHz, f_L = 100 Hz
FM Distortion		0.1			0.1		%	±10% FM Deviation
Recommended Range of Timing Resistors	1.5		2000	1.5		2000	KΩ	See Characteristic Curves
Impedance at Timing Pins		75			75		Ω	Measured at pins 4, 5, 6, or 7
DC Level at Timing Terminals		10			10		mV	
BINARY KEYING INPUTS								
Switching Threshold	1.4	2.2	2.8	1.4	2.2	2.8	V	Measured at pins 8 and 9, Referenced to pin 10
Input Impedance		5			5		KΩ	
OUTPUT CHARACTERISTICS								
Triangle Output								Measured at pin 13
Amplitude	4	6		4	6		V_{pp}	
Impedance		10			10		Ω	
DC Level		+100			+100		mV	Referenced to pin 10
Linearity		0.1			0.1		%	From 10% to 90% to swing
Squarewave Output								Measured at pin 13, S_2 closed
Amplitude	11	12		11	12		V_{pp}	
Saturation Voltage		0.2	0.4		0.2	0.4	V	Referenced to pin 12
Rise Time		200			200		nsec	$C_L \leq 10$ pF
Fall Time		20			20		nsec	$C_L \leq 10$ pF

PRECAUTIONS

The following precautions should be observed when operating the XR-2207 family of integrated circuits:

1. Pulling excessive current from the timing terminals will adversely effect the temperature stability of the circuit. To minimize this disturbance, it is recommended that the *total current* drawn from pins 4, 5, 6, and 7 be limited to ≤6 mA. In addition, permanent damage to the device may occur if the total timing current exceeds 10 mA.
2. Terminals 2, 3, 4, 5, 6, and 7 have very low internal impedance and should, therefore, be protected from accidental shorting to ground or the supply voltages.
3. The keying logic pulse amplitude should not exceed the supply voltage.



EQUIVALENT SCHEMATIC DIAGRAM

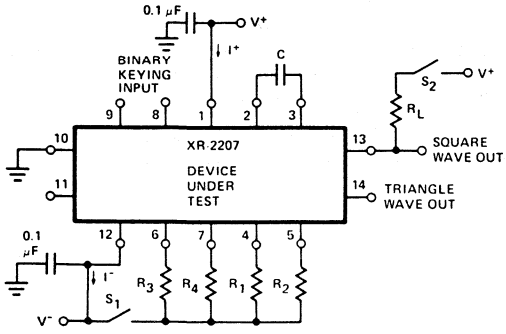


Figure 1. Test Circuit For Split Supply Operation

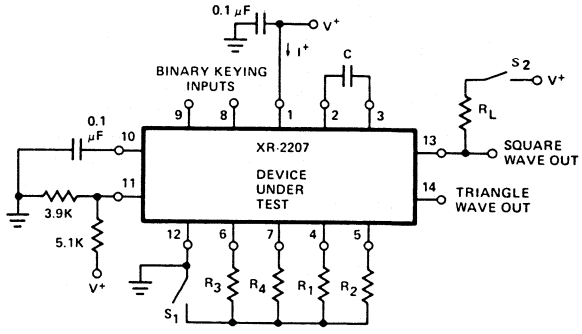


Figure 2. Test Circuit For Single Supply Operation

PRINCIPLES OF OPERATION

TIMING CAPACITOR (PINS 2 AND 3)

The oscillator frequency is inversely proportional to the timing capacitor, C, as indicated in Figure 8. The minimum capacitance value is limited by stray capacitances and the maximum value by physical size and leakage current considerations. Recommended values range from 100 pF to 100 μF. The capacitor should be non-polar.

TIMING RESISTORS (PINS 4, 5, 6, AND 7)

The timing resistors determine the total timing current, I_T, available to charge the timing capacitor. Values for timing resistors can range from 2 KΩ to 2 MΩ; however, for optimum temperature and power supply stability,

recommended values are 4 KΩ to 200 KΩ (see Figures 4, 5, and 7). To avoid parasitic pick up, timing resistor leads should be kept as short as possible. For noisy environments, unused or deactivated timing terminals should be bypassed to ground through 0.1 μF capacitors.

SUPPLY VOLTAGE (PINS 1 AND 12)

The XR-2207 is designed to operate over a power supply range of ±4V to ±13V for split supplies, or 8V to 26V for single supplies. At high supply voltages, the frequency sweep range is reduced (see Figures 3 and 4). Performance is optimum for ±6V, or 12V single supply operation.

BINARY KEYING INPUTS (PINS 8 AND 9)

The internal impedance at these pins is approximately 5 KΩ. Keying levels are <1.4V for "zero" and >3V for "one" logic levels referenced to the dc voltage at pin 10 (see Figure 8).

BIAS FOR SINGLE SUPPLY (PIN 11)

For single supply operation, pin 11 should be externally biased to a potential between $V^+/3$ and $V^+/2$ volts (see Figure 2). The bias current at pin 11 is nominally 5% of the total oscillation timing current, I_T.

GROUND (PIN 10)

For split supply operation, this pin serves as circuit ground. For single supply operation, pin 10 should be ac grounded through a 1 μF bypass capacitor. During split supply operation, a ground current of $2I_T$ flows out of this terminal, where I_T is the total timing current.

SQUAREWAVE OUTPUT (PIN 13)

The squarewave output at pin 13 is a "open-collector" stage capable of sinking up to 20 mA of load current. R_L serves as a pull-up load resistor for this output. Recommended values for R_L range from 1 KΩ to 100 KΩ.

TRIANGLE OUTPUT (PIN 14)

The output at pin 14 is a triangle wave with a peak swing of approximately one-half of the total supply voltage. Pin 14 has a very low output impedance of 10Ω and is internally protected against short circuits.

BYPASS CAPACITORS

The recommended value for bypass capacitors is 1 μF, although larger values are required for very low frequency operation.

SPLIT SUPPLY OPERATION

Figure 1 is the recommended circuit connection for split supply operation. The frequency of operation is determined by the timing capacitor, C, and the activated timing resistors (R_1 through R_4). The timing resistors are activated by the logic signals at the binary keying inputs (pins 8 and 9), as shown in the logic table (Table 1). If a single timing resistor is activated, the frequency is 1/RC. Otherwise, the frequency is either $1/(R_1 \| R_2)C$ or $1/(R_3 \| R_4)C$.

The squarewave output is obtained at pin 13 and has a peak-to-peak voltage swing equal to the supply voltages. This output is an "open-collector" type and requires an external pull-up load resistor (nominally 5 KΩ) to the positive supply. The triangle waveform obtained at pin 14 is centered about ground and has a peak amplitude of $V^+/2$.

The circuit operates with supply voltages ranging from ±4V to ±13V. Minimum drift occurs with ±6 volt supplies. For operation with unequal supply voltages, see Figure 3.

Note: For Single-Supply Operation, Logic Levels are Referenced to Voltage at Pin 10

SINGLE SUPPLY OPERATION

The circuit should be interconnected as shown in Figure 11 for single supply operation. Pin 12 should be grounded, and pin 11 biased from V^+ through a resistive divider to a value of bias voltage between $V^+/3$ and $V^+/2$. Pin 10 is bypassed to ground through a 1 μF capacitor.

For single supply operation, the dc voltage at pin 10 and the timing terminals (pins 4 through 7) are equal and approximately 0.6V above V_B, the bias voltage at pin 11. The logic levels at the binary keying terminals are referenced to the voltage at pin 10.

For a fixed frequency of $f_3 = 1/R_3C$, the external circuit connections can be simplified as shown in Figure 11b.

Table 1
Logic Table for Binary Keying Controls

LOGIC LEVEL		SELECTED TIMING PINS	FREQUENCY	DEFINITIONS
8	9			
0	0	6	f_1	$f_1 = 1/R_3C$, $\Delta f_1 = 1/R_4C$
0	1	6 and 7	$f_1 + \Delta f_1$	$f_2 = 1/R_2C$, $\Delta f_2 = 1/R_1C$
1	0	5	f_2	Logic Levels: 0 = Ground
1	1	4 and 5	$f_2 + \Delta f_2$	1 = >3 V

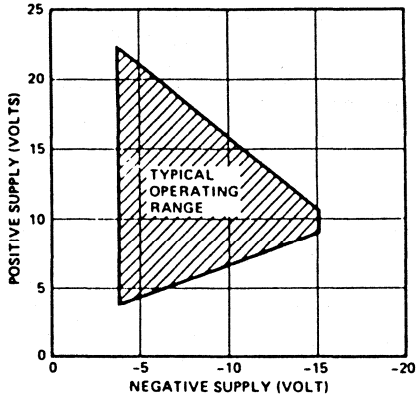


Figure 3. Typical Operating Range For Split Supply Voltage

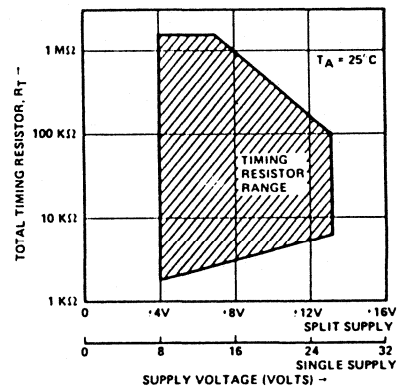


Figure 4. Recommended Timing Resistor Value vs. Power Supply Voltage*

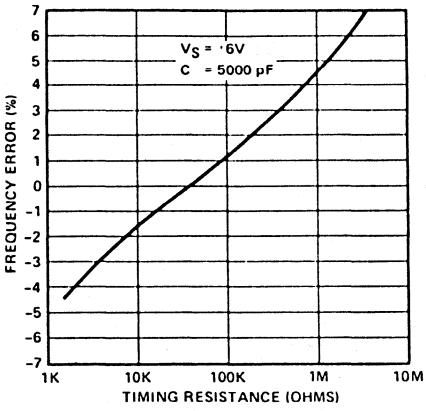


Figure 5. Frequency Accuracy vs. Timing Resistance

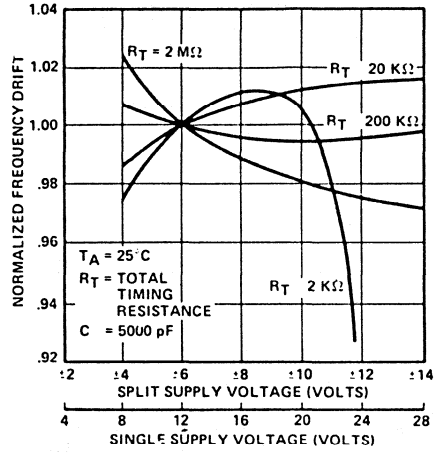


Figure 6. Frequency Drift vs. Supply Voltage

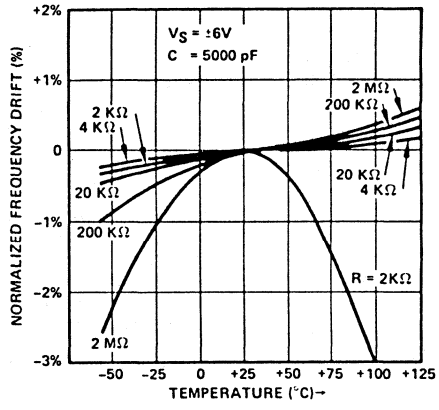


Figure 7. Normalized Frequency Drift With Temperature

LOGIC LEVEL		SELECTED TIMING PINS	FREQUENCY	
A	B			DEFINITIONS
0	0	6	f_1	$f_1 = 1/R_3C, \Delta f_1 = 1/R_4C$
0	1	6 and 7	$f_1 + \Delta f_1$	$f_2 = 1/R_2C, \Delta f_2 = 1/R_1C$
1	0	5	f_2	Logic Levels: 0 = Ground
1	1	4 and 5	$f_2 + \Delta f_2$	1 = > 3V

Figure 8. Logic Table For Binary Keying Controls. Note: For Single-Supply Operation, Logic Levels are Referenced to Voltage at Pin 10

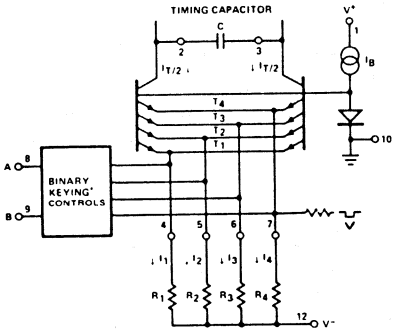


Figure 9. Simplified Schematic of Frequency Control Mechanism

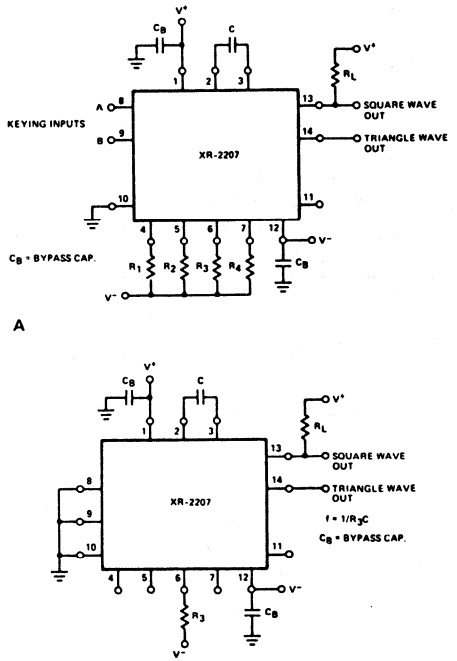


Figure 10. Split-Supply Operation: (a) General (b) Fixed Frequency

FREQUENCY CONTROL (SWEEP AND FM)

The frequency of operation is controlled by varying the total timing current, I_T, drawn from the activated timing pins 4, 5, 6, or 7. The timing current can be modulated by applying a control voltage, V_C, to the activated timing pin through a series resistor R_C as shown in Figures 12 & 13.

For split supply operation, a *negative* control voltage, V_C, applied to the circuits of Figures 15 & 16 causes the total timing current, I_T, and the frequency, to increase.

As an example, in the circuit of Figure 12, the binary keying inputs are grounded. Therefore, only timing pin 6 is activated.

The frequency of operation, normally $f = \frac{1}{R_3C}$, is now proportional to the control voltage, V_C, and determined as:

$$f = \frac{1}{R_3C}\left[1 - \frac{V_C R_3}{R_C V-}\text{ Hz}\right]$$

The frequency f will increase as the control voltage is made more negative. If $R_3 = 2\ M\Omega$, $R_C = 2\ K\Omega$, $C = 5000\ pF$, then a 1000: 1 frequency sweep would result for a negative sweep voltage $V_C \approx V-$.

The voltage to frequency conversion gain, K, is controlled by the series resistance R_C and can be expressed as:

$$K = \frac{\Delta f}{\Delta V_C} = -\frac{1}{R_C C V-}\text{ Hz/volt}$$

The circuit of Figure 12 can operate both with positive and negative values of control voltage. However, for positive values of V_C with small (R_C/R_3) ratio, the direction of the timing current I_T is reversed and the oscillations will stop.

Figure 13 shows an alternate circuit for frequency control where two timing pins, 6 and 7, are activated. The frequency and the conversion gain expressions are the same as before, except that the circuit would operate only with negative values of V_C. For $V_C > 0$, pin 7 becomes deactivated

and the frequency is fixed at $f = \frac{1}{R_3C}$.

CAUTION

For operation of the circuit, total timing current I_T must be less than 6 mA over the frequency control range.

DUTY CYCLE CONTROL

The duty cycle of the output waveforms can be controlled by frequency shift keying at the end of every half cycle of oscillator output. This is accomplished by connecting one or both of the binary keying inputs (pins 8 or 9) to the squarewave output at pin 13. The output waveforms can then be converted to positive or negative pulses and sawtooth waveforms.

Figure 14 is the recommended circuit connection for duty cycle control. Pin 8 is shorted to pin 13 so that the circuit switches between the "0,0" and the "1,0" logic states given in Figure 11. Timing pin 5 is activated when the output is "high," and the timing pin is activated when the squarewave output goes to a low state.

The duty cycle of the output waveforms is given as:

$$\text{Duty Cycle} = \frac{R_2}{R_2 + R_3}$$

and can be varied from 0.1% to 99.9% by proper choice of timing resistors. The frequency of oscillation, f, is given as:

$$f = \frac{2}{C}\left[\frac{1}{R_2 + R_3}\right]$$

The frequency can be modulated or swept without changing the duty cycle by connecting R_2 and R_3 to a common control voltage V_C, instead of to V^- (see Figure 15). The sawtooth and the pulse output waveforms are shown in Figure 15.

ON-OFF KEYING

The XR-2207 can be keyed on and off by simply activating an open circuited timing pin. Under certain conditions, the circuit may exhibit very low frequency (<1 Hz) residual oscillations in the "off" state due to internal bias currents. If this effect is undesirable, it can be eliminated by connecting a 10 MΩ resistor from pin 3 to V^+.

TWO-CHANNEL FSK GENERATOR (MODEM TRANSMITTER)

The multi-level frequency shift-keying capability of XR-2207 makes it ideally suited for two-channel FSK generation. A recommended circuit connection for this application is shown in Figure 16.

For two-channel FSK generation, the "mark" and "space" frequencies of the respective channels are determined by the timing resistor pairs (R_1, R_2) and (R_3, R_4). Pin 8 is the "channel-select" control in accord with Figure 11. For a "high" logic level at pin 8, the timing resistors R_1 and R_2 are activated. Similarly, for a "low" logic level, timing resistors R_3 and R_4 are enabled.

The "high" and "low" logic levels at pin 9 determine the respective high and low frequencies within the selected FSK channel.

Recommended component values for various commonly used FSK frequencies are given in Table 1. When only a single FSK channel is used, the remaining channel can be deactivated by connecting pin 8 to either V^+ or ground. In this case, the unused timing resistors can also be omitted from the circuit.

The low and high frequencies, f_1 and f_2, for a given FSK channel can be fine tuned using potentiometers connected in series with respective timing resistors. In fine tuning the frequencies, f_1 should be set first with the logic level at pin 9 in a "low" level.

Typical frequency drift of the circuit for 0°C to 75°C operation is ±0.2%. Since the frequency stability is directly related to the external timing components, care must be taken to use timing components with low temperature coefficients.

FSK TRANSCEIVER (FULL-DUPLEX MODEM)

The XR-2207 can be used in conjunction with the XR-210, FSK demodulator, to form a full-duplex FSK transceiver, or modem. A recommended circuit connection for this application is shown in Figure 20. Table 1 shows the recommended component values for 300-Baud (103-type) and 1200-Baud (202-type) Modem applications.

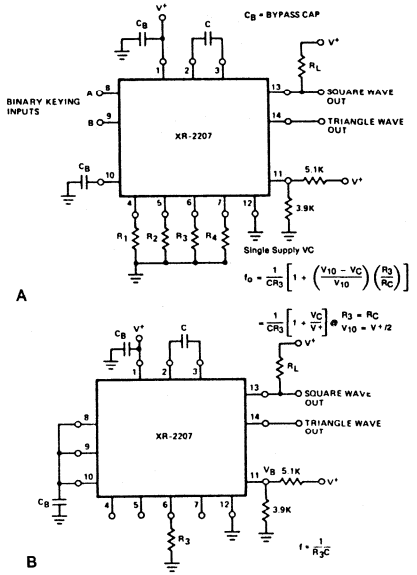


Figure 11. Single Supply Operation:
(a) General
(b) Fixed Frequency

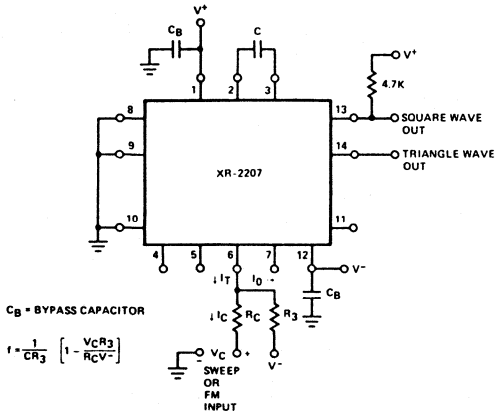


Figure 12. Frequency Sweep Operation

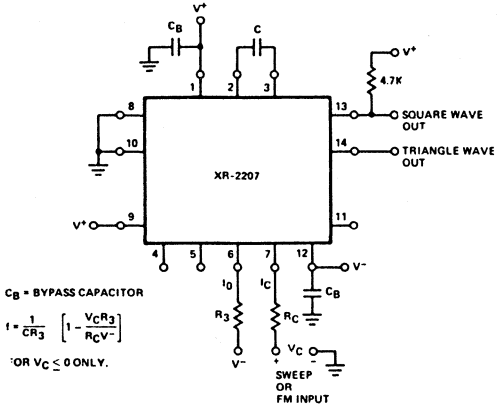


Figure 13. Alternate Frequency Sweep Operation

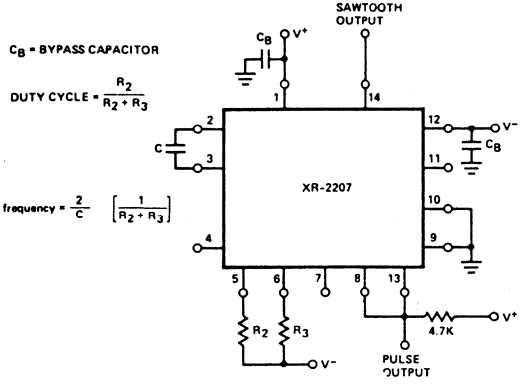


Figure 14. Sawtooth and Pulse Outputs

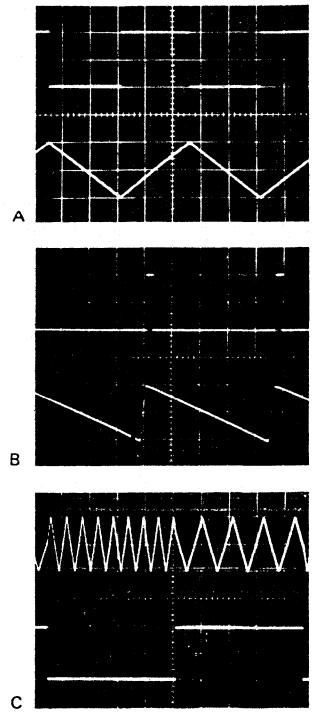


Figure 15. Output Waveforms:
(a) Squarewave and Triangle Outputs
(b) Pulse and Sawtooth Outputs
(c) Frequency-Shift Keyed Output
Top: FSK Output With $f_2 = 2f_1$
Bottom: Keying Logic Input

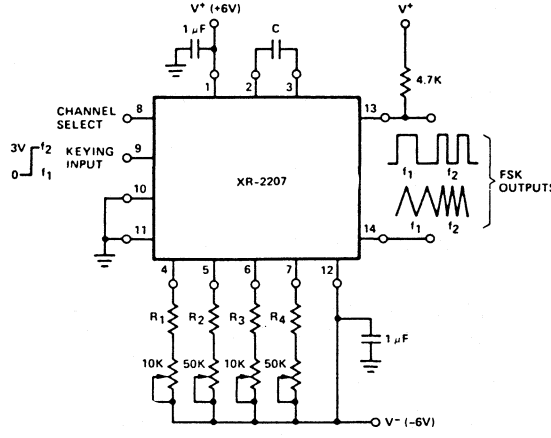


Figure 16. Multi-Channel FSK Generation

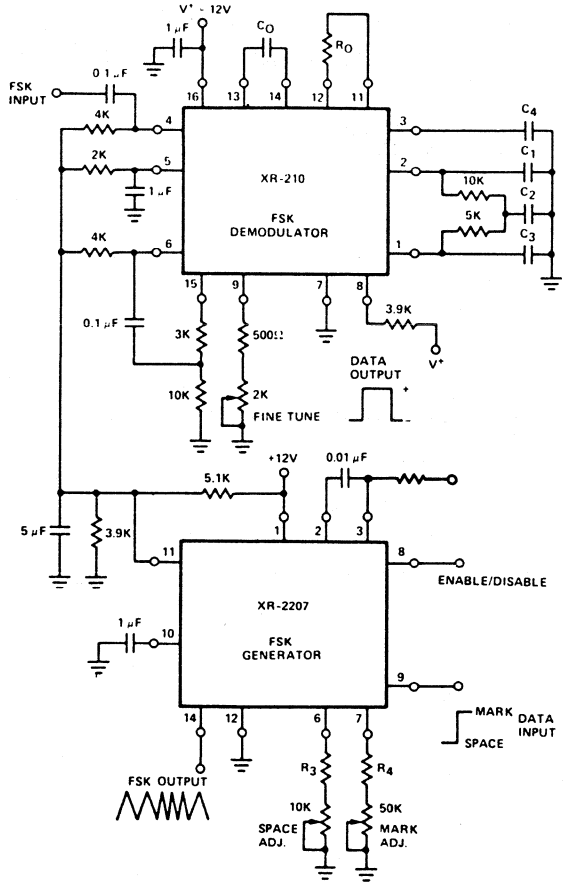


Figure 17. Full Duplex FSK Modem Using XR-210 and XR-2207 (See Table 1 For Component Values)

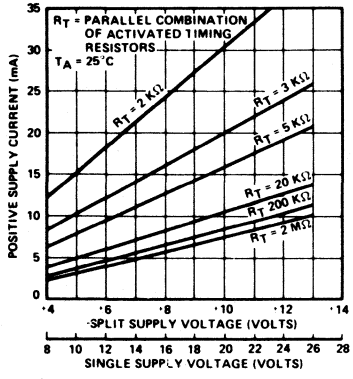


Figure 18. Positive Supply Current, I^+ (Measured at Pin 1) vs. Supply Voltage*

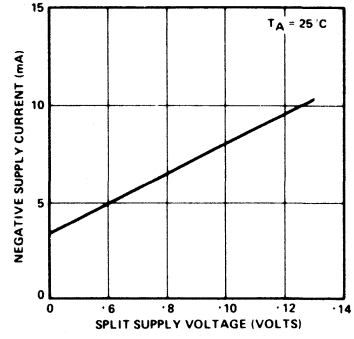


Figure 19. Negative Supply Current, I^- (Measured at Pin 12) vs. Supply Voltage

***Note: R_T = Parallel Combination of Activated Timing Resistors**

Precision Oscillator

GENERAL DESCRIPTION

The XR-2209 is a monolithic variable frequency oscillator circuit featuring excellent temperature stability and a wide linear sweep range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01 Hz to 1 MHz. The frequency is set by an external RC product. It is ideally suited for frequency modulation, voltage to frequency or current to frequency conversion, sweep or tone generation as well as for phase-locked loop applications when used in conjunction with a phase comparator such as the XR-2208.

FEATURES

Excellent Temperature Stability (20 ppm/°C)
Linear Frequency Sweep
Wide Sweep Range (1000:1 Min)
Wide Supply Voltage Range (±4V to ±13V)
Low Supply Sensitivity (0.15%/V)
Wide Frequency Range (0.01 Hz to 1 MHz)
Simultaneous Triangle and Squarewave Outputs

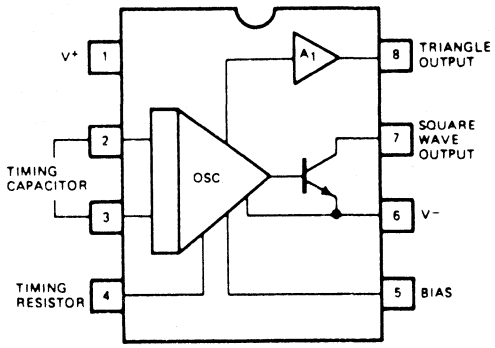
APPLICATIONS

Voltage and Current-to-Frequency Conversion
Stable Phase-Locked Loop
Waveform Generation
FM and Sweep Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate above +25°C	8.3 mW/°C
Operating Temperatue Range	
XR-2209M	−55°C to +125°C
XR-2209C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2209M	Ceramic	−55°C to +125°C
XR-2209CN	Ceramic	0°C to +70°C
XR-2209CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2209 precision oscillator is comprised of three functional blocks: a variable frequency oscillator which generates the basic periodic waveforms and two buffer amplifiers for the triangle and the squarewave outputs. The oscillator frequency, set by an external capacitor, C, and the timing resistor, R, operates over 8 frequency decades, from 0.01 Hz to 1 MHz. With no sweep signal applied, the frequency of oscillation is equal to 1/RC.

The XR-2209 has a typical drift specification of 20 ppm/°C. Its frequency can be linearly swept over a 1000:1 range with an external control signal. Output duty cycle is adjustable from less than 1% to over 99%. The device may operate from either single or split supplies from 8 V to 26 V (±4 V to ±13 V).

ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of Figure 1, $V^+ = V^- = 6V$, $T_A = +25°C$, C = 5000 pF, R - 20 KΩ, R_L = 4.7 kΩ. S_1 and S_2 closed unless otherwise specified.

PARAMETERS	XR-2209M			XR-2209C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage								
Single Supply	8		26	8		26	V	See Figure 2
Split Supplies	±4		±13	±4		±13	V	See Figure 1
Supply Current								
Single Supply		5	7		5	8	mA	Measured at pin 1, S_1, S_2 open See Figure 2
Split Supplies								
Positive		5	7		5	8	mA	Measured at pin 1, S_1, S_2 open
Negative		4	6		4	7	mA	Measured at pin 4, S_1, S_2 open
OSCILLATOR SECTION — FREQUENCY CHARACTERISTICS								
Upper Frequency Limit	0.5	1.0		0.5	1.0		MHz	C = 500 pF, R = 2 KΩ
Lowest Practical Frequency		0.01			0.01		Hz	C = 50 μF, R = 2 MΩ
Frequency Accuracy		±1	±3		±1	±5	% of f_o	
Frequency Stability								
Temperature		20	50		30		ppm/°C	0°C < T_T < 70°C *
Power Supply		0.15			0.15		%/V	
Sweep Range	1000:1	3000:1			1000:1		f_H/f_L	R = 1.5 KΩ for f_{H1} R = 2 MΩ for f_L
Sweep Linearity							%	C = 5000 pF
10:1 Sweep		1	2		1.5			f_H = 10 kHz, f_L = 1 kHz
1000:1 Sweep		5			5			f_H = 100 kHz, f_L = 100Hz
FM Distortion		0.1			0.1		%	±10% FM Deviation
Recommended Range of Timing Resistors	1.5		2000	1.5		2000	KΩ	See Characteristic Curves
Impedance at Timing Pin		75			75		Ω	Measured at pin 4
OUTPUT CHARACTERISTICS								
Triangle Output								Measured at pin 8
Amplitude	4	6		4	6		Vpp	
Impedance		10			10		Ω	
Linearity		0.1			0.1		%	10% to 90% of swing
Squarewave Output								Measured at pin 7, S_2 closed
Amplitude	11	12		11	12		Vpp	
Saturation Voltage		0.2	0.4		0.2	0.4	V	Referenced to pin 6
Rise Time		200			200		nsec	C_L ≤ 10 pF, R_L = 4.7 KΩ
Fall Time		20			20		nsec	C_L ≤ 10 pF

* These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

PRECAUTIONS

The following precautions should be observed when operating the XR-2209 family of integrated circuits:

1. Pulling excessive current from the timing terminal will adversely effect the temperature stability of the circuit. To minimize this disturbance, it is recommended that the *total current* drawn from pin 4 be limited to ≤6 mA.
2. Terminals 2, 3, and 4 have very low internal impedance and should, therefore, be protected from accidental shorting to ground or the supply voltages.
3. Triangle waveform linearity is sensitive to parasitic coupling between the square and the triangle-wave outputs (pins 7 and 8). In board layout or circuit wiring care should be taken to minimize stray wiring capacitances between these pins.

DESCRIPTION OF CIRCUIT CONTROLS

TIMING CAPACITOR (PINS 2 and 3)

The oscillator frequency is inversely proportional to the timing capacitor, C. The minimum capacitance value is limited by stray capacitances and the maximum value

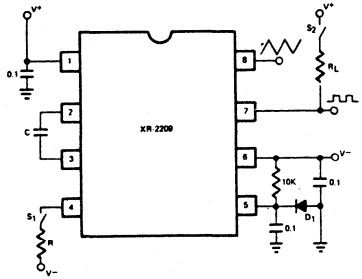


Figure 1. Test Circuit for Split Supply Operation (D_1 = 1N 4148 or Equivalent)

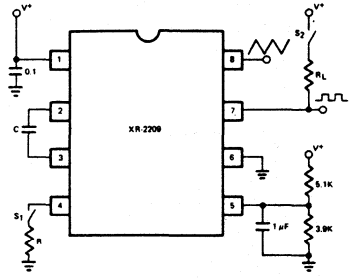


Figure 2. Test Circuit for Single Supply Operation

CHARACTERISTIC CURVES

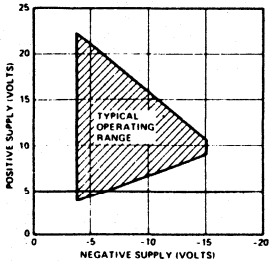


Figure 3. Typical Operating Range For Split Supply Voltage

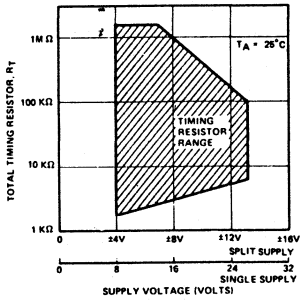


Figure 4. Recommended Timing Resistor Value vs. Power supply Voltage*

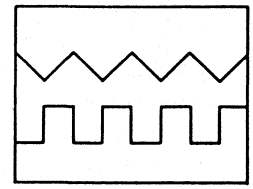


Figure 5. Output Waveforms
Top: Triangle Output (Pin 8)
Bottom: Squarewave Output (Pin 7)

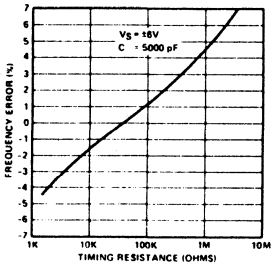


Figure 6. Frequency Accuracy vs. Timing Resistance

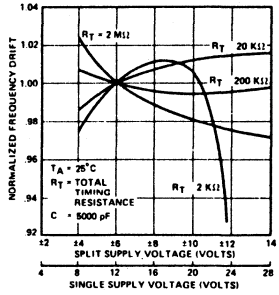


Figure 7. Frequency Drift vs. Supply Voltage
*Note: R_T = Timing Resistor at Pin 4

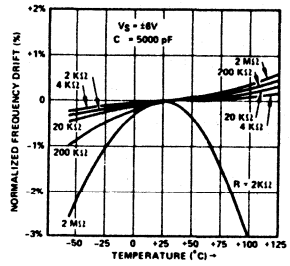


Figure 8. Normalized Frequency Drift With Temperature

RECOMMENDED CIRCUIT CONNECTIONS

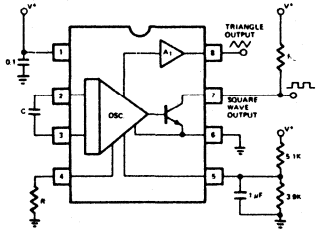


Figure 9. Circuit Connection for Single Supply Operation

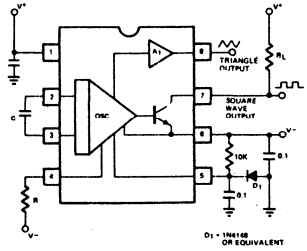


Figure 10. Generalized Circuit Connection for Split Supply Operation

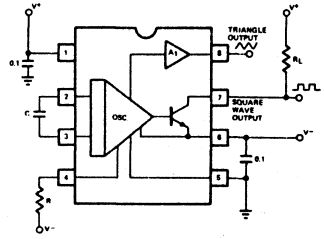


Figure 11. Simplified Circuit Connection for Split Supply Operation With V_{CC} = V_{EE} > ±7V *(Note: Triangle wave output has +0.6V offset with respect to ground.)*

by physical size and leakage current considerations. Recommended values range from 100 pF to 100 μF. The capacitor should be non-polar.

TIMING RESISTOR (PIN 4)

The timing resistor determines the total timing current, I_T, available to charge the timing capacitor. Values for the timing resistor can range from 1.5 KΩ to 2 MΩ; however, for optimum temperature and power supply stability, recommended values are 4 KΩ to 200 KΩ (see Figures 4, 7, and 8). To avoid parasitic pick up, timing resistor leads should be kept as short as possible.

SUPPLY VOLTAGE (PINS 1 AND 6)

The XR-2209 is designed to operate over a power supply range of ±4V to ±13V for split supplies, or 8V to 26V for single supplies. At high supply voltages, the frequency sweep range is reduced (see Figures 3 and 4). Performance is optimum for ±6V, or 12V single supply operation.

BIAS FOR SINGLE SUPPLY (PIN 5)

For single supply operation, pin 5 should be externally biased to a potential between $V^+/3$ and $V^+/2$ volts (see Figure 9). The bias current at pin 5 is nominally 5% of the total oscillation timing current, I_T, at pin 4. This pin should be bypassed to ground with 0.1 μF capacitor. To prevent triangular clipping the voltage at pin 5 should be 5V above V^-.

SQUAREWAVE OUTPUT (PIN 7)

The squarewave output at pin 7 is a "open-collector" stage capable of sinking up to 20 mA of load current. R_L serves as a pull-up load resistor for this output. Recommended values for R_L range from 1 KΩ to 100 KΩ.

TRIANGLE OUTPUT (PIN 8)

The output at pin 8 is a triangle wave with a peak swing of approximately one-half of the total supply voltage. Pin 8 has a very low output impedance of 10Ω and is internally protected against short circuits.

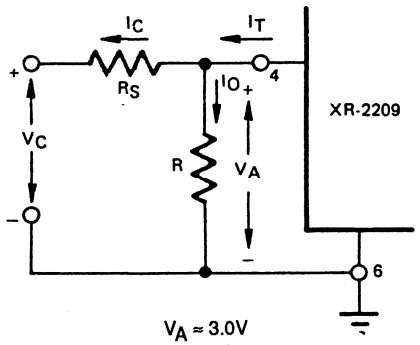


Figure 12. Frequency Sweep Operation

OPERATING INSTRUCTIONS

SPLIT SUPPLY OPERATION

The recommended circuit for split supply operation is shown in Figure 10. Diode D_1 in the figure assures that the triangle output swing at pin 8 is symmetrical about ground. This circuit operates with supply voltages ranging from ±4V to ±13V. Minimum drift occurs at ±6V supplies. See Figure 3 for operation with unequal supplies.

Simplified Connection

For operation with split supplies in excess of ±7 volts, the simplified circuit connection of Figure 11 can be used. This circuit eliminates the diode D_1 used in Figure 10; however the triangle wave output at pin 8 now has a +0.6 volt DC offset with respect to ground.

SINGLE SUPPLY OPERATION

The recommended circuit connection for single-supply operation is shown in Figure 9. Pin 6 is grounded; and pin 5 is biased from V^+ through a resistive divider as shown in the figure, and is bypassed to ground with a 1 μF capacitor.

For single supply operation, the DC voltage at the timing terminal, pin 4, is approximately 0.6 volts above V_B, the bias voltage at pin 5.

The frequency of operation is determined by the timing capacitor C and the timing resistor R, and is equal to 1/RC. The squarewave output is obtained at pin 7 and has a peak-to-peak voltage swing equal to the supply voltage. This output is an "open-collector" type and requires an external pull-up load resistor (nominally 5 KΩ) to V^+. The triangle waveform obtained at pin 8 is centered about a voltage level V_O where:

$$V_O = V_B + 0.6V$$

where V_B is the bias voltage at pin 5. The peak-to-peak output swing of triangle wave is approximately equal to $V^+/2$.

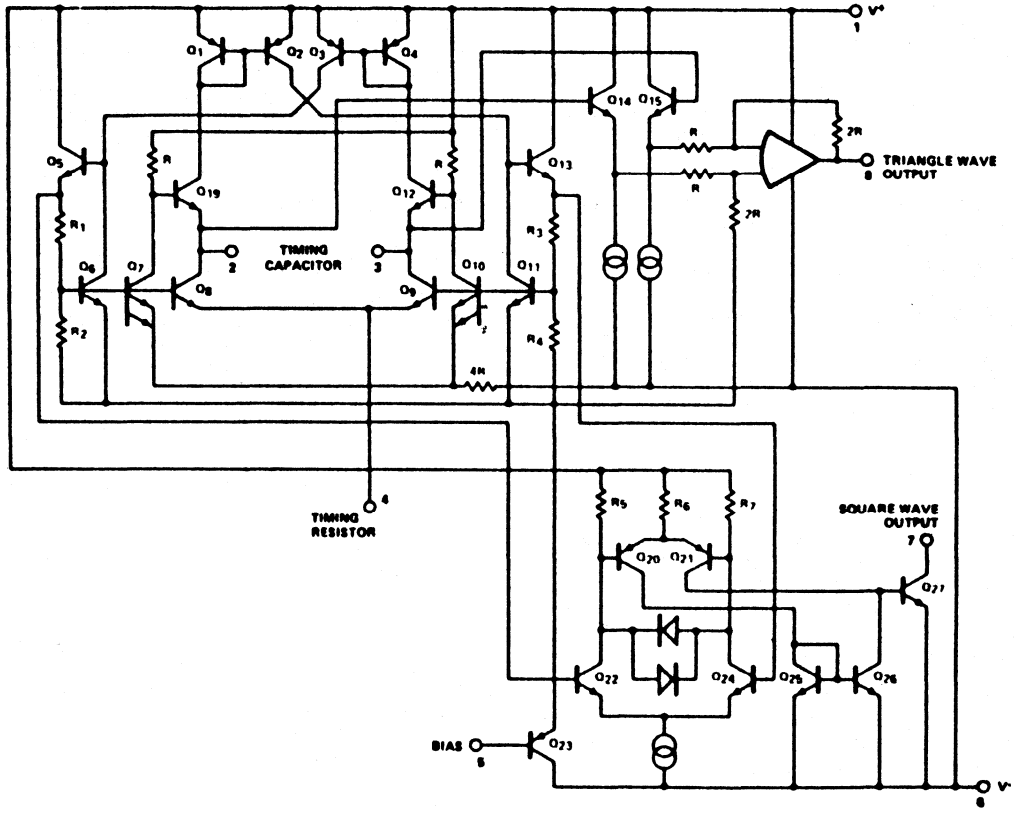
FREQUENCY CONTROL (SWEEP AND FM)

The frequency of operation is proportional to the *total* timing current I_T drawn from the timing pin, pin 4. This timing current, and the frequency of operation can be modulated by applying a control voltage, V_C, to the timing pin, through a series resistor, R_S, as shown in Figure 12. If V_C is negative with respect to V_A, the voltage level at pin 4, then an additional current I_O is drawn from the timing pin causing I_T to increase, thus increasing the frequency. Conversely, making V_C higher than V_A causes the frequency to decrease by decreasing I_T.

The frequency of operation, is determined by:

$$f = f_o\left[1 + \frac{R}{R_S} - \frac{V_C}{V_A}\frac{R}{R_S}\right]$$

where $f_o = 1/RC$. $V_A = 3.0V$



EQUIVALENT SCHEMATIC DIAGRAM

Precision Waveform Generator

GENERAL DESCRIPTION

The XR-8038 is a precision waveform generator IC capable of producing sine, square, triangular, sawtooth and pulse waveforms with a minimum number of external components and adjustments. Its operating frequency can be selected over eight decades of frequency, from 0.001 Hz to 200 KHz by the choice of external R-C components. The frequency of oscillation is highly stable over a wide range of temperature and supply voltage changes. Both full frequency sweeping as well as smaller frequency variations (FM) can be accomplished with an external control voltage. Each of the three basic waveforms, i.e., sinewave, triangle and square wave outputs are available simultaneously, from independent output terminals.

The XR-8038 monolithic waveform generator uses advanced processing technology and Schottky-barrier diodes to enhance its frequency performance. It can be readily interfaced with a monolithic phase-detector circuit, such as the XR-2208, to form stable phase-locked loop circuits.

FEATURES

Pin for pin replacement for Intersil 8038
With Improved Sweep Range, Frequency Drift (50 ppm/°C Typ.), and Max. Operating Frequency
Simultaneous Sine, Triangle and Square-Wave Outputs
Low Sine Wave Distortion—THD ≃ 1%
High FM and Triangle Linearity
Wide Frequency Range—0.001 Hz to 200 KHz
Variable Duty-Cycle—2% to 98%

APPLICATIONS

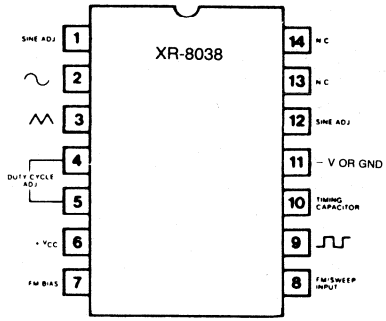
Precision Waveform Generation: Sine, Triangle, Square, Pulse
Sweep and FM Generation
Tone Generation
Instrumentation and Test Equipment Design
Precision PLL Design

ABSOLUTE MAXIMUM RATINGS

Power Supply	36V
Power Dissipation (package limitation)	
Ceramic package	750 mW
Derate above +25°C	6.0 mW/°C
Plastic package	625 mW
Derate above +25°C	5 mW/°C
SO-14	390mW
Derate above +25°C	3mW /°C
Storage Temperature Range	-65°C to +150°C

Note: Combinations of V_{CC}, V_{EE} and timing resistors may exceed the above value. Caution is recommended.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-8038M	Ceramic	−55°C to +125°C
XR-8038N	Ceramic	0°C to +70°C
XR-8038P	Plastic	0°C to +70°C
XR-8038CN	Ceramic	0°C to +70°C
XR-8038CP	Plastic	0°C to +70°C
XR-8038MD	Japanese SOIC	0°C to 70°C

SYSTEM DESCRIPTION

The XR-8038 precision waveform generator produces highly stable and sweepable square, triangle, and sine waves across eight frequency decades. The device time base employs resistors and a capacitor for frequency and duty cycle determination. The generator contains dual comparators, a flip-flop driving a switch, current sources, buffers, and a sine wave converter. Three identical frequency waveforms are simultaneously available. Supply voltage can range from 10V to 30V, or ±5V to ±15V with dual supplies.

Unadjusted sine wave distortion is typically less than 0.7%, with Pin 1 open and 82 kΩ from Pin 12 to Pin 11 (− V or ground). Sine wave distortion may be improved by including two 100 kΩ potentiometers between V_{CC} and − V (or ground), with one wiper connected to Pin 1 and the other connected to Pin 12.

Small frequency deviation (FM) is accomplished by applying modulation voltage to Pins 7 and 8; large frequency deviation (sweeping) is accomplished by applying voltage to Pin 8 only. Sweep range is typically 1000:1.

The square wave output is an open collector transistor; output amplitude swing closely approaches the supply voltage. Triangle output amplitude is typically 1/3 of the supply, and sine wave output reaches 0.22 of the supply voltage.

XR-8038

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_S = \pm 5V$ to $\pm 15V$, $T_A = 25°C$, $R_L = 1\ M\Omega$, $R_A = R_B = 10\ k\Omega$, $C_1 = 3300\ pF$, S_1 closed, unless otherwise specified. See Test Circuit of Figure 1.

PARAMETERS	XR-8038M/XR-8038			XR-8038C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage, V_S								
Single Supply	10		30	10		30	V	
Dual Supplies	±5		±15	±5		±15	V	
Supply Current		12	15		12	20	mA	$V_S = \pm 10V$. See Note 1.
FREQUENCY CHARACTERISTICS (Measured at Pin 9)								
Range of Adjustment								
Max. Operating Frequency	200			200			KHz	$R_A = R_B = 1.5\ k\Omega$, $C_1 = 680$ pf $R_L = 10\ k\Omega$
Lowest Practical Frequency		0.001			0.001		Hz	$R_A = R_B = 1\ M\Omega$, $C_1 =$ 500 μF (Low Leakage Capacitor)
Max. Sweep Frequency of								
FM Input		100			100		kHz	
FM Sweep Range		1000:1			1000:1			S_1 Open. See Notes 2 and 3.
FM Linearity 10:1 Ratio		0.1			0.2		%	S_1 Open. See Note 3.
Range of Timing Resistors	0.5		1000	0.5		1000	kΩ	Values of R_A and R_B
Temperature Stability								
XR-8038M		50	100	—	—	—	ppm/°C	$T_T = 0°C$ to $70°C$ *See note 8
XR-8038AM		125	150				ppm/°C	$T_T = -55°C$ to $+125°C$*See note 8
XR-8038		50	100	—	—	—	ppm/°C	$T_T = 0°C$ to $70°C$ *See note 8
XR-8038C	—	—	—		50		ppm/°C	
Power Supply Stability		0.05			0.05		%/V	See Note 4.
OUTPUT CHARACTERISTICS								
Square-Wave								Measured at Pin 9.
Amplitude (Peak-to-Peak)	0.9	0.98		0.9	0.98		X V_{SPLY}	$R_L = 100\ k\Omega$
Saturation Voltage		0.2	0.4		0.2	0.5	V	$I_{sink} = 2$ mA
Rise Time		100			100		nsec	$R_L = 4.7\ k\Omega$
Fall Time		40			40		nsec	$R_L = 4.7\ k\Omega$
Duty Cycle Adj.	2		98	2		98	%	
Triangle/Sawtooth/Ramp								Measured at Pin 3.
Amplitude (Peak-to-Peak)	0.3	0.33		0.3	0.33		X V_{SPLY}	$R_L = 100\ k\Omega$
Linearity		0.05			0.1		%	
Output Impedance		200			200		Ω	$I_{out} = 5$ mA
Sine-Wave Amplitude (Peak-to-Peak)	0.2	0.22		0.2	0.22		X V_{SPLY}	$R_L = 100\ k\Omega$
Distortion								
Unadjusted		0.7	1.5		0.8	3	%	$R_L = 1\ M\Omega$. See Note 5, 6
Adjusted		0.5			0.5		%	$R_L = 1\ M\Omega$ and 7.

Note 1: Currents through R_A and R_B not included.

Note 2: $V_{SUPPLY} = 20V$

Note 3: Apply sweep voltage at Pin 8.
$V_{CC} - (1/3\ V_{SUPPLY} - 2) \leq V_{PIN\ 8} \leq V_{CC}$
V_{SUPPLY} = Total Supply Voltage across the IC

Note 4: $10V \leq Vs < 30V$ or $\pm 5V \leq Vs \leq 15V$

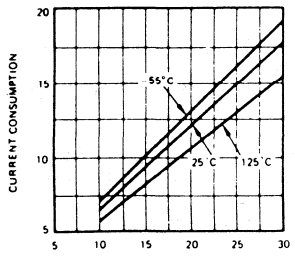
Note 5: 82kΩ resistor connected between Pins 11 and 12

Note 6: Triangle duty cycle set at 50%, use R_A and R_B.

Note 7: As R_L is decreased distortion will increase, R_L min ≈ 50kΩ.

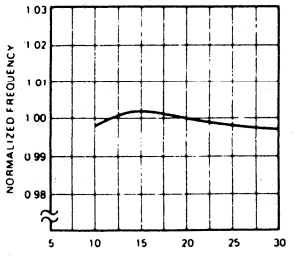
Note 8: Guaranteed but not tested.

CHARACTERISTIC CURVES



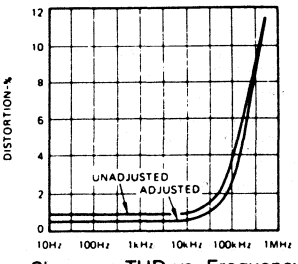
Supply Voltage

Power Dissipation vs. Supply Voltage



Supply Voltage

Frequency Drift vs. Power Supply



Sinewave THD vs. Frequency

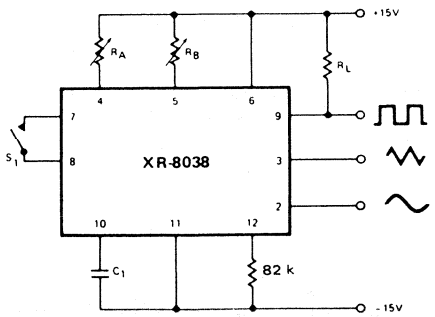


Figure 1. Generalized Test Circuit

PRINCIPLES OF OPERATION

This circuit operates through the charging and discharging of external capacitor C by the currents I_A and $2I_B$. See Figure 3. When switch S is open, current I_A charges capacitor C from $V_{CC} - 2/3\ V_{SUPPLY}$ to $V_{CC} - 1/3\ V_{SUPPLY}$ (V_{SUPPLY} being the total supply voltage across the chip), at which point comparator #1 switches, causing the flip-flop to change state. As a result of the flip-flop changing state, switch S closes, causing capacitor C to be discharged by the current $2I_B - I_A$ since both current sources are now connected to the capacitor. Capacitor C is discharged from $V_{CC} - 1/3\ V_{SUPPLY}$ to $V_{CC} - 2/3\ V_{SUPPLY}$, at which point comparator #2 switches, causing the flip-flop to again change state. Switch S opens, and the cycle begins again with the charging of capacitor C.

The charging and discharging of capacitor C creates a triangle wave voltage across the capacitor, which is connected to pin 10. This pin 10 signal is buffered, and the result is the triangle wave output appearing at pin 3. This buffered triangle wave is passed through a sine-converter network, thus creating the sine wave output at pin 2. The square wave output at pin 9 is simply the buffered output of the flip-flop, which changes its output state as a result of the charge and discharge of capacitor C.

Producing a 50% duty cycle square wave output, a symmetrical triangle (as opposed to sawtooth) wave output, and a symmetrically-shaped sine wave output, require that current I_A be chosen equal to current I_B. When I_A is set equal to I_B, the current I_A charging the capacitor is equal to the net current $2I_B - I_A = I_A$ which alternately discharges the capacitor. As a result of this, the waveform appearing at pin 10 is a symmetrical triangle wave, as is the buffered triangle wave output at pin 3. This symmetrical triangle wave output at pin 3 produces a symmetrically-shaped sine wave output at pin 2. Also, the symmetrical triangle wave at pin 10 causes the flip-flop to produce a 50% duty cycle square wave output at pin 9. Sawtooth wave and asymmetrically-shaped sine and square wave outputs can be produced by setting up currents I_A and I_B to be unequal.

In order to understand how magnitudes for currents I_A and I_B are determined, refer to Figure 4. For typical operation of the 8038, Pin 7, the output of the internal voltage divider, is connected to Pin 8. As a result, a voltage of

$$V_{CC} - \frac{R_2\ V_{SUPPLY}}{R_1 + R_2} = V_{CC} - \frac{V_{SUPPLY}}{5}$$

is present at the ends of both timing resistors R_A and R_B (the ends of R_A and R_B not connected to the positive supply). Consequently,

$$I_A = \frac{V_{CC} - \left(V_{CC} - \frac{V_{SUPPLY}}{5}\right)}{R_A},$$

$$I_A = \frac{V_{SUPPLY}}{5R_A};$$

$$I_B = \frac{V_{SUPPLY}}{5R_B}.$$

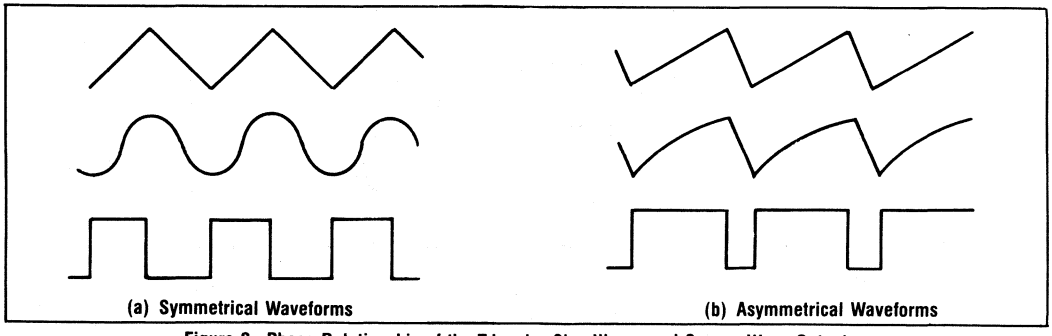


Figure 2. Phase Relationship of the Triangle, Sine Wave, and Square Wave Outputs

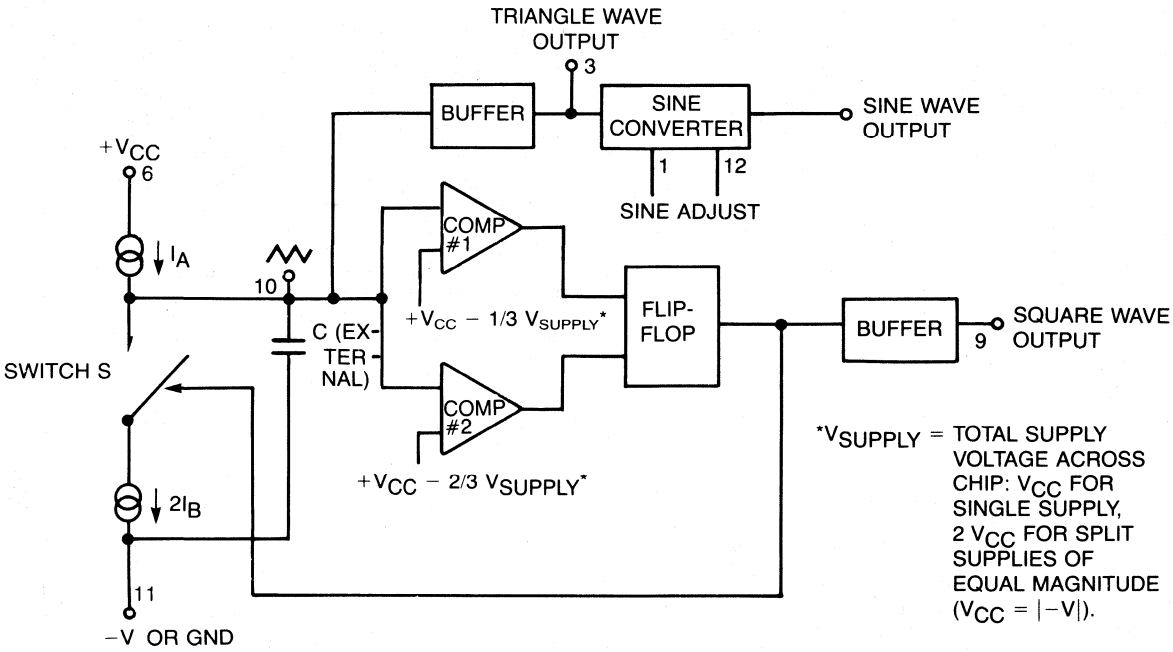


Figure 3. Functional Block Diagram

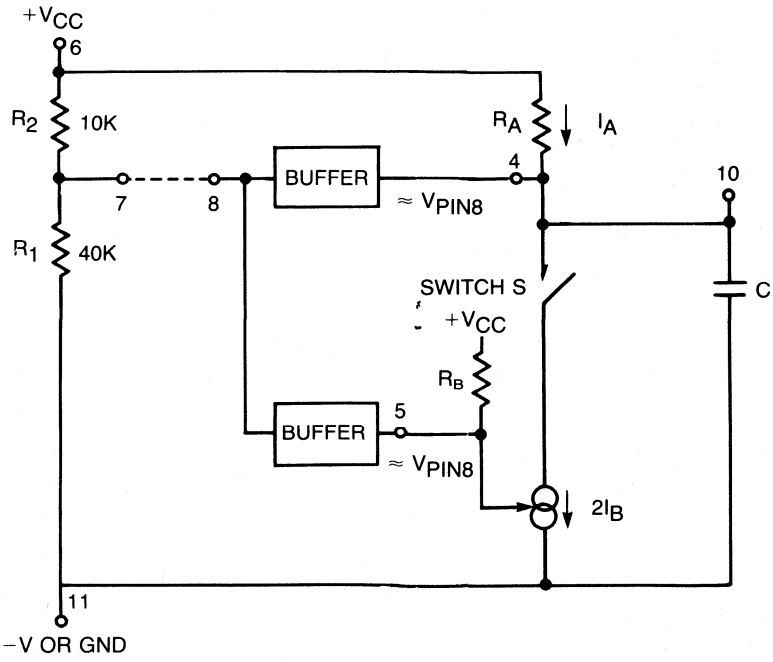


Figure 4. Detailed View of Current Sources I_A and $2I_B$.

For the case of SINGLE-SUPPLY operation, these equations can be simplified to

$$I_A = \frac{V_{CC}}{5R_A} \text{ and } I_B = \frac{V_{CC}}{5R_B}.$$

For the case of SPLIT-SUPPLY operation, where the negative and positive supplies are equal in magnitude, the equations for I_A and I_B can be simplified to

$$I_A = \frac{2V_{CC}}{5R_A} \text{ and } I_B = \frac{2V_{CC}}{5R_B}.$$

WAVEFORM ADJUSTMENT

The equations pertinent to waveform adjustment are derived here assuming single-supply operation (and the connection of pin 7 to pin 8). However, these same equations for t_1, t_2, and f apply to split-supply operation also, regardless of whether the magnitudes of the positive and negative supplies are equal.

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figures 5a and 5b. Best results are obtained by keeping the timing resistors R_A amd R_B separate (5a). R_A controls the rising portion of the triangle and sine waves and the "high" state of the square wave.

Referring to Figure 3, it is apparent that the pin 10 triangle wave will have a minimum amplitude of 1/3 V_{CC} and a maximum amplitude of 2/3 V_{CC}; therefore, the duration of the rising portion of the triangle wave is

$$t_1 = \frac{C \times |\Delta V|}{I_A} = \frac{C \times |2/3\ V_{CC} - 1/3\ V_{CC}|}{\frac{V_{CC}}{5R_A}}$$

$$= \frac{5}{3} R_A C.$$

The duration of the falling portion of the triangle and sine wave and the "low" state of the square wave is

$$t_2 = \frac{C \times |\Delta V|}{2I_B - I_A} = \frac{C \times |1/3\ V_{CC} - 2/3\ V_{CC}|}{\frac{2V_{CC}}{5R_B} - \frac{V_{CC}}{5R_A}}$$

$$= \frac{5}{3} \times \frac{R_A R_B C}{2R_A - R_B}.$$

Thus a 50% duty cycle is achieved when $R_A = R_B$.

If the duty cycle is to be varied over a small range, centered around a duty cycle of 50%, the connection shown in Figure 5b is slightly more convenient. If no adjustment of the duty cycle is desired, pins 4 and 5 can be shorted together, as shown in Figure 5c. This connection, however, carries an inherently larger variation of the duty cycle as frequency is varied.

With two separate timing resistors the *frequency* is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1}{5/3\ R_A C \left(1 + \frac{R_B}{2R_A - R_B}\right)};$$

or, if $R_A = R_B = R$

$$f = 0.3/RC \text{ (for Figure 5a)}$$

If a single timing resistor is used (Figure 5b and c), the frequency is

$$f = 0.15/RC.$$

The frequency accuracy of the 8038 is typically within ±8.5% of the frequency calculated using the above formula f = 0.3/RC (under the test conditions shown at the top of the electrical characteristics section and V_{SUPPLY} = 20V). For tighter frequency accuracies, Pin 8 can be disconnected from Pin 7 and set at $V_{PIN8} = V_{CC} - \frac{V_{SUPPLY}}{5}$. Using this approach, the frequency accuracy of the part is typically within ±4% of the calculated frequency (tested at V_{CC} = V_{SUPPLY} = 20V, V_{PIN8} = 16V).

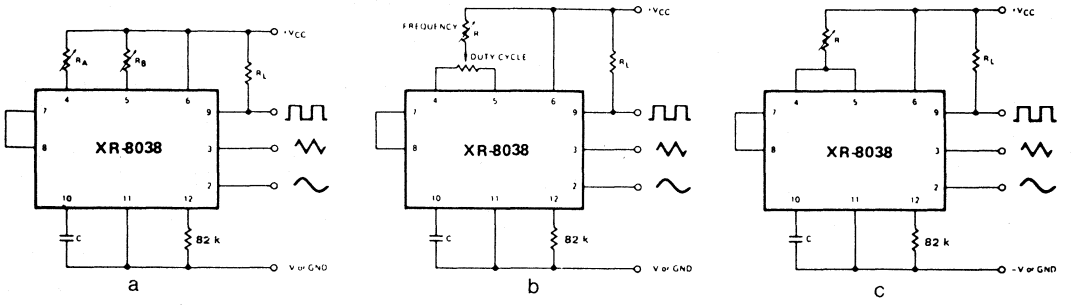


Figure 5. Possible Connections for the External Timing Resistors.

TIMING COMPONENT CONSTRAINTS

For any given output frequency, there is a wide range of RC combinations that will work. However, certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 0.1 μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (I > 5ma), transistor betas and saturation voltages will contribute increasingly large errors. Optimum performance will be obtained for charging currents of 1 μA to 1 mA. To determine the magnitudes of the charging currents I_A and I_B, see the Principles of Operation section.

When the duty cycle is chosen to be greater than 60% or less than 40%, the device may not oscillate every time unless the rise time of the positive supply is ten times slower than the time constant R_A C, for the 60% duty cycle case, or ten times slower than the time constant R_B C, for the 40% duty cycle case. If the rise time of the positive supply is faster than what is required, oscillation can be guaranteed by tying a 0.1 μF capacitor from Pins 7 and 8 to ground.

DISTORTION ADJUSTMENT

To minimize *sine-wave* distortion the 82 kΩ resistor between pins 11 and 12 is best made a variable one. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 6. This configuration allows a reduction of sine-wave distortion close to 0.5%.

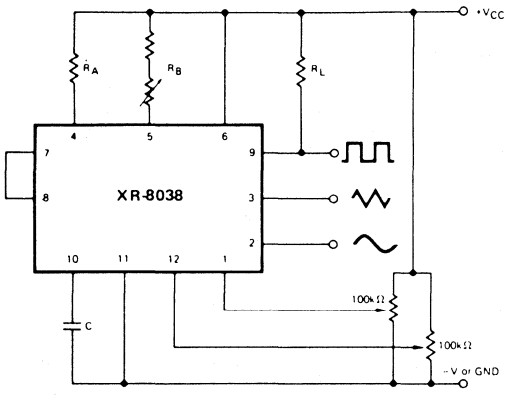


Figure 6. Connection to Achieve Minimum Sine-Wave Distortion.

SINGLE-SUPPLY AND SPLIT-SUPPLY OPERATION

The waveform generator can be operated either from a single power-supply (10 to 30 Volts) or a dual power-supply (±5 to ±15 Volts). With a single power-supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square-wave alternates between $+V_{CC}$ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square-wave output is not committed. A load resistor can be connected to a different power-supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (36V). In this way, the square-wave output will be TTL compatible (load resistor connected to +5 Volts) while the waveform generator itself is powered from a higher supply voltage.

FREQUENCY MODULATION AND SWEEP

The frequency of the waveform generator is an inverse function of the DC voltage at pin 8. In other words, the frequency increases as the pin 8 voltage is swept from its upper limit of V_{CC} (and slightly higher) to its lower limit of approximately $V_{CC} - (1/3\ V_{SUPPLY} - 2)$.

For small deviations (e.g., ±10%), the modulating signal can be applied to pin 8 through a capacitor while pin 8 is connected to pin 7 (or while pin 8 and pin 7 are connected together through a resistor). This mode of operation (shown in Figure 7a) makes use of the DC bias provided by pin 7 and thus eliminates the need for the modulating signal to have a particular DC level. The external resistor between pins 7 and 8 can be used to increase input impedance. Without this resistor (i.e., pins 7 and 8 connected together), the input impedance is 8 KΩ; with it, this impedance increases to (R + 8 KΩ).

For larger FM deviations or for frequency sweeping, Pin 7 is not used. Instead, the entire bias for the 8038 current sources is created by the modulating signal at Pin 8. The circuit of Figure 7b, which shows this mode of operation, will allow a sweep range of typically 1000:1, the frequency approaching 0 Hz when the voltage at Pin 8 is equal to V_{CC} and the frequency reaching its maximum at the lower Pin 8 voltage limit of $V_{CC} - (1/3\ V_{SUPPLY} - 2)$. Waveform symmetry variations which occur when the frequency is swept can be reduced by adding a large fixed resistor (e.g., 10M) or potentiometer from Pin 5 to Pin 11 (GND or − V). Even with this resistor added, there will still be some symmetry variation at lower frequencies (e.g., 200 Hz and lower).

Care must be taken to regulate the supply voltage, as frequency becomes dependent on the supply voltage in this configuration. The frequency of oscillation of this circuit is given by

$$f = \frac{1}{t_1 + t_2}$$

where $$t_1 = \frac{R_A C\, V_{SUPPLY}}{3\,(V_{CC} - V_{PIN8})},$$

and $$t_2 = \frac{R_A\, R_B C\, V_{SUPPLY}}{3\,(V_{CC} - V_{PIN8})\,(2R_A - R_B)};$$

or, if $R_A = R_B = R$

$$t_1 = \frac{RC\, V_{SUPPLY}}{3\,(V_{CC} - V_{PIN8})}$$

and $$t_2 = \frac{RC\, V_{SUPPLY}}{3\,(V_{CC} - V_{PIN8})},$$

V_{SUPPLY} being the total supply voltage across the chip (e.g., V_{SUPPLY} = 20 V for ±10 V split supplies).

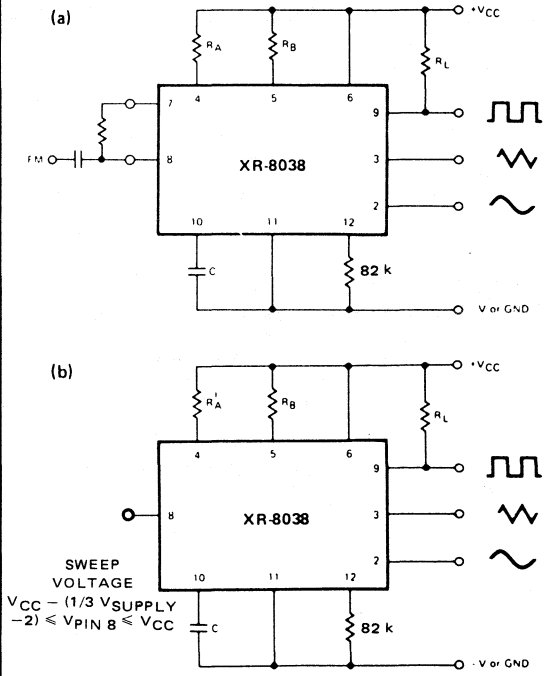


Figure 7. Connections for Frequency Modulation (a) and Sweep (b).

Precision Waveform Generator

GENERAL DESCRIPTION

The XR-8038A is a precision waveform generator IC capable of producing sine, square, triangular, sawtooth, and pulse waveforms, with a minimum number of external components and adjustments. The 8038A allows the elimination of the external distortion adjusting resistor which greatly improves the temperature drift of distortion, as well as lowering external parts count. Its operating frequency can be selected over eight decades of frequency, from 0.001 Hz to 200 KHz, by the choice of external R-C components. The frequency of oscillation is highly stable over a wide range of temperature and supply voltage changes. Both full frequency sweeping as well as smaller frequency variations (FM) can be accomplished with an external control voltage. Each of the three basic waveform outputs, (i.e., sine, triangle and square) are simultaneously available from independent output terminals.

The XR-8038A monolithic waveform generator uses advanced processing technology and Schottky-barrier diodes to enhance its frequency performance. It can be readily interfaced with a monolithic phase-detector circuit, such as the XR-2228 to form stable phase-locked circuits.

FEATURES

Low Frequency Drift	50 ppm/°C, Typical
Simultaneous Sine, Triangle, and Square Wave Outputs	
Low Sine Wave Distortion—THD ≈ 1%	
High FM and Triangle Linearity	
Wide Frequency Range	0.001 Hz to 200 KHz
Variable Duty Cycle	2% to 98%
Low Distortion Variation with Temperature	

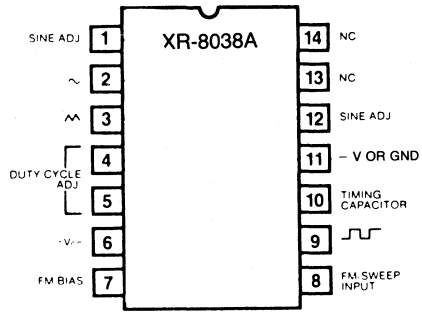
APPLICATIONS

Precision Waveform Generation
Sweep and FM Generation
Tone Generation
Instrumentation and Test Equipment Design
Precision PLL Design

ABSOLUTE MAXIMUM RATINGS

Power Supply	36V
Power Dissipation (package limitation)	
Ceramic Package	750 mW
Derate Above +25°C	6.0 mW/°C
Plastic Package	625 mW
Derate Above +25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-8038AM	Ceramic	−55°C to +125°C
XR-8038AN	Ceramic	0°C to +70°C
XR-8038AP	Plastic	0°C to +70°C
XR-8038ACN	Ceramic	0°C to +70°C
XR-8038ACP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-8038A precision waveform generator produces highly stable and sweepable square, triangle, and sine waves across eight frequency decades. The XR-8038A is an advanced version of the XR-8038, with improved sine distortion temperature drift. The device time base employs resistors and a capacitor for frequency and duty cycle determination. The generator contains dual comparators, a flip-flop driving a switch, current sources, buffers, and a sine wave convertor. Three identical frequency outputs are simultaneously available. Supply voltage can range from 10V to 30V, or ±5V to ±15V with dual supplies.

Unadjusted sine wave distortion is typically less than 0.7% with the sine wave distortion adjust pin (Pin 1) open. Distortion levels may be improved by including a 100kΩ potentiometer between the supplies, with the wiper connected to Pin 1.

Small frequency deviation (FM) is accomplished by applying modulation voltage to Pins 7 and 8; large frequency deviation (sweeping) is accomplished by applying voltage to Pin 8 only. Sweep range is typically 1000:1.

The square wave output is an open collector transistor; output amplitude swing closely approaches the supply voltage. Triangle output amplitude is typically 1/3 of the supply, and sine wave output reaches 0.22 of the supply voltage.

XR-8038A

ELECTRICAL CHARACTERISTICS

Test Conditions: V_S = ±5V to ±15V, T_A = 25°C, R_L = 1 MΩ, R_A = R_B = 10 kΩ, C_1 = 3300 pF, S_1 closed, unless otherwise specified.

PARAMETERS	XR-8038AM/XR-8038A			XR-8038AC			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage, V_S								
Single Supply	10		30	10		30	V	
Dual Supplies	±5		±15	±5		±15	V	
Supply Current		12	15		12	20	mA	V_S = ±10V (Note 1)
FREQUENCY CHARACTERISTICS (Measured at Pin 9)								
Range of Adjustment								
Max. Operating Frequency	200			200			KHz	$R_A = R_B$ = 1.5K, C_1 = 680 pf R_L = 10 K
Lowest Practical Frequency		0.001			0.001		Hz	$R_A = R_B$ = 1 MΩ, C_1 = 500 μF (Low Leakage Capacitor)
Max. Sweep Frequency of FM Input		100			100		kHz	
FM Sweep Range		1000:1			1000:1			S_1 Open (Note 2 & 3)
FM Linearity 10:1 Ratio		0.1			0.2		%	S_1 Open (Note 3)
Range of Timing Resistors	0.5		1000	0.5		1000	kΩ	Values of R_A and R_B
Temperature Stability								
XR-8038AM		50		—	—	—	ppm/°C	T_A = −55°C to +125°C
XR-8038A		50	100					
XR-8038AC					50		ppm/°C	T_A = 0°C to +70°C
Power Supply Stability		0.05			0.05		%/V	(Note 4)
OUTPUT CHARACTERISTICS								
Square-Wave								Measured at Pin 9
Amplitude (Peak-to-Peak)	0.9	0.98		0.9	0.98		x V_{sply}	R_L = 100 kΩ
Saturation Voltage		0.2	0.4		0.2	0.5	V	I_{sink} = 2 mA
Rise Time		100			100		nsec	R_L = 4.7 kΩ
Fall Time		40			40		nsec	R_L = 4.7 kΩ
Duty Cycle Adjustment	2		98	2		98	%	
Triangle/Sawtooth/Ramp								Measured at Pin 3
Amplitude (Peak-to-Peak)	0.3	0.33		0.3	0.33		x V_{sply}	R_L = 100 kΩ
Linearity		0.05		1	0.1		%	
Output Impedance		200			200			I_{out} = 5 mA
Sine-Wave Amplitude (Peak-to-Peak)	0.2	0.22		0.2	0.22		x V_{sply}	R_L = 100 kΩ
Distortion		0.7	1.5		0.8	3	%	R_L = 1 MΩ (Note 5, 6 & 7)
Unadjusted		0.5			0.5		%	R_L = 1 MΩ (Note 5, 6 & 7)
Adjusted		0.5			0.3		%	
ΔTHD/ΔT								

Note 1: Currents through R_A ad R_B not included.

Note 2: V_{SUPPLY} = 20V

Note 3: Apply sweep voltage at Pin 8.

$V_{CC} - (1/3\ V_{SUPPLY} - 2) \leq V_{PIN8} \leq V_{CC}$ V_{SUPPLY} = total supply voltage across the IC.

Note 4: 10V ≤ V_S ≤ 30V or ±5V ≤ V_S ≤ ±15V.

Note 5: Pin 12 open circuited (No 82 kΩ resistor as standard 8038).

Note 6: Triangle duty cycle set to 50%, use R_A and R_B.

Note 7: As R_L is decreased distortion will increase, R_L min. ≈ 50 kΩ.

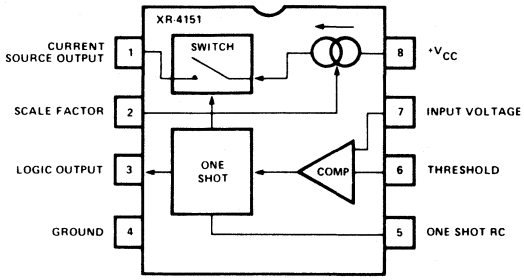
5

Voltage-to-Frequency Converter

GENERAL DESCRIPTION

The XR-4151 is a device designed to provide a simple, low-cost method for converting a DC voltage into a proportional pulse repetition frequency. It is also capable of converting an input frequency into a proportional output voltage. The XR-4151 is useful in a wide range of applications including A/D and D/A conversion and data transmission.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Single Supply Operation (+8V to +22V)
Pulse Output Compatible With All Logic Forms
Programmable Scale Factor (K)
Linearity ±0.05% Typical–Precision Mode
Temperature Stability ±100% ppm/°C Typical
High Noise Rejection
Inherent Monotonicity
Easily Transmittable Output
Simple Full Scale Trim
Single-Ended Input, Referenced to Ground
Also Provides Frequency-to-Voltage Conversion
Direct Replacement for RC/RV4151

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-4151P	Plastic	−40°C to +85°C
XR-4151CP	Plastic	0°C to +70°C

APPLICATIONS

Voltage-to-Frequency Conversion
A/D and D/A Conversion
Data Transmission
Frequency-to-Voltage Conversion
Transducer Interface
System Isolation

ABSOLUTE MAXIMUM RATINGS

Power Supply	22V
Output Sink Current	20 mA
Internal Power Dissipation	500 mW
Input Voltage	−0.2V to +V_{CC}
Output Short Circuit to Ground	Continuous

SYSTEM DESCRIPTION

The XR-4151 is a precision voltage to frequency convertor featuring 0.05% conversion linearity (precision mode), high noise rejection, monotonicity, and single supply operation from 8V to 22V. An RC network on Pin 5 sets the maximum full scale frequency. Input voltage on Pin 7 is compared with the voltage on Pin 6 (which is generally controlled by the current source output, Pin 1). Frequency output is proportioned to the voltage on Pin 7. The current source is controlled by the resistance on Pin 2 (nominally 14kΩ with I = 1.9 V/R. The output is an open collector at Pin 3.

ELECTRICAL CHARACTERISTICS

Test Conditions: (V_{CC} = 15V, T_A = +25°C, unless otherwise specified)

PARAMETERS	XR-4151CP MIN	XR-4151CP MAX	XR-4151P MIN	XR-4151P MAX	TYP	UNITS	CONDITIONS
Supply Current	2.0	6.0	2.0	6.0	3.5	mA	8V<V_{CC}<15V
	2.0	7.5	2.0	7.5	4.5	mA	15V<V_{CC}<22V
Conversion Accuracy Scale Factor	0.90	1.10	0.92	1.08	1.00	kHz/V	Circuit of Fig. 3, V_I= 10V R_S = 14.0k
Drift with Temperature	-	-	-	-	±100	ppm/°C	Circuit of Fig. 3, V_I= 10V
Drift with V_{CC}	-	-	-0.9	0.9	0.2	%/V	Circuit Fig. 3, VI=1.0V 8V<V_{CC}<18V
Input Comparator							
Offset Voltage	-	10	-	10	5	mV	
Offset Current	-	±100	-	±100	±50	nA	
Input Bias Current	-	-300	-	-300	-100	nA	
Common Mode Range (Note 1)	0	V_{CC}-3.0	0	V_{CC}-3.0	0 to V_{CC} -2	V	
One-Shot							
Threshold Voltage, Pin 5	0.63	0.70	0.63	0.70	.667	xV_{CC}	
Input Bias Current, Pin 5	-	-500	-	-500	-100	nA	
Reset V_{SAT}	-	50.0	-	50.0	0.15	V	Pin 5, 1 = 2.2mA
Current Source							
Output Current	-	-	-	-	138.7	µA	Pin 1,V=0, RS=14.0kΩ
Change with Voltage	-	2.5	-	2.5	1.0	µA	Pin 1,V=0V to V=10V
Off Leakage	-	50.0	-	50.0	0.15	nA	Pin 1, V = 0V
Reference Voltage	1.70	2.08	1.70	2.08	1.9	V	Pin 2
Logic Output							
V_{SAT}	-	0.50	-	0.50	0.15	V	Pin 3, 1 = 3.0mA
V_{SAT}	-	0.30	-	0.30	0.10	V	Pin 3, 1 = 3.0mA
Off Leakage	-	1.0	-	1.0	.1	µA	

Note 1: Input Common Mode Range includes ground.

PRINCIPLES OF OPERATION

SINGLE SUPPLY MODE VOLTAGE-TO-FREQUENCY CONVERTER

In this application, the XR-4151 functions as a stand-alone voltage-to-frequency converter operating on a single positive power supply. Refer to the functional block diagram and Figure 3, the circuit connection for single supply voltage-to-frequency conversion. The XR-4151 contains a voltage comparator, a one-shot, and a precision switched current source. The voltage comparator compares a positive input voltage applied at pin 7 to the voltage at pin 6. If the input voltage is higher, the comparator will fire the one-shot. The output of the one-shot is connected to both the logic output and the precision switched current source. During the one-shot period, T, the logic output will go low and the current source will turn on with current I. At the end of the one shot period the logic output will go high and the current source will shut off. At this time the current source has injected an amount of charge Q = I_OT into the network R_B–C_B. If this charge has not increased the voltage V_B such that V_B > V_I, the comparator again fires the one-shot and the current source injects another lump of charge, Q, into the R_B–C_B network. This process continues until V_B > V_I. When this condition is achieved, the current source remains off and the voltage V_B decays until V_B is again equal to V_I. This completes one cycle. The VFC will now run in a steady state mode. The current source dumps lumps of charge into the capacitor C_B at a rate fast enough to keep $V_B \geq V_I$. Since the discharge rate of capacitor C_B is proportional to V_B/R_B, the frequency at which the system runs will be proportional to the input voltage.

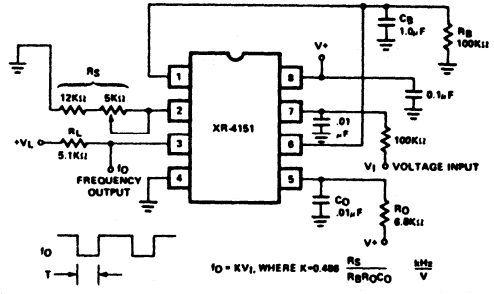


Figure 3. Voltage-to-Frequency Converter

TYPICAL APPLICATIONS

SINGLE SUPPLY VOLTAGE-TO-FREQUENCY CONVERTER

Figure 3 shows the simplest type of VFC that can be made with the XR-4151. The input voltage range is from 0 to +10V, and the output frequency is from 0 to 10 kHz. The full scale frequency can be tuned by adjusting R_S, the output current set resistor. This circuit has the advantage of being simple and low in cost, but it suffers from inaccuracy due to a number of error sources. Linearity error is typically 1%. A frequency offset will also be introduced by the input comparator offset voltage. Also, response time for this circuit is limited by the passive integration network R_B C_B. For the component values shown in Figure 3, response time for a step change input from 0 to +10V will be 135 msec. For applications which require fast response time and high accuracy, use the circuit of Figure 4. C_B should have a high stability dielectric (mica, polystyrene, polyester).

PRECISION VOLTAGE-TO-FREQUENCY CONVERTER

In this application (Figure 4) the XR-4151 is used with an operational amplifier integrator to provide typical linearity of 0.05% over the range of 0 to −10V. Offset is adjustable to zero. Unlike many VFC designs which lose linearity below 10mV, this circuit retains linearity over the full range of input voltage, all the way to 0V.

Trim the full scale adjust pot at V_I = −10V for an output frequency of 10kHz. The offset adjust pot should be set for 10Hz with an input voltage of −10mV.

The operational amplifier integrator improves linearity of this circuit over that of Figure 3 by holding the output of the source, Pin 1, at a constant 0V. Therefore, the linearity error due to the current source output conductance is eliminated. The diode connected around the op-amp prevents the voltage at pin 7 of the XR-4151 from going below 0. Use a low-leakage diode here, since any leakage will degrade the accuracy. This circuit can be operated from a single positive supply if an XR-3403 ground-sensing op-amp is used for the integrator. In this case, the diode can be left out. Note that even though the circuit itself will operate from a single supply, the input voltage is necessarily negative. For operation above 10kHz, bypass pin 6 of the XR-4151 with .01μF.

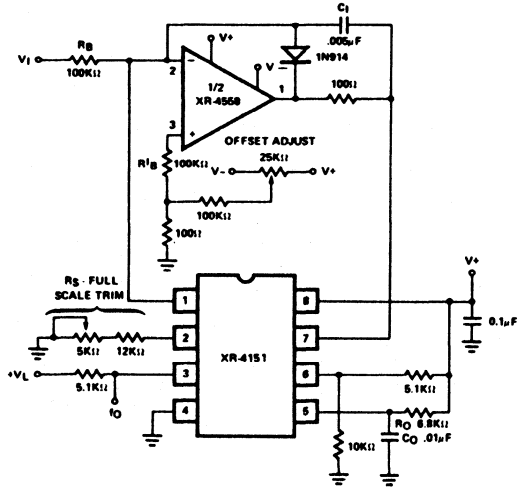


Figure 4. Precision Voltage-to-Frequency Converter

FREQUENCY-TO-VOLTAGE CONVERSION

The XR-4151 can be used as a frequency-to-voltage converter. Figure 5 shows the single-supply FVC configuration. With no signal applied, the resistor bias networks tied to pins 6 and 7 hold the input comparator in the off state. A negative going pulse applied to pin 6 (or positive pulse to pin 7) will cause the comparator to fire the one-shot. For proper operation, the pulse width must be less than the period of the one-shot, T = 1.1 R_O C_O. For a 5V p-p square-wave input the differentiator network formed by the input coupling capacitor and the resistor bias network will provide pulses which correctly trigger the one-shot. An external voltage comparator can be used to "square-up" sinusoidal input signals before they are applied to the XR-4151. Also, the component values for the input signal differentiator and bias network can be altered to accommodate square waves with different amplitudes and frequencies. The passive integrator network R_B C_B filters the current pulses from the pin 1 output. For less output ripple, increase the value of C_B.

For increased accuracy and linearity, use an operational amplifier integrator as shown in Figure 6, the precision FVC configuration. Trim the offset to give −10mV out with 10Hz in and trim the full scale adjust for −10V out with 10kHz in. Input signal conditioning for this circuit is necessary just as for the single supply mode and the scale factor can be programmed by the choice of component values. A tradeoff exists between the amount of output ripple and the response time, through the choice or integration capacitor C_I. If C_I = 0.1 μf the ripple will be about 100mV. Response time constant τR = R_B C_I. For R_B = 100 kΩ and C_I = 0.1 μf, τR = 10msec.

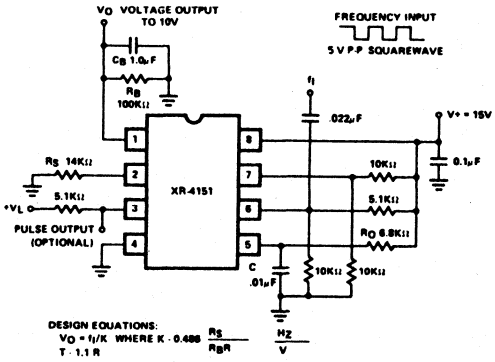


Figure 5. Frequency-to-Voltage Converter

PRECAUTIONS

1. The voltage applied to comparator input pins 6 and 7 should not be allowed to go below ground by more than 0.3 volt.

2. Pins 3 and 5 are open-collector outputs. Shorts between these pins and $+V_{CC}$ can cause overheating and eventual destruction.

3. Reference voltage terminal pin 2 is connected to the emitter of an NPN transistor and is held at approximately 1.9 volts. This terminal should be protected from accidental shorts to ground or supply voltages. Permanent damage may occur if the current in pin 2 exceeds 5mA.

4. Avoid stray coupling between pins 5 and 7; it could cause false triggering. For the circuit of Figure 3, bypass pin 7 to ground with at least 0.01μf. This is necessary for operation above 10kHz.

5. **C_B for stability overtime should have a silver mica, polystyrene or polyester di-eletric.**

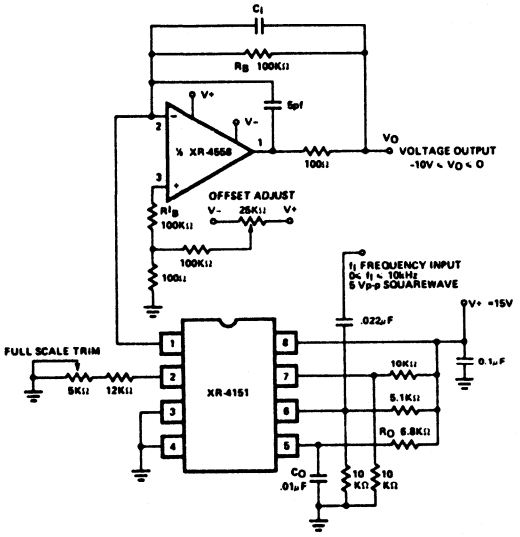


Figure 6. Precision Frequency-to-Voltage Converter

PROGRAMMING THE XR-4151

The XR-4151 can be programmed to operate with a full scale frequency anywhere from 1.0Hz to 100kHz. In the case of the VFC configuration, nearly any full scale input voltage from 1.0V and up can be tolerated if proper scaling is employed. Here is how to determine component values for any desired full scale frequency.

1. Set R_S = 14kΩ or use a 12k resistor and 5k pot as shown in the figures. (The only exception to this is Figure 4.)

2. Set $T = 1.1\ R_0C_0 = 0.75[1/fo]$ where fo is the desired full scale frequency. For optimum performance make 6.8kΩ $> R_0 >$ 680kΩ and 0.001μf $< C_0 <$ 1.0μf.

3. a) For the circuit of Figure 3 make $C_B = 10^{-2}$ [1/fo] Farads.

   Smaller values of C_B will give a faster response time, but will also increase the frequency offset and nonlinearity.

   b) For the active integrator circuit make

   $C_I = 5 \times 10^{-5}$ [1/fo] Farads.

   The op-amp integrator must have a slew rate of at least $135 \times 10^{-6}\ [1/C_1]$ volts per second where the value of C_1 is in Farads.

4. a) For the circuit of Figure 4 keep the values of R_B and R_B as shown and use an input attenuator to give the desired full scale input voltage.

   b) For the precision mode circuit of Figure 4, set $R_B = V_{IO}/100\mu A$ where V_{IO} is the full scale input voltage.

   Alternately, the op-amp inverting input (summing node) can be used as a current input with the full scale input current $I_{IO} = -100\mu A$.

5. For the FVC's, pick the value of C_B or C_I to give the optimum tradeoff between the response time and output ripple for the particular application.

DESIGN EXAMPLE

I. Design a precision VFC (from Figure 5) with fo = 100kHz and $V_{IO} = -10V$.

1. Set R_S = 14.0kΩ

2. $T = 0.75\ [1/10^5] = 7.5\mu$sec

   Let R_0 = 6.8kΩ and C_0 = 0.001μf.

3. $C_I = 5 \times 10^5\ [1/10^5] = 500$pf.

   Op-amp slew rate must be at least

   $SR = 135 \times 10^6\ [1/500pf] = 0.27V/\mu$sec

4. R_B = 10V/100μA = 100kΩ.

II. Design a precision VFC with fo = 1Hz and V_{IO} = 10V.

1. Let R_S = 14.0kΩ

2. $T = 0.75\ [1/1] = 0.75$ sec

   Let R_0 = 680kΩ and C_0 = 1.0μf.

3. $C_I = 5 \times 10^{-5}\ [1/1]F = 50\mu$f.

4. R_B = 100kΩ.

III. Design a single supply FVC to operate with a supply voltage of 9V and full scale input frequency fo = 83.3 Hz. The output voltage must reach at least 0.63 of its final value in 200msec. Determine the output ripple.

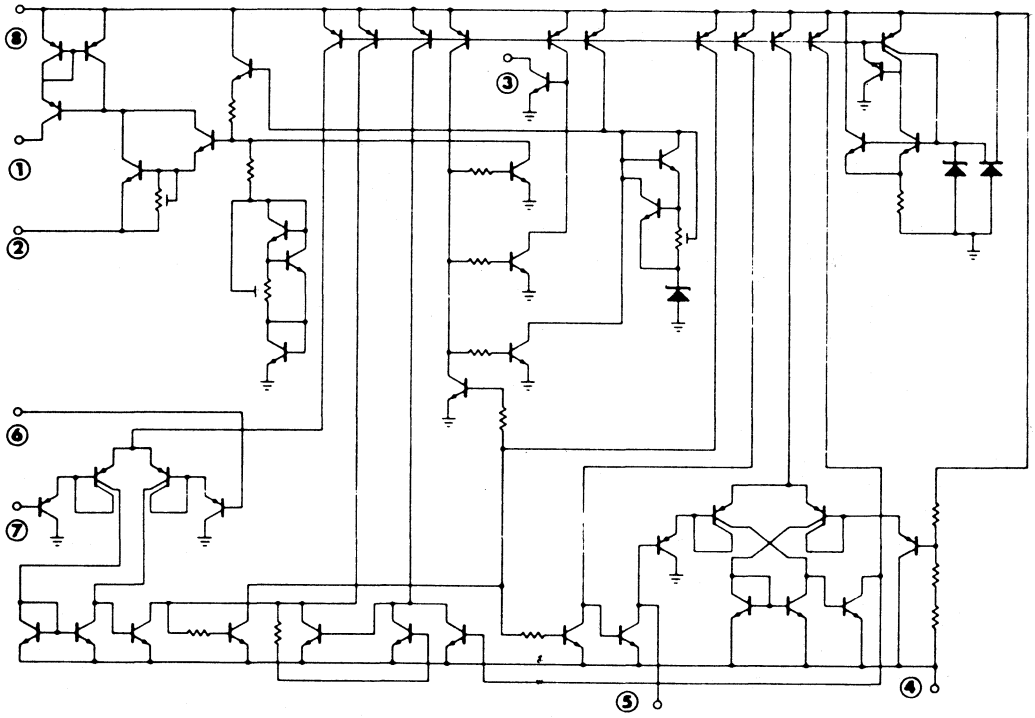
1. Set R_S = 14.0kΩ
2. T = 0.75 [1/83.3] = 9msec

   Let R_0 = 82kΩ and C_O = 0.1 μf.
3. Since this FVC must operate from 8.0V, we shall make the full scale output voltage at pin 6 equal to 5.0V.
4. R_B = 5V/100μA = 50kΩ.
5. Output response time constant is $\tau R \leq 200$ msec
   Therefore-

   $C_B \leq \tau_R/R_B = (200 \times 10^{-3})/(50 \times 10^3) = 4\mu f$

   Worst case ripple voltage is

   V_R = (9mS × 135μA) / 4μf = 304mV.



EQUIVALENT SCHEMATIC DIAGRAM

General Purpose Low Pass Filter

GENERAL DESCRIPTION

Each of these devices in the series is a fourth order switched capacitor low pass filter providing 24 dB/octave (Butterworth) of roll off outside of the pass band. Within this series Butterworth, Bessel or Chebyshev (0.5 or 0.1 dB of ripple) filter responses can be obtained. Also, each filter response is available in either a 50:1 or 100:1 clock-to-corner ratio device for added flexibility. All devices have the same pin out (8 pin dual-in-line), so one can easily be substituted for the other, depending on the application.

Switched capacitor filters provide the ability to tune the corner frequency of the filter response with the adjustment of the input clock. The XR-1001/1008 can also be used in a stand alone mode, where an external resistor and capacitor will set the input clock frequency. For additional precision, a external crystal can be used to set the corner frequency.

The XR-1001 is pin-for-pin compatible with the MF-4-100 and the XR-1002 in pin-for-pin compatible with the MF-4-50. The XR-1001/1008 are fabricated in 3 micron dual-polysilicon gate single metal CMOS for additional performance over other processes.

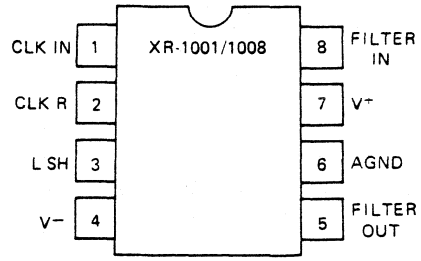
FEATURES

Single 5 Volt Operation
Low Power Consumption
Precise Filter Positioning
Stand Alone Mode with RC or Crystal
Low Noise – Typically –78 dBm
Corner Frequency Adjustable to 40 kHz

APPLICATIONS

Mechanical Processes
Telecommunications
Instrumentation
Anti-alias Filters
Reconstruction Filters
Digital Signal Processing
Musical Effects

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply (Single Supply)	14 V
Input Signal Level	$V^+ - 0.7$ to $V^- + 0.7$ V
Power Dissipation (Package Limitation)	
Ceramic Package	385 mW
Derate Above $T_A = 25°C$	5 mW/°C
Plastic Package	300 mW
Derate Above $T_A = 25°C$	6 mW/°C
Storage Temperature Range	–65°C to +150°C

SYSTEM DESCRIPTION

The XR-1001 and XR-1002 with its Butterworth filter response is suitable for applications where the pass band must be maximally flat, such as instrumentation. The XR-1003 and XR-1004 with the Bessel filter response has a maximally flat group delay response. This is ideal for telecommunication and modem applications where phase distortion would affect the performance. The XR-1005 through XR-1008 provide the Chebyshev filter response. With the Chebyshev filter response, the roll-off outside of the pass band is steeper and attenuates out-of-band signals greater than the Bessel or Butterworth responses. The ripple in the band is larger to obtain the steeper roll-off. The application will determine the amount of ripple which can be accepted within the pass band of the filter response.

Part Number	Package	Response/Ripple	f_{clock}/f_{corner}	Operating Temperature
XR-1001CP/CN	Plastic/Ceramic	Butterworth	100:1	0°C to 70°C
XR-1002CP/CN	Plastic/Ceramic	Butterworth	50:1	0°C to 70°C
XR-1003CP/CN	Plastic/Ceramic	Bessel	100.1	0°C to 70°C
XR-1004CP/CN	Plastic/Ceramic	Bessel	50:1	0°C to 70°C
XR-1005CP/CN	Plastic/Ceramic	Chebyshev (0.1dB)	100:1	0°C to 70°C
XR-1006CP/CN	Plastic/Ceramic	Chebyshev (0.1 dB)	50:1	0°C to 70°C
XR-1007CP/CN	Plastic/Ceramic	Chebyshev (0.5 dB)	100:1	0°C to 70°C
XR-1008CP/CN	Plastic/Ceramic	Chebyshev (0.5 dB)	50:1	0°C to 70°C

ELECTRICAL CHARACTERISTICS

Test Conditions: V^+ = 5 VDC, V^- = −5 VDC, f_{CLOCK} = 1 MHz, R_{Load} = 1 Megohm, C_{Load} = 40 pF, T_A = 25°C, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
GENERAL CHARACTERISTICS						
V_{DD}	Supply Voltage					
	Single Supply	4.5		11.0		VDC Referenced to V_{SS}
	Split Supply	+2.25		5.5		VDC (Pin 4)
V_{SS}	Supply Voltage					
	Split Supply	-5.5		-2.25		VDC Reference to AGND (Pin 6)
I_{DD}	Supply Current					
	Single Supply		2.5	3.5	mA	V_{DD} = 10.0 VDC
	Split Supply		2.5	3.5	mA	V_{DD} = -5 VDC
	Split Supply		1.50	2.25	mA	V_{DD} = 2.25 VDC
I_{SS}	Supply Current					
	Split Supply	-3.5	-2.5		mA	V_{DD} = 5.0 VDC, V_{SS} = -5.0 VDC
	Split Supply	-2.25	-1.5		mA	V_{DD} = +2.25 VDC, V_{SS} = -2.25
FILTER CHARACTERISTICS						
$f_{CLOCKMAX}$	Upper Clocking Freq. Limit	1.0	1.5		MHz	
$f_{CLOCKMIN}$	Lowest Practical Clock		100		Hz	For 1001,1003,1005,1007
			50		Hz	For 1002,1004,1006,1008
	Gain at Corner Frequency	-3.5	-3	-2.5	dB	
$A_{2f_{corner}}$	Attenuation at 2 Times					
	The Corner Frequency	23	24.6	26	dB	For 1001,1002
		11	13	14	dB	For 1003,1004
		30	31	33	dB	For 1005,1006
		33	34	36	dB	For 1007,1008
V_{out}	Maximum Output Signal	8			Vpp	Input = ±4.2 VDC
$e_{n\ out}$	Output Noise		0.5		mvrms	From 1 Hz to 25 kHz
S/N	Signal-to-Noise Ratio		84		dB	
THD	Total Harmonic Distortion		0.1		%	V_{in} = 2.4 Vrms, f_{in} = 1 kHz
V_{OS}	Output Offset Voltage (DC)	-0.4		+0.4	VDC	f_{clock} = 1 MHz
	Clock Feedthrough		50		mvpp	
I_{OSS}	Output Short Circuit					
	Current Source	-60	-50		mA	See Note #1
	Sink		30	50	mA	
	Temperature Coefficient					
	Of f_{corner}		±35		ppm/°C	From -40°C to + 85°C ; not tested in production
	Passband Gain					
	For 1001,1002	-0.3	0	+0.3	dB	Tested at 3 and 5 kHz for 1001,1003,1005,1007
	For 1003,1004	-1.0	-0.1	+0.2	dB	Tested at 6 and 10 kHz for 1002,1004,1006,1008
	For 1005,1006	-0.4	-0.1	+0.3	dB	
	For 1007,1008	-0.7	-0.2	+0.3	dB	

#1 Caution should be used so that the power dissipation does not exceed the package limitation.

	Passband Gain For 1001,1002 For 1003,1004 For 1005,1006 For 1007,1008	 -0.7 -2.0 -0.3 0.7	 -0.06 -1.5 -0.1 -0.2	 -0.0 -1.0 +0.3 +0.3	 dB dB dB dB	 Tested at 7.5 kHz for 1001,1003,1005,1007 Tested at 15 kHz for 1002,1004,1006,1008
FILTER CHARACTERISTICS: $V^+ = 2.25$, $V^- = -2.25$ VDC						
$f_{CLOCKMAX}$	Upper Clocking Freq. Limit	0.25	0.5		MHz	
$f_{CLOCKMIN}$	Lower Practical Clock		100 50		Hz Hz	For 1001,1003,1005,1007 For 1002,1004,1006,1008
$A_{2f_{corner}}$	Attenuation at 2 Times The Corner Frequency	23 11 30 33	24.6 13 31 34	26 14 33 36	dB dB dB dB	For 1001,1002 For 1003,1004 For 1005,1006 For 1007,1008
	Maximum Output Signal	3	4		Vpp	Vin = ±2.0 VDC
S/N	Signal-to-Noise Ratio		76		dB	
V_{OS}	DC Offset Voltage	-0.4	±0.05	+0.4	VDC	
LOGIC INPUT & LOGIC OUTPUT TESTS: V = ±2.25 VDC and V = ±5 VDC, Pin 3 tied to V_{SS}						
	Schmitt Trigger Input					
V_{T+}	Positive Going Threshold Voltage	0.6 0.0	1.3 0.55	2.0 +1.1	V V	V = ±5.0 VDC V = ±2.25 VDC
V_{T-}	Negative Going Threshold Voltage	-1.4 -0.6	-0.7 -0.2	0.0 +0.4	V V	V = ±5.0 VDC V = ±2.25 VDC
$V_{T+}-V_{T-}$	Hysteresis	0.8 0.2	2.1 0.75	2.9 1.3	V V	V = ±5.0 VDC V = ±2.25 VDC
V_{OH}	Output High Voltage	4.5 2.03			V V	V = ±5.0 VDC V = ±2.25 VDC, I_O = 400μA
V_{OL}	Output Low Voltage	1 0.5			V V	V = ±5.0 VDC V = ±2.25 VDC, I_O = 400μA
I_{OS}	Output Sink Current Output Source Current	2.5 0.65 3.0 0.75	5.0 1.3 6.0 1.5		mA mA mA mA	V = ±5.0 VDC V = ±2.25 VDC V = ±5.0 VDC V = ±2.25 VDC
TTL CLOCK INPUT: V = ±5.0 VDC, Pin 3 tied to 0 VDC						
V_{IL}	Input Low Voltage		0.8		V	
V_{IH}	Input High Voltage		2.8		V	
STAND ALONE OPERATION: R = 5.0 kilohms and C = 120 pF for f_O = 985 kHz						
f_O	Frequency Accuracy of Oscillator	-15	±4	+15	%	Measured at Pin 2 Error increases at lower f_O (<500kHz). See Figure 3.

5

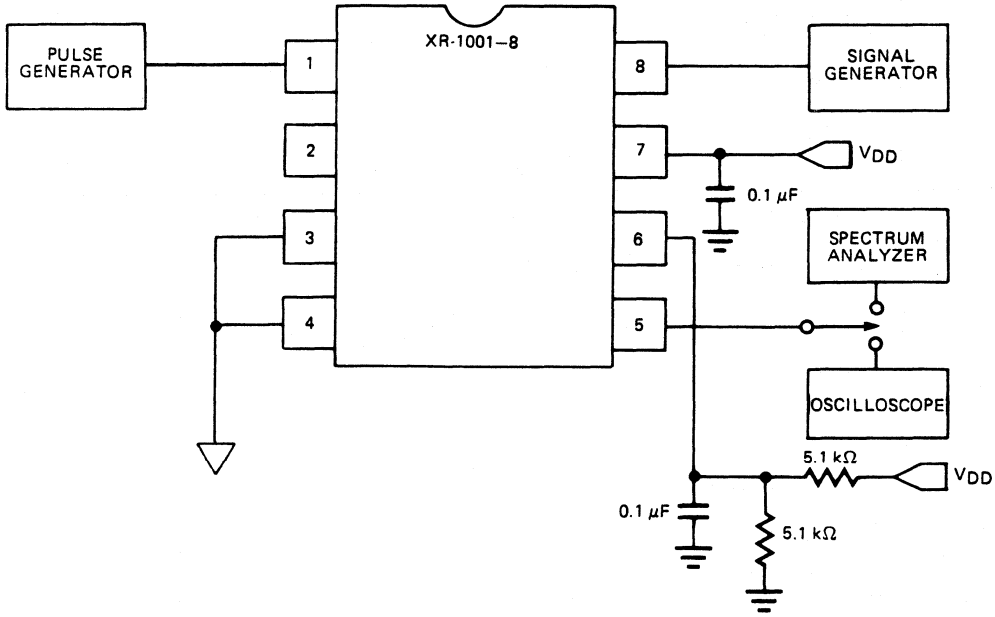


Figure 1. Single Supply Test Circuit

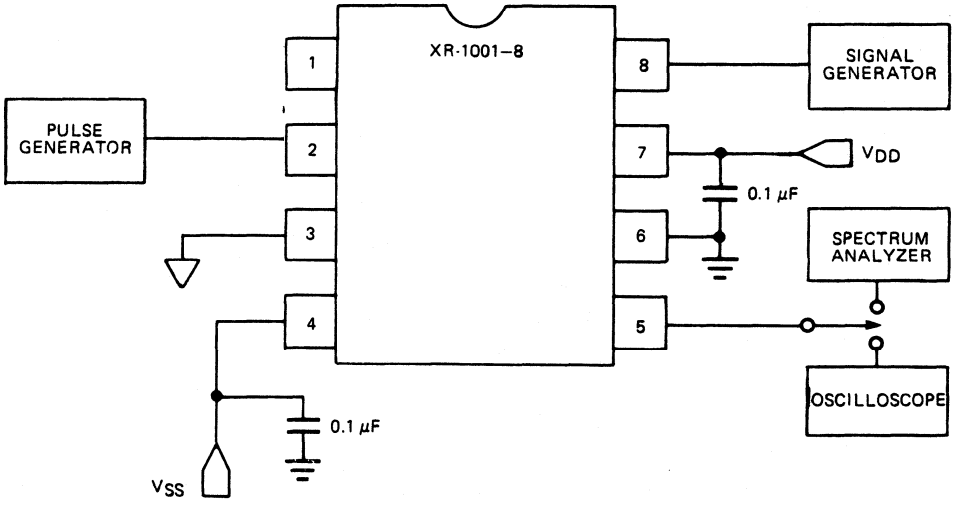


Figure 2. Split Supply Test Circuit

XR-1001/1008 PIN DESCRIPTIONS

Pin	Numonic	Description
1	CLKIN	Clock Input: This input pin is for application of the MOS-level clock used for sampling and switching. For best results, this clock should be approximately 50% duty cycle. A crystal can be used from Pin 1 to Pin 2 to create a self-contained oscillator. A 10 megohm resistor should be hooked up in parallel with the crystal The maximum clock frequency is > 1 MHz. For stand alone operation with a resistor and capacitor, the capacitor should be tied from this point to ground.
2	CLKR	Clock Resistor: This is an inverted output of signal found on Pin 1. It is used for creating a crystal oscillator or a RC network can be used. The resistor would be tied back to Pin 1. The frequency of oscillation would be equal to 1/(1.7xRC). It is also used **as the TTL-level clock input. Figure 4 shows the connections for RC mode.**
3	LSH	Level Shift: This input is used to set the logic zero point of the clock input. For MOS level clocks, it should be tied to VSS. For TTL-level clock. it should be grounded (split supply). For single supply operation, MOS level clock operation is recommended. When a crystal and resistor, or a resistor and capacitor are used to create an oscillator, the level shift pin should be tied to VSS.
4	V−	VSS: This is the negative supply. It should have substantial decoupling to prevent noise on the output of the filter. A minimum 0.1 μF capacitor to ground as close to the device as possible is strongly recommended. The range of operation for dual supplies is from −2.5 VDC to −5 VDC. This device can also be operated from ground positive. In this case, the VSS pin is tied to the analog ground of the circuit. The quality of the ground in this mode of operation is very important. It should be very low in series inductance.
5	FILTEROUT	Filter Ouput: This is the output of the low pass filter. A 10 kilohm load or larger is the smallest load recommended for the output.
6	AGND	Analog Ground: This should be tied to the analog ground of the circuit the device is being used in. The filter output of this device will swing around this potential. For single supply operation, this pin is externally biased at a point one half of the VDD voltage. A 0.1 μF capacitor is the minimum capacitance needed for decoupling with single supply operation.
7	V+	VDD: The positive supply is tied here. Since this pin is also common with the substrate, a 0.1 μF and 1 μF capacitor to ground is recommended to decouple any noise on the positive supply. The range of operation is from +5 to +10 VDC for single supply operation. For dual supply operation, +2.5 to +5 VDC can be applied to this pin.
8	FILTERIN	This is the input of the low pass filter. The input signal should be biased to mid-supply before applying to this pin. Also, to prevent alias frequencies from being created, the input frequency should be less than ½ of the clock frequency.

5

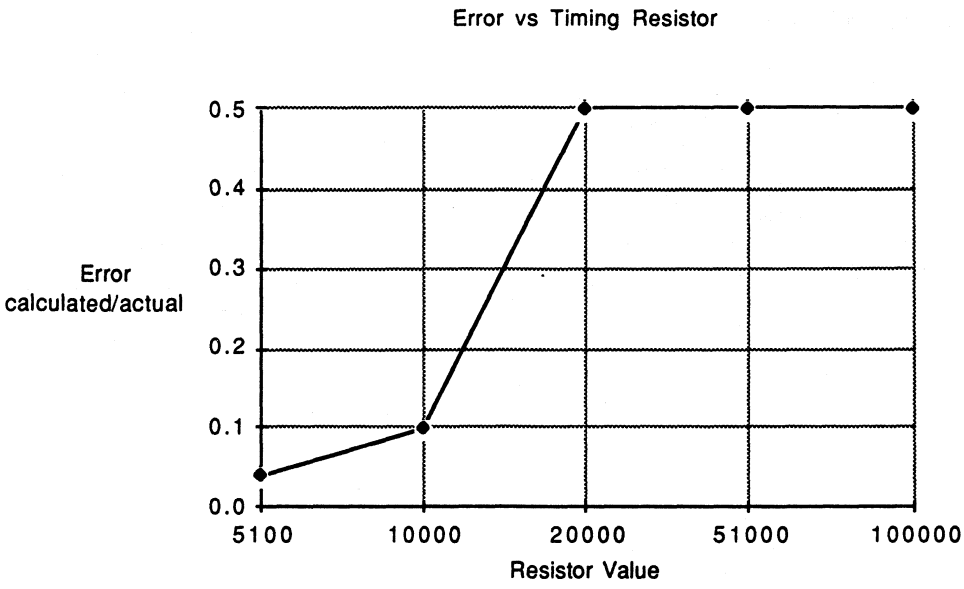


Figure 3

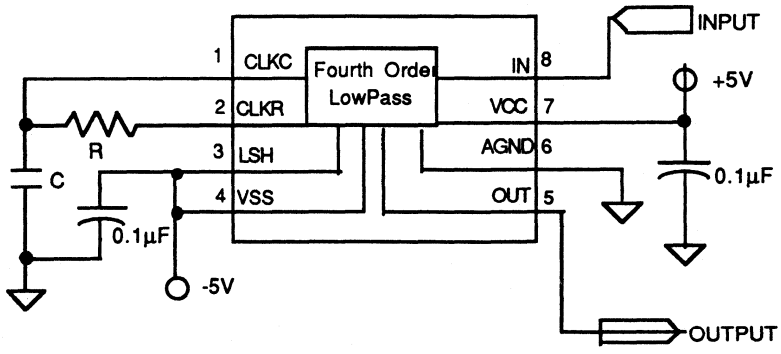
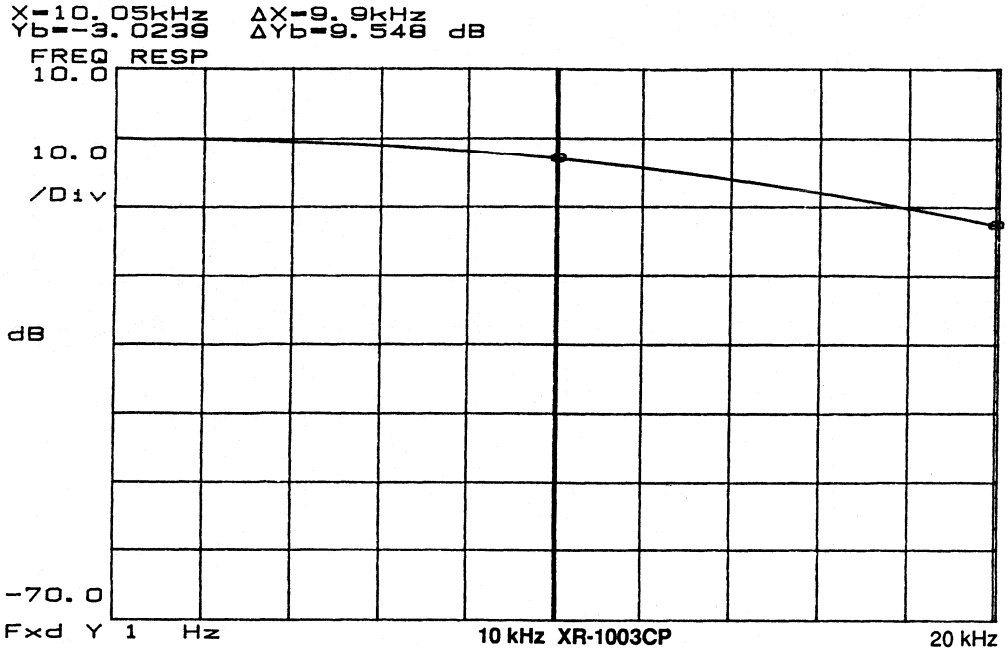
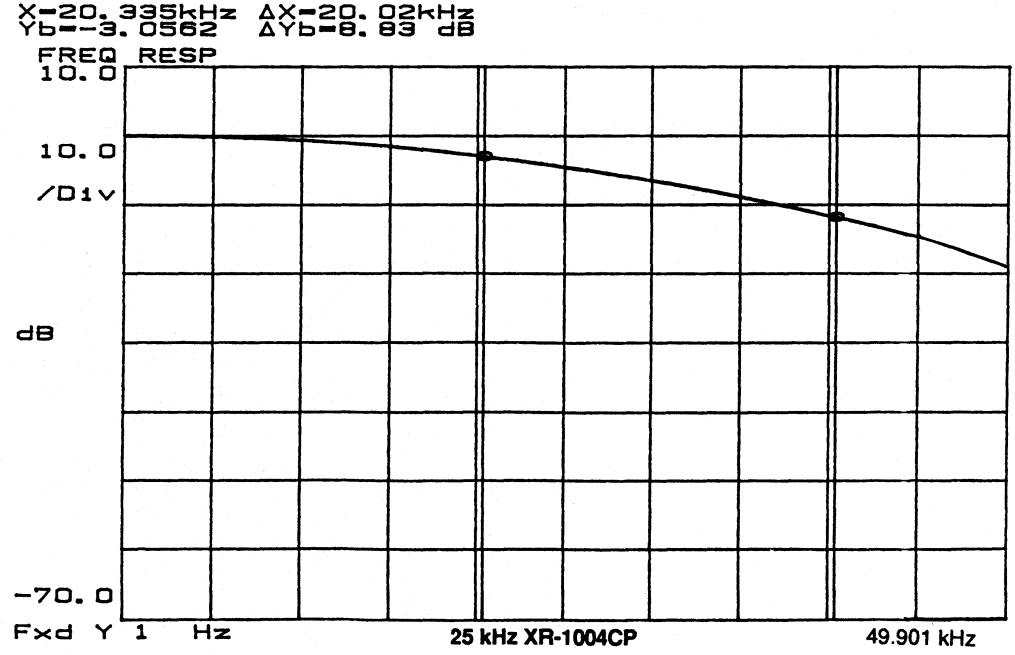
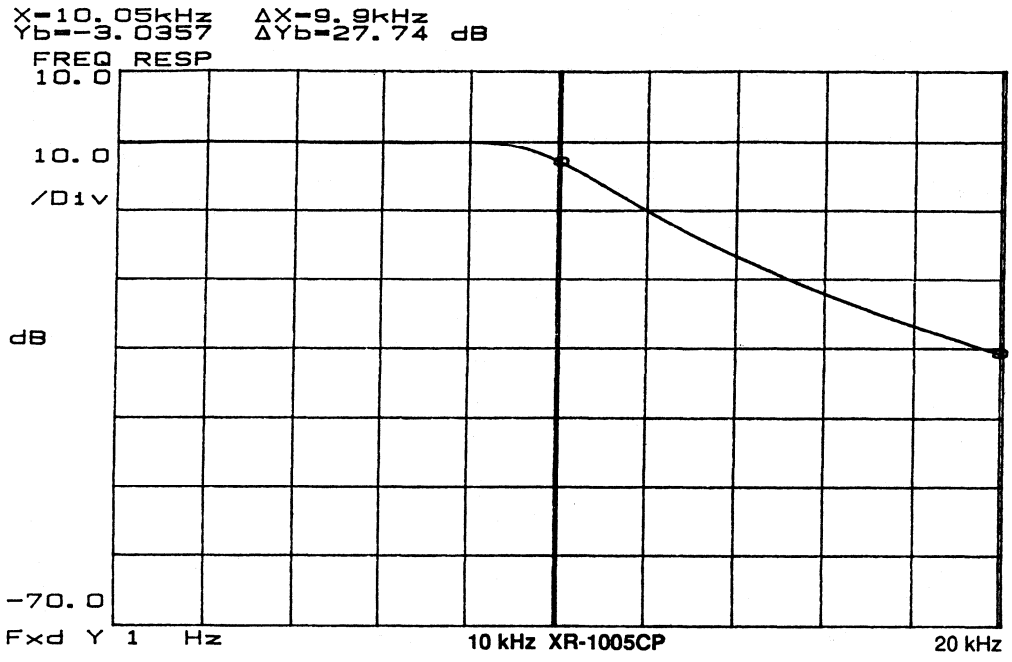
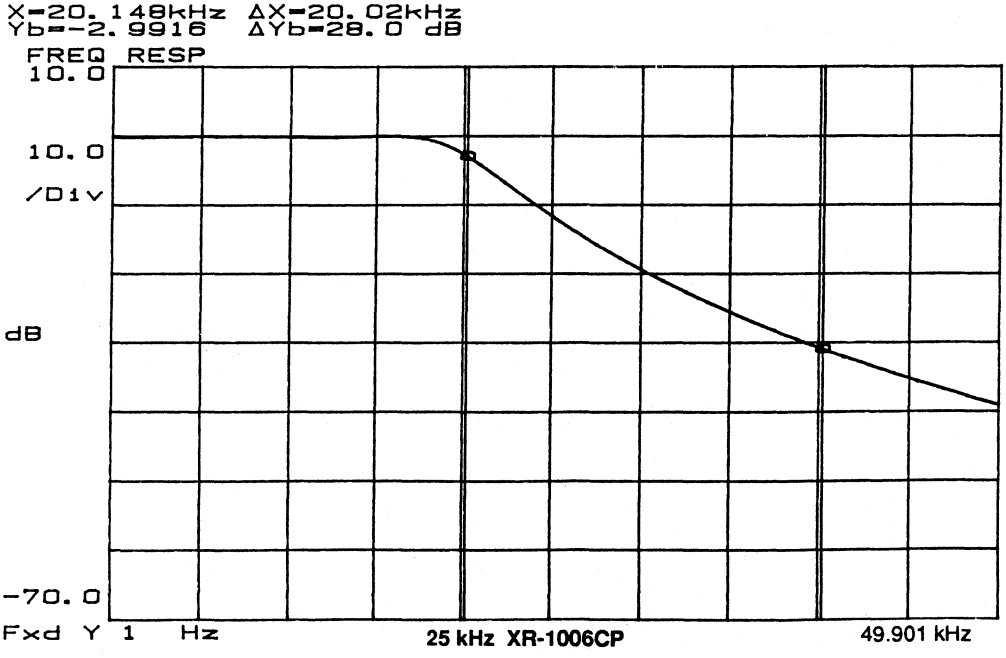


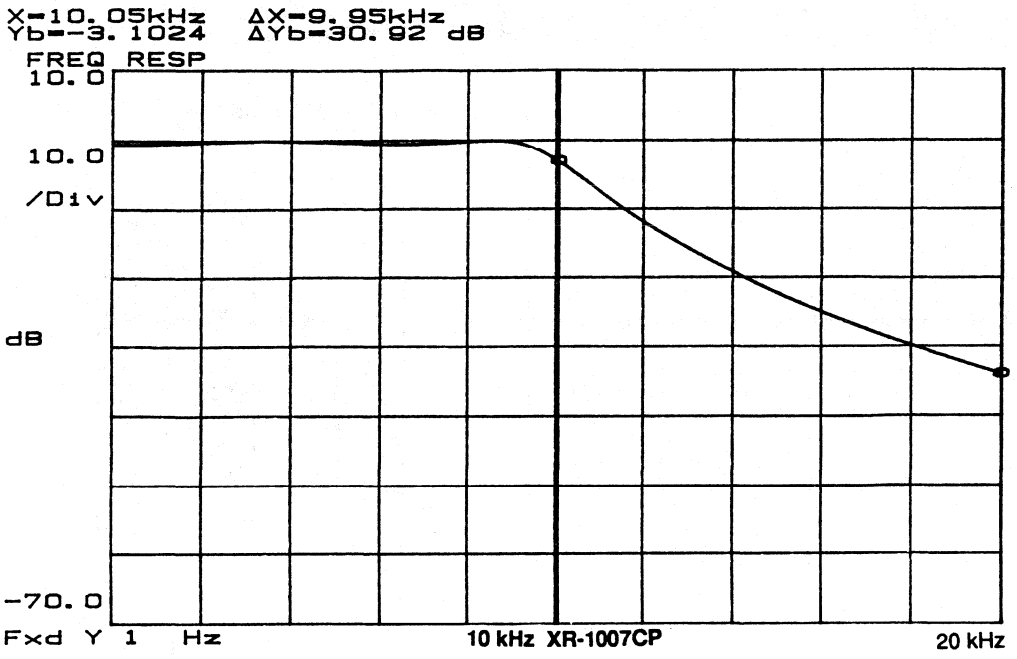
Figure 4. Operation of XR-1001/8 in RC Mode

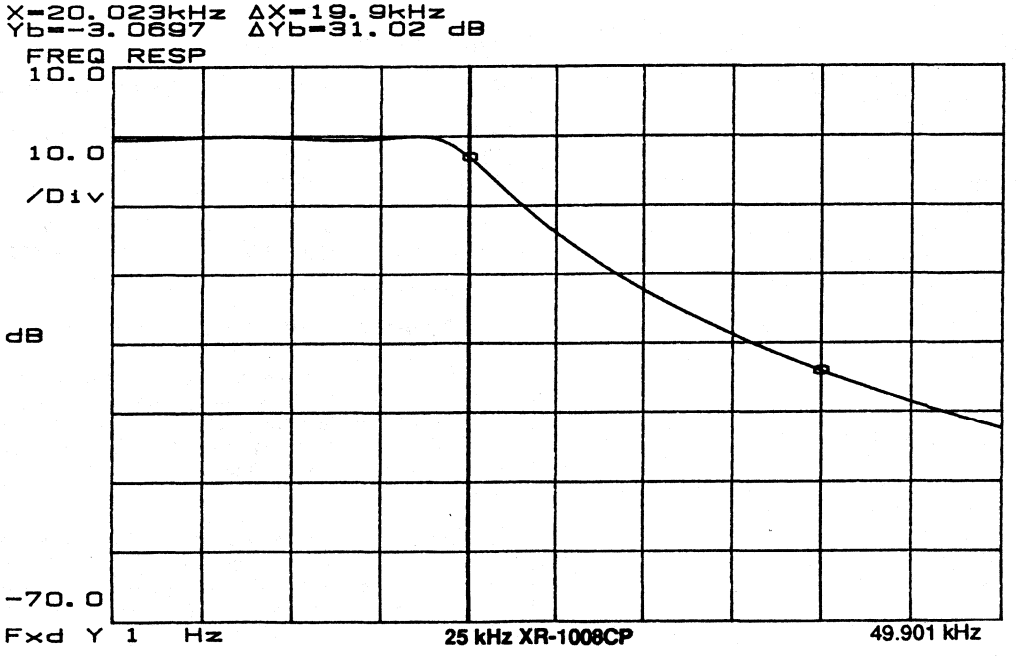

X=10.05kHz ΔX=9.9kHz
Yb=-3.0239 ΔYb=9.548 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
10 kHz XR-1003CP
20 kHz


X=20.335kHz ΔX=20.02kHz
Yb=-3.0562 ΔYb=8.83 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
25 kHz XR-1004CP
49.901 kHz


X=10.05kHz ΔX=9.9kHz
Yb=-3.0357 ΔYb=27.74 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
10 kHz XR-1005CP
20 kHz


X=20.148kHz ΔX=20.02kHz
Yb=-2.9916 ΔYb=28.0 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
25 kHz XR-1006CP
49.901 kHz


X=10.05kHz ΔX=9.95kHz
Yb=-3.1024 ΔYb=30.92 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
10 kHz XR-1007CP
20 kHz


X=20.023kHz ΔX=19.9kHz
Yb=-3.0697 ΔYb=31.02 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
25 kHz XR-1008CP
49.901 kHz

Second Order Switched Capacitor Filter

GENERAL DESCRIPTION

The XR-1010 is a fully adjustable dual second order switched capacitor filter. With the intermediate nodes of the switched capacitor filter brought out, many different filter functions can be obtained. One half of the XR-1010 is composed of an operational amplifier, and two switched capacitor integrators. With the use of external resistors, to adjust the amplitude of the feedback, notch, band pass, all pass, low pass and high pass filter functions can be obtained.

By cascading the two halves of the XR-1010, a fourth order filter can be obtained. With the use of additional XR-1010, higher order filters can be obtained.

The XR-1010 is fabricated in polysilicon gate 3-micron CMOS. With single +6 VDC operation (at 250 kHz) low power consumption can be obtained.

FEATURES

Easy to Use: Simple resisitor divider equations for filter Q
No External Capacitors Needed to Set Corner Frequency
Cascadable to Obtain Higher Order Filter Eunctions
Pin-for-Pin Compatible With the National Semiconductor MF-10

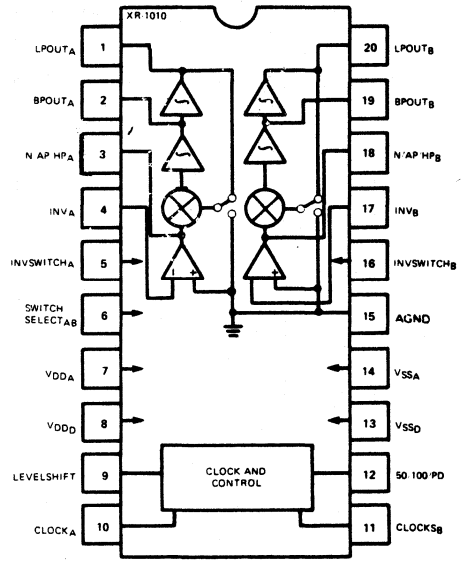
APPLICATIONS

Low Pass, High Pass, Band Pass, Notch & All Pass Filters
Group Delay Compensation Filtering
Modem Filters (CCITT V.21, V.23, V.26)
Band Separation for Analog Front End
Linear Phase Filtering (All Pole Filtering)
Loop Filter for Phase-Lock Loops

ABSOLUTE MAXIMUM RATINGS

Power Supply	14 V_{DC}
Input Signal Level (Logic)	V_{DD} +0.3 to V_{SS} −0.3 V_{DC}
Power Dissipation (Package Limitation)	
Ceramic Package	1.3 W
Derate Avove 25°C	5 mW/°C
Plastic Package	1.0 W
Derate Above 25°C	8 mW/°C
Storage Temperature	−55°C to +160°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Package	Operating Temperature
XR-1010N	Ceramic	−40°C to +85°C
XR-1010P	Plastic	−40°C to +85°C
XR-1010CN	Ceramic	0°C to +70°C
XR-1010CP	Plastic	0°C to +70°C
XR-1010CD	JEDEC SO	0°C to 70°C
Δ XR-1010AD	JEDEC SO	−40°C to +85°C

Δ Consult factory for availability

SYSTEM DESCRIPTION

The XR-1010 can be operated with either dual supplies or with a single supply. The center frequency of the filter response is set precisely by the clock frequency. This clock to center ratio can be changed with the use of the 50/100/PD pin on the XR-1010. Either TTL or CMOS clocks can be used.

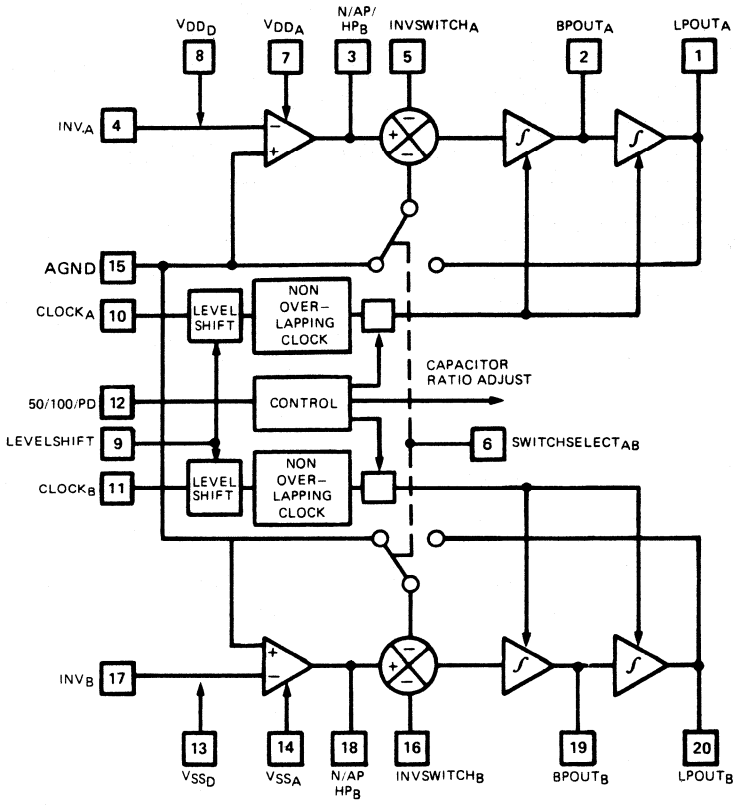
With the use of external resistors to control the amplitude of the feedback, many different filter functions can be obtained with the XR-1010. Simple algebraic calculations allow for the determination of the values of the resistor to obtain the filter shape needed.

ELECTRICAL CHARACTERISTICS

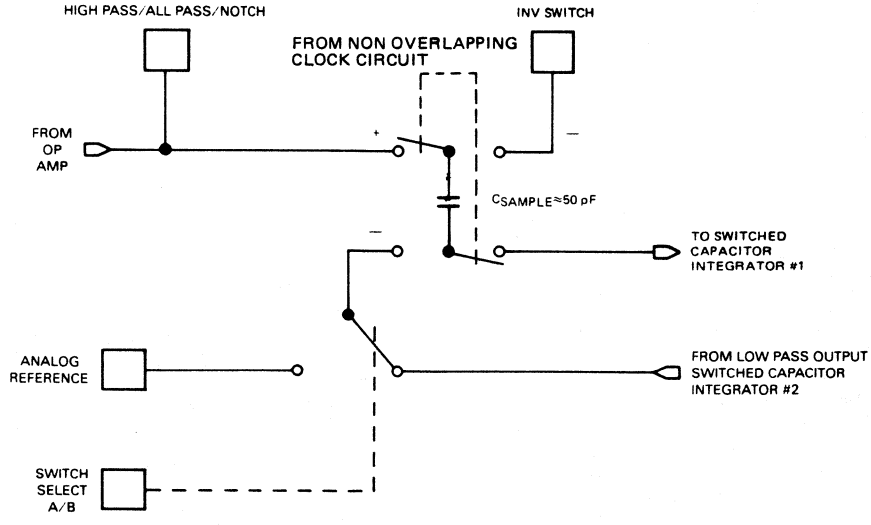
Test Conditions: $V^+ = 5$ V $V^- = -5$ V, $f_{clock} = 1$ MHz, $R_{load} = 1$ Megohms, $C_{load} = 40$ pF, $T_A = 25°C$: Mode 1 with R1 = 100 kilohms, R2 = 10 kilohoms, and R3 = 100 kilohms, unless specified otherwise.

SYMBOL	PARAMETERS	XR-1010/A MIN	XR-1010/A TYP	XR-1010/A MAX	XR-1010C MIN	XR-1010C TYP	XR-1010C MAX	UNIT	CONDITIONS
GENERAL CHARACTERISTICS									
V_{DD}	Positive Supply Voltage	3	5.0	5.25	3	5.0	5.25	V	f_{clock} = 1 MHz f_{clock} = 250 kHz
V_{SS}	Negative Supply Voltage	−5.25	−5.0	−3	−5.25	−5.0	−3	V	f_{clock} = 2 MHz f_{clock} = 250 kHz
I_{DD}	Current on V_{DD}		10	15		10	15	mA	
I_{SS}	Current on V_{SS}	−15	−10		−15	−10		mA	
$I_{PD_{DD}}$	Power Down Current		300			300		μA	Pin 12 = −5 VDC
FILTER CHARACTERISTICS									
f_o	Frequency Range	20	30		20	30		kHz	Pin 12 High
f_{clock} k f_o	Clock-to-Corner Frequency Ratio		49.94 99.35	±0.6% ±0.6%		49.94 99.35	±1.5% ±1.5%		Pin 12 High Pin 12 at 0 V
Q	Accuracy of f_o bandwidth			±3%			±6%		Q = 10 $f_o \times Q \leq 200$ kHz
f_{clock}	Maximum Clock Freq.	1	1.5		1	1.5		MHz	
$H_{lowpass}$	DC Low Pass Gain Accuracy			±2%			±2%		
	Crosstalk		70			70		dB	
	Clock Feedthrough		30			30		mVpp	f_{clock} = 1 MHz
V_{in}	Maximum Input (Unclipped)	8			8			Vpp	$A_V = 1 \frac{V}{V}$
THD	Total Harmonic Distortion		0.1%			0.1%			Input Level = 1 Vpp
tco_Q	Temperature Coefficient of Q		700			700		ppm/°C	From −40 to +85°C not tested in production
	Temperature Coefficient of f_o		120			120		ppm/°C	From −40 to +85°C not tested in production
OPERATIONAL AMPLIFIER CHARACTERISTICS									
GBW	Gain Bandwidth Product		2.5			2.5		MHz	
I_{OSS}	Output Short Circuit Current								
	Source Sink		26 1.5			26 1.5		mA mA	

5



Equivalent Schematic Diagram



Detail Switched Capacitor Summer

PRINCIPLES OF OPERATION

The XR-1010 is a dual second order switched capacitor state variable filter. Since the state variable filter provides all of the basic filter functions at the same time, it is the most versatile building block to use. With only a few external feedback resistors, band pass, low pass, high pass, notch, and all pass filter functions can be obtained.

With the switched capacitor implementation of the state variable filter, capapcitors, switched at a certain frequency will simulate resistors of a particular value. To allow greater flexibility, the feedback resistors to create the particular filter function are external to the device.

Since switched capacitor filters are sampled data systems, in that they divide a a continuous time signal into samples of charge, some thought must be given to out-of-band signals causing an aliased component to appear in the band of interest. To prevent the appearance of aliased signals, there should be at least two samples per cycle of signal applied to the input of the XR-1010. The sampling frequency of the filter is ½ of the clock frequency applied to Pin 10 and 11.

One reference on the subject of sampled data systems is the book "Digital Signal Processing" by Oppenheim and Schaffer, published by Prentice Hall. This book fully covers the concept of aliased signals as well as the Nyquist Criteria.

PIN DESCRIPTIONS

Pin No.	Numonic	Description
1	$LPOUT_A$	Low Pass Output A: The output of the second switched capacitor integrator. The low pass filter function is obtained at this pin. It can typically drive a 10 kilohm load.
2	$BPOUT_A$	Band Pass Output B: The output of the first switched capacitor integrator. The band pass filter function would be obtained at this output. This output can typically drive a 10 kilohm load.
3	$N/AP/HP_A$	Notch / All Pass / High Pass Output: This output provides the notch, all pass or high pass filter functions. The actual filter on the output is dependant upon the connection of external resistors and is decribed in the section on Modes of Operation.
4	INV_A	Inverting Input A: This is the inverting input of op amp A. It is normally used as the input for the filter function. Please note that the input impedance of the filter depends upon the value of the input resistor, R1, when used in some modes of operation. The noninvertising input to this operational amplifier is tied internally to the AGND, Pin 15.
5	$INVSWITCH_A$	Signal Input A: This input is used for the filter input in some modes of operation. The input impedance of this point varies with the clock frequency. For typical operation the source for the signal applied here should be 1 kilohms or less. With a 1 MHz sampling frequency, the input impedance is typically 20 kilohoms.
6	$SWITCHSELECT_{AB}$	Signal Switch AB: This logic input controls the other negative summing input of the filter. When low, the negative input of the summing section of the switched capacitor filter is connected to AGND, Pin 15. If this input is tied high, the other negative summing input is tied internally to the LP output. With this switch the various filter functions can be implemented. Please note that this input is not affected by the setting of LEVELSHIFT. A logic low is at VSS; a logic high is at VDD.
7	VDD_A	Analog Positive Supply: This input provides the positive voltage for the analog portions of the filter. It should be decoupled using a 0.68μF capacitor to ground. If it is known that the noise on the supply is large due to the use of a switching power supply, an additional 10μF capacitor should be used.

8	VDD_D	Digital Positive Supply: This input provides the positive voltage for the digital portions of the XR-1010. It should be decoupled with a 1.0μF capacitor to digital ground.
9	LEVELSHIFT	Logic Level Select: This input controls the acceptable clock input swing. With ±5 VDC operation, LEVELSHIFT should be tied to ground. This will allow either TTL or CMOS level clocks to be applied. With single supply operation, this pin should be tied to a voltage that is ½ of the algebraic sum of the supply voltages. This will allow input clocks at the VSS level to clock the XR-1010.
10	$CLOCK_A$	Clock Input A: This is the clock input for the XR-1010 side A. It must be at the same levels as the clock applied to $CLOCK_B$. The frequency of this clock and the setting of 50/100/PD will determine the center frequency of the filter response. The sampling frequency is always one half of the clock frequency applied to CLOCK A.
11	$CLOCK_B$	Clock Input B: This is the clock input for the XR-1010 side B. The level applied can be either CMOS or TTL depending upon the voltage present on the pin LEVELSHIFT.
12	50/100/PD	Clock to Corner/Power Down: This input controls the clock to corner ratio as well as providing a power down standby mode. With this pin tied to VDD (digital) the clock to corner ratio is set for 50:1. When this pin is tied to a voltage that is one-half of the sum of the amplitudes of VDD and VSS, the clock to corner ratio is 100:1. When this pin is tied to VSS, the XR-1010 is in the power down mode and the filter no longer provides an output. If the INVSWITCH input is used, then the input impedance should be infinite. If other modes of operation are used with the op amp the impedance will depend on external resistor values.
13	VSS_D	Negative Digital Supply: This input provides the negative supply for the digital portions of the XR-1010. It should be decoupled with a 1 μF capacitor to digital ground.
14	VSS_A	Negative Analog Supply: This input provides the negative supply for the analog portions of the XR-1010. It should have a 0.68 μF ceramic capacitor to decouple any noise to analog ground. If the analog negative supply is known to be noisey such as from a switching power supply, then an additional 1 μF capacitor for decoupling of the supply should be used.
15	AGND	Analog Reference: This input is used for providing the reference for the analog signals applied to the XR-1010. With equal split supplies, this pin should be tied to the analog ground of the system. When single supplies or unequal split supplies are used, then this input should be biased to a point that is one half of the algebraic sum of the VDD and VSS voltages. In this application, the AGND pin should be decoupled to the system ground with a 0.68 μF capacitor.
16	$INVSWITCH_B$	Negative Switch Input B: This is the negative switch input used for producing the various filter responses. Its input impedance varies with the clocking frequency. When it is being used as an input, the signal source should be 1 kilohms or less in output impe-

dance. With a 1 MHz sampling clock, the input impedance is typically 20 kilohms. As the sampling frequency decreases, the input impedance increases.

17 INV_B — Inverting Input B: This is the inverting input of operational amplifier B. It is normally used as the input for the filter function.

18 $N/AP/HP_B$ — Notch, All Pass, High Pass Output B: This output provides three of the filter functions as well as a source for feedback for producing other filter functions.

19 $BPOUT_B$ — Band Pass Filter Output B: This output provides the band pass filter response as well as a a source for feedback signals for other filter functions.

This output is capable of driving typically a 10 kilohm load.

20 $LPOUT_B$ — Low Pass Filter Output B: This provides the low pass filter response. It is capable of driving a 10 kilohm load.

SELECTION OF MODE

Table 1 shows which mode can provide which filter shape. Also shown in the table is which input is used. This helps to determine the most efficient use of the dual XR-1010 since Pin 6, SWITCHSELECT AB controls both sides of the XR-1010.

If one of the modes selected requires the internal feedback path from the low pass filter output to the switched capacitor summer mode, then the mode for the second half must have the same configuration, although not necessarily the same mode. This is not normally a problem since in most designs, both halves are used to obtain the final filter function needed.

OFFSET VOLTAGES

With any operational amplifier or integrator circuit, some offset voltage is seen on the output. The XR-1010 output offset voltages typically are less than 100 mv. This in most applications is neglible.

If the output offset voltage is not acceptable, then typical offset compensation circuits can be employed, as used with any operational amplifier.

5

TABLE I

FILTER SHAPES AVAILABLE WITH A PARTICULAR MODE

	Mode 1	Mode 1a	Mode 2	Mode 3	Mode 3a	Mode 4	Mode 5	Mode 6a	Mode 6b
Low Pass	yes	yes	yes	yes	yes	yes	yes	yes	inv. non-inv.
High Pass	no	no	no	yes	yes	no	*	yes	no
Band Pass	yes	inv. non-inv.	yes	yes	yes	yes	yes	no	no
Notch	yes	no	yes	no	yes	no	yes	no	no
All Pass	no	no	no	no	no	yes	yes	no	no
Input Used	Op Amp	Inv. Switch	Op Amp	Op Amp	Op Amp	Op Amp & Inv. Switch	Op Amp & Inv. Switch	Op Amp	Inv. Switch

*Depends on Band Pass location

GLOSSARY

f_{CLOCK} — The frequency of the clock applied to the switched capacitor filter. It is this clock that will determine the position of the corner or center of the filter (along with 50/100/PD).

f_o — The center frequency of the filter. This also sets the complex pole pair of the filter. Figure 1A shows a normalized complex pole pair on the $j\omega$ vs. ω axis. Figure 1B shows the response seen on the band pass filter output with this pole pair position. f_{center} corresponds to the peak of the band pass filter.

Q — The quality of the filter. With a band pass filter it is defined as the center frequency of the band pass response divided by the −3 dB bandwidth of the band pass filter.

The Q of the filter also indicates the position of the complex conjugate pole positions. Figure 2a shows the position of the complex pole positions and Figure 2b shows its affect on the band pass filter's −3 dB bandwidth.

$H_{bandpass}$ — The gain of the band pass filter at $f_o = f_{center}$. This parameter is unitless.

$H_{lowpass}$ — The gain of the low pass filter as f approaches 0 Hz. This is shown in Figure 3.

$H_{highpass}$ — The gain of the high pass filter output as f_o approaches $f_{clock}/2$. This is shown in Figure 4.

Q_{zero} — The quality of the complex zero pair. This specification has no units. It is difficult to measure this specification externally from the band pass output. Figure 5a shows the effect of a particular complex zero position on a output frequency response.

Figure 5b also shows an all pass filter response. This synthesized filter response has no amplitude ripple which would be the ideal response. Figure 5c shows the phase response of the all pass filter.

f_{zero} — The center frequency of the notch as see at the N/AP/HP output. In situations of high Q_{zero}, the f_{notch} will match f_{zero}.

f_{notch} — The center frequency of the notch as seen at the N/AP/HP output. In situations of high Q_{zero}, the f_{notch} will match f_{zero}.

$H_{notch@0}$ — The gain of the notch output as f_{notch} approaches 0 Hz.

$H_{notch@f_{clock}/2.}$ — The gain of the notch output as f_{notch} approaches $f_{clock}/2$.

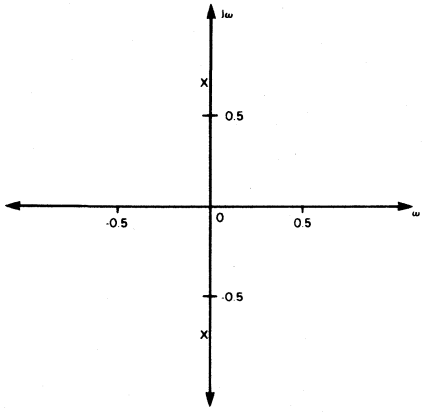


Figure 1A. Band Pass Complex Pole Position

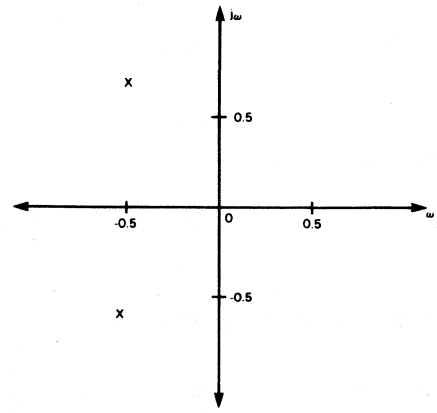


Figure 2A. Low Pass Complex Pole Position

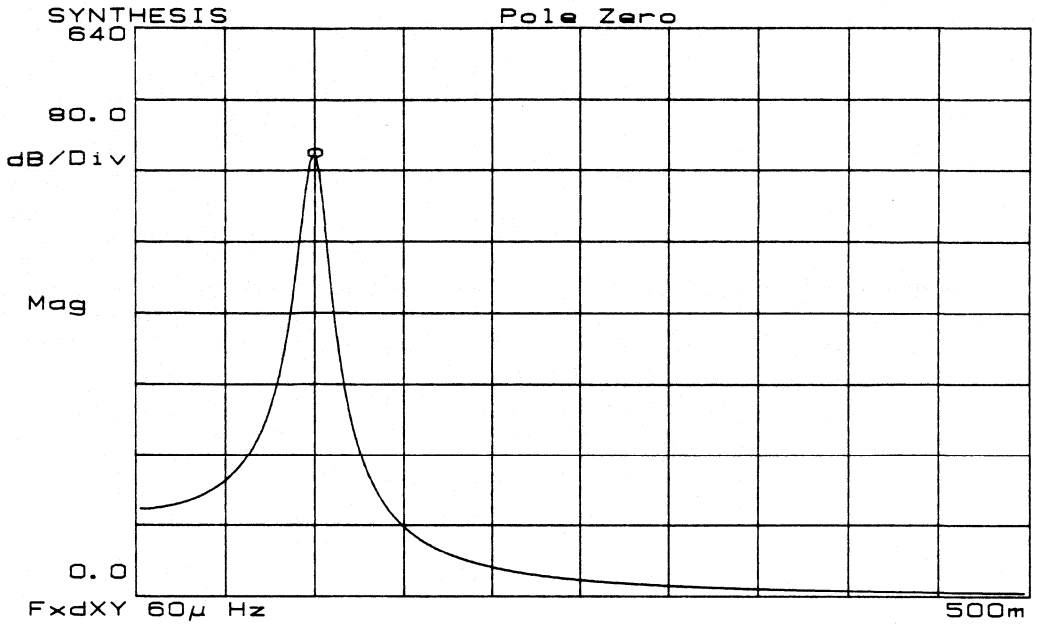


Figure 1B. Band Pass Filter

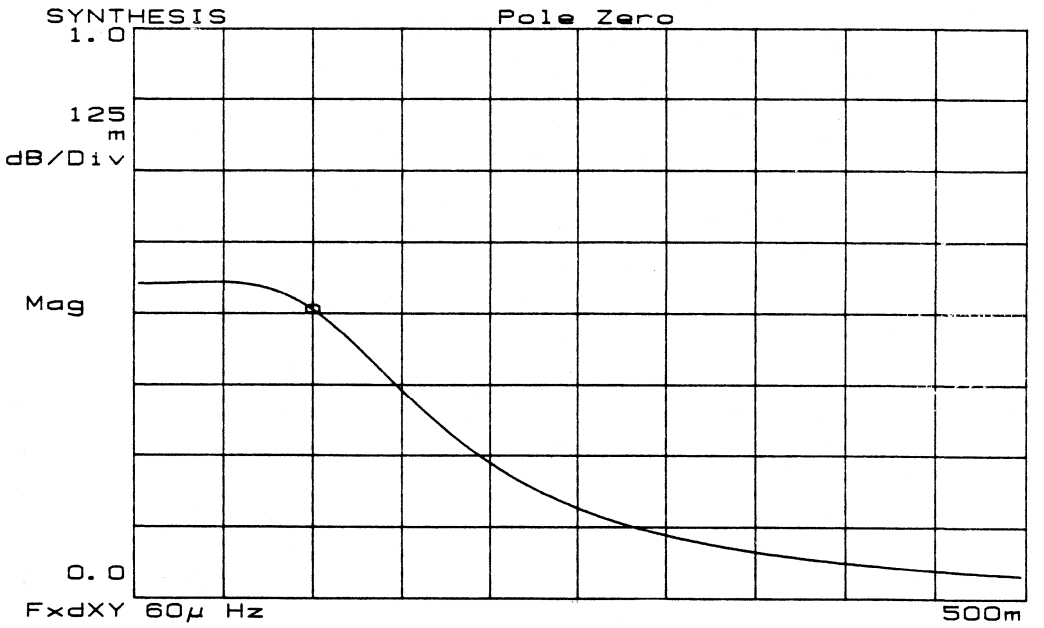


Figure 2B. Low Pass Filter

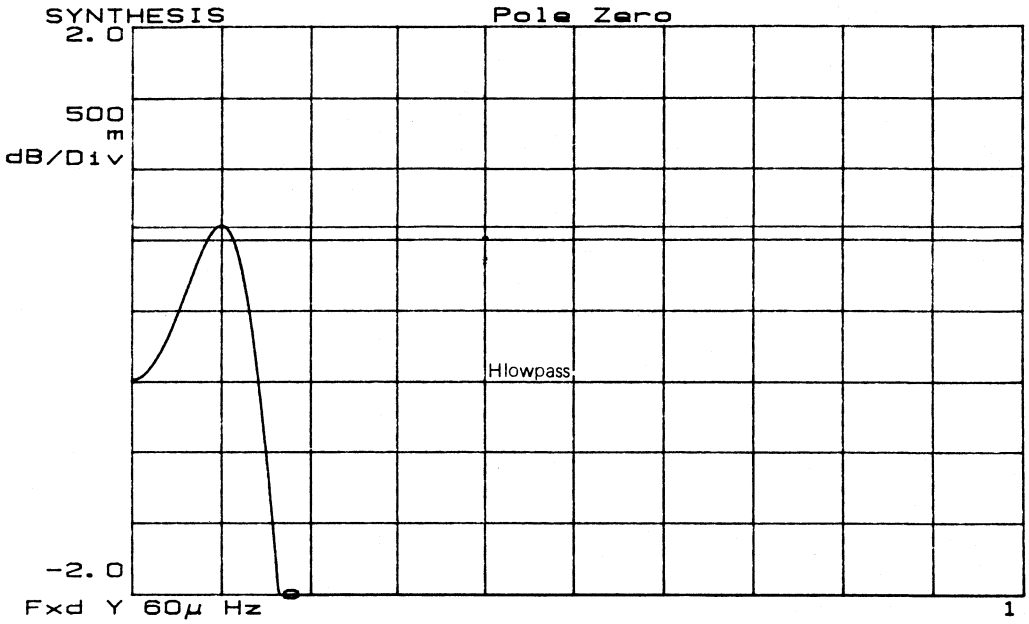


Figure 3. Definition of $H_{LOWPASS}$

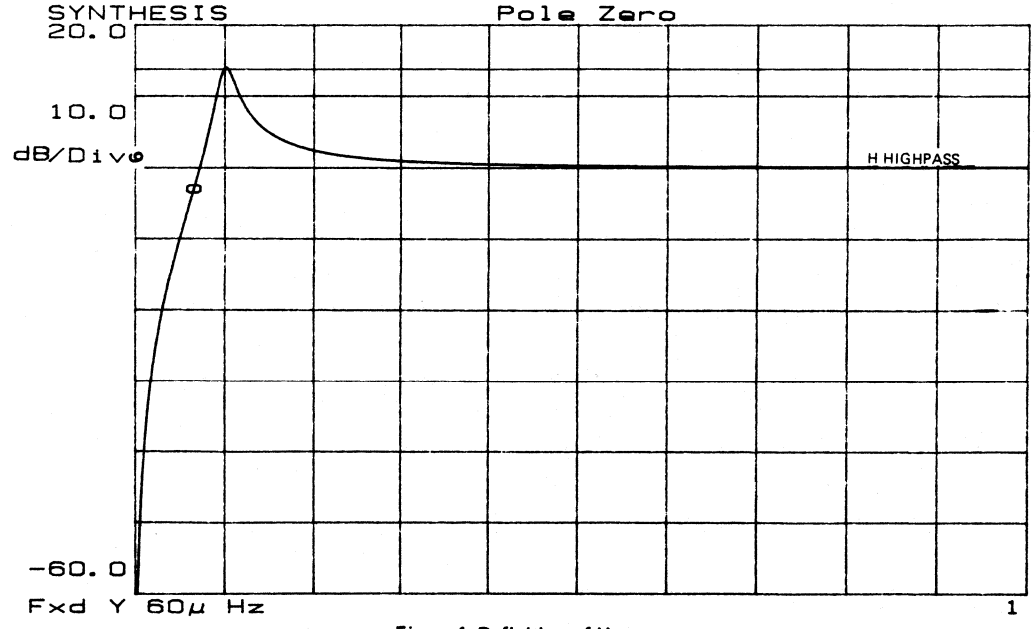


Figure 4. Definition of $H_{HIGHPASS}$

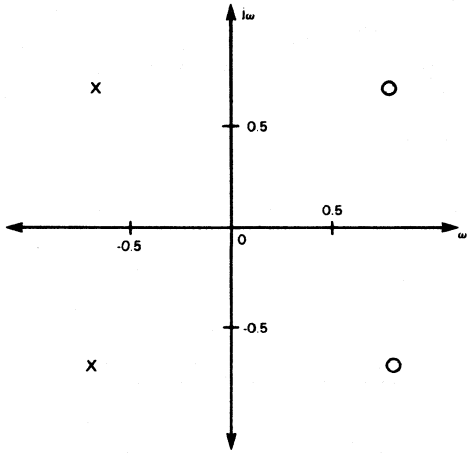


Figure 5A. All Pass Filter

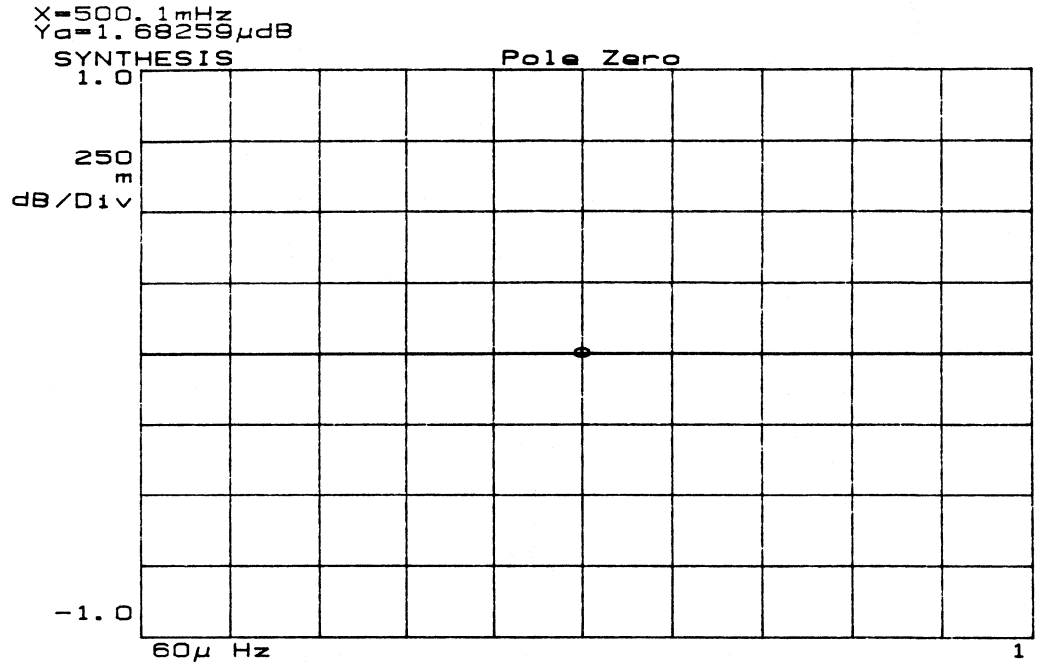


Figure 5B. Amplitude Response of a Perfect All Pass Filter

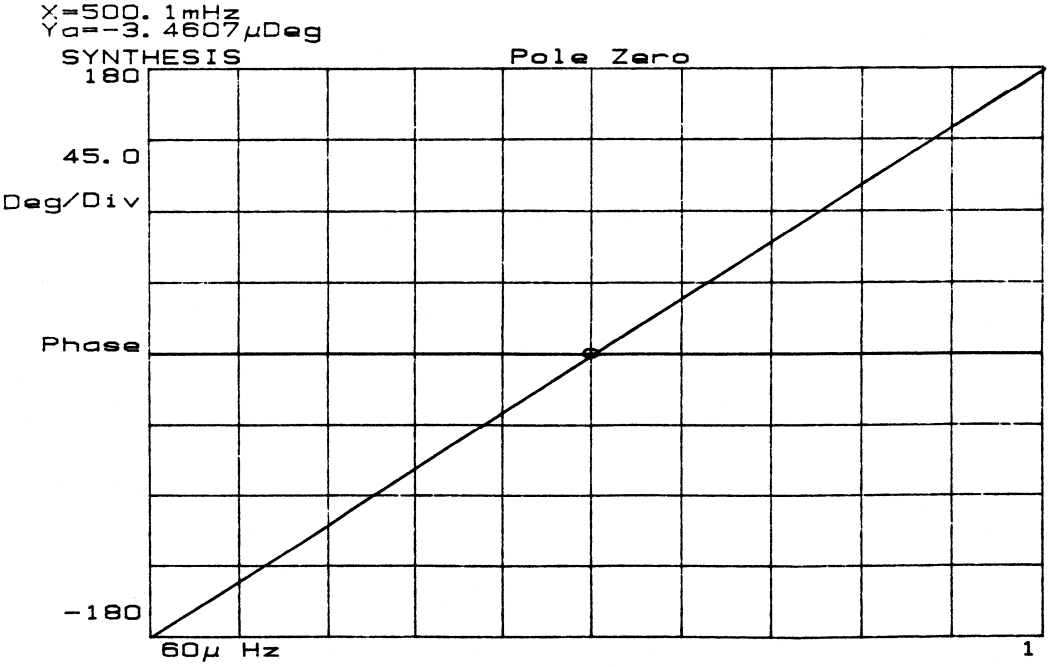


Figure 5C. Phase Response of a Perfect All Pass Filter

MODES OF OPERATION

The XR-1010 is a switched capacitor filter using switched capacitors to simulate resistors and controlled feedback to simulate inductors. This is a sampled data device which is most easily studied in the frequency domain.

The value of the resistors control the amount of feedback, and consequently, the gain of the filter responses and the Q of the filters. The following are the formulas used to calculate the resistor values needed to obtain the various filter responses.

Mode 1: Inverting Notch, Bandpass or Lowpass Filter Response

This mode involves a small number of external resistors. High Q band pass filters can be constructed with this circuit, however at the same time, the gain of the low pass filter response. The gain of all outputs are controlled by a separate feedback resistor. Figure 6 shows the connections to be made to side A of the XR-1010.

$f_O = \frac{f_{clock}}{100}$ or $\frac{f_{clock}}{50}$ — depending on the level at 50/100/PD.

$H_{lowpass} = -\frac{R2}{R1}$ — Please note that in this configuration R1 is the input impedance of the filter. In this fashion, the formula becomes an equation with only one unknown, R2, the amount of feedback.

$f_{zero} = f_o$ — The center frequency of the complex zero pair is equal to the center frequency of the real pole pair. In this mode, the uncertainty of the position of the zero is reduced.

$H_{bandpass} = -\frac{R3}{R1}$ — The gain of the band pass filter at the center frequency is set by this resistor ratio.

$H_{notch} = -\frac{R2}{R1}$ — The gain of the notch filter output as f_O approaches 0 Hz or as f_O approaches $f_{clock}/2$. Please note that the depth of the notch is a factor of the band pass filter's Q.

$Q = \frac{R3}{R2}$ — The quality factor of the second order pole pair is controlled by the ratio of R3/R2. This quality is also defined by f_O/bandwidth where the bandwidth is the −3 dB points of the band pass filter.

Dynamic Gain Calculations

$H_{bandpass} = H_{lowpass} \times Q$

$H_{bandpass} = H_{notch} \times Q$

This can be seen through the algebraic manipulations of the formula for notch low pass and Q from above. It can be seen from this that the device gain of the bandpass filter is independant of the Q of the filter.

$H_{lowpass(peak)} = Q \times H_{lowpass}$ — The gain of the low pass filter is affected by the Q of the filter at the center frequency of the band pass filter. If clipping of the low pass filter output occurs, the feedback of this clipping used to create the band pass response will cause distortion.

Mode 1a: Inverting Band Pass, Non-Inverting Band Pass, and Low Pass Filter Responses

This is the simplest configuration of the XR-1010, requiring only two external resistors. Please refer to Figure 7 for details.

$f_O = \frac{f_{clock}}{100}$ or $f_O = \frac{f_{clock}}{50}$ — Depending on the level at Pin 12, 50/100/PD.

$Q = \frac{R3}{R2}$ — The Q and the gain of the band pass are related. In the situation of large Q values, clipping may occur at certain signal levels.

$H_{lowpass} = 1$ — This is due to the unity gain configuration.

$H_{lowpass@f_O} = Q \times H_{lowpass}$ — This is true for applications with high Q values.

$H_{bandpass(inverting)} = -\frac{R3}{R2}$

Dynamic Calculations

$H_{bandpass(inverting)} = Q$ — If the input signal is too large, the output at this pin will be clipped causing an increase of noise. Clipping at this output will affect the device operation at other outputs.

$H_{lowpass(peak)} = Q \times H_{lowpass}$ — This is true in the case of high Q filters. This again shows the importance of preventing clipping from occurring in the filter. Such clipping would not be normally visible on the low pass filter output, but, this would affect the performance.

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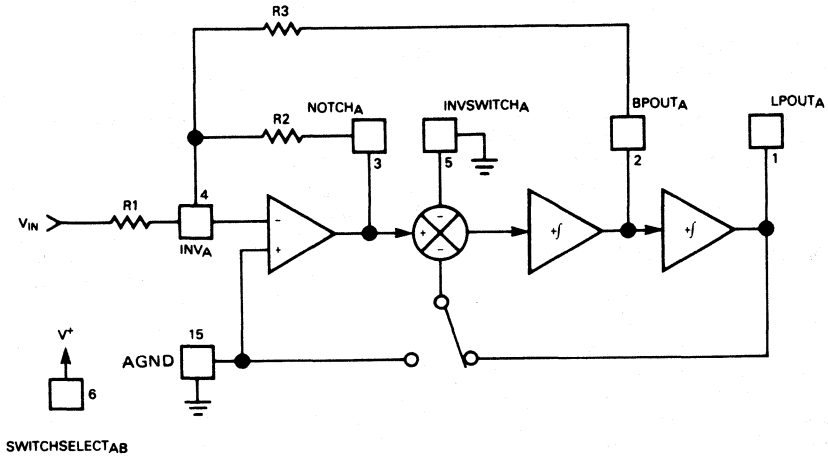

Figure 6. Mode 1 Shown for Side A of XR-1010

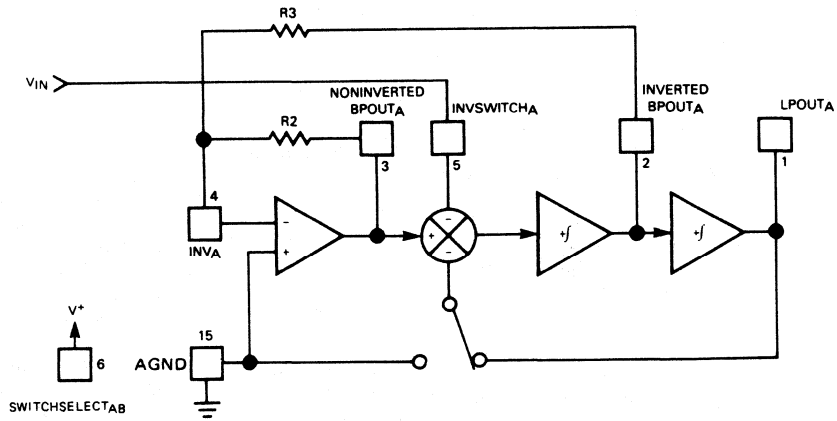

Figure 7. Mode 1A

This mode can provide a very large gain band pass filters due to the effect of the Q on the filter gain. It is not normally recommended for high Q filters due to the danger of clipping the inverting band pass output. The clock-to-corner ratio is fixed in this mode of operation due to the simplicity of the feedback of the filter.

The signal input impedance, Pin 5 or Pin 16, will vary with the clock frequency. With a clock frequency of 1 MHz, the input impedance is 20 kilohms typically.

Mode 2: $Notch_{mode2}$ (f_{notch} less than f_o) Band Pass, Low Pass Filters

Mode 2 provides adjustment of the center frequency of the band pass and low pass filters. This is done through the use of the feedback resistor R4. Please note that in Mode 2, the feedback path of the low pass filter output is through R4 to the inverting input of the operational amplifier, Pin 4 (17) as well as to the inverting input of the switched summing circuit. Figure 8 provides the detail for connection of the external resistors for side A of the XR-1010. Mode 2 is best duited for notch filter applications since the clock-to-corner ratio is reduced for the other shapes.

Design Equations

$$f_o = \frac{f_{clock}}{100}\left(\frac{R2}{R4}+1\right)^{1/2} \text{ or } f_o = \frac{f_{clock}}{50}\left(\frac{R2}{R4}+1\right)^{1/2}$$

depending on the level at Pin 12 50/100/PD. It should be noted that the f_o frequency must be greater than 100 times (50 times - Pin 12 high) the clock frequency or negative resistance will result when these equations are used.

$$f_{notch} = \frac{f_{clock}}{50} \text{ or } f_{notch} = \frac{f_{clock}}{100}$$

depending on the level set on Pin 12, 50/100/PD.

$$Q = \left(1+\frac{R2}{R4}\right)^{1/2}\frac{R2}{R3}$$

The Q of the filter is related to the gain of the low pass and notch filter as well as the band pass gain.

$$H_{lowpass} = \frac{\frac{-R2}{R1}}{\frac{R2}{R4}+1}$$

The low pass filter gain is the same as the gain for the notch filter as f_o approaches 0 Hz.

$$H_{notch} = \frac{\frac{-R2}{R1}}{\frac{R2}{R4}+1}$$

Mode 3: Inverting High Pass, Band Pass, and Low Pass Filters

This circuit allows high Q band pass filters with the ability to adjust the band pass filter gain without significantly affecting the Q of the filter. It is also possible to obtain a shift in the f_{corner} or the f_o of the filter with the adjustment of the values of the resistors R2 and R4, as shown in the equations below. This allows, with a single clock frequency, multiple-pole filters. Figure 9 shows the external resistor interconnections.

Design Equations

$$f_o = \frac{f_{clock}}{100} \times \left(\frac{R2}{R4}\right)^{1/2}$$

This formula calculates the center frequency of the band pass filter, or the corner frequency of the low pass filter. When 50/100/PD is tied to ground. It is with the adjustment of the value of R2 and R4 that the variation of the center frequency or the corner frequency is obtained.

$$f_o = \frac{f_{clock}}{50}\left(\frac{R2}{R4}\right)^{1/2}$$

This formula is used if Pin 12 50/100/PD is tied to V_+.

$$Q = \frac{R3}{R2}\left(\frac{R2}{R4}\right)^{1/2}$$

The Q of the filter is affected by the value of the feedback resistors R2 and R4 as well.

$$H_{highpass} = \frac{-R2}{R1}$$

It can be seen that the adjustment of the gain of the high pass filter output will have some effect on the Q of the filter as well as on the f_o of the filter outputs.

$$H_{bandpass} = \frac{-R3}{R1}$$

The gain of the band pass filter output will affect the Q of the filters.

$$H_{lowpass} = \frac{-R4}{R1}$$

The gain of the low pass filter output will have some effect on the f_o of the filter as well as on the Q of the filter.

Equations for Dynamic Circuit Operation

$$H_{highpass} = H_{lowpass}$$

This equation shows that the band pass filter will be affected by the Q of the filter as well as by the amount of shift created by the ratio R2 of the corner frequency.

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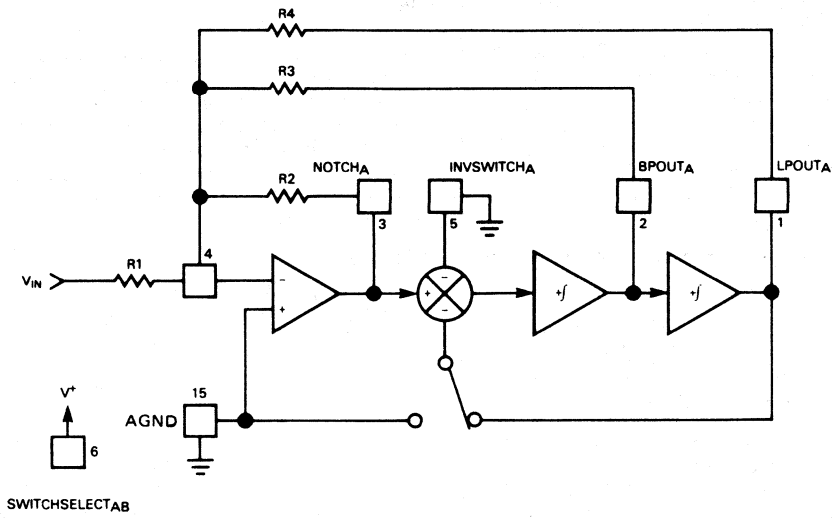

Figure 8. Mode 2

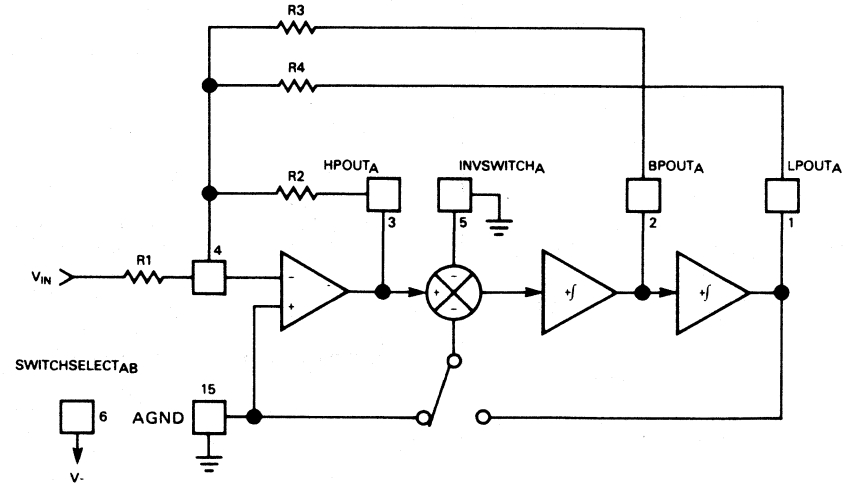

Figure 9. Mode 3

$H_{lowpass} @ f_o = Q \times H_{lowpass}$

The Q of the filter will have an effect on the amount of gain at the corner frequency of the low pass response. In situations of extremely large values of Q, this can cause clipping and should be considered.

$H_{bandpass} = (Q \times H_{highpass} \times H_{lowpass})^{1/2}$

The Q of the filter will have an effect on the gain of band pass filter output. The gain of the high pass and low pass filters will also have some effect on the band pass filter gain.

Mode 3A: High Pass, Band Pass, Low Pass and Notch Filters

With the addition of an external operational amplifier such as the XR-4560, XR-082 or the XR-5532A a notch filter can be obtained from the same circuit as Mode 3. The output of the high pass and the low pass filter are summed to obtain a notch filter response. The limitation of the notch depth will be the slope of the rolloff of the high pass and low pass filter responses. An operational amplifier with a large gain bandwidth product is recommended to minimize its effect on the filter response.

Figure 10 gives the details as to the filter configuration.

Design Equations

$$f = \frac{f_{clock}}{100}\left(\frac{R2}{R4}\right)^{1/2}$$

The center frequency of the notch or band pass filter or the corner frequency of the low pass can be adjusted to some degree by the ratio of the low pass and high pass filter gain resistors. This formula is used if Pin 12, 50/100/PD is tied to analog ground.

$$f_o = \frac{f_{clock}}{50} \times \left(\frac{R2}{R4}\right)^{1/2}$$

This formula is used if 50/100/PD is tied to VDD.

$$f_{notch} = \frac{f_{clock}}{50} \times \left(\frac{R2}{R4}\right)^{1/2}$$

or

$$f_{notch} = \frac{f_{clock}}{100} \times \left(\frac{R2}{R4}\right)^{1/2}$$

The notch filter center frequency at the output of the external operational amplifier.

$$H_{bandpass} = \frac{-R3}{R1}$$

The gain of the band pass filter output is controlled by the ratio between the feedback resistor (R2) and the input resistance (R1).

$$H_{highpass} = \frac{-R2}{R1}$$

The gain of the high pass filter output is controlled by the ratio between the feedback resistor R2 (operational amplifier output to inverting input) and the input resistor R1.

$$H_{lowpass} = \frac{-R4}{R1}$$

The gain of the low pass filter output is adjusted by the ratio between the feedback resistor R4 (integrator 2 output to inverting input of operational amplifier) and resistor R1.

$$H_{notch@0} = \frac{R_{gain}}{R_{lowpass}} \times \frac{R4}{R1}$$

The gain of the notch filter as the input frequency approaches 0 Hz can be calculated using the formula at left. From Figure 10, it can be seen that the gain of the external operational amplifier will affect the gain seen at the notch output. Also, this does allow some adjustment to the gain of the pass band of the notch filter without affecting the gain of the low pass filter output.

The outputs of the XR-1010 can typically drive a 10 kilohm load. The parallel combination of R4 and $R_{lowpass}$ should be 10 kilohms or greater.

$$H_{notch@f_{clock}} = \frac{R_{gain}}{R_{highpass}} \times \frac{R2}{R1}$$

The gain of the notch filter output as the input frequency approaches f_{clock} is calculated using the equation at left. Figure 10 shows how the gain of the high pass filter output can be adjusted independently of the notch filter gain. Care should be taken to ensure that clipping of the signal does not occur, due to excessive gain set at the notch filter output.

It should be considered that the output of the XR-1010 can drive 10 kilohms typically. Care should be taken so that the parallel combination of the feedback resistor R2 and the input resistor $R_{lowpass}$ is not less than 20 kilohms.

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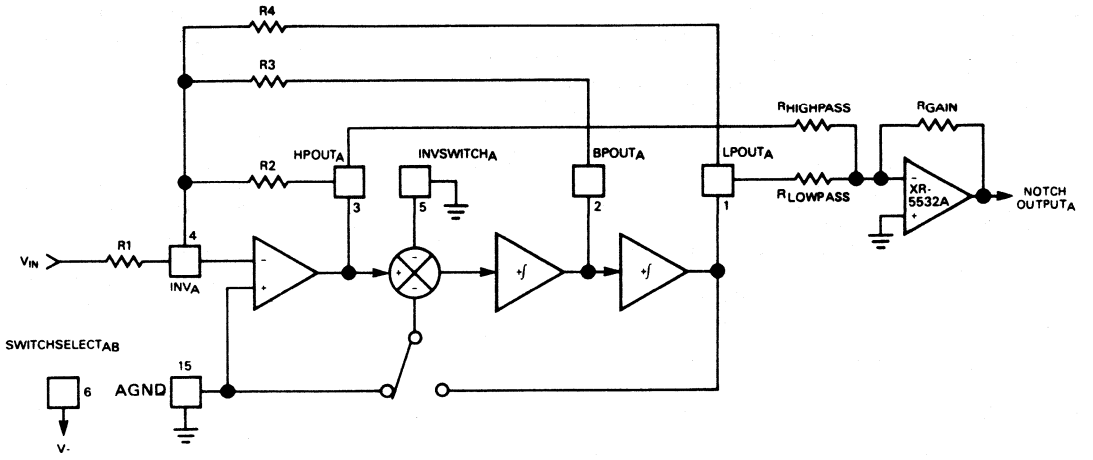

Figure 10. Mode 3A

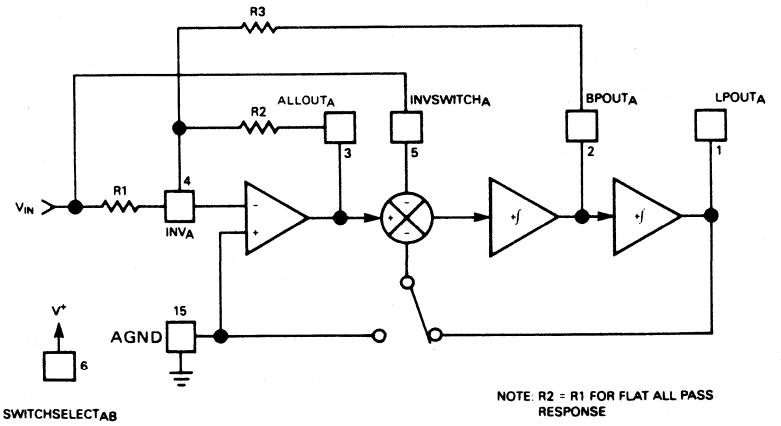

Figure 11. Mode 4

Mode 4: All Pass, Band Pass, and Low Pass Filtering

This mode provides an inverted all pass, band pass, and low pass filter output. Through variation of the f_{clock}, the amount of delay through the all pass filter can be varied. The output gain of the all pass filter is fixed at −1 to reduce the amount of ripple. Unlike other all pass filters, the XR-1010 has typically less than 1 dB of ripple in the response of the all pass filter output. This allows the use of Mode 4 in any all pass system. The f_O in this mode is fixed to either 100:1 or 50:1.

Figure 11 shows the external connections for Mode 4. As with the other circuits, it is important that the connections to the inverting input of the operational amplifier should be kept short to prevent noise pickup. Figure 12 (a/b) shows the change in delay for f_{clock} = 500 kHz and f clock = 1 MHz. From this, it can be determined that for maximum delay, the frequency of the clock should be decreased within the limits of the maximum input frequency.

Design Equations

$f_O = \frac{f_{clock}}{100}$

The center or corner frequency of the filter responses does not vary with the adjustment of the resistor values. The formula at left is used when Pin 12, 50/100/PD is tied to 0 V DC.

$f_O = \frac{f_{clock}}{50}$

The formula at left is used when the 50/100/PD pin is tied to V^+

The f_O of the complex zero pair is approximately equal to the f_O of the complex pole.

$Q = \frac{R3}{R2}$

The Q of the band pass filter output can be calculated using the equation at left. In the case of the large Q, this will have some effect on the gain of the low pass filter outputs at f_{corner}.

$Q_{zero} = \frac{R3}{R1}$

The Q of the complex zero pair which cannot be measured externally.

$H_{allpass} = \frac{-R2}{R1}$

The gain of the all pass filter output should be set to −1 (R2 = R1). When R2 is larger than R1, a slope will appear on the all pass output.

$H_{bandpass} = -2 \times \frac{R3}{R1}$

The gain of the band pass filter output is controlled by the ratio of R3 to R1.

$H_{lowpass} = -2 \frac{V}{V}$

The gain of the low pass filter output is fixed at −2 where f_O approaches 0 Hz. This can be seen by the two inputs used in this mode (Mode 4). The one input is applied directly to the INVSWITCH input. The second is applied through R1 to the inverting input of the operational amplifier. At the switched capacitor summer, the amplitude of the two signals would be equal in amplitude (@ 180°) providing twice the amplitude to be applied to the low pass integrator.

Mode 5- Complex Zero, Band Pass and Low Pass Filter Outputs

This mode provides additional flexibility over Mode 4, in that the complex zero location can be moved separately from the complex pole position. This can reduce the amount of ripple in the all pass response, as well as provide additional control over the position of the corner frequency of the low pass filterand the center frequency of the band pass filter output. Please see Figure 13.

Design Equations

$f_O = \left(1+\frac{R2}{R4}\right)^{1/2} \times \frac{f_{clock}}{100}$

The formula at left calculates the corner or center frequency of the XR-1010 filter outputs when Pin 12 50/100/PD is tied to analog ground.

$f_O = \left(1+\frac{R2}{R4}\right)^{1/2} \times \frac{f_{clock}}{50}$

When 50/100/PD is tied to VDD, the formula at left should be used. This formula shows the advantage that Mode 5 has over Mode 4 in that the corner or center frequency of the filter can be moved relative to the fixed clock-to-corner ratio.

If only a small change to the clock-to-corner (center) ratio is desired, then R4 can be made larger. However, this will have a direct effect on the gain of the low pass filter output. Clipping on the output of the low pass filter could occur, which would affect the other filter outputs.

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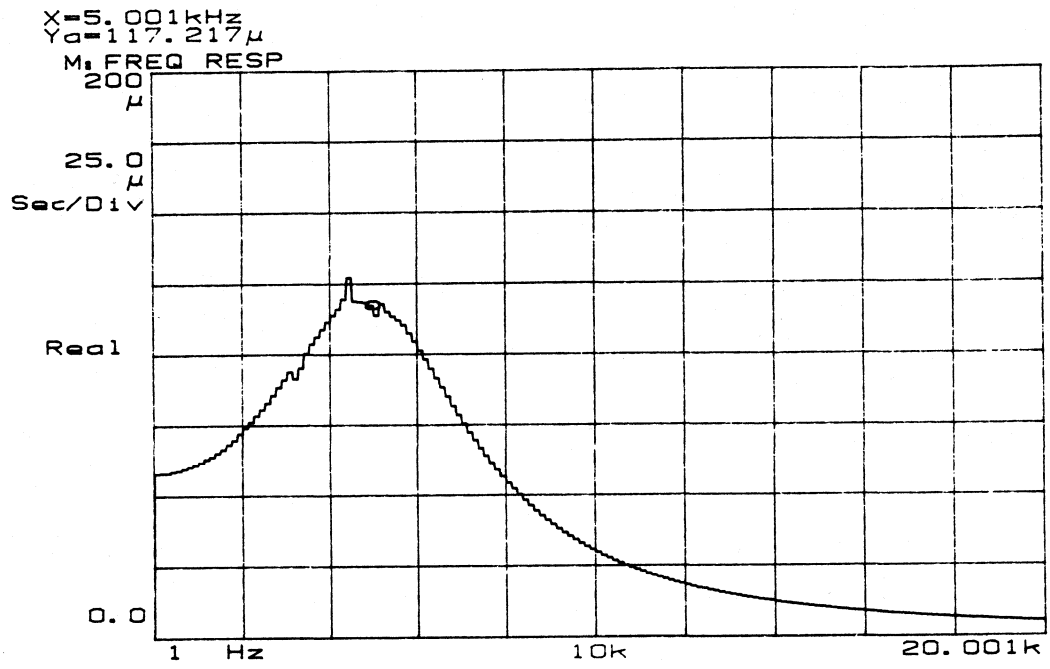


Figure 12A. Delay of Mode 4 All Pass Output f_{clock} = 500kHz

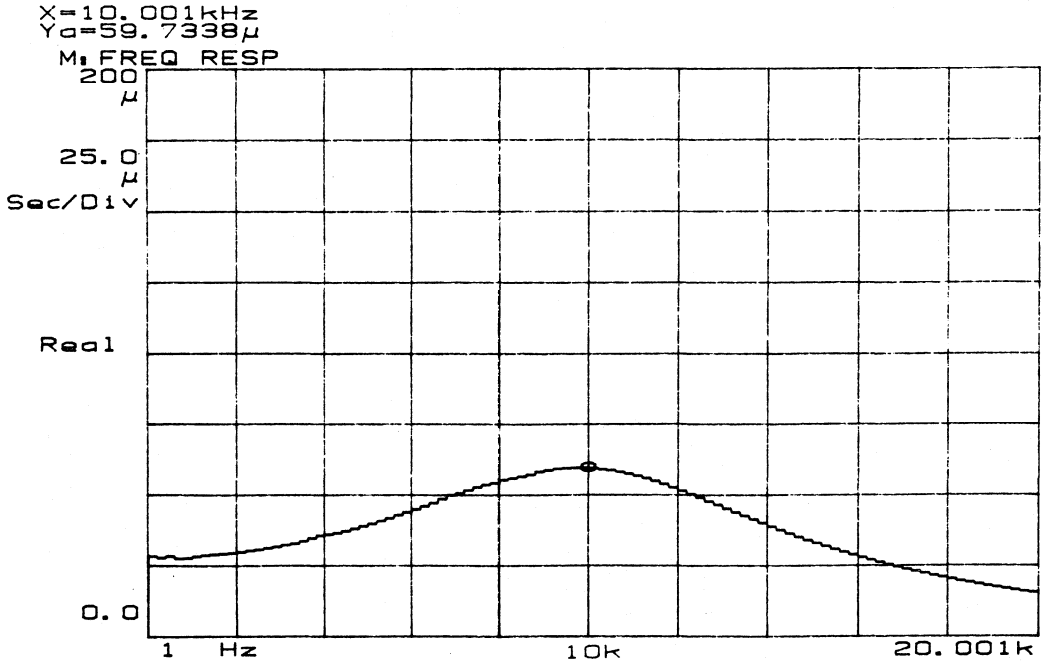


Figure 12B. Delay of Mode 4 All Pass Output f_{clock} = 1 MHz

$$f_{zero} = \left(1 - \frac{R1}{R4}\right)^{1/2} \times \frac{f_{clock}}{100}$$

The equation at left is used for caluclating the location of the complex zero pair, when Pin 12, 50/100/PD is tied to ground. With the ability of moving the complex zero to a location of the pole, many different filter shapes can be obtained.

In the case of a large value for R1 and a small value of R4, the location of the zero would be close to 0 Hz. The equation is not defined for values of R1/R4 which are greater than or equal to 1.

$$f_{zero} = \left(1 - \frac{R1}{R4}\right)^{1/2} \times \frac{f_{clock}}{50}$$

This equation is used when Pin 12 50/100/PD is tied to VDD.

$$Q_{pole} = \left(1 + \frac{R2}{R4}\right)^{1/2} \times \left(\frac{R3}{R2}\right)$$

The equation at left calculates the quality of the filter relative to the complex pole pair. With the variation of R3 (band pass feedback) and R4 (inverting low pass filter feedback), the magnitude of the real component can be varied.

$$Q_{zero} = \left(1 - \frac{R2}{R4}\right)^{1/2} \times \left(\frac{R3}{R1}\right)$$

This equation is used to calulate the quality of the complex zero pair. The magnitude of R4 (inverting low pass filter feedback) and R3 (band pass filter feedback) control the location of the zero on the $j\omega, \omega$ axis.

This formula works well with large values (relative to R2) of resistance of R4. When R4 becomes equal to, or smaller than R2, the formula becomes meaningless.

The Q_{zero} in such a case is much less than 1 and does not have any practical use.

$$H_{zero\ @\ 0} = \frac{R2(R4-R1)}{R1(R2+R4)}$$

The gain on the output of the complex zero filter as the input frequency approaches 0 Hz is calculated by this formula.

$$H_{zero\ @\ \frac{f_{clock}}{2}} = -\frac{R2}{R1}$$

As the input frequency approaches $f_{clock}/2$, the gain of the output is limited by the gain of the operational amplifier.

$$H_{bandpass} = \left(\frac{R2}{R1} + 1\right) \times \frac{R3}{R2}$$

The gain of the bandpass filter is f_O is calculated using the formula at left.

$$H_{lowpass} = \left(\frac{R2 + R1}{R2 + R4}\right) \times \frac{R4}{R1}$$

The formula at left is used to caluculate the gain of the low pass filter as f_O approaches 0 Hz. The response of the filter near the corner frequency is affected by the gain of the band pass filter.

Mode 6a: First Order Clock Controlled High Pass and Low Pass Filter (Inverted)

This mode allows the construction of first order high pass and low pass filters with the f_{corner} adjustable from the clock frequency or by adjusting the resistor ratios. This is far more useful than the continuous time RC version, since the XR-1010 will track any other stage in the system.

The output of the second integrator is not normally used. The output is typically near VDD or VSS.

Design Equations

$$f_O = \frac{f_{clock}}{50} \times \left(\frac{R2}{R3}\right)$$

This equation is used for calculation of the position of the corner frequency of the low pass filter or the high pass filter when Pin 12, 50/100/PD is tied to VDD.

$$f_O = \frac{f_{clock}}{100} \times \left(\frac{R2}{R3}\right)$$

This equation is used when Pin 12, 50/100/PD is tied to analog reference. Please note that if the gain of the low pass and high pass filter outputs is not the same, the clock-to-corner ratio will be affected.

$$H_{highpass} = \frac{-R2}{R1}$$

This formula is used to calculate the gain of the high pass filter output.

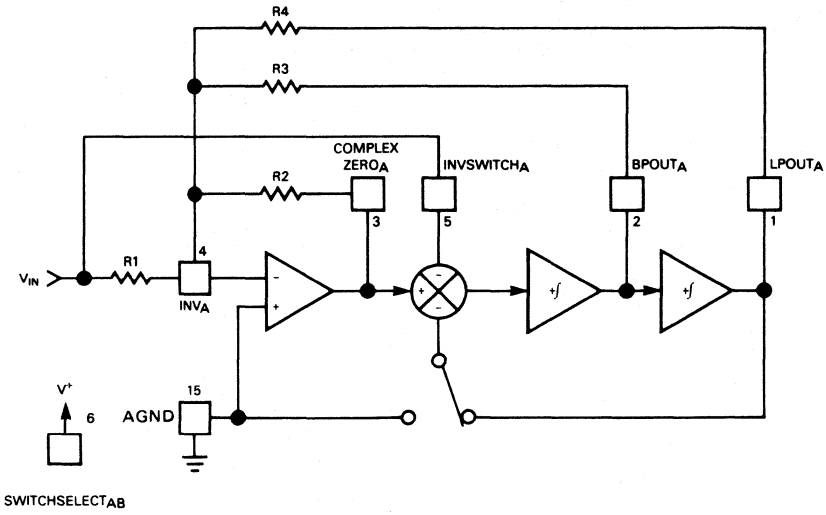


Figure 13. Mode 5

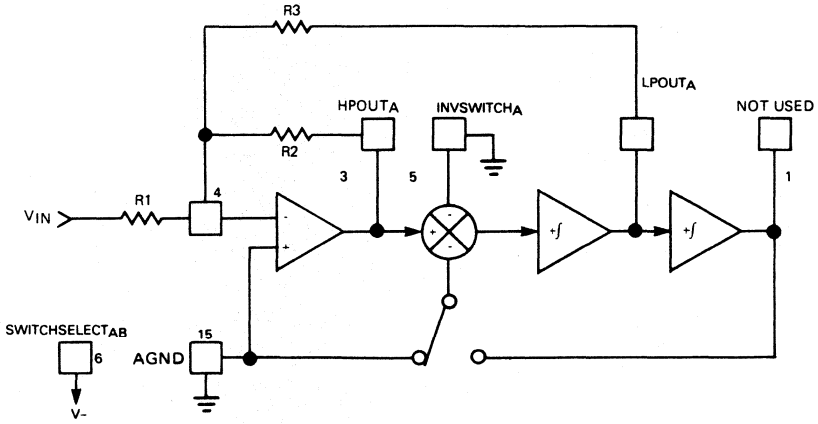


Figure 14. Mode 6A

Mode 6b: Single Pole Low Pass Filter - Inverting and Non-Inverting Output

This mode is used for circuits which only need a single pole, but, need the flexibility of clock control for the corner frequency. As with Mode 6, the output at Pin 1 is not used and is normally either near VDD or VSS.

Design Equations

$$f_{corner} = \frac{f_{clock}}{100} \times \left(\frac{R2}{R3}\right)$$

This equation is used when Pin 12, 50/100/PD is tied to mid-supplies usually 0 VDC.

$$f_{corner} = \frac{f_{clock}}{50} \times \left(\frac{R2}{R3}\right)$$

When Pin 12, 50/100/PD is tied to VDD, this formula is used to calculate the position of the corner of the low pass filter.

$$H_{lowpass(inverting)} = \frac{-R3}{R2}$$

The gain of the inverting low pass filter output is controlled by the ratio of the feedback resistor R3 to the resistor R2.

$$H_{lowpass(noninverting)} = +1\frac{V}{V}$$

The gain of the non-inverting low pass filter output is fixed at +1.

GENERAL APPLICATION CRITERIA

The following aspects of the use of any filter should be considered when the design is started:

1. Prevention of saturation of the first stage or any subsequent stages. If a design is composed of two stages, consideration to the output amplitude of the first stange must be given. The Q of the filter could cause clipping on the first stage, which would be filtered by the second stage back to a sinusoidal signal. This would cause an increase in noise, and error in the phase response of the filter.

   Any DC offset of the signal can cause clipping or even rectification of the signal. The offset of the signal should be determined for the first stage and any other stages.

2. The order of the filters may be important to the design. Once again this would be due to the gain or Q of the filters. For example, a low pass filter may be desired before a band pass filter to reduce the chance that out-of-band signals will affect the band pass filter. Also, any clipping at the output of the band pass filter would be apparent. This would not be the case if the band pass filter was the first stage and the low pass filter was second.

3. The signal-to-noise ratio should be maximized. In most designs the limiting factor for the signal to noise ratio is not the filter itself, rather the layout of the board and decoupling of the supplies. Proper use of analog and digital grounds should be observed in any system using a filter. Proper grounds imply that no differential voltage will occur from the INV SWITCH when grounded and AGND. A separate analog VDD and VSS should be provided when possible.

   Shielding of the low amplitude signals from large digital signals should be considered also.

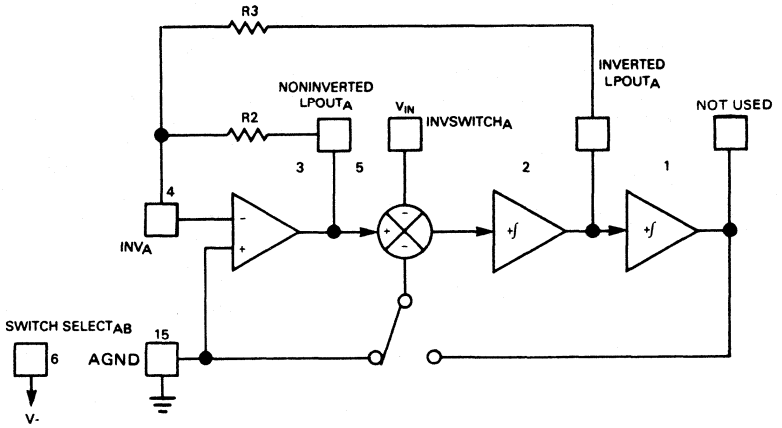


Figure 15. Mode 6B

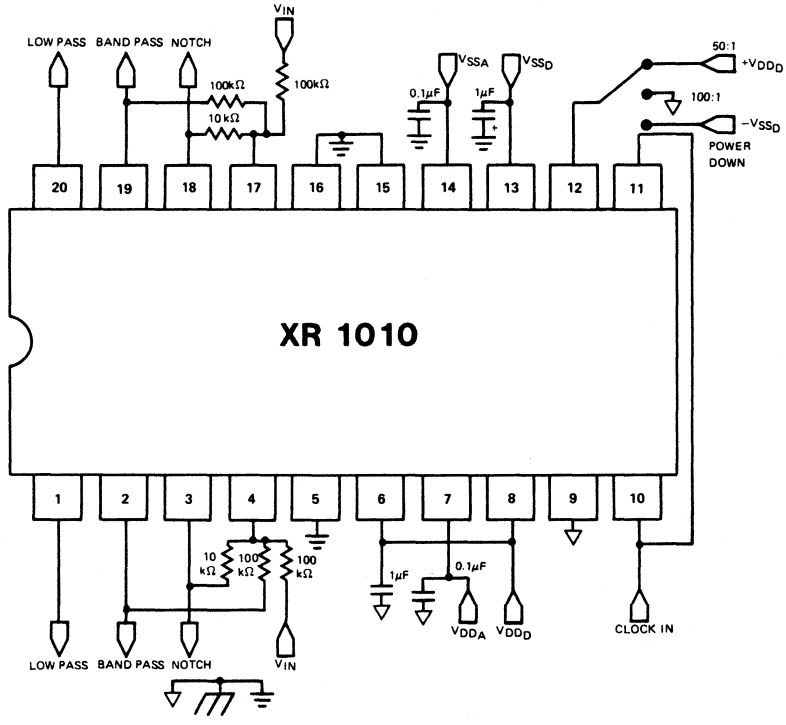


Figure 16. Spilt Supply Operation Mode 1

Seventh Order Elliptic Low Pass Filters

GENERAL DESCRIPTION

The XR-1015 and XR-1016 are seven pole and six zero elliptic low pass switched capacitor filters. The position of the passband of the filter is set by the frequency of the clock which allows for easy adjustment. The use of switched capacitor filters reduces the amount of variation in the filter response that occurs with discrete use of capacitors, inductors and resistors. The XR-1015 and XR-1016 also provide synchronized sampled inputs and outputs that allows the device to be cascaded without the need of an additional sample and-hold. The XR-1015 and XR-1016 are produced with a 3 um polysilicon gate dual metal CMOS process for low power consumption.

The XR-1015 is an eight pin device that can operate from +3, −2.0 VDC to ± VDC. The device can also be biased so that it can be operated with a single +5 to +10 VDC supply. It is pin-for-pin compatible with the Reticon R5609 with the added advantage of operating to +5 VDC single supply. The clock to corner ratio of the XR-1015 is fixed at 100:1.

The XR-1016 is a 14 pin device which provides two uncommitted operational amplifiers for use as a reconstruction filter, anti-aliasing filters or for additional pre-filter gain. The XR-1016, as does the XR-1015, provides a clock output with the voltage output from rail to rail. The XR-1016 has the ability to change the clock to corner ratio from 100:1 to 50:1. The output clock can be used to strobe an analog to digital converter or to synchronize any additional circuits in the system.

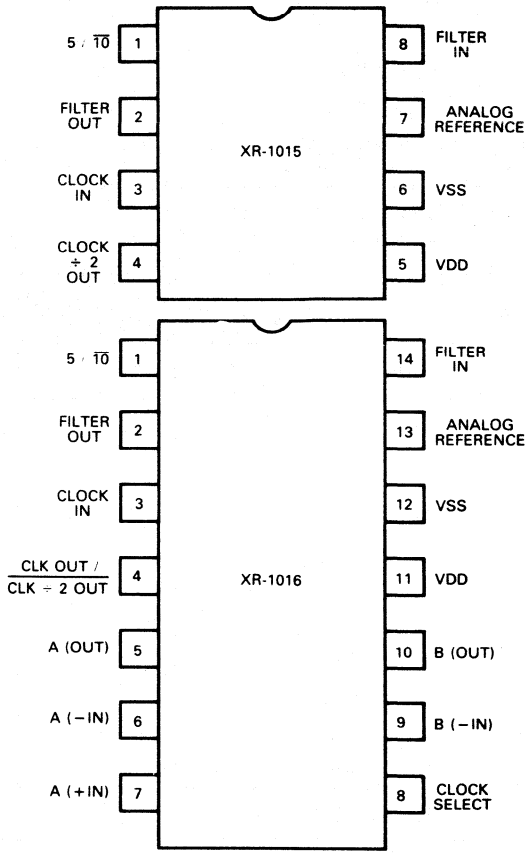
FEATURES

Greater than 70 dB Stopband Rejection
Operation at +5 VDC
Precise Filter Positioning
Low Power Consumption
No External Components Required for Filter

APPLICATIONS

General Purpose Filtering
Anti-alias Filters (for analog-to-digital converters)
Reconstruction Filters (for digital-to-analog converters)
Band Limiting of Voice
Digital Signal Processing Front End
Filtering of Voice for Music for Special Effects (echo, phasing, etc.)

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply	14 V
Input Signal Level	V+ +0.3 to V- ±0.3V
Power Dissipation - XR-1016 (Package Limitation)	
Ceramic Package	1000 mW
Derate Above T_A = +25°C	6 mW/°C
Plastic Package	800 mW
Derate Above T_A = +25°C	7 mW/°C
Power Dissipation - XR-1015	
Ceramic Package	385 mW
Derate Above T_A = +25°C	8.3 mW/°C
Plastic Package	300 mW
Derate Above T_A - +25°C	8.3 mW/°C
Storage Temperature	−55°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1015CN	Ceramic	0°C to 70°C
XR-1015CP	Plastic	0°C to 70°C
XR-1016CN	Ceramic	0°C to 70°C
XR-1016CP	Plastic	0°C to 70°C
XR-1016CD	JEDEC SOL-16	0°C to 70°C

SYSTEM DESCRIPTION

The XR-1015 and XR-1016 General Purpose Seventh Order Elliptic Switched Capacitor Low Pass Filters are usually used as the first or last stage in any sampled signal system. Any signal from the −3 dB point of the low pass response to ½ of the sampling frequency (¼ of the clock frequency) will be attenuated by typically 75 dB, referenced to the passband. This allows its use with analog-to-digital converters to prevent the A-to-D from aliasing signals that are above ½ of the sampling frequency of the analog-to-digital converter. A simple second order active filter can be used in front of the XR-1015 or XR-1016 if it is known that some input signals will be above the Nyquist frequency of the XR-1015 or XR-1016.

The reverse of the above circuit can be used for digital-to-analog converters, to prevent the sampling frequency from causing difficulties with other stages in the system.

ELECTRICAL CHARACTERISTICS

Test Conditions: V+ = 5 VDC, V− = −5 VDC, f_{CLOCK} = 2 MHz, R_L = 1 Megohm, C_L = 40 pF, T_A = 25°C, unless otherwise noted.

		XR-1015			XR-1016				
SYMBOL	**PARAMETERS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
GENERAL CHARACTERISTICS									
	Supply Voltage								
	Single Supply	5		10.5				V	See Figure 1
					5		10.5	V	See Figure 3
	Split Supply	+3		±5.25				V	See Figure 2
		−2			+3		±5.25	V	See Figure 4
					−2				
	Supply Current								
	Single Supply		10	11				mA	See Figure 1
						10	11	mA	See Figure 3
	Split Supply								
	Positive		10	**12**				mA	See Figure 1
	Negative		10	**12**				mA	
	Positive					10	**12**	mA	See Figure 3
	Negative					10	**12**	mA	
FILTER SECTION									
f_{CLOCK}	Upper Frequency Limit	2	2.5					MHz	See Figure 2
					2	2.5		MHz	See Figure 4
$f_{CLOCKMIN}$	Lowest Practical		1					kHz	See Figure 2
						1		kHz	See Figure 4
	Input Impedance								
	Pin 8		1					MΩ	See Figure 2, f_{CLOCK} = 1 MHz
	Pin 14					1		MΩ	See Figure 4, f_{CLOCK} = 1 MHz
tpw	Minimum f_{CLOCK} Pulse Width	200						ns	See Figure 2
					200			ns	See Figure 4

ELECTRICAL CHARACTERISTICS CONTINUED

Test Conditions: V+ = 5 VDC, V– = –5 VDC, f_{CLOCK} = 2 MHz, R_L = 1 Megohm, C_L = –40 pF, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETERS	XR-1015 MIN	XR-1015 TYP	XR-1015 MAX	XR-1016 MIN	XR-1016 TYP	XR-1016 MAX	UNITS	CONDITIONS
FILTER SECTION CONTINUED									
THD	Total Harmonic Distortion		0.02% 0.1%			0.02% 0.1%			Vin = 2 Vpp f_{CLOCK} = 500 kHz f_{CLOCK} = 2 MHz
	Clock Feedthrough		30			30		mVpp	
V_{INMAX}	Maximum Input Voltage			8			8	Vpp	Above which distortion increases.
	Corner Freq. Accuracy		±0.5%	±1%		±0.5%	±1%		f_{CLOCK} = 2 MHz
A_V	Passband Gain	–0.5	0	+0.5	–0.5	0	+0.5	dB	Tested at f_{in} = 293 Hz, 3.9 kHz, 8.6 kHz, 12.1 kHz
		–1	0	+1	–1	0	+1	dB	Tested at f_{in} = 15.3 kHz, 17.1 kHz
	Ripple Passband		±0.1 ±0.5	 1		±0.1 ±0.5	 1	dB dB	f_{CLOCK} = 500 kHz f_{CLOCK} = 2 MHz
VOS	Voltage Offset	-0.5	-0.2	+0.5	-0.5	-0.2	+0.5	VDC	
	Output Noise		0.6			0.6		mVrms	1 Hz-20Hz, See Figure 8
OPERATIONAL AMPLIFIER									
	Unity Gain Bandwidth		1.2			1.2		MHz	
CMRR	Common Mode Rejection Ratio (2 Vpp Input)		50			50		dB	
V_{IO}	Input Offset Voltage	-30		30	-30		30	mV	

Application Information

The XR-1015 and XR-1016 are fabricated in P-well CMOS. This uses a N^- substrate and requires the V_{DD} to be applied first before V_{SS} in order to prevent latchup of the device.

In addition to the above caution, the input signals should not be applied above the power supply levels, to prevent latchup. The same is true of the input clock.

The input signal should not have any traces or wires near the clock or other system clocks. The same is true of the output. This will help to reduce the clock feedthrough and provide measurements equal to the datasheet values, or better.

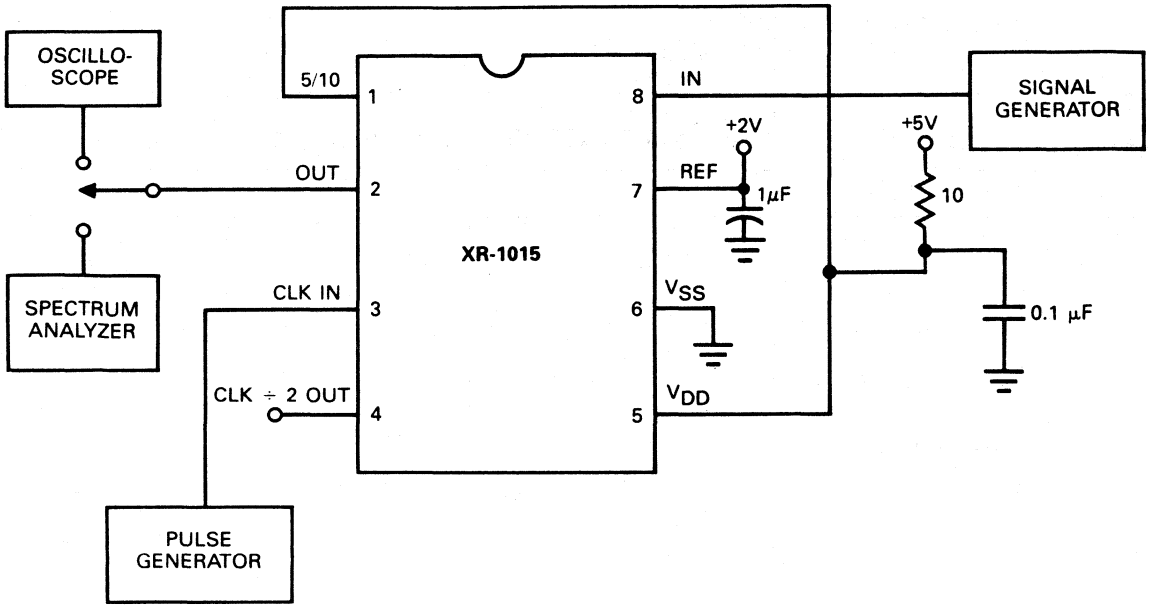


Figure 1. XR-1015 Test Circuit: 5V Operation (V_{DD} = + 5V, V_{SS} = 0V, Ref = +2 V)

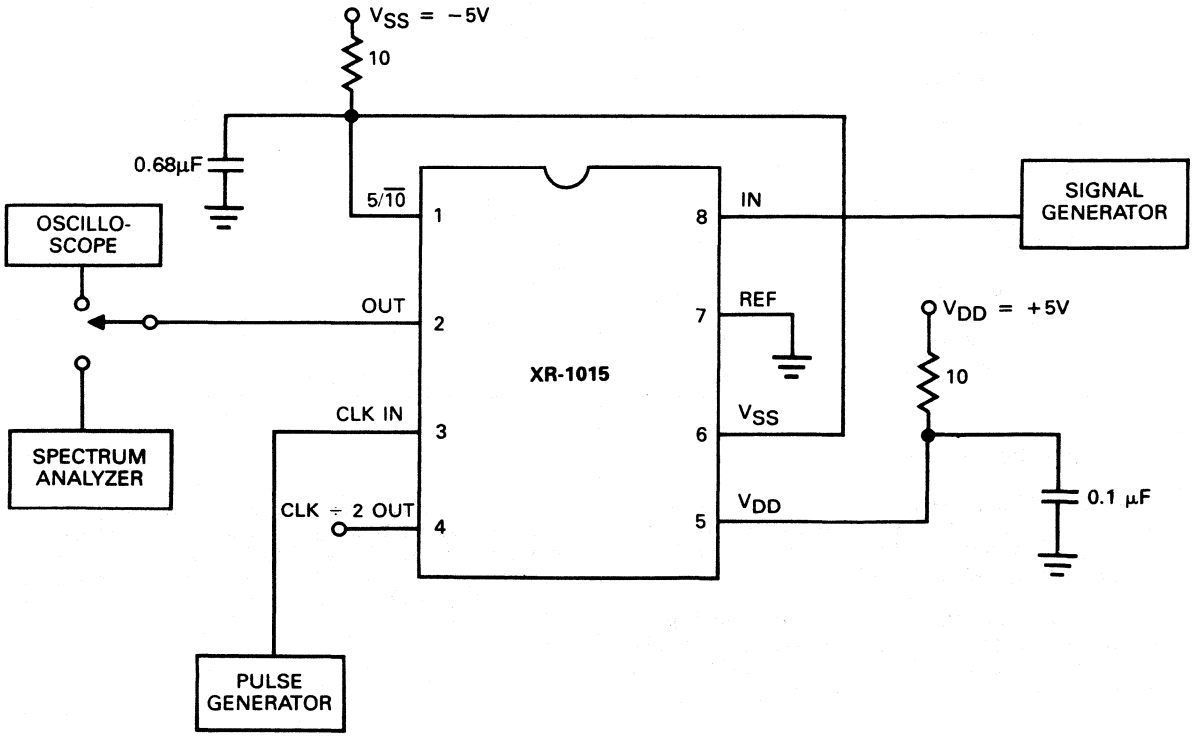


Figure 2. XR-1015 Test Circuit: 10V Operation (V_{DD} = + 5V, V_{SS} = −5V)

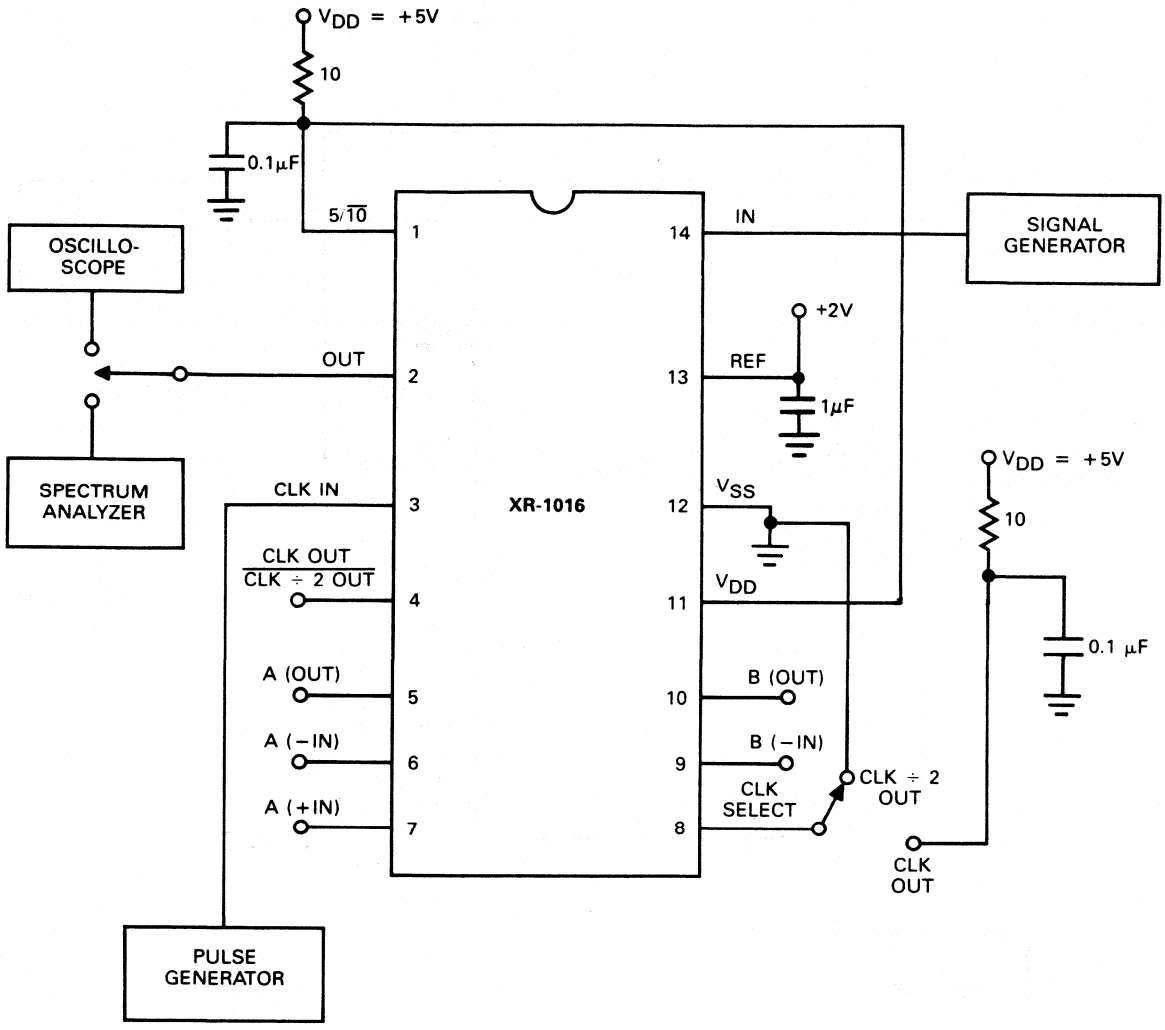


Figure 3. XR-1016 Test Circuit: 5V Operation (V_{DD} = +5V, V_{SS} = 0V, Ref = +2V)

PRINCIPLES OF OPERATION

The XR-1015 and XR-1016 are switched capacitor filters with seven poles and six zeros with an elliptic response. With the elliptic response of the filter, the stop band rejection is greater than 75 dB. The elliptic filter response is called an equal-ripple response, where the ripple in the stop band is an approximation of the ripple in the pass band. In this way the rolloff of the filter response is very fast as shown in Figure 5.

The use of zeros to obtain the stop band attenuation does cause some change in the linearity of the group delay of the elliptic filter. The rapid change in group delay occurs near the corner frequency as shown in Figure 6. This would only be a factor in situations where the output signal must not be delayed by different times for different input frequencies. For applications where the distortion of the phase information is important, the corner frequency of the filter can be placed higher in frequency so that the linear portion of the group delay response of the filter can be located within the information band.

Since the XR-1015 and XR-1016 are sample data filters in that they divide the continuous time signal into an amount of charge at a given time certain limitations must

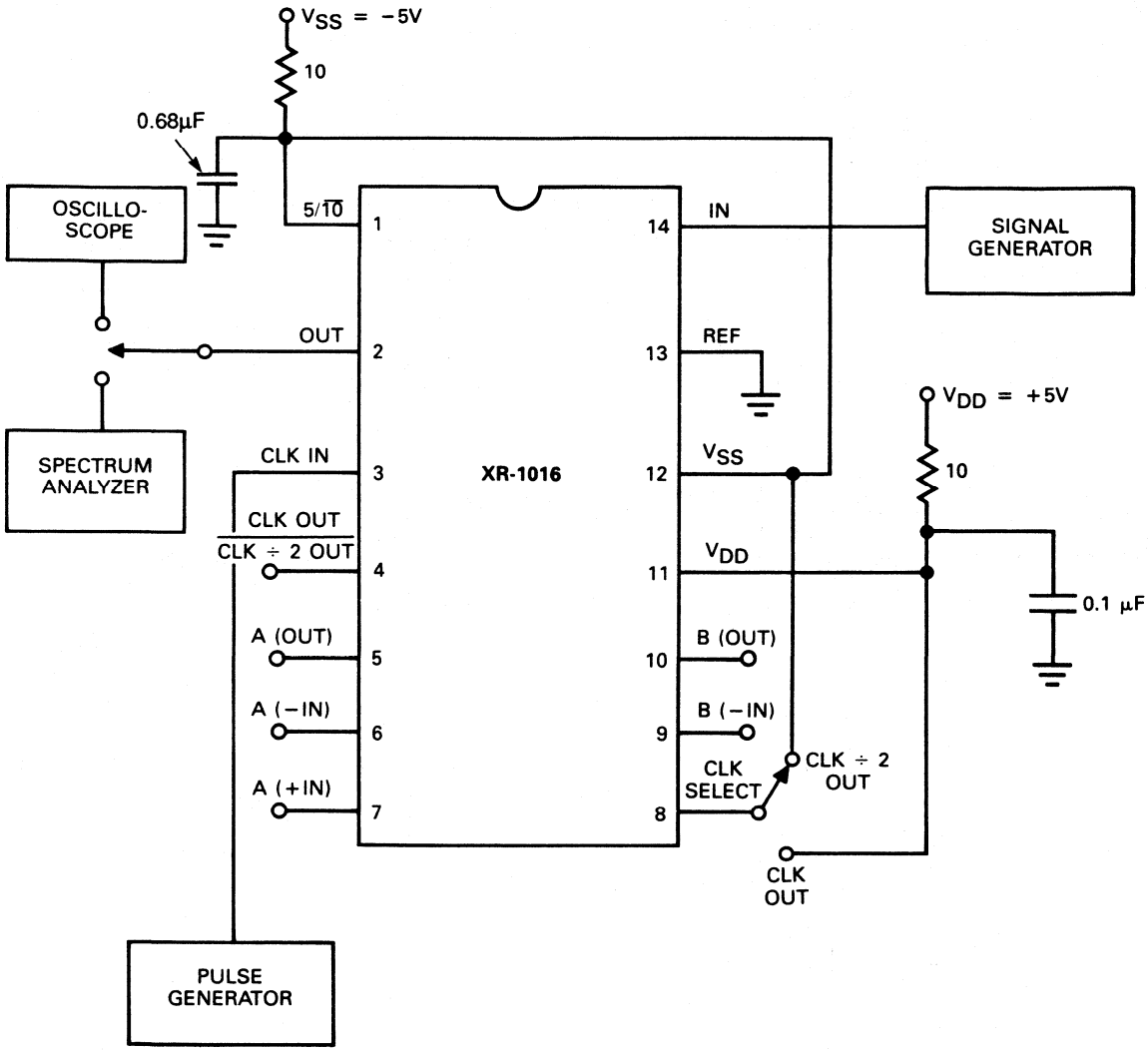


Figure 4. XR-1016 Test Circuit: 10V Operation (V_{DD} = 5V, V_{SS} = −5VDC)

be made on the signals placed on the input of the filters. The frequency of the signal applied to this input must have a period so that at least two samples of the signal are made during the period of the signal. This is true even if the signal is in the stop band response of the filter. The reason for this is that it would take a minimum of two samples of the frequency being applied to establish the period of the signal as well as an approximation of the amplitude. If this sampling criteria is not followed, then the output of the filter will be an aliased signal of the input since the period of the signal would be not accurately known and the frequency would not be known.

If this situation may occur, a simple second order filter can be added to the input. With the XR-1016, operational amplifier A could be used to create this filter. The precision of the location of the corner frequency of the filter is not critical in this situation so that precision resistors and capacitors would not be needed.

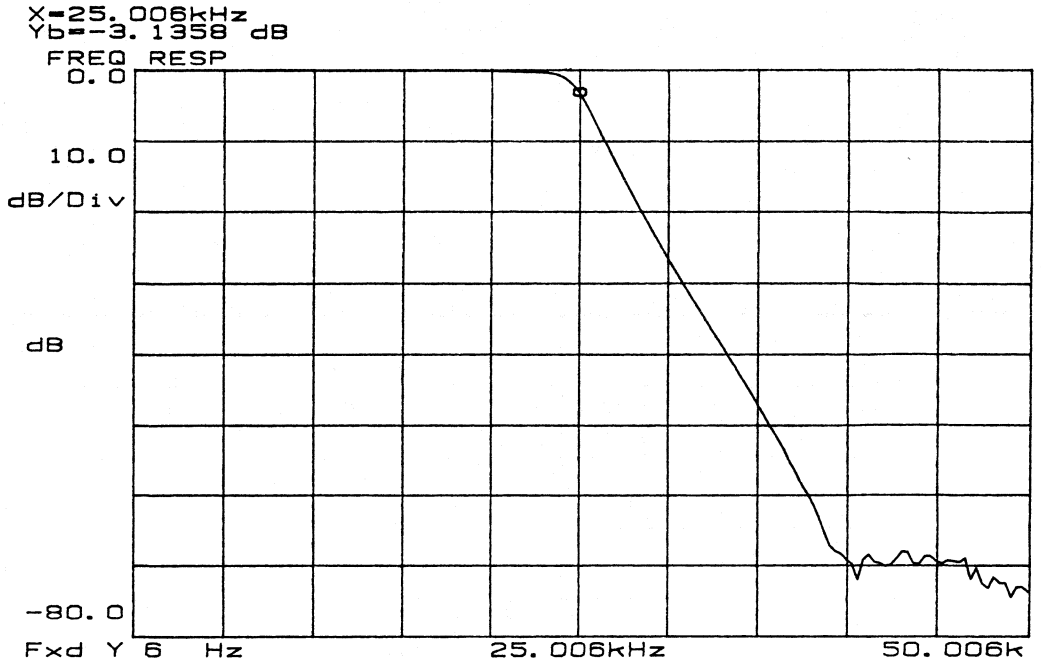


Figure 5. Amplitude Response

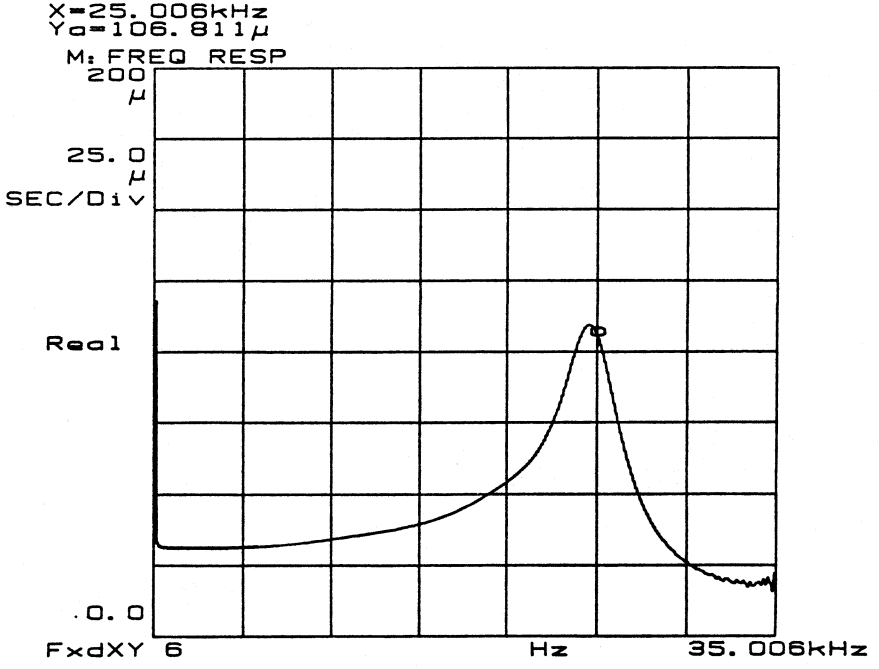


Figure 6. Group Delay Response

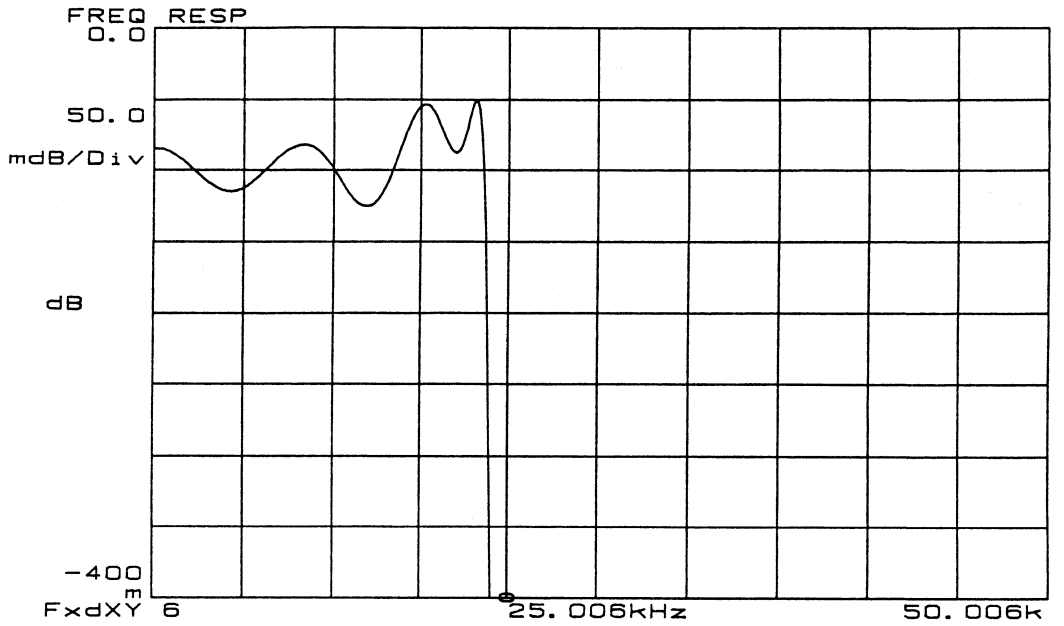


Figure 7. Typical Passband Ripple

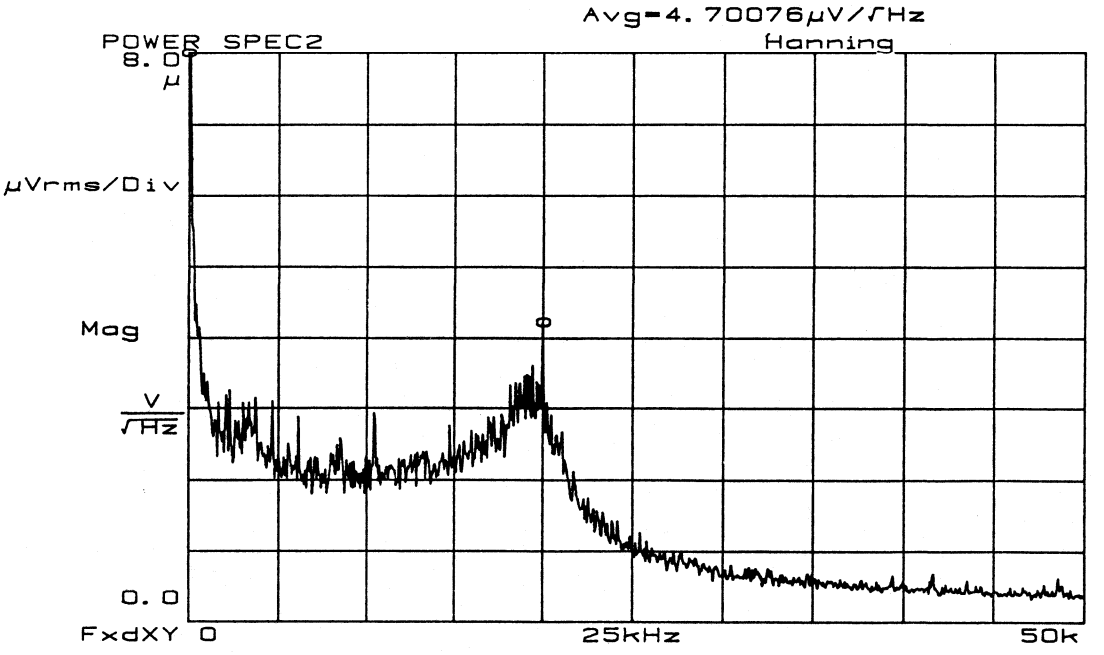


Figure 8. Typical Output Noise

PIN DESCRIPTIONS

1015 Pin	1016 Pin	Name	Description
1	1	5/$\overline{10}$	This controls the reference level of the internal level shifters of the XR-1015 or XR-1016 in order to determine the point at which the device considers the digital inputs to be a logic 1 or a logic 0. When this input is at VSS, the decision level is at 2/3 of the sum of the magnitudes of the VDD and VSS levels relative to VSS. When the 5/$\overline{10}$ pin is tied high, then the decision level is set for 2/3 of the sum of the magnitudes of the VDD and VSS in voltage relative to VDD. Table I shows some of the possibilities of the input logic thresholds. The level at pin 1 does not affect the clock output amplitude. This output is always from near VDD to near VSS in amplitude.

Table 1

VDD / VSS	Level at Pin 1	Logic Decision Level
+5 / −5 VDC	−5 VDC	1.8 VDC
	+5	−1.8 VDC
+5 / 0 VDC	0	3.7 VDC
	+5	1.8 VDC
+2.5 / −2.5 VDC	−2.5	1.2 VDC
	+2.5	−0.7 VDC
+10 / 0 VDC	0	6.8 VDC
	+10	3.2 VDC

2	2	OUTPUT	The filter output. This output will drive a 10 kilohm load. The signal will be centered around the voltage set by ANALOG REFERENCE.
3	–	CLOCKIN	The input clock is applied at this point. The input clock controls the position of the corner frequency of the filter using the ratio: $\frac{\text{fclock}}{\text{fcorner}} = 100{:}1$ The logic threshold level needed at this point is controlled by pin 1, 5/$\overline{10}$. Please see the pin description of 5/$\overline{10}$ for details.
–	3	CLOCKIN	The input clock is applied to this point. The XR-1016 has an internal divider which provides either a clock to corner ratio of 100:1 or 50:1. This is controlled by pin 8 (CLOCK SELECT). If CLOCKIN is low, f_{CLOCK}/f_{CORNER} = 100:1.
4	4	CLOCK/2	This output is the same frequency as the sampling frequency of the XR-1015 or XR-1016. It can be used to synchronize an analog-to-digital converter to the filter's output. The falling edge of the CLOCK/2 output is the edge at which the output (pin 2) should be sampled in order to ensure that the output has settled.
–	5	A(OUT)	Operational amplifier A output. This is provided for creating additional filtering if desired. This output can drive a load of typically 10 kilohms.
–	6	A(−INPUT)	Operational amplifier A negative input. This is a CMOS gate input with virtually infinite input impedance.
–	7	A(+INPUT)	Operational amplifier A positive input. This is a CMOS gate input with virtually infinite input impedance.
–	8	CLOCK SELECT	This pin on the XR-1016 will select the clock to corner ratio of the filter. When this pin is at logic 0, the filter will have a clock to corner of 100:1. When this pin is tied to a logic 1, the clock to corner ratio will be 50:1. The CLOCK CLOCK/2 will always represent the sampling frequency of the XR-1016. This logic level control of this digital input is controlled by pin 1 5/$\overline{10}$ as described under that pin description.
–	9	B(−INPUT)	Operational amplifier B negative input. Notice that the positive input of this operational amplifier B is tied internally to the ANALOG REFERENCE.
–	10	B(OUT)	Operational amplifier B output.

5

5	11	VDD	Positive supply input. The range of voltages of this point is from +2.5 VDC to +5 VDC when used with dual supplies of equal magnitude. If a single supply is used the range is from +5 VDC to +10 VDC. It is recommended that a 0.47 μF capacitor be tied from this pin to ground to decouple the noise on the supply line which can degrade the performance of the filter. If very low clock frequencies are used, then the size of the capacitor should be increased to keep the noise on the supply at a minimum. This capacitor should be located as close to the VDD pin as possible. It is suggested that a 10 ohm resistor from the positive supply to VDD be used to filter system supply noise from the filter.
6	12	VSS	Negative supply input. The range of the input is from −5 VDC to 0 VDC depending on the voltage present at VDD. It is recommended that the pin be decoupled with a 0.47 μF capacitor located as physically close as possible to the VSS pin and tied from VSS to ground. It is recommended that a 10 ohm resistor from the negative supply to VSS be used to filter system supply noise from the filter.
7	13	ANALOG REFERENCE	This pin provides the level at which the analog signals will be referenced. If equal split supplies are used, then this point is tied to ground. If unequal supplies or a single supply is used, then this point should be tied to a resistor divider circuit to provide a voltage at the analog reference pin that is ½ of the algebraic sum of the two supplies. Since this point is used as analog ground inside the device, it is recommended that a 0.47μF capacitor be tied from this pin to ground. As with the VDD and VSS decoupling, the size of this capacitor should be made larger if the clock frequency is decreased.
8	14	FILTER IN	Filter input: The signal that needs to be filtered is applied to this point. It has an input impedance of 4 Megohms at 1 MHz clock frequency. It should be noted that any signal applied to this input greater than ½ of the sampling frequency will be aliased into the band of interest.

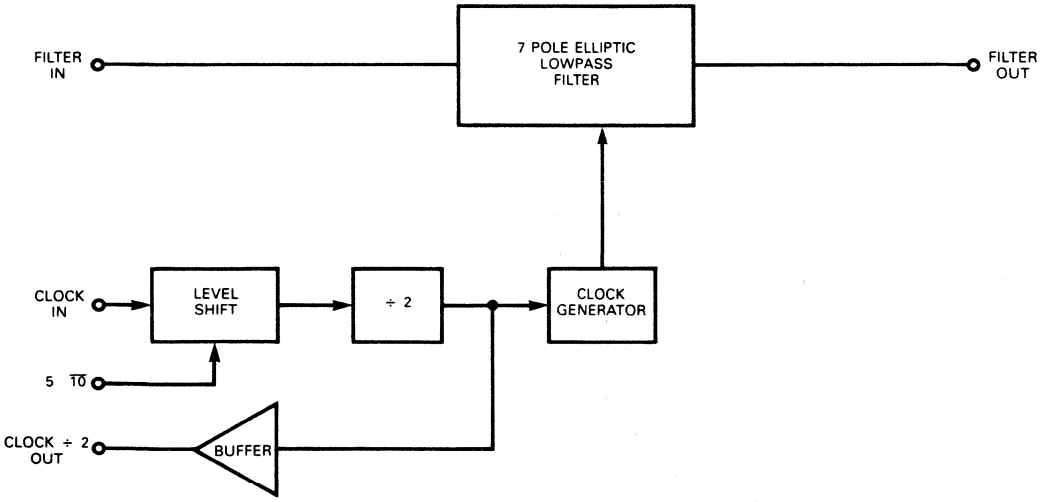


Figure 9. XR-1015 Block Diagram

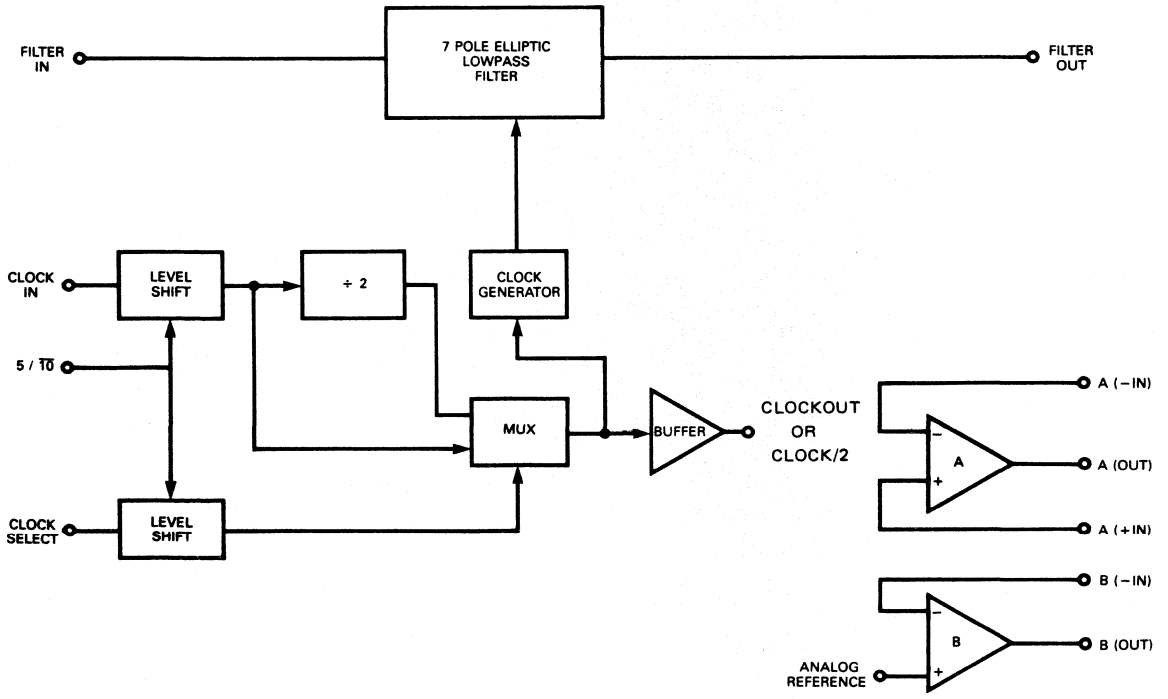
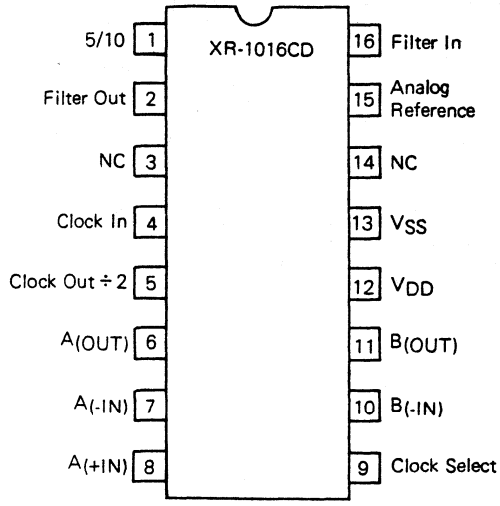


Figure 10. XR-1016 Block Diagram


XR-1016CD
5/10 1
Filter Out 2
NC 3
Clock In 4
Clock Out ÷ 2 5
A(OUT) 6
A(-IN) 7
A(+IN) 8
16 Filter In
15 Analog Reference
14 NC
13 VSS
12 VDD
11 B(OUT)
10 B(-IN)
9 Clock Select

Telecom Instrumentation Filter

GENERAL DESCRIPTION

The XR-1020A is a data communication/telecommunication instrumentation filter. This device provides ten of the filters used to characterize communication links for both IEEE/Bell and CCITT standards. The filters are:

1. C-message weighting filter
2. C-notch filter (1010 Hz)
3. Psophometric filter (CCITT equivalent of C-message weighting filter)
4. CCITT psophometric notch filter (825 Hz)
5. Program weighting filter
6. 3 kHz flat filter
7. 15 kHz flat filter
8. 1 kHz band-pass filter (phase jitter measurements)
9. 50 kilobit filter (low-pass filter portion only)
10. Peak-to-average ratio band-pass filter (P/AR)

The control and selection of the ten filters is achieved with an eight bit microprocessor bus structure, complete with a strobe line ($\overline{S}$) and chip select ($\overline{CS}$). This simplifies the control of the filter functions. On-chip reconstruction filters provide the smoothing of the signals needed for precise **measurements. The XR-1020A provides lower output noise then the original XR-1020.**

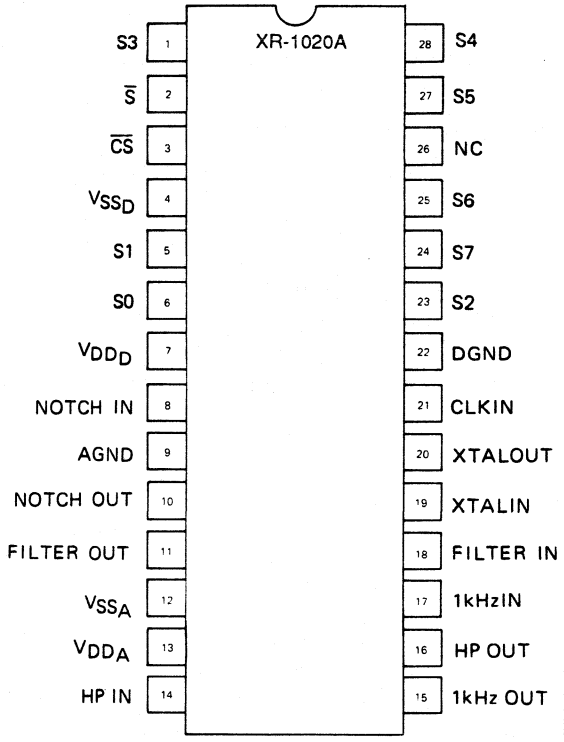
The XR-1020A uses a single 3.579545MHz crystal to provide the clock needed for the switched capacitor filters. This creates a nearly self-contained unit, requiring only digital controls for the filter selection. Additional external clock input is provided if a crystal controlled clock cannot be obtained. Also included is a power down mode allowing the device to be used in battery operated applications.

The **XR-1020A** uses switched capacitor techniques to implement the filter functions. The **XR-1020A** is fabricated in 3 micron polysilicon gate CMOS process for low noise.

FEATURES

Ten Filters Provided in One 28 Pin Dual In-Line (DIP) Package
Microprocessor Bus Interface
Low Noise
Power Down Mode for Battery Operation
3.579 MHz Clock Operation with On-chip Oscillator
Separate Notch Filter Output
Separate 1 kHz Band-Pass (Phase Jitter Measurements) Filter Output
TTL/CMOS Compatible Digital Inputs
On-chip Output Smoothing Filters

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS

Telephone Impairment Measurement Sets (TIMS)
C-message Weighted Meters
Telecommunication Test Instruments
Audio Test Systems
General Instrumentation Puposes
Network Management Systems

ABSOLUTE MAXIMUM RATINGS

Power Supply (Relative to V_{SS})	14 VDC
Power Dissipation (Package Limitation)	
Ceramic Package	1.4 W
Derate Above 25°C	5 mW/°C
Plastic Package	1 W
Derate Above 25°C	6 mW/°C
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage at any Input	V_{SS} – 0.3 to V_{DD} + 0.3 VDC

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1020ACN	Ceramic	0°C to 70°C
XR-1020ACP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The **XR-1020A** provides most of the filters used to characterize telephone line quality as well as other telecommunication lines. It can be used with a microprocessor, allowing easy selection of a particular filter function.

The **XR-1020A** supplies the filters for the Bell Systems Technical Reference 41009, the IEEE Standard 743-1984 and the CCITT Series O Recommendations. The XR-1020 is used either with an external clock or with a 3.579545 MHz Colorburst crystal.

The **XR-1020A** provides an on-chip latch which allows the device to be memory mapped, that is, considered a memory location rather than a special access port. This simplifies the software writing and increases the versatility of the device.

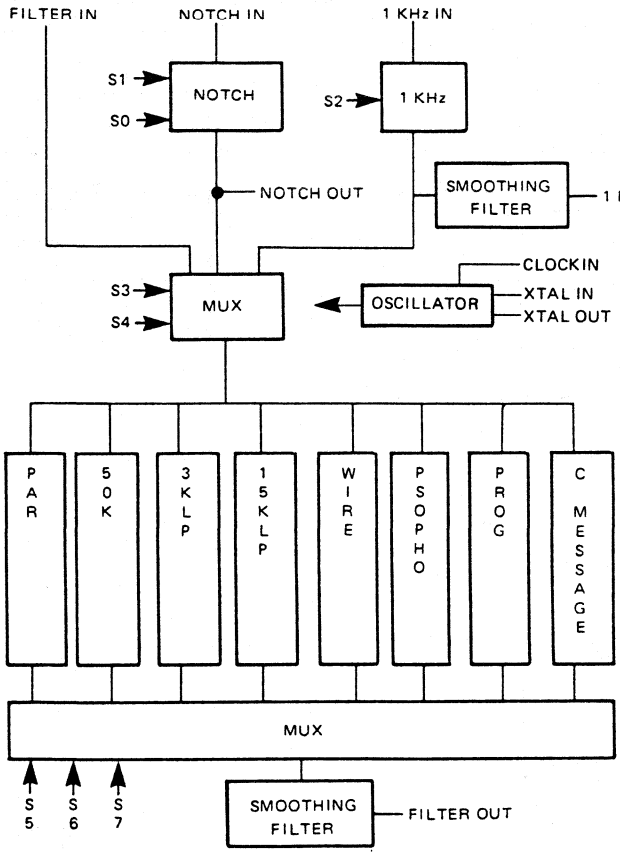
The functional block diagram of the device is illustrated in Figure 1.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = +5 VDC, V_{SS} = -5 VDC, R_{load} = 1 Megohm, C_{load} = 40 pF, T_A = 25°C, unless specified otherwise.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL CHARACTERISTICS						
V_{DD}	Positive Supply Voltage Single Supply Split Supply	 9.5 4.75	 10 5	 10.50 5.25	 VDC VDC	 V_{SS} = 0 VDC
V_{SS}	Negative Supply Voltage Split Supply	 -5.25	 -5	 -4.75	 VDC	
I_{DD}	Positive Supply Current Single Supply Split Supply		 10 10	 14 14	 mA mA	 V_{SS} = 0 VDC
I_{SS}	Negative Supply Current		-10	-14	mA	
BUS INPUT CHARACTERISTICS						
V_{IL}	Input Voltage, Logic Low			0.8	V	
V_{IH}	Input Voltage, Logic High	2.8			V	
I_{IL}	Input Current, Logic Low	-1.0		+1.0	μA	
I_{IH}	Input Current, Logic High	-1.0		+1.0	μA	
t_{CS}	Time for Chip, Select To Latch	100			nS	See Figure 5
t_{SB}	Time for Strobe to Latch	100			nS	See Figure 5
t_{data}	Time for Data to Be Stable	150			nS	See Figure 5
t_{delay}	Delay Time from Strobe or Chip Select to Data Change	50			nS	

S1	S0	FUNCTION
X	0	Notch Off (Powered Down)
0	1	1010 Hz Notch
1	1	825 Hz Notch



S2	FUNCTION
0	1K Off (Powered Down)
1	1K

S4	S3	FUNCTION *
0	X	FILTER IN PIN
1	0	NOTCH OUTPUT
1	1	1K OUTPUT

* S4-S3 determine what is selected by the input mux as input to the mode selected by S7-S5.

S7	S6	S5	FUNCTION
0	0	0	PAR
0	0	1	50K
0	1	0	3K LP
0	1	1	15K LP
1	0	0	WIRE
1	0	1	PSOPHOMETRIC
1	1	0	PROG-WEIGH
1	1	1	C MESSAGE

—The 1 KHz and NOTCH (825 Hz & 1010 Hz) filters have separate outputs. The 1 KHz output is passed through a smoothing filter. The WIRE mode can be used for smoothing the NOTCH filter output, if desired.

—The highpass portion of the 50 K filter (external) is connected in between the HPIN and HPOUT terminals: HPIN is connected to the output of the highpass? HPOUT is connected to the input of the highpass.

—3.579545 MHz colorburst crystal is connected in between the XTALIN and XTALOUT pins. In this case, the CLKIN pin should be connected HI or LO. 20pF capacitors on both sides of the crystal to ground, as well as a 10MΩ resistor across the crystal are needed.

If the above clock frequency is already available in the system, then the CLKIN pin can be used. In this case, the XTALIN pin should be connected to V_{DD} or to V_{SS}.

—The microcompatibility is controlled by the S (strobe) and CS (chip select) pins. Both inputs must be LO for input to latch.

Figure 1. Block Diagram

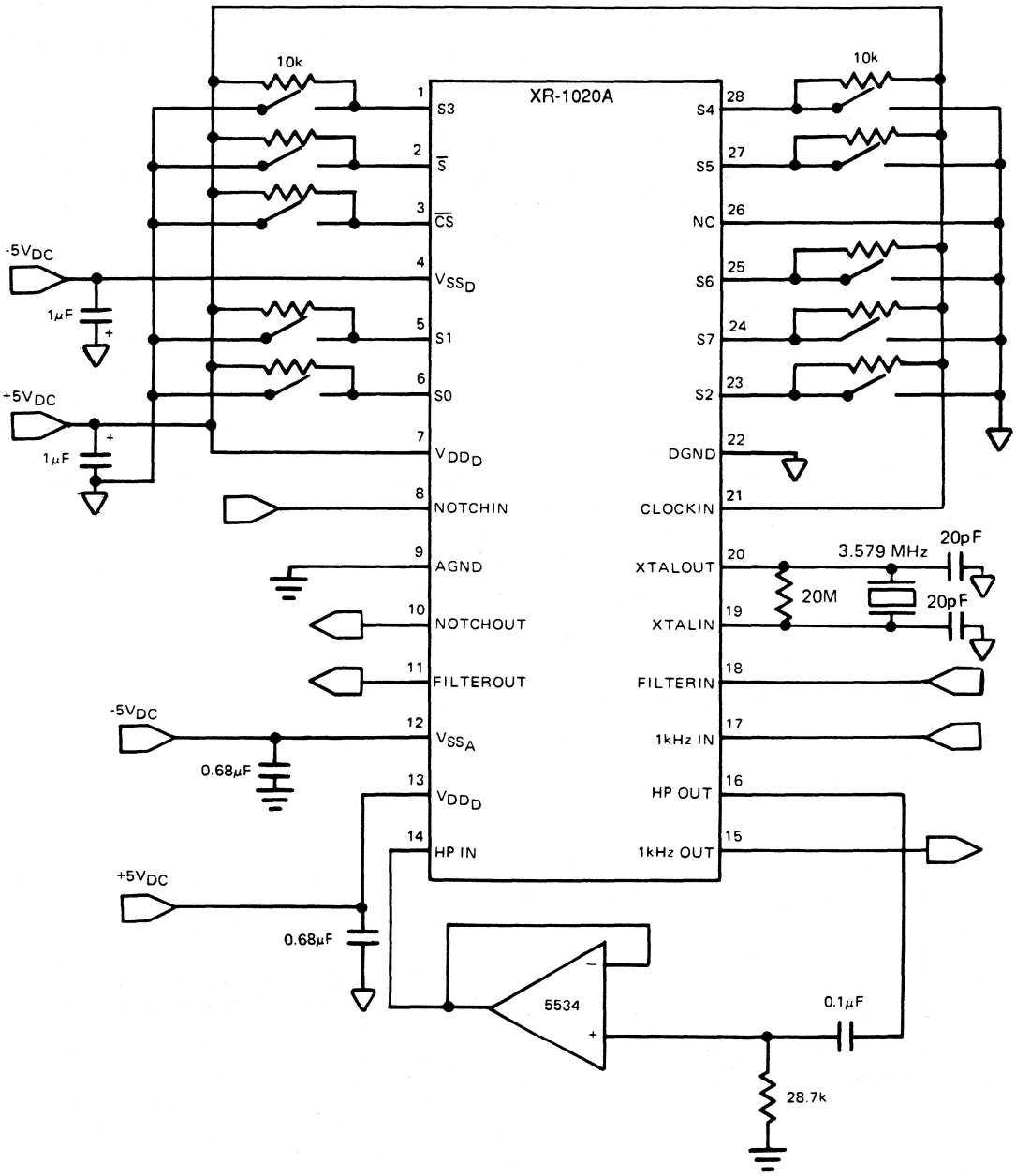


Figure 2. Typical Test Circuit

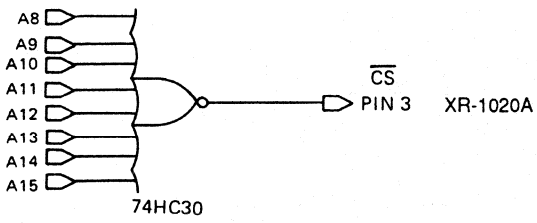


Figure 3. Typical Method for High Order Byte Decoding

SYSTEM DESIGN USING THE XR-1020

The XR-1020A has been optimized for use with a standard 16 bit wide address bus. A decoder circuit will be needed for using the $\overline{CS}$ pin of the XR-1020. The lower 8 bits should be tied directly to the S0 through S7 digital inputs of the XR-1020A.

The higher order bits A8 through A15 need a decoder depending upon the system and the present use of the microprocessor. In one application, where location OXFFXX is to be used for the XR-1020A the 74HC30 can be used for decoding the location. Figure 3 shows the use of the XR-1020A with the 74HC30. When the high order byte is high, the output of the 74HC30 will go low, which would select the XR-1020A for use. With the use of inverters, other locations can be decoded and used.

Figure 1 gives information as to which function is selected. The pin description provides information as to which bit controls which filter function.

The strobe pin, used to latch in the information present on the address bus, can be used when the data lines and lower byte address are multiplexed on the same eight lines.

In applications where a microprocessor will not be used (analog meters or other manual select systems), a decoder can be used such as the 74HC148 to convert the switch information to a binary format. Figure 5 shows the use of the XR-1020A with the 74HC148 for a push button system. The pin descriptions can be used in this application to determine the decoding of the button function of the system.

The use of the 50 kilobit filter requires a 50 Hz high-pass filter to be added to the HPOUT and HPIN pins of the XR-1020A. Figure 13 shows the filter shape used for this: The schematic for this first order, continuous time high-pass filter is shown in Figure 1. To prevent degradation of the performance of the XR-1020A it is recommended that a low noise operational amplifier such as the XR-5532 be used for the filter shaping. Also, the components should be 1% precision in order to prevent the filter shape from changing with production variations. Such a situation may cause peaking in the pass-band response and affect the measurements obtained with the 50 kBPS filter.

If no consideration is given to the layout of the external operational amplifier circuit, additional noise may be added to the signal present on the output of the low-pass reducing the dynamic range of the 50 kBPS amplitude and distortion tests. The feedback trace from the operational amplifier output to the inverting input should be kept as short as possible. This will reduce the chance of any stray noise from being amplified by the filter.

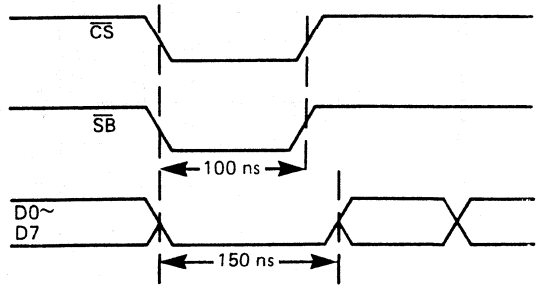


Figure 4. Typical Timing for $\overline{CS}$ and $\overline{S}$ Data Bus

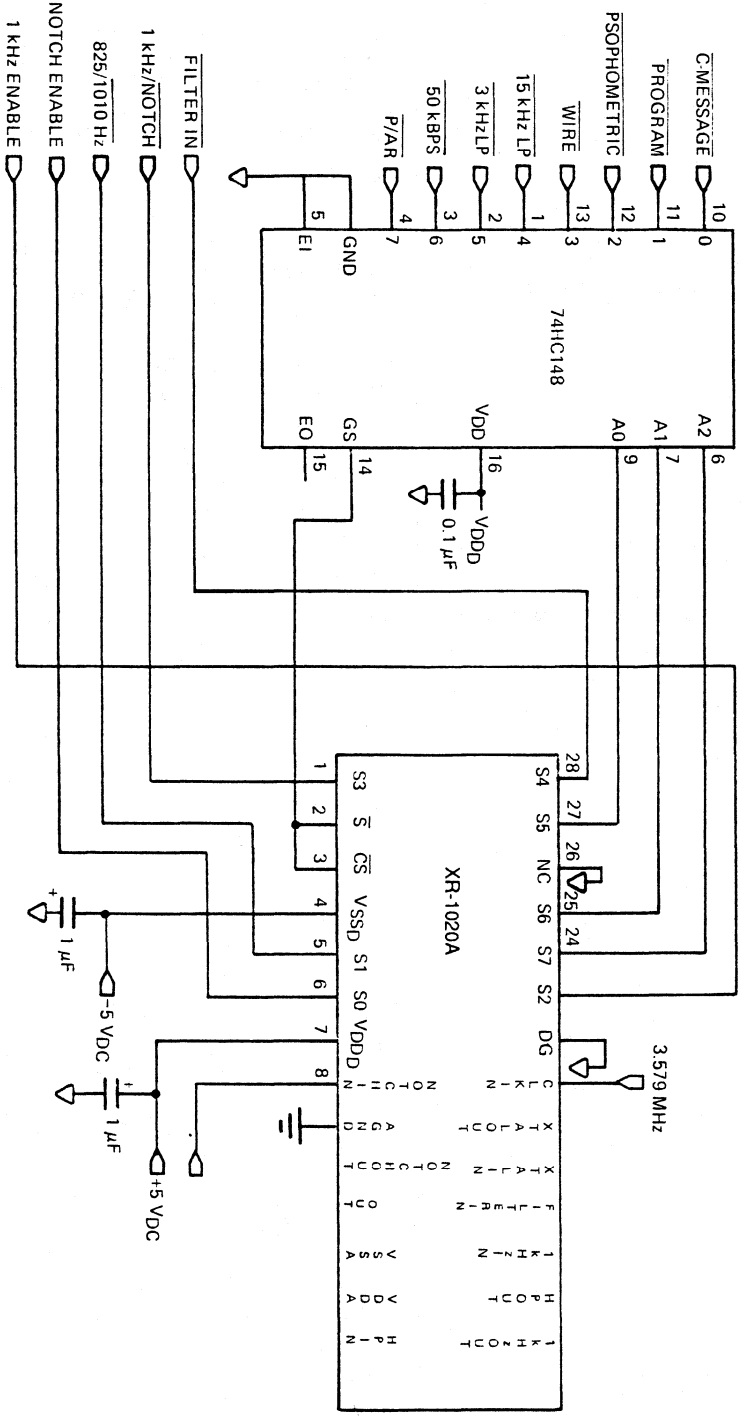


Figure 5. Push Button Interface with the XR-1020 (without microprocessor)

PIN DESCRIPTIONS

Pin	Mnemonic	Description
1	S3	Digital Input S3: This with S4, Pin 28 selects which input is applied to the filter bank as shown in the block diagram.
2	$\overline{S}$	Strobe: This input, when high, latches in the data present on the lines S0 through S7. When $\overline{S}$ is high, changes on the address bus will not affect the state of **XR-1020A.**
3	$\overline{CS}$	Chip Select: This input, when low, selects the **XR-1020A** for addressing. The delay between chip select going high and strobing in the new address is 50 ns.
4	V_{SSD}	Digital V_{SS}: This input is the negative supply for the digital portion of the **XR-1020A.** In order to obtain the low noise operation that is needed in an instrumentation filter, this input must be decoupled with a 10 μF tantalum, in parallel with a 0.68 μF ceramic capacitor.
5	S1	Digital Input S1: Selection of the 825 Hz or 1010 Hz filter is done with this input. When this input is latched high, the 825 Hz notch for CCITT standard measurements is selected. When this input is latched low, the 1010 Hz notch filter for Bell standard measurements is selected. This assumes that S0 is latched high.
6	S0	When high, the notch filter is selected. When a logic low is latched on this pin, the notch filter is in the power down mode. S1 input is in a "don't care" situation when S0 is latched low.
7	V_{DDD}	Digital V_{DD}: This input is the positive supply for the digital **portion of the XR-1020A. Proper** decoupling of this pin is required for low noise operation of this instrumentation filter. Decoupling with a 10μF tantalum capacitor, in parallel with a 0.68μF ceramic capacitor is required.
8	NOTCH IN	Notch filter input: This is the input to the notch filter. The location of the notch (1010 Hz or 825 Hz) is set with the address bus as outlined Figure 1. Since this is an analog input, it is best to keep this signal as far as possible from any digital inputs. Shielding is recommended in most applications to prevent any clock coupling from occurring. The input impedance at this pin is 1 megohms.
9	AGND	Analog ground: This pin is the analog reference for the XR-**1020A. In order to obtain the low** noise operation possible with the **XR-1020A, it is very important to** have a very low noise ground available. For split supply operation, the AGND pin should have its own separate trace from the supply connector on the edge of the system board to here. To prevent any inductive components, this trace should be as wide as possible, or as short as possible. An ideal case would be to have the analog ground also act as a ground plane or shield for pins 8 through 18. The shield should be kept away from the digital inputs and clocks.
10	NOTCH OUT	Notch filter output: This is the output of the 1010 or 825 Hz notch filter. It is designed to drive a typical 10 kilohm load. For distortion analysis, it is necessary to keep this signal from any clocks or other signals that may couple to this trace and cause an error in measurements. Note that the notch filter input (Pin 8) is separated from the output by analog ground for this reason.

To combine the notch output with other portions of the system, the SD5000 quad NMOS **field-effect transistors or the 74HC4053 is recommended, due to the low on resistance and the small cross coupling.**

11 FILTER OUT

Filter output: This is the output of the output multiplexer and continous-time smoothing filter. The filter shape available at this point is controlled by the address lines S0 through S7. The C-message weighting, Program weighting, psophometric, 3 or 15 kHz low pass, 50 kBPS low pass, and peak-to-average filters can be obtained at this pin.

This output should be kept away from other clocks in the system to avoid coupling of this signal to the signal present at this pin.

As with the notch filter output, this output is designed to typically drive a 10 kilohm load.

12 V_{SSA}

Analog V_{SS}: This is the negative supply for the analog portions of the XR-1020A. **It must be** a low noise, low impedance supply to obtain satisfactory performance from the XR-1020A, and avoid any degradation in the operation of the filters.

With split supply operation, this pin is tied to -5 VDC ±5%. It must be decoupled with a 0.68 µF ceramic capacitor to analog ground. In parallel with the ceramic capacitor, a 10µF tantalum capacitor must be used. This will prevent any noise on the supply lines from being coupled to the signals to be filtered. These two caps must be located as close as possible to Pin 12 of the device. If possible, the best arrangement is obtained when a separate V_{SS} **regulator is used. The LM79L05AC could be used in such a case. The output of the regulator should be tied only to V_{SS}A, Pin 12 of the XR-1020A.**

13 V_{DDA}

Analog V_{DD}: This is the positive analog supply and must be decoupled to analog ground with a 10µF tantalum capacitor as well as a 0.68µF ceramic capacitor. These capacitors should be as physically close to Pin 13 of the package as possible.

This analog V_{DD} should be separated from the digital V_{DD} throughout the system connecting only at the supply connector of the system This pin is set to +5 VCD (±5%).

Note that in both single and split supply operation, the decoupling is needed. In single supply operation, this pin should be tied to +10 VDC (±5%).

For optimum performance, a regulator such as the XR-4194 with the above decoupling should be used. This regulated should only be used with the XR-1020 V_{DDA}. An LM78L-05AC could be used as well. This prevents any noise present on the system V_{DD} from affecting the measurements made with the **XR-1020A.**

14 HP IN

50 kBPS input: This, in most applications, is tied to the output of the external 50 Hz high-pass filter. Note that this input is tied internally to the output multiplexer so that no external selector needs to be used in most applications.

The entire 50 Hz continuous time high-pass filter as well as the input and output of the 50 kBPS filter should be kept away from the rest of the system's clocks, to prevent degradation of the measurements made.

15 1 kHz OUT

1 kHz band-pass filter output: This output is provided separate from the other filters for tests requiring phase jitter measurements at the same time as other measurements.

A continuous time smoothing filter is provided to eliminate the need of an external filter.

Note that there are some address selections that can keep the 1 kHz (phase jitter) filter in the power down mode and provide no output. Refer to Figure 1 for details.

As with other outputs, this pin can typically drive a 10 kilohm load.

16 HP OUT

50 kBPS filter output: This output is used to add the external 50 Hz high-pass filter to the 50 kBPS low-pass filter shape.

Note that no output will appear at this pin if the 50 kBPS is not selected using the address bus. Refer to Figure 1 for more information.

The output is designed to drive a 10 kilohm load. This should be considered when the external circuit is designed.

17 1 kHz IN

1 kHz band-pass filter input: This input provides access to the phase jitter band-pass filter input. It is separated from the other filter functions in order to allow for flexibility in measurements.

As with the other filter inputs, this input should be kept away from any system clocks that may add noise to the inputs. A ground plane or trace surrounding this and other filter input pins will be helpful.

The input impedance at this pin is 1 megohms.

18 FILTER IN

Filter multiplexer input: This input provides access to the eight filter functions, as described in Figure 1.

The input impedance at this pin is 1 megohms.

19 XTAL IN

Crystal input: This is used with the XTAL OUT to create a 3.579545 MHz oscillator. A parallel ressonant crystal should be used to obtain the ±0.01% accuracy to prevent clock inaccuracy from affecting the position of the filter shape. If not used, it must be tied to either V_{DD_D} or V_{SS_D}.

20 XTAL OUT

Crystal output: This input is used with the Pin 19 crystal input to obtain the clock. Note that the external capacitors used to accurately set the crystal oscillating frequency as shown in the Typical Application Circuit diagram.

A parallel resonant crystal must be used to obtain the proper oscillatory frequency. If this pin is not used, it should be disconnected.

21 CLK IN

Clock input: At this pin is applied the 3.579545 MHz clock from the system if it is desired not to use the on-chip oscillator. If this pin is not used, it should be tied to either V_{DD_D} or V_{SS_D}.

22 DGND

Digital ground: This input provides the reference for the digital portions of the XR-1020A. It should be tied to the digital ground of the system, separate from the analog ground of Pin 9, AGND. The two grounds may connect at the supply.

As with the analog ground, a wide trace is needed to reduce any inductive components in the system.

23 S2

Digital input S2: This is address line 2 and controls the use of the 1 kHz band-pass (phase jitter) filter. When latched high, the 1 kHz band-pass filter is selected. When this input is latched low, the 1 kHz band-pass filter is in the power down mode. Details on its operation are given in Figure 1. With split supply operation, all digital inputs are TTL compatible.

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24	S7	Digital input S7: This input, along with the address lines S6 and S5, control the selection of the eight filters obtained with the on-chip multiplexers. Details are given with the pin description for digital input S5.
25	S6	Digital Input S6: This input, with address lines S7 and S5, controls the input and output multiplexers. This is detailed with the pin description for S5, digital input S5 (Pin 27).
26	NC	No internal connection: Due to the closeness to the other digital inputs, it is recommended that this pin be tied to digital ground (DGND), Pin 22.
27	S5	Digital input S5: This digital input, along with S7 and S6, controls which of eight filter functions will be selected using the on-chip multiplexers.

S7	S6	S5	Function
0	0	0	Peak-to-average filter is selected.
0	0	1	50 kBPS filter is selected.
0	1	0	3 kHz low-pass filter is selected.
0	1	1	15 kHz low-pass filter is selected.
1	0	0	Wire (direct from input multiplexer to output multiplexer).
1	0	1	Psophometric weighting filter (for CCITT noise measurements).
1	1	0	Program-weighting filter.
1	1	1	C-message weighting filter (for Bell noise measurements).

28	S4	Digital input S4: This digital input along with S3 (Pin 1) selects which of the three inputs will be applied to the input multiplexer.

S4	S3	Function
0	X	Filter input. Note that when S4 is latched low, S3 is in the "don't care" mode.
1	0	1010 Hz (825 Hz) notch filter is the input selected. Note that if S0 is latched low, then no usable signal would be applied to the filter bank since the notch filter would be in the power down mode.
1	1	When this combination is latched into the XR-1020, the 1 kHz band-pass (phase jitter) filter is selected. Note that S2, the 1 kHZ band-pass filter enable must be latched high, or no usable output will appear at the filter output.

Board Layout

The device is divided approximately in half with Pins 1 through 7, and Pins 19 through 28 having digital functions, and the rest having an analog function. It is best to use the **XR-1020A at the dividing point between the analog and digi**tal portions of the systems as would be done with an analog-to-digital converter.

An analog ground plane for the filter inputs and outputs is recommended, as long as the trace from the ground plane to the supply ground can be made wide enough to prevent the ground plane from acting as a capacitor or an antenna.

FILTER CHARACTERISTICS

1 KHz Band-pass Filter (Phase Jitter), see Figure 6

Parameter	Min.	Typ.	Max.	Unit	Conditions
Output Offset Voltage	-0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency					
Less than 100 Hz		-35		dB	V_{in} = 1 Vrms
150 Hz			-28	dB	
250 Hz		-20		dB	
300 Hz	-15		-18	dB	
500 Hz	-10		-8	dB	
600 Hz	-5	-5		dB	
700 Hz	-3	-3		dB	
1000 Hz	-1	0	+1	dB	
2000 Hz		-2		dB	
3000 Hz		-20	-18	dB	
Greater than 3500 Hz	-25			dB	

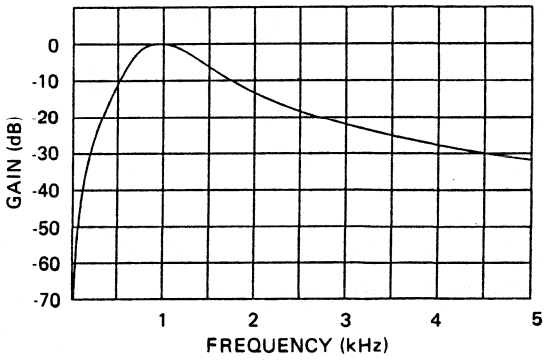

Figure 6. Amplitude Response: 1 kHz Band-pass

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FILTER CHARACTERISTICS

C-Message Weighting Filter, see Figure 7

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output Offset Voltage	-0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency					
		-55.7		dB	Vin = Vrms
100 Hz		-42.5		dB	
200 Hz	-27.0	-25.1	-23.0	dB	
300 Hz		-16.3		dB	
400 Hz	-12.2	-11.2	-10.2	dB	
500 Hz		-7.7		dB	
600 Hz		-5.0		dB	
700 Hz		-2.8		dB	
800 Hz		-1.3		dB	
900 Hz		-0.3		dB	
1000 Hz	-1.0	0.0	+1.0	dB	
1200 Hz		-0.4		dB	
1300 Hz		-0.7		dB	
1500 Hz		-1.2		dB	
1800 Hz		-1.3		dB	
2000 Hz		-1.1		dB	
2500 Hz		-1.1		dB	
2800 Hz		-2.0		dB	
3000 Hz	-4.0	-3.0	-2.0	dB	
3300 Hz		-5.1		dB	
3500 Hz	-9.1	-7.1	-5.1	dB	
4000 Hz		-14.6		dB	
4500 Hz		-22.3		dB	
5000 Hz	-31.7	-28.7	-25.7	dB	

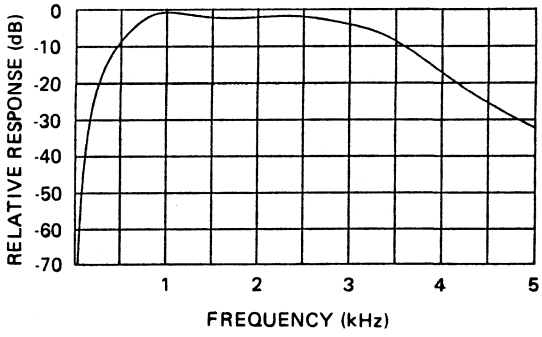

Figure 7. Amplitude Response: C-Message

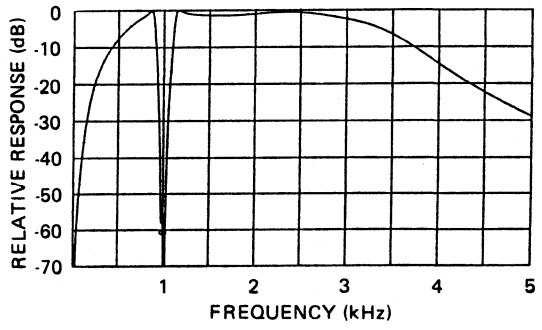

Figure 8. Amplitude Response: C-Notch (1010 Notch with C-Message Weighting Filter)

FILTER CHARACTERISTICS

Psophometric Weighting Filter, see Figure 9.

Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OS} Output Offset Voltage	-0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency					
16.66 Hz		-85		dB	Vin = Vrms
50 Hz		-63.0		dB	
100 Hz		-41.0		dB	
200 Hz	-23.0	-21.0	-19.0	dB	
300 Hz		-10.6		dB	
400 Hz	-7.3	-6.3	-5.3	dB	
500 Hz		-3.6		dB	
600 Hz		-2.0		dB	
700 Hz		-0.9		dB	
800 Hz	-1.0		+1.0	dB	
900 Hz		+0.6		dB	
1000 Hz		+1.0		dB	
1200 Hz	-1.0	0.0	+1.0	dB	
1400 Hz		-0.9		dB	
1600 Hz		-1.7		dB	
1800 Hz		-2.4		dB	
2000 Hz		-3.0		dB	
2500 Hz		-4.2		dB	
3000 Hz	-6.6	-5.6	-4.6	dB	
3500 Hz		-8.5		dB	
4000 Hz		-15.0		dB	
4500 Hz		-25.0		dB	
5000 Hz		-36.0		dB	
6000 Hz	-47	-43	-39	dB	

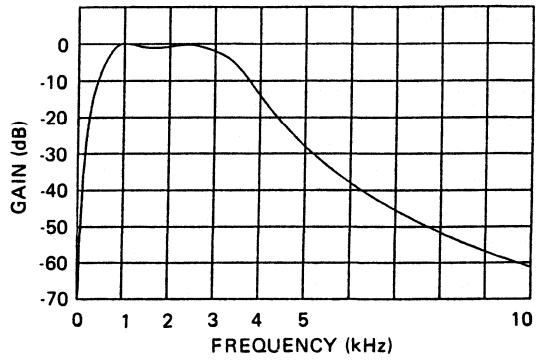

Figure 9. Amplitude Response: Psophometric Filter

FILTER CHARACTERISTICS

3 kHz Low-Pass Filter, see Figure 10

Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OS} Output Offset Voltage	-0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency					
30 Hz		0		dB	Vin = Vrms
60 Hz		0		dB	
400 Hz	-1	0	+1	dB	
1000 Hz	-1	0	+1	dB	
2010 Hz	-1.8	-0.2	+0.2	dB	
3000 Hz	-4.8	-3.0	-1.2	dB	
6000 Hz	-15.3	-12.3	-9.3	dB	

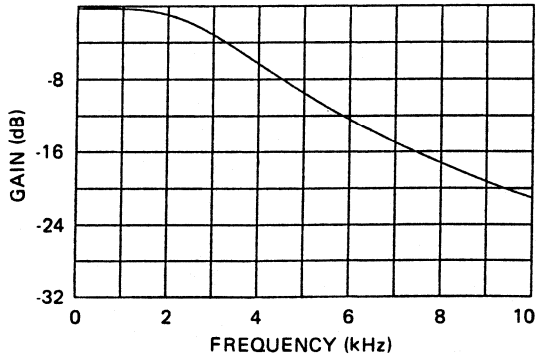

Figure 10. Amplitude Response: 3 kHz Low-pass Filter

FILTER CHARACTERISTICS
825 Hz Notch, see Figure 11

Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OS} Output Offset Voltage	-0.5	0	+0.5	V	V_{IN} = 0V
325 Hz	-1.5	0		dB	Vin = Vrms
570 Hz	-2.0	0		dB	
690 Hz	-4	0		dB	
827 Hz	-50	-70		dB	
855 Hz	-50	-70		dB	
000 Hz	-4	0		dB	
105 Hz	-2	0		dB	
360 Hz	-1.5	5	0	dB	

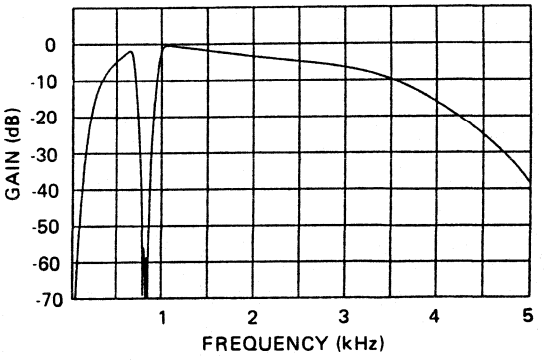

Figure 11. 825 Hz Notch and Psophmetric Filter

FILTER CHARACTERISTICS
1010 Hz Notch Filter, see Figure 12

Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OS} Output Offset Voltage	-0.5	0.1	0.5	VDC	V_{IN} = 0V
Input Frequency: f_o					
400 Hz	-1.5	0		dB	Vin = Vrms
529 Hz		0		dB	
700 Hz	-2.0	0		dB	
860 Hz	-4	-1		dB	
995 Hz	-50	-70		dB	
1010 Hz	-50	-70		dB	
1025 Hz	-50	-70		dB	
1180 Hz	-4.0	0		dB	
1330 Hz	-2.0	0		dB	
1700 Hz	-1.5	0		dB	

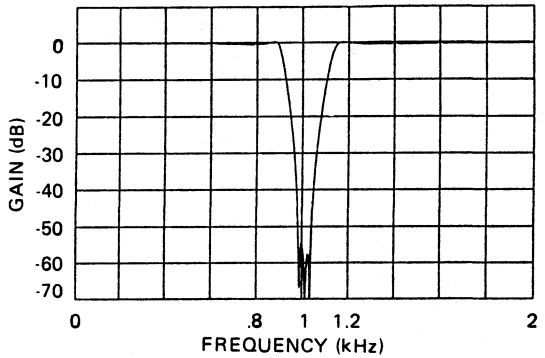

Figure 12. 1010 Hz Notch Amplitude Response

FILTER CHARACTERISTICS
50 kBPS Weighting Filter Low-Pass Filter Section, see Figure 13

Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OS} Output Offset Voltage	-0.5		+0.5	VDC	V_{IN} = 0V
Input Frequency: f_o					
50 Hz		0		dB	Vin = Vrms
200 Hz		0		dB	
400 Hz	-1	0	+1	dB	
1000 Hz	-0.2	0.0	+0.2	dB	
5000 Hz		0		dB	
10000 Hz	-1.8	-0.1	+0.2	dB	
15000 Hz	-4.8	-0.4	-1.2	dB	
20000 Hz		-1.0		dB	
25000 Hz	-3.1	-1.9	-1.1	dB	
30000 Hz	-4.6	-3.1	-1.6	dB	
35000 Hz		-4.7		dB	
40000 Hz		-7.9		dB	
45000 Hz		-14.0		dB	
55000 Hz			-29.0	dB	
Greater than 550000 Hz			-30.0	dB	

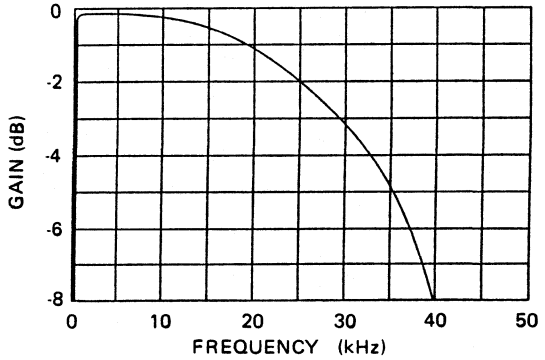

Figure 13. Amplitude Response: 50 kBPS Filter with 50 Hz High-pass Filter

FILTER CHARACTERISTICS

Peak-to-Average Ratio (P/AR) Band-pass Filter, see Figure 14

Receiver Response

Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OS} Output Offset Voltage	-0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency: f_o					
140 Hz		-50.5		db	Vin = Vrms
390 Hz	-34.5	-31.5	-28.5	dB	
640 Hz	-22.4	-20.4	-18.4	dB	
890 Hz	-12.63	-10.6	-8.63	dB	
1140 Hz		-2.1		dB	
1390 Hz	-1.6	-0.6	+0.4	dB	
1640 Hz		-5.5		dB	
1890 Hz	-12.5	-10.5	-8.5	dB	
2140 Hz		-14.5		dB	
2390 Hz		-17.7		dB	
2640 Hz	-22.4	-20.4	-18.4	dB	
2890 Hz		-22.7		dB	
3140 Hz		-24.6		dB	
3390 Hz		-26.4		dB	
3640 Hz		-27.9		dB	
3890 Hz	-33.3	-29.3	-26.3	dB	

Receiver Phase

Includes removal of an approximate ½ cycle (at 56 kHz) linear phase error (inherent in sample data devices) which can be subtracted out by normal system linear phase compensation networks.

Parameter	Min.	Typ.	Max.	Unit	Condition
Input Frequency: f_o					
140 Hz		173.77		degree	
390 Hz		161.2		degree	
640 Hz		143.6		degree	
890 Hz		114.0		degree	
1140 Hz		55.2		degree	
1390 Hz		-31.2		degree	
1640 Hz		-87.2		degree	
1890 Hz		-114.5		degree	
2140 Hz		-129.6		degree	
2390 Hz		-138.8		degree	
2640 Hz		-145.1		degree	
2890 Hz		-149.8		degree	
3140 Hz		-153.3		degree	
3390 Hz		-156.1		degree	

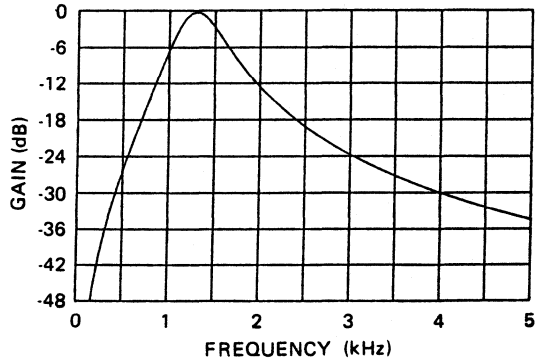

Figure 14. Amplitude Response: Peak-to-Average Ratio Band-pass Filter

FILTER CHARACTERISTICS
Program Weighting Filter, see Figure 15

Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OS} Output					
Offset Voltage	-0.5	0.1	+0.5	VDC	V_{IN} = 0V
Input Frequency: f_o					
100 Hz		-26.3		dB	Vin = Vrms
200 Hz	-19.3	-17.3	-15.3	dB	
300 Hz		-12.2		dB	
400 Hz		-9.0		dB	
500 Hz	-8.6	-6.6	-4.6	dB	
600 Hz		-4.7		dB	
700 Hz		-3.2		dB	
800 Hz		-2.0		dB	
900 Hz		-0.8		dB	
1000 Hz	-1.0		+1.0	dB	
1500 Hz	+2.2	+3.2	+4.2	dB	
2000 Hz	+3.5	+4.8	+5.5	dB	
2500 Hz		+5.6		dB	
3000 Hz		+6.0		dB	
4000 Hz		+6.5		dB	
5000 Hz	+3.5	+6.5	+9.5	dB	
6000 Hz		+6.4		dB	
7000 Hz		+5.8		dB	
8000 Hz	0.0	+4.0	+8.0	dB	
9000 Hz		+1.5		dB	
0000 Hz	-12.5	-8.5	-4.5	dB	

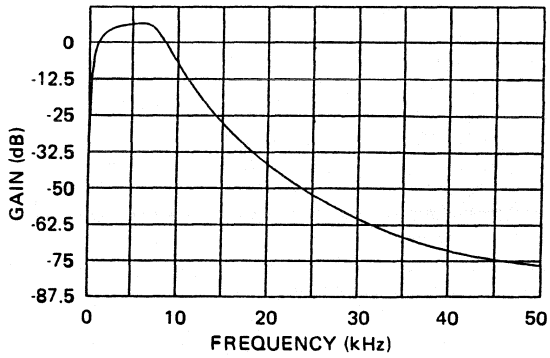

Figure 15. Amplitude Response: Program Weighting Filter

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FILTER CHARACTERISTICS
15 kHz Low-Pass Filter, see Figure 16

Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OS} Output					
Offset Voltage	-0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency: f_o					
30 Hz		0		dB	Vin = Vrms
60 Hz		0		dB	
400 Hz	-1	0	+1	dB	
000 Hz	-1	0	+1	dB	
000 Hz	-1.8	0.8	+0.2	dB	
000 Hz	-4.8	-3.0	-1.2	dB	
000 Hz	-15.3	-12.3	-9.3	dB	

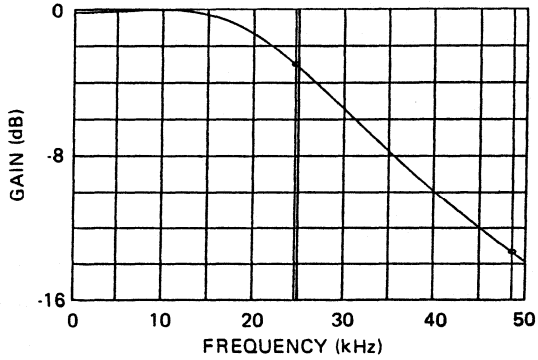


Figure 16. Amplitude Respone: 15 kHz Low-pass Filter

Graphic Equalizer Display Filter

GENERAL INFORMATION

The XR-1091 is an eight output switched-capacitor band pass filter dedicated for use in audio applications. Seven of the outputs are from band pass filters spaced 1 1/2 octaves apart starting at 63 Hz. The eighth output is peak of the seven outputs. All of the outputs provide a peak hold for use with most display circuits. The two inputs allows the left and right channels to be summed. This reduces the display space and prevents redundant information in the audio from being displayed.

The XR-1091 is available in 16 pin plastic packages. The XR-1091 is fabricated in 2 µm double polysilicon CMOS for lower noise and less clock feedthrough. The nominal operating voltages are +5VDC. The self contained oscillator is designed to operate at 800 kHz with an external resistor and capacitor.

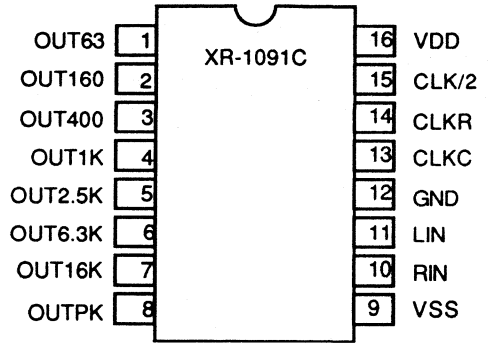
FEATURES

Internal R/C Oscillator
Provides seven filters in one 16 pin package
Dual Inputs for summing Left and Right Channels
Provides 30 dB of Gain
Low Noise CMOS
Electro-Static Discharge (ESD) Protection

APPLICATIONS

Graphic Equalizers
Tape Recorders
Receivers
Portable Systems

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

V_{DD}	7VDC
V_{SS}	-7VDC
Power Dissipations (**Package Limitation**)	
16 Pin Plastic Package	650 mW
derate above 25°C	5 mW/°C
Storage Temperature	-60°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-1091DCP	16 Pin Plastic DIP	0°C to 70°C

SYSTEM DESCRIPTION

The XR-1091 unlike most switched-capacitor filters does not require an external clock source in order to provide the sampling clocks. This frees the designer to place the XR-1091 in any application where an active filter design was in place. The XR-1091 provides bandpass filters with central frequency at 63 Hz, 160 Hz, 400 Hz, 1kHz, 2.5 kHz, 6.3 kHz, and 16 kHz. This frequencies are relative standards in the consumer audio market. The peak detector outputs referenced to 0V can be applied to a variety of display decoders.

The XR-1091 contains a continuous time anti-aliasing filter with a corner at 80kHz. This prevents most signals from affecting the filters performance. If two separate displays are desired, then two XR-1091 could be used, and the extra input is grounded.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = +6V, DC V_{SS} = -6V DC, T_A = 25°C, S1 open, S2, S3 to sgnal source, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
IDD5	Supply Current		14		mA	V_{DD} = 5V DC V_{SS} = -5V DC
IDD6	Supply Current		14.7	19.5	mA	
IIL	Input Leakage	-10		+10	µA	
TCLKRP (R-C)	Clock Freq	385	399.7	415	kHz	R = 1.46kΩ C = 1nF
TCLK2P (R-C)	Clock/2 Freq	185	199.4	215	kHz	R_L = 100K Ω CL = 100pF
ECLKR (A360)	External Clock Voltage	5			Vpp	$V_{CLK\ IN}$ = ± 2.5V pk
ECLK2 (A360)	Clock/2 External Source	190	200.2	210	kHz	R_L = 100K Ω CL = 100pF
VOS	Output Offset	0	125	200	mV	V_{IN} = 0V S2, S3 to ground
VOUT6KR	6.3kHz Output, RIN	3.33	3.95	4.7	V	V_{IN} = 125 mV pk f_{IN}=6.3 kHz
		28.5	30.0	31.5	dB	Calculated
		4.65	5.2	6	V	V_{IN} = 200 mVpk f_{IN} = 6.3 k Hz
VOUT63	63 Hz Output	3.33	3.95	4.7	V	V_{IN} = 125 mV pk f_{IN} = 63 Hz
		28.5	30.0	31.5	dB	Calculated
		4.65	5.2	6	V	V_{IN} = 200 mV pk f_{IN} = 63Hz
VOUT160	160 Hz Output	3.33	3.95	4.7	V	V_{IN} = 125 mV pk f_{IN} = 160Hz
		28.5	30.0	31.5	dB	Calculated
		4.65	5.2	6	V	V_{IN} = 200 mV pk f_{IN} = 160Kz
VOUT400	400 Hz Output	3.33	3.95	4.7	V	V_{IN} = 125 mV f_{IN} = 400Hz
		28.5	30.0	31.5	dB	Calculated
		4.65	5.2	6	V	V_{IN} = 200 mVpk f_{IN} = 400Hz
VOUT1K	1kHz Output	3.33	3.95	4.7	V	V_{IN} = 125 mVpk f_{IN} = 1kHz
		28.5	30.0	31.5	dB	Calculated
		4.65	5.2	6	V	V_{IN} = 200 mVpk f_{IN} = 1kHz
VOUT2K	2.5 kHz Output	3.33	3.95	4.7	V	V_{IN} = 125 mVpk f_{IN} = 2.5kHz
		28.5	30.0	31.5	dB	Calculated
		4.65	5.2	6	V	V_{IN} = 200 mVpk f_{IN} = 2.5kHz
VOUT6.3K	6.3 kHz Output	3.33	3.95	4.7	V	V_{IN} = 125 mVpk f_{IN} = 6.3kHz
		28.5	30.0	31.5	dB	Calculated
		4.65	5.2	6	V	V_{IN} = 200mVpk f_{IN} = 6.3kHz

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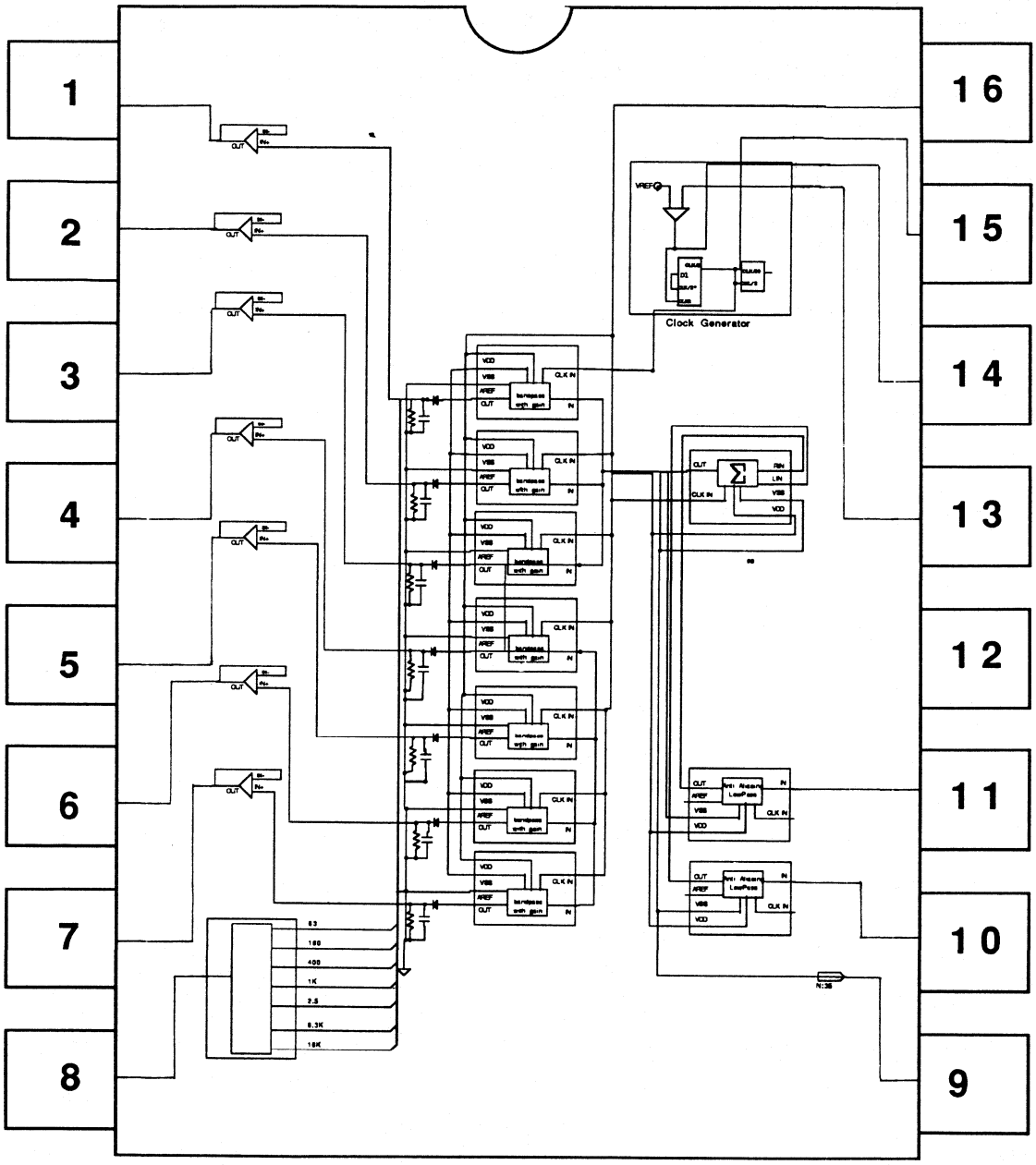


Figure 1. Functional Block Diagram

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
VOUT16K	16 KHz Output	3.33	3.75	4.7	V	V_{IN} = 125mVpk f_{IN} = 15.8kHz
		28.5	30.0	31.5	dB	Calculated
		4.4	5.2	6	V	V_{IN} = 200 mVpk f_{IN} = 15.8kHz
VOUT PK	PEAK OUT	3.33	3.95	4.7	V	V_{IN} = 125 mVpk f_{IN} = 1kHz
		28.5	30.0	31.5	dB	Calculated
		4.65	5.2	6	V	V_{IN} = 200mVpk f_{IN} = 1kHz

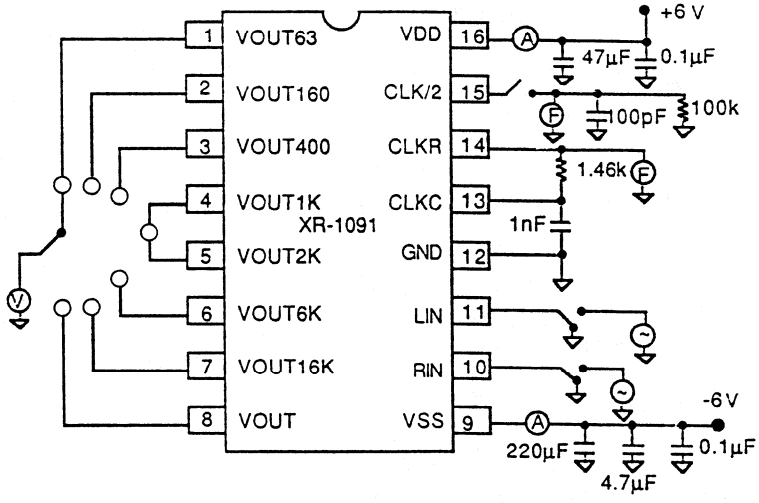


Figure 2. Test Circuit

PIN DESCRIPTION

Pin Number	MNEUMONIC	Description
1	OUT63	Peakheld output of the 63 Hz filter. This output can drive a 10 kΩ load.
2	OUT160	Peak held output of the 160 Hz band pass filter.
3	OUT400	Peak held output of the 400 Hz band pass filter.
4	OUT1k	Peak held output of the 1 kHz band pass filter.
5	OUT2.5k	Peak held output of the 2.5 kHz band pass filter.
6	OUT6.3k	Peak held output of the 6.3 kHz band pass filter.
7	OUT16k	Peak held output of the 16 kHz band pass filter.
8	OUTPK	Peak output of the above also peak held.
9	VSS	Nominally -6VDC. This should be decoupled with a 4.7 µF capacitor to ground. The capacitor should be physically close to pin 9.
10	RIN	Right Channel input. The input impedance of this pin is greater than 1×10^{12} ohms. Although protected, some care should be taken with respect to static electricity.
11	LIN	Left Channel Input: The input impedance of this pin is greater than 1×10^{12} ohms.
12	GND	Ground for both digital and analog of the XR-1090 and XR-1091.
13	CLKC	Clock Capacitor: The timing capacitor should be tied to this pin to ground.
14	CLKR	Clock resistor: The timing resistor would be tied from this pin to pin 13, CLKC.
15	CLK/2	This output is at 200 kHz in normal operation. The clock swings from VSS to VEE.
16	VDD	Nominally tied to +6VDC. This pin should be decoupled with a .47 µF capacitor to ground located as close as possible to this pin.

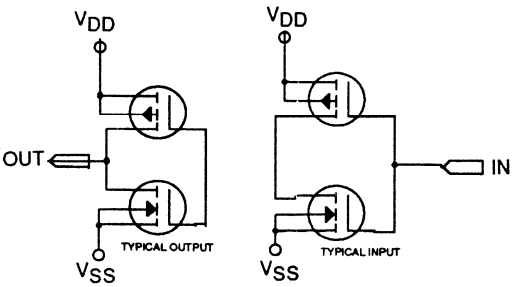


Figure 2. Input and Output Structure

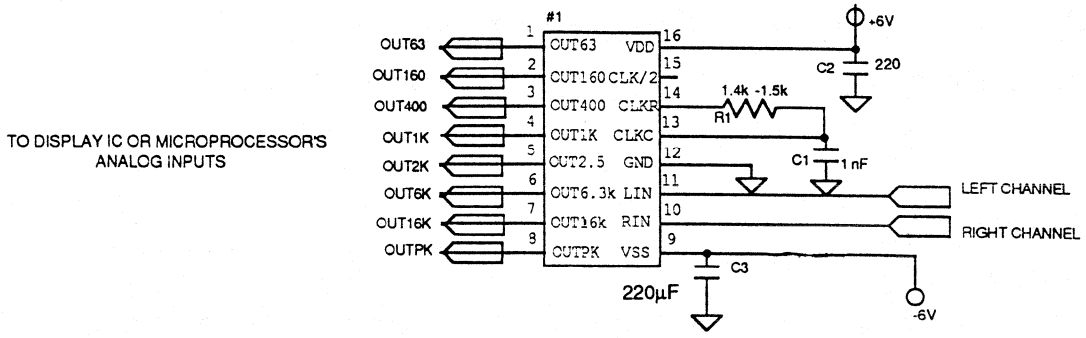


Figure 3. Typical Applications Circuit

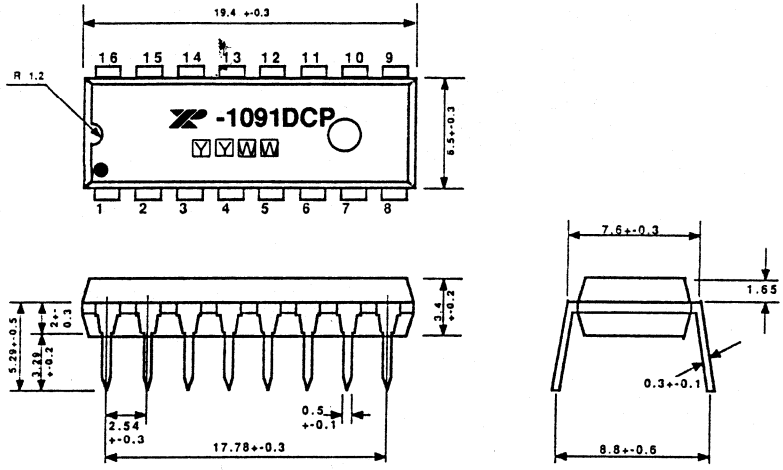


Figure 4. Physical Dimension - Plastic Package

Programmable Timer/Counter

GENERAL DESCRIPTION

The XR-2240 Programmable Timer/Counter is a monolithic controller capable of producing ultra-long time delays without sacrificing accuracy. In most applications, it provides a direct replacement for mechanical or electromechanical timing devices and generates programmable time delays from micro-seconds up to five days. Two timing circuits can be cascaded to generate time delays up to three years.

As shown in Figure 1, the circuit is comprised of an internal time-base oscillator, a programmable 8-bit counter and a control flip-flop. The time delay is set by an external R-C network and can be programmed to any value from 1 RC to 255 RC.

In astable operation, the circuit can generate 256 separate frequencies or pulse-patterns from a single RC setting and can be syncronized with external clock signals. Both the control inputs and the outputs are compatible with TTL and HCMOS logic levels.

FEATURES

Timing from micro-seconds to days
Programmable delays: 1RC to 255 RC
Wide supply range; 4V to 15V
TTL and DTL compatible outputs
High accuracy: 0.5%
External Sync and Modulation Capability
Excellent Supply Rejection: 0.2%/V

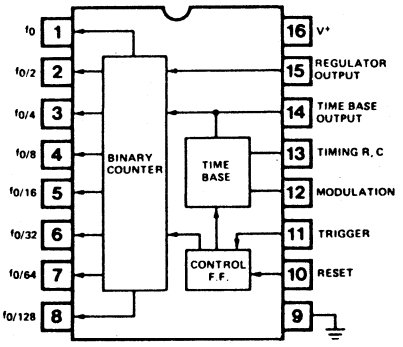
APPLICATIONS

Precision Timing	Frequency Synthesis
Long Delay Generation	Pulse Counting/Summing
Sequential Timing	A/D Conversion
Binary Pattern Generation	Digital Sample and Hold

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Power Dissipation	
Ceramic Package	750 mW
Derate above +25°C	6 mw/°C
Plastic Package	625 mW
Derate above +25°C	5 mW/°C
Storage Temperature	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2240M	Ceramic	−55°C to +125°C
XR-2240N	Ceramic	0°C to +70°C
XR-2240CN	Ceramic	0°C to +70°C
XR-2240P	Plastic	0°C to +70°C
XR-2240CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2240 is a combination timer/counter capable of generating accurate timing intervals ranging from microseconds through several days. The time base works as an astable multivibrator with a period equal to RC. The eight bit counter can divide the time base output by any integer value from 1 to 255. The wide supply voltage range of 4.5 to 15 V, TTL and HCMOS logic compatibility, and 0.5% accuracy allow wide applicability. The counter may operate independently of the time base. Counter outputs are open collector and may be wire or connected.

The circuit is triggered or reset with positive going pulses. By connecting the reset pin (Pin 10) to one of the counter outputs, the time base will halt at timeout. If none of the outputs are connected to the reset, the circuit will continue to operate in the astable mode. Activating the trigger terminal (Pin 11) while the timebase is stopped will set all counter outputs to the low state and start the timebase.

ELECTRICAL CHARACTERISTICS

Test Conditions: See Figure 2, $V^+ = 5V$, $T_A = 25°C$, $R = 10\ k\Omega$, $C = 0.1\ \mu F$, unless otherwise noted.

PARAMETERS	XR-2240 MIN	XR-2240 TYP	XR-2240 MAX	XR-2240C MIN	XR-2240C TYP	XR-2240C MAX	UNIT	CONDITIONS
GENERAL CHARACTERISTICS								
Supply Voltage	4		15	4		15	V	For $V^+ < 4.5V$, Short Pin 15 to Pin 16
Supply Current								
Total Circuit		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
		12	16		13	18	mA	$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
Counter Only		1			1.5		mA	See Figure 3
Regulator Output, V_R	4.1	4.4		3.9	4.4		V	Measured at Pin 15, $V^+ = 5V$
	6.0	6.3	6.6	5.8	6.3	6.8	V	$V^+ = 15V$, See Figure 4
TIME BASE SECTION								See Figure 2
Timing Accuracy*		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ $0°C \le T \le 75°C$
		80			80		ppm/°C	$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \ge 8$ Volts, See Figure 11
Max. Frequency	100	130			130		kHz	$R = 1\ k\Omega$, $C = 0.007\ \mu F$
Modulation Voltage Level								Measured at Pin 12
	3.00	3.50	4.0	2.80	3.50	4.20	V	V^+ 5V
		10.5			10.5		V	$V^+ = 15V$
TRIGGER/RESET CONTROLS								
Trigger								Measures at Pin 11, $V_{RS} = 0$
Trigger Threshold		1.4	2.0		1.4	2.0	V	
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time**		1			1		μsec.	
Reset								
Reset Threshold		1.4	2.0		1.4	2.0	V	
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time**		0.8			0.8		μsec.	
COUNTER SECTION								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.8	1.5			1.5		MHz	$V_{RS} = 0$, $V_{TR} = 5V$ Measured at Pin 14
Input:								
Impedance		20			20		kΩ	
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 1 thru 8
Rise Time		180			180		nsec.	$R_L = 3k$, $C_L = 10\ pF$
Fall Time		180			180		nsec.	
Sink Current	3	5		2	4		mA	$V_{OL} \le 0.4V$
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} = 15V$

*Timing error solely introduced by XR-2240, measured as % of ideal time-base period of T = 1.00 RC.
**Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at pin 1.

Recommended Range of Timing Components								See Figure 8
Timing Resistor, R	0.001		10	0.001		10	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	

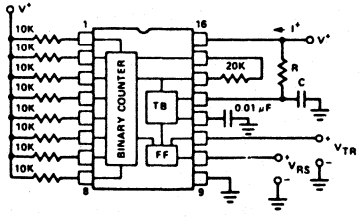


Figure 2. Generalized Test Circuit

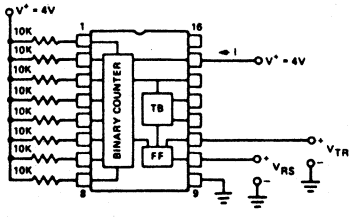


Figure 3. Test Circuit for Low-Power Operation (Time-Base Powered Down)

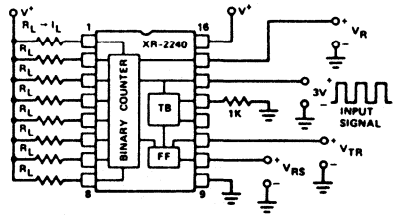


Figure 4. Test Circuit for Counter Section

PRINCIPLES OF OPERATION

The timing cycle for the XR-2240 is initiated by applying a positive-going trigger pulse to pin 11. The trigger input actuates the time-base oscillator, enables the counter section, and sets all the counter outputs to "low" state. The time-base oscillator generates timing pulses with its period, T, equal to 1 RC. These clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to pin 10.

Figure 5 gives the timing sequence of output waveforms at various circuit terminals, subsequent to a trigger input. When the circuit is at reset state, both the time-base and the counter sections are disabled and all the counter outputs are at "high" state.

In most timing applications, one or more of the counter outputs are connected back to the reset terminal, as shown in Figure 6, with S_1 closed. In this manner, the circuit will start timing when a trigger is applied and will automatically reset itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the reset terminal (switch S_1 open), the circuit would operate in its astable or free-running mode, subsequent to a trigger input.

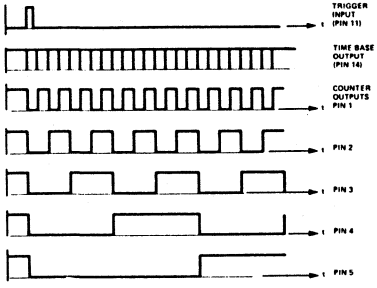


Figure 5. Timing Diagram of Output Waveforms

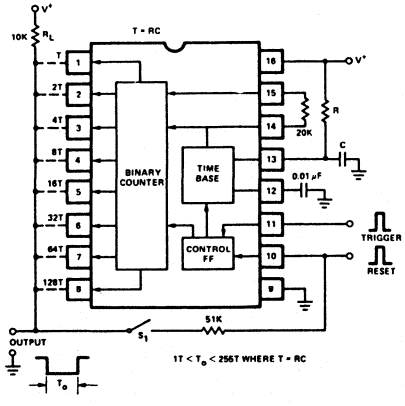


Figure 6. Generalized Circuit Connection for Timing Applications (Switch S_1 Open for Astable Operations, Closed for Monostable Operations)

PROGRAMMING CAPABILITY

The binary counter outputs (pins 1 through 8) are open-collector type stages and can be shorted together to a common pull-up resistor to form a "wired-or" connection. The combined output will be "low" as long as any one of the outputs is low. In this manner, the time delays associated with each counter output can be *summed* by simply shorting them together to a common output bus as shown in Figure 6. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, would be 32T. Similarly, if pins 1, 5, and 6 were shorted to the output bus, the total time delay would be $T_O = (1 + 16 + 32)\ T = 49T$. In this manner, by proper choice of counter terminals connected to the output bus, one can program the timing cycle to be: $1T \leq T_O \leq 255T$, where $T = RC$.

TRIGGER AND RESET CONDITIONS

When power is applied to the XR-2240 with no trigger or reset inputs, the circuit reverts to "reset" state. Once triggered, the circuit is immune to additional trigger inputs, until the timing cycle is completed or a reset input is applied. If both the reset and the trigger controls are activated simultaneously trigger overrides reset.

DESCRIPTION OF CIRCUIT CONTROLS

COUNTER OUTPUTS (PINS 1 THROUGH 8)

The binary counter outputs are buffered "open-collector" type stages, as shown in Figure 15. Each output is capable of sinking ≈ 5 mA of load current. At reset condition, all the counter outputs are at high or non-conducting state. Subsequent to a trigger input, the outputs change state in accordance with the timing diagram of Figure 5.

The counter outputs can be used individually, or can be connected together in a "wired-or" configuration, as described in the Programming section.

RESET AND TRIGGER INPUTS (PINS 10 AND 11)

The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11. The threshold level for these controls is approximately two diode drops (≈1.4V) above ground.

Minimum pulse widths for reset and trigger inputs are shown in Figure 10. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle. Figure 12 should be referenced for time between reset and trigger.

MODULATION AND SYNC INPUT (PIN 12)

The period T of the time-base oscillator can be modulated by applying a dc voltage to this terminal (see Figure 13). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to pin 12, as shown in Figure 16. Recommended sync pulse widths and amplitudes are also given in the figure.

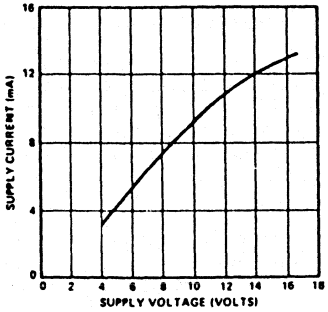


Figure 7. Supply Current vs. Supply Voltage in Reset Condition (Supply Current Under Trigger Condition is ≈0.7 mA less)

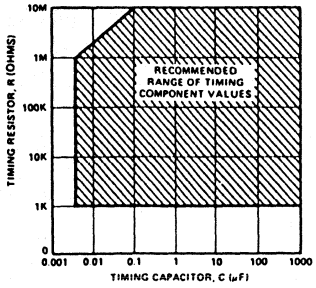


Figure 8. Recommended Range of Timing Component Values.

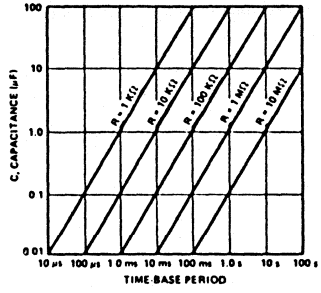


Figure 9. Time-Base Period, T, as a Function of External RC

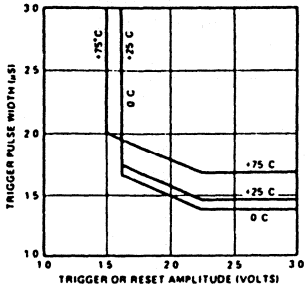


Figure 10. Minimum Trigger and Reset Pulse Widths at Pins 10 and 11

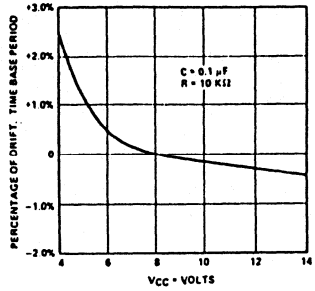


Figure 11. Power Supply Drift

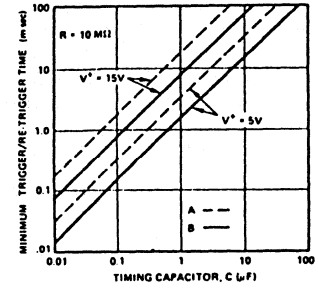


Figure 12.
A) Minimum Trigger Delay Time Subsequent to Application of Power
B) Minimum Re-trigger Time, Subsequent to a Reset Input

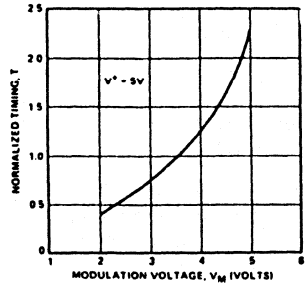
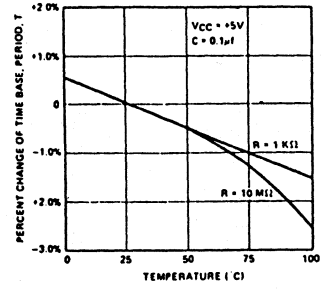


Figure 13. Normalized Change in Time-Base Period As a Function of Modulation Voltage at Pin 12



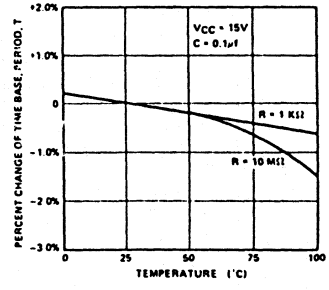


Figure 14. Temperature Drift of Time-Base Period, T

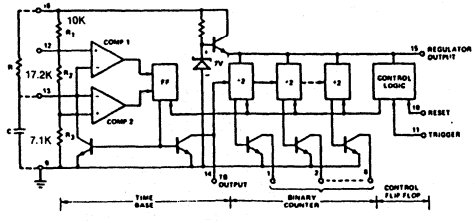


Figure 15. Simplified Circuit Diagram of XR-2240

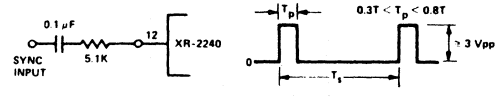


Figure 16. Operation with External Sync Signal.
(a) Circuit for Sync Input
(b) Recommended Sync Waveform

HARMONIC SYNCHRONIZATION

Time-base can be synchronized with *integer multiples or harmonics* of input sync frequency, by setting the time-base period, T, to be an integer multiple of the sync pulse period, T_S. This can be done by choosing the timing components R and C at pin 13 such that:

$$T = RC = (T_S/m) \text{ where}$$

$$m \text{ is an integer, } 1 \leq m \leq 10.$$

Figure 17 gives the typical pull-in range for harmonic synchronization, for various values of harmonic modulus, m. For $m < 10$, typical pull-in range is greater than ±4% of time-base frequency.

TIMING TERMINAL (PIN 13)

The time-base period T is determined by the external R-C network connected to this pin. When the time-base is triggered, the waveform at pin 13 is an exponential ramp with a period T = 1.0 RC. A 1KΩ resistor to ground should be placed on this pin to disable the timebase.

TIME-BASE OUTPUT (PIN 14)

Time-Base output is an open-collector type stage, as shown in Figure 15 and requires a 20 KΩ pull-up resistor to Pin 15 for proper operation of the circuit. At reset state, the time-base output is at "high" state. Subsequent to triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of Figure 5.

Time-base output is internally connected to the binary counter section and also serves as the input for the external clock signal when the circuit is operated with an external time-base.

The counter input triggers on the negative-going edge of the timing or clock pulses applied to pin 14. The trigger threshold for the counter section is ≈ +1.5 volts. The counter section can be disabled by clamping the voltage level at pin 14 to ground.
Note:
Under certain operating conditions such as high supply voltages ($V^+ > 7V$) and small values of timing capacitor ($C < 0.1\ \mu F$) the pulse-width of the time-base output at pin 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 620 pF capacitor from pin 14 to ground.

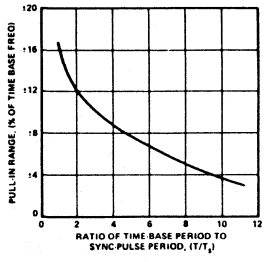


Figure 17. Typical Pull-In Range for Harmonic Synchronization

REGULATOR OUTPUT (PIN 15)

This terminal can serve as a V^+ supply to additional XR-2240 circuits when several timer circuits are cascaded (See Figure 20), to minimize power dissipation. For circuit operation with external clock, pin 15 can be used as the V^+ terminal to power-down the internal time-base and reduce power dissipation. The output current shall not exceed 10 mA.

When the internal time-base is used with $V^+ \leq 4.5V$, pin 15 should be short to pin 16. For wide temperature appllication and if V+ = 5 VDC pin 15 should be tied to pin 16.

APPLICATIONS INFORMATION

PRECISION TIMING (Monostable Operation)

In precision timing applications, the XR-2240 is used in its monostable or "self-resetting" mode. The generalized circuit connection for this application is shown in Figure 18.

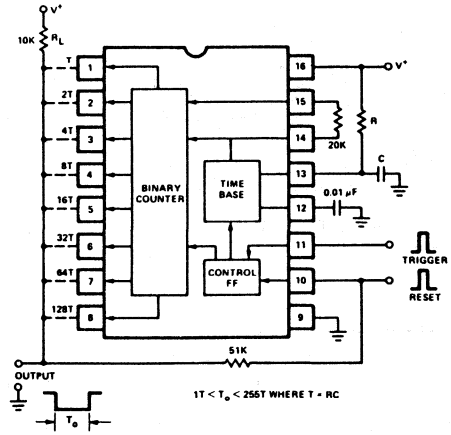


Figure 18. Circuit for Monostable Operation (T_0 = NRC where $1 \leq N \leq 255$)

The output is normally "high" and goes to "low" subsequent to a trigger input. It stays low for the time duration T_0 and then returns to the high state. The duration of the timing cycle T_0 is given as:

$$T_0 = NT = NRC$$

where T = RC is the time-base period as set by the choice of timing components at pin 13 (See Figure 9). N is an integer in the range of:

$$1 \leq N \leq 255$$

as determined by the combination of counter outputs (pins 1 through 8) connected to the output bus, as described below.

PROGRAMMING OF COUNTER OUTPUTS: The binary counter outputs (pins 1 through 8) are open-collector type stages and can be shorted together to a common pull-up resistor to form a "wired-or" connection where

the combined output will be "low" as long as any one of the outputs is low. In this manner, the time delays associated with each counter output can be summed by simply shorting them together to a common output bus as shown in Figure 18. For example if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, would be 32T. Similarly, if pins 1, 5, and 6 were shorted to the output bus, the total time delay would be $T_O = (1+16+32)\,T = 49T$. In this manner, by proper choice of counter terminals connected to the output bus, one can program the timing cycle to be: $1T \leq T_O \leq 255T$.

ULTRA-LONG DELAY GENERATION

Two XR-2240 units can be cascaded as shown in Figure 19 to generate extremely long time delays. In this application, the reset and the trigger terminals of both units are tied together and the time base of Unit 2 disabled. In this manner, the output would normally be high when the system is at reset. Upon application of a trigger input, the output would go to a low stage and stay that way for a total of $(265)^2$ or 65,536 cycles of the time-base oscillator.

PROGRAMMING: Total timing cycle of two cascaded units can be programmed from $T_O = 256RC$ to $T_O = 65{,}536RC$ in 256 discrete steps by selectively shorting any one or the combination of the counter outputs from Unit 2 to the output bus.

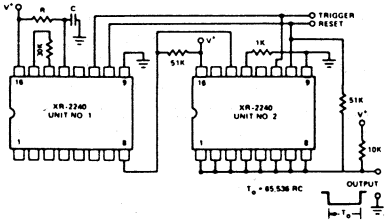


Figure 19. Cascaded Operation for Long Delay Generation

LOW-POWER OPERATION

In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption, by using the circuit connection of Figure 20. In this case, the V^+ terminal (pin 16) of Unit 2 is left open-circuited, and the second unit is powered from the regulator output of Unit 1, by connecting pin 15 of both units.

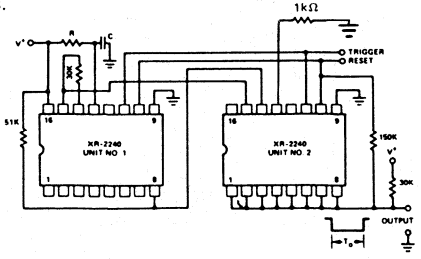


Figure 20. Low-Power Operation of Cascaded Timers

ASTABLE OPERATION

The XR-2240 can be operated in its astable or free-running mode by disconnecting the reset terminal (pin 10) from the counter outputs. Two typical circuit connections for this mode of operation are shown in Figure 21. In the circuit connection of Figure 21(a), the circuit operates in its free-running mode, with external trigger and reset signals. It will start counting and timing subsequent to a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 10, the circuit reverts back to its rest state. The circuit of Figure 21(a) is essentially the same as that of Figure 6, with the feedback switch S_1 open.

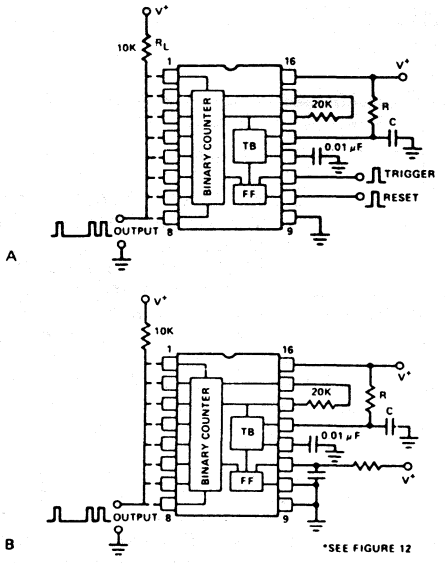


Figure 21. Circuit Connections for Astable Operation
(a) Operation with External Trigger and Reset Controls
(b) Free-running or Continuous Operation

The circuit of Figure 21(b) is designed for continuous operation. The circuit self-triggers automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely.

In astable or free-running operation, each of the counter outputs can be used individually as synchronized oscillators; or they can be interconnected to generate complex pulse patterns.

BINARY PATTERN GENERATION

In astable operation, as shown in Figure 21, the output of the XR-2240 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 5 which shows the phase relations between the counter outputs. Figure 22 shows some of these complex pulse patterns. The pulse pattern repeats itself at a rate equal to the period of the *highest* counter bit connected

to the common output bus. The minimum pulse width contained in the pulse train is determined by the *lowest* counter bit connected to the output.

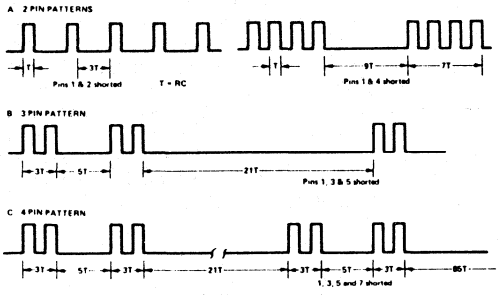


Figure 22. Binary Pulse Patterns Obtained by Shorting Various Counter Outputs

OPERATION WITH EXTERNAL CLOCK

The XR-2240 can be operated with an external clock or time-base, by disabling the internal time-base oscillator and applying the external clock input to pin 14. The recommended circuit connection for this application is shown in Figure 23. The internal time-base can be deactivated by connecting a 1 KΩ resistor from pin 13 to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 volts is required. Minimum external clock pulse width must be ≥ 1 µS. The external clock must have a duty cycle of 50% or more.

For operation with supply voltages of 6V or less, the internal time-base section can be powered down by open-circuiting pin 16 and connecting pin 15 to V+. In this configuration, the internal time-base does not draw any current, and the over-all current drain is reduced by ≈ 3 mA. The pulse width of the trigger must be at least 60% of the period of the external clock for reliable operation.

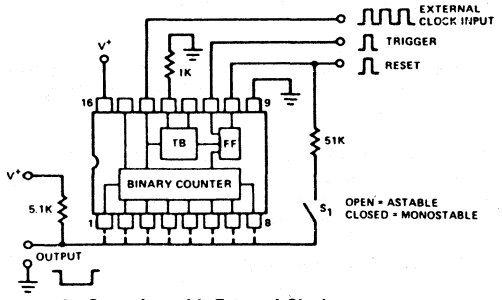


Figure 23. Operation with External Clock

FREQUENCY SYNTHESIZER

The programmable counter section of XR-2240 can be used to generate 255 discrete frequencies from a given time base setting using the circuit connection of Figure 24. The output of the circuit is a positive pulse train with a pulse width equal to T, and a period equal to (N + 1) T where N is the programmed count in the counter.

The modulus N is the *total count* corresponding to the counter outputs connected to the output bus. Thus, for example, if pins 1, 3 and 4 are connected together to the output bus, the total count is: N = 1 + 4 + 8 = 13; and the period of the output waveform is equal to (N + 1) T or 14T. In this manner, 256 different frequencies can be synthesized from a given time-base setting.

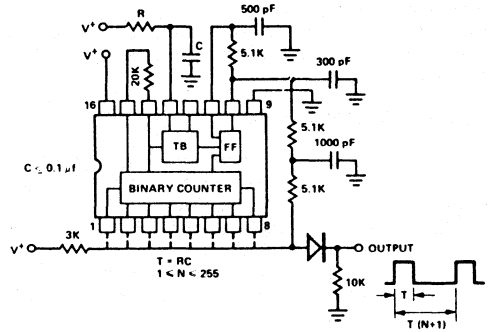


Figure 24. Frequency Synthesis from Internal Time-Base

SYNTHESIS WITH HARMONIC LOCKING: The harmonic synchronization property of the XR-2240 time-base can be used to generate a wide number of discrete frequencies from a given input reference frequency. The circuit connection for this application is shown in Figure 25. (See Figures 16 and 17 for external sync waveform and harmonic capture range.) If the time base is synchronized to $(m)^{th}$ harmonic of input frequency where $1 \leq m \leq 10$, as described in the section on "Harmonic Synchronization", the frequency f_O of the output waveform in Figure 25 is related to the input reference frequency f_R as:

$$f_O = f_R \frac{m}{(N + 1)}$$

where m is the harmonic number, and N is the programmed counter modulus. For a range of $1 \leq N \leq 255$, the circuit of Figure 25 can produce 1500 separate frequencies from a single fixed reference.

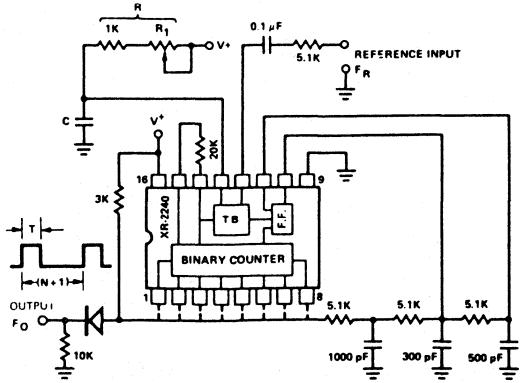


Figure 25. Frequency Synthesis by harmonic Locking to an External Reference

One particular application of the circuit of Figure 25 is generating frequencies which are not harmonically related to a reference input. For example, by choosing the external R-C to set m = 10 and setting N = 5, one can obtain a 100 Hz output frequency synchronized to 60 Hz power line frequency.

STAIRCASE GENERATOR

The XR-2240 Timer/Counter can be interconnected with an external operational amplifier and a precision resistor ladder to form a staircase generator, as shown in Figure 26. Under reset condition, the output is low. When a trigger is applied, the op. amp. output goes to a high state and generates a negative going staircase of 256 equal steps. The time duration of each step is equal to the time-base period T. The staircase can be stopped at any desired level by applying a "disable" signal to pin 14, through a steering diode, as shown in Figure 26. The count is stopped when pin 14 is clamped at a voltage level less than 1.4V.

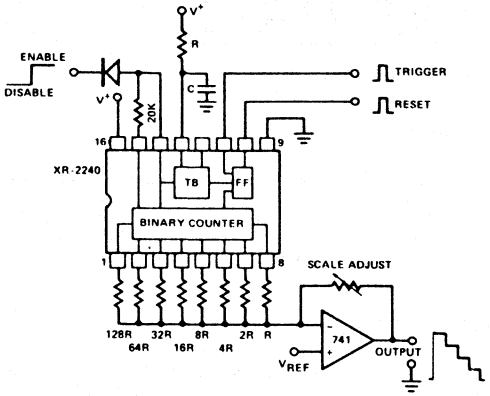


Figure 26. Staircase Generator

DIGITAL SAMPLE/HOLD

Figure 27 shows a digital sample and hold circuit using the XR-2240. The principle of operation of the circuit is similar to the staircase generator described in the previous section. When a "strobe" input is applied, the RC low-pass network between the reset and the trigger inputs of XR-2240 causes the timer to be first reset and then triggered by the same strobe input. This strobe input also sets the output of the bistable latch to a high state and activates the counter.

The circuit generates a staircase voltage at the output of the op. amp. When the level of the staircase reaches that of the analog input to be sampled, comparator changes state, activates the bistable latch and stops the count. At this point, the voltage level at the op. amp. output corresponds to the sampled analog input. Once the input is sampled, it will be held until the next strobe signal. Minimum re-cycle time of the system is ≈6 msec.

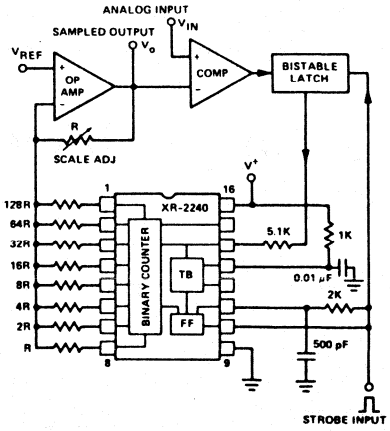


Figure 27. Digital Sample and Hold Circuit

ANALOG-TO-DIGITAL CONVERTER

Figure 28 shows a simple 8-bit A/D converter system using the XR-2240. The operation of the circuit is very similar to that described in connection with the digital sample/hold system of Figure 15. In the case of A/D conversion, the digital output is obtained in parallel format from the binary counter outputs, with the output at pin 8 corresponding to the most significant bit (MSB). The re-cycle time of the A/D converter is ≈6 msec.

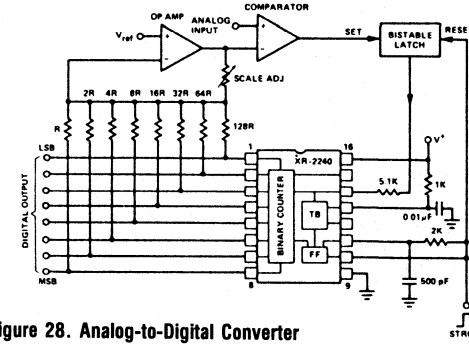
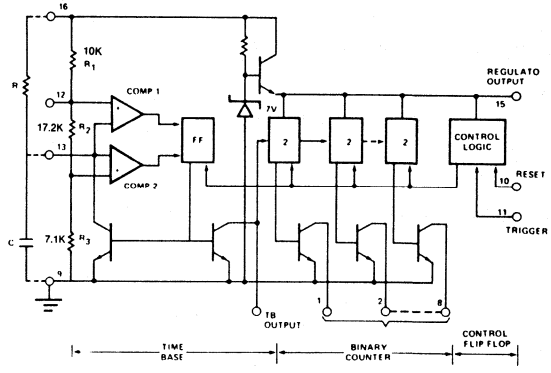


Figure 28. Analog-to-Digital Converter



EQUIVALENT SCHEMATIC DIAGRAM

Long Range Timer

GENERAL DESCRIPTION

The XR-2242 is a monolithic timer/controller capable of producing ultra-long time delays from milliseconds to days. Two timing circuits can be cascaded to generate time delays or timing intervals up to one year. The circuit is comprised of an internal time-base oscillator, an 8 bit binary counter and a control flip-flop. For a given external R-C network connected to the timing terminal, the circuit produces an output timing pulse of 128 RC. If two circuits are cascaded, a total time delay of $(128)^2$ or 16,384 RC is obtained.

Three output pins are provided on the device: the time base (RC) on Pin 8, 2 RC on Pin 2, and the counter output (128 RC) on Pin 3.

FEATURES

Timing from micro-seconds to days
Wide supply range: 4.5V to 15V
TTL and HCMOS compatible outputs
High accuracy: 0.5%
Excellent Supply Rejection: 0.2%/V
Monostable and Astable Operation

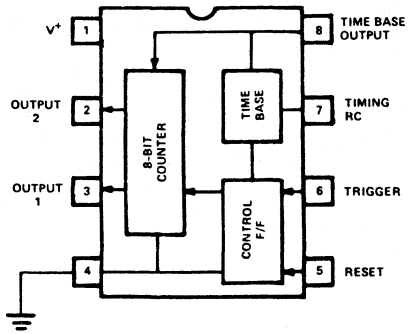
APPLICATIONS

Long Delay Generation
Sequential Timing
Precision Timing
Ultra-Low Frequency Oscillator

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate above +25°C	2.5 mW/°C
Storage Temperature Range	−65° to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2242M	Ceramic	−55°C to +125°C
XR-2242CN	Ceramic	0°C to +70°C
XR-2242CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The timing cycle for the XR-2242 is initiated by applying a positive-going trigger pulse to Pin 6. The trigger input actuates the time-base oscillator, enables the counter section, and sets the output to "low" state. The time-base oscillator generates timing pulses with its period, T, equal to 1 RC. These clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to Pin 5.

In monostable timer applications the output terminal (Pin 3) is connected back to the reset terminal. In this manner, after 128 clock pulses are applied to the circuit, this output goes to "high" state and resets the circuit thus completing the timing cycle. Thus, subsequent to triggering, the output at Pin 3 will produce a total timing pulse of 128 RC before the circuit resets itself to complete the timing cycle. During the timing interval, the secondary output at Pin 2 produces a square-wave output with the period of 2 RC.

If the output at Pin 3 is not connected back to the reset terminal, the circuit continues to operate in an astable mode, subsequent to a trigger input.

ELECTRICAL CHARACTERISTICS

Test Conditions: See Figure 3, $V^+ = 5V$, $T_A = 25°C$, $R = 10\ k\Omega$, $C = 0.1\ \mu F$, unless otherwise noted.

PARAMETERS	XR-2242M MIN	XR-2242M TYP	XR-2242M MAX	XR-2242C MIN	XR-2242C TYP	XR-2242C MAX	UNIT	CONDITIONS
GENERAL CHARACTERISTICS								
Supply Voltage	4		15	4		15	V	
Supply Current		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
Total Circuit		12	16		13	18	mA	$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
TIME BASE SECTION								See Figure 3
Timing Accuracy*		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ 0°C ≤ T ≤ 70°C
		80			80		ppm/°C	$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \geq 8$ Volts
Max Frequency	100	130			130		kHz	$R = 1\ k\Omega$, $C = C = 0.007\ \mu F$
Recommended Range of Timing Components								See Figure 5
Timing Resistor, R	0.001		10	0.001		5	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	Low-Leakage Capacitor Required.
TRIGGER/RESET CONTROLS								
Trigger								Measured at Pin 6, $V_{RS} = 0$
Trigger Threshold		1.4	2.0		1.4	2.0	V	
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time**		1			1		μsec.	
Reset								Measured at Pin 5, $V_{TR} = 0$
Reset Threshold		1.4	2.0		1.4	2.0	V	
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time**		0.8			0.8		μsec.	
COUNTER								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.5	1.0			1.0		MHz	$V_{RS} = 0$, $V_{TR} = 5V$
Input:								
Impedance		20			20		kΩ	
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 2 and 3
Rise Time		180			180		nsec.	$R_L = 3K\Omega$, $C_L = 10$ pF
Fall Time		180			180		nsec.	
Sink Current	3	5		2	4		mA	$V_{OL} \leq 0.4V$
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} \leq 15V$

*Timing error solely introduced by XR-2242, measured as % of ideal time-base period of T = 1.00 RC.

**Propagation delay from application of trigger (or reset) input to corresponding state change in first stage counter output at pin 2.

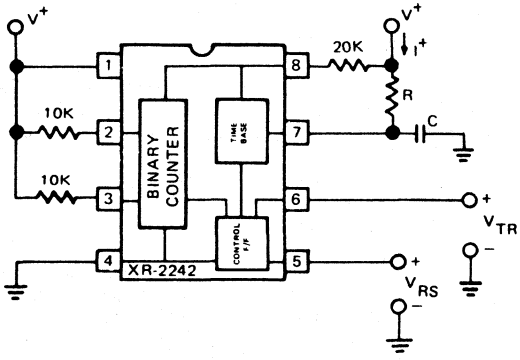


Figure 3. Generalized Test Circuit

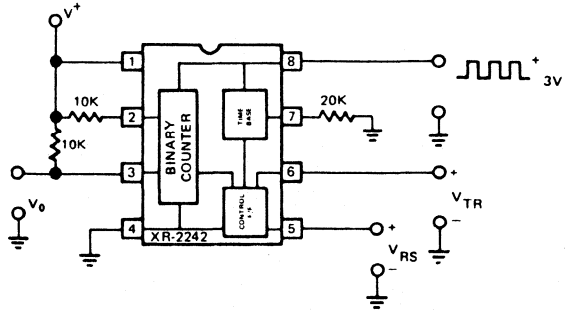


Figure 4. Test Circuit for Counter Section

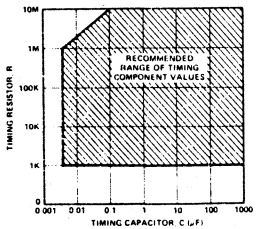


Figure 5. Recommended Range of Timing Component Values

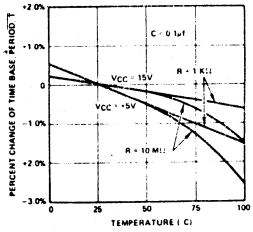


Figure 6. Temperature Drift of Time-Base Period, T

DESCRIPTION OF CIRCUIT CONTROLS

COUNTER OUTPUTS (PINS 2 AND 3)

The binary counter outputs are buffered "open-collector" type stages. Each output is capable of sinking ≈ 5 mA of load current. At reset condition, all the counter outputs are at high or non-conducting state. Subsequent to a trigger input, the outputs change state in accordance with the timing diagram of Figure 7.

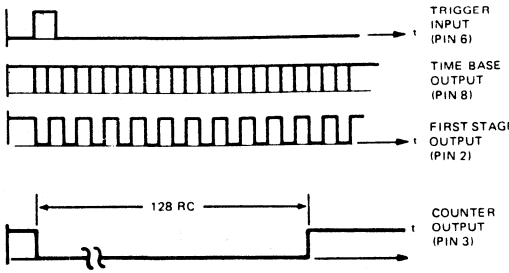


Figure 7. Timing Diagram of Output Waveforms

Basic circuit connection for timing applications is shown in Figure 8. Subsequent to a positive trigger pulse applied to pin 6, the timing output at pin 3 goes to a "low" state and will stay low for a total time duration T_0 = 128 RC, where R and C are the timing components connected to pin 7. If the switch S_1 is *open,* then the output at pin 3 would alternately change state every T_0 interval of time, and the circuit would operate in its "astable" mode. If the switch S_1 is *closed,* the circuit will reset itself and complete its timing cycle after a time interval of T_0, when the output at pin 3 goes to a "high" state. This corresponds to the "monostable" mode of operation.

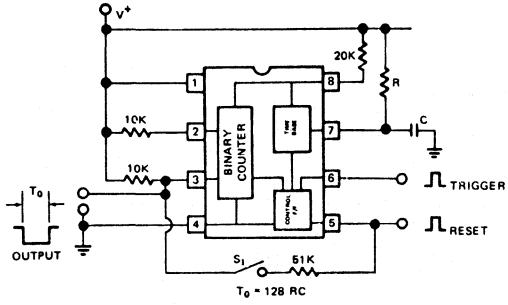


Figure 8. Circuit Connection for Timing Applications (Switch S_1 Open for Astable Operations, Closed for Monostable Operations)

RESET AND TRIGGER INPUTS (PINS 5 AND 6)

The circuit is reset or triggered with positive-going control pulses applied to pins 5 and 6. The threshold level for these controls is approximately two diode drops (≈ 1.4V) above ground.

Minimum pulse widths for reset and trigger inputs, minimum trigger delay time and minimum re-trigger delay time are shown in Figures 9 and 10. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Note: In noisy operating environment, 0.01 μF capacitors to ground are recommended from reset and trigger terminals.

When power is applied with no trigger or reset inputs, the circuit reverts to "reset" state. Once triggered, the circuit is immune to additional trigger inputs, until the timing cycle is completed or a reset input is applied. If both the reset and the trigger controls are activated simultaneously, trigger overrides reset.

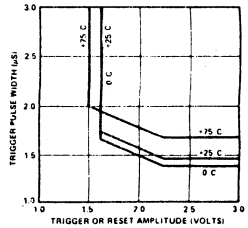


Figure 9. Minimum Trigger and Reset Pulse Widths at Pins 5 and 6

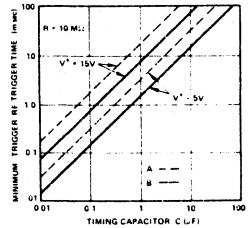


Figure 10. Trigger and Retrigger Delay Time

(A) Minimum Trigger Delay Time Subsequent to Application of Power

(B) Minimum Re-trigger Time, Subsequent to a Reset Input

TIMING TERMINAL (PIN 7)

The time-base period T is determined by the external R-C network connected to this pin. When the time-base is triggered, the waveform at pin 7 is an exponential ramp with a period T = 1.0 RC. A 1KΩ resistor to ground should be tied to this pin disable the time base.

TIME-BASE OUTPUT (PIN 8)

Time-base output is an open-collector type stage, as shown in Figure 1 and requires a 20 KΩ pull-up resistor to Pin 1 (V^+) for proper operation of the circuit. At reset state, the time-base output is at "high" stage. Subsequent to triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of Figure 7.

ASTABLE OPERATION

The XR-2242 can be operated in its astable or free-running mode by disconnecting the reset terminal (pin 5) from the counter output (pin 3). Two typical circuit connections for this mode of operation are shown in Figures 11 and 12. In the circuit connection of Figure 11, the circuit operates in its free-running mode, with external trigger and reset signals. It will start counting and timing subsequent to a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 5, the circuit reverts back to its rest state. The circuit of Figure 11 is essentially the same as that of Figure 8, with the feedback switch S_1 open.

The circuit of Figure 12 is designed for continuous operation. The circuit self-triggering automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely.

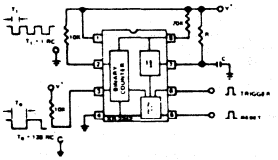


Figure 11. Astable Operation with External Trigger and Reset Controls

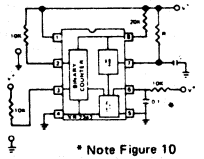


Figure 12. Free-running Operation Self-Triggered When Power Supply is Turned On

OPERATION WITH EXTERNAL CLOCK

The XR-2242 can be operated with an external clock or time-base, by disabling the internal time-base oscillator and applying the external clock input to pin 8. The internal time-base can be de-activated by connecting a 1 KΩ resistor from pin 7 to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 volts is required. Minimum external clock pulse width must be ≥ 1 μS.

CASCADED OPERATION:

a) Ultra-Long Delay Generation:

Ultra-long time delays, up to one-year duration, can be generated by cascading two XR-2242 timers as shown in Figure 13. In this configuration, the counter section of Unit 2 is cascaded with the counter output of Unit 1, to provide a total count of 32,640 clock cycles before the output (pin 3 of Unit 2) changes state. In the application circuit of Figure 13, the output (pin 3) of Unit 1 is directly connected to the time-base output (pin 8) of Unit 2, through a common pull-up resistor. In this manner, the counter section of Unit 2 is triggered every time the output of Unit 1 makes a *positive-going* transition. The time-base section of Unit 2 is disabled by connection pin 7 of Unit 2 to ground through a 1 KΩ resistor. The reset and trigger terminals of both units are connected together for common controls. If an additional XR-2242 were cascaded with Unit 2 of Figure 13, the total available time delay can be extended to (1.065) (10^9) RC. With an external RC = 0.1 sec, this would correspond to a time delay of 3.4 years.

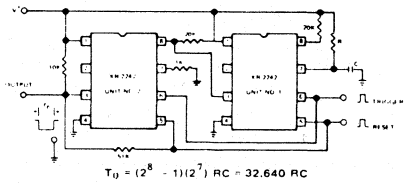


Figure 13. Cascaded Operation of Two XR-2242 Timer Circuits

b) Sequential Timing:

Two XR-2242 timers can be cascaded to produce sequential or delayed-timing pulses as shown in Figure 14. In this configuration, the second timer is triggered by the first timer, subsequent to the completion of its timing cycle. Thus, the triggering of Unit 2 is delayed by a time interval, T_1 (= 128 R_1C_1) corresponding to the timing cycle of Unit 1.

The output of Unit 2, which is normally at "high" state will stay high for a duration of T_1 = 128 R_1C_1, subsequent to the application of a trigger pulse; then go to a low state for a duration of T_2 = 128 R_2C_2 corresponding to the timing interval of Unit 2; and finally revert back to its rest state after the completion of the entire timing sequence.

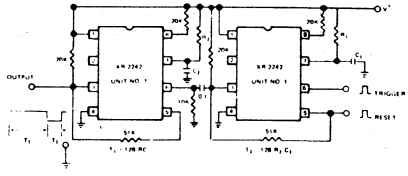
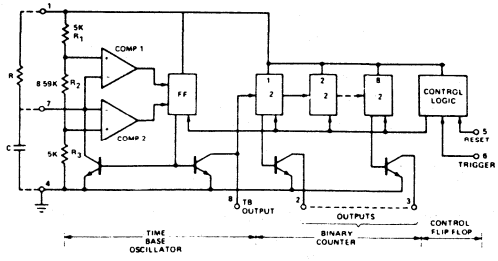


Figure 14. Sequential Timing Using Two XR-2242 Timer Circuits



EQUIVALENT SCHEMATIC DIAGRAM

Micropower Long Range Timer

GENERAL DESCRIPTION

The XR-2243 is a monolithic Timer/Controller capable of producing ultra-long time delays from micro-seconds to days. Two timing circuits can be cascaded to generate time delays or timing intervals up to one year. The circuit is comprised of an internal time-base oscillator, an 11-bit binary counter and a control flop-flop. For a given external R-C network connected to the timing terminal, the circuit produces an output timing pulse of 1024 RC. If the two circuits are cascaded, a total time delay of $(1024)^2$ or 1,048,576 RC is obtained.

The XR-2243 long range timer was designed for low power operation. Its supply current requires less than 100 μA in standby or reset mode. Normal operation requires less than 1mA.

The timing cycle is initiated by applying a positive going pulse to the trigger input, Pin 6. The time-base oscillator generates timing pulses with its period, T, equal to 1 RC. These clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to Pin 5.

In monostable timer applications, the output terminal (Pin 3) is connected to the reset terminal, Pin 5. In this manner, after 1024 clock pulses are counted, this output goes to "high" state and resets the circuit, thus completing the timing cycle. Therefore, after triggering, the output at Pin 3 will produce a total timing pulse of 1024 RC before the circuit resets itself to complete the timing cycle. During the timing interval, the secondary output at Pin 2 produces a square-wave output with the period of 2 RC.

If the output at Pin 3 is not connected back to the reset terminal, the circuit continues to operate in an astable mode, subsequent to a trigger input.

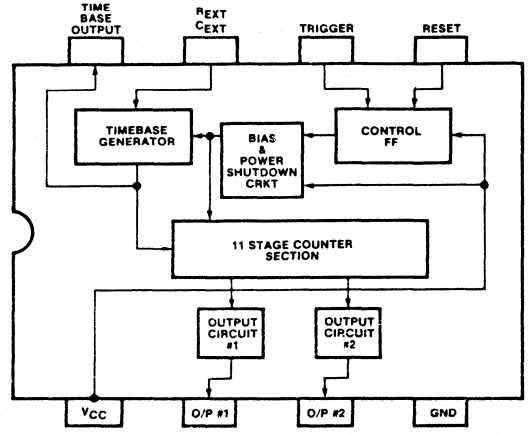
APPLICATIONS

Long Delay Generation
Sequential Timing
Precision Timing
Ultra-Low Frequency Oscillator
Battery Powered Applications

FEATURES

High Output Current Sink Capability
Timing from Micro-seconds to Days
Wide Supply Range: 2.7V to 15V
TTL and HCMOS Compatible Outputs

FUNCTIONAL BLOCK DIAGRAM



High Accuracy: 0.5%
Excellent Supply Rejection
Monostable and Astable Operation
Micro Power Consumption-Standby Operation
Low Power Consumption-Normal Operation

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 Volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic package	300 mW
Derate above +25°C	2.5 mW/°C
Temperature Range	
Operating	
XR-2243C	0°C to +70°C
Storage	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2243CN	Ceramic	0°C to +70°C
XR-2243CP	Plastic	0°C to +70°C

PRINCIPLES OF OPERATION

The ultra-long time delay micropower timer, in simplest block diagram terms, consists of a timing section followed by a counter section and a control flip-flop.

The main functional portion of the circuit is the time base section. It is a relaxation oscillator whose period

ELECTRICAL CHARACTERISTICS

Test Conditions: See Figure 3, $V^+ = 5V$, $T_A = 25°C$, $R = 22\ k\Omega$, $C = 0.047\ \mu F$, unless otherwise noted.

PARAMETERS	XR-2243C MIN	XR-2243C TYP	XR-2243C MAX	UNIT	CONDITIONS
Supply Voltage	2.7		15	V	
Supply Current		45	95	μA	$V_{CC} = 2.7V\ V_{TR} = 0V\ V_{RS} = 5V$
Standby		80	135	μA	$V_{CC} = 5V$
		250	415	μA	$V_{CC} = 15V$
Operating		900	1000	μA	$V_{CC} = 5V\ V_{TR} = 5V\ V_{RS} = 0V$
		750	900	μA	$V_{CC} = 2.7V$
		1250	1500	μA	$V_{CC} = 15V$
Time Base Section					
Timing Accuracy[1]		0.5	3	%	
Temperature Drift		80	125	ppm/°C	$V_{CC} = 2.7V\ V_{TR} = 5V\ V_{RS} = 0V$
		150	225	ppm/°C	$V_{CC} = 5V$
		300	650	ppm/°C	$V_{CC} = 15V\ 0°C \le T_A \le 70°C$
Supply Drift		0.30	1.0	%/V	$V_{CC} = 8V$
Maximum Frequency	25	35		kHz	
Recommended Range of Timing Components					
Timing Resistor, R	0.005		10	MΩ	
Timing Capacitor, C	0.005		1000	μF	**Low Leakage Capacitor**
Trigger/Reset Controls					
Trigger					Measures at Pin 6, $V_{RS} = 0$
Trigger Threshold		1.4	2.0	V	
Trigger Current		22	30	μA	$V_{RS} = 0, V_{TR} = 2V$
Impedance		25		kΩ	
Response Time[2]		**20**		**μS**	**Nominal**
Reset					
Reset Threshold		1.4	2.0	V	
Reset Current		22	30	μA	$V_{TR} = 0, V_{RS} = 2V$
Impedance		25		kΩ	
Response Time		**20**		**μS**	**Nominal**
Counter Section					See Figure 4, $V^+ = 5V$
Max. Toggle Rate	100	250		kHz	$V_{RS} = 0, V_{TR} = 5V$ Measured at Pin 8
Input:					
Impedance		15		kΩ	
Threshold		1.4		V	**$2.7V \le V_{CC} \le 15V$**
Output:					
Sink Current		10		mA	$V_{OL} \le 0.4V$
Leakage Current		0.01		μA	$V_{OH} \le 15V$

1. Timing error solely introduced by XR-2243.
2. Minimum time between reset and trigger is dependent upon timing capacitor values.

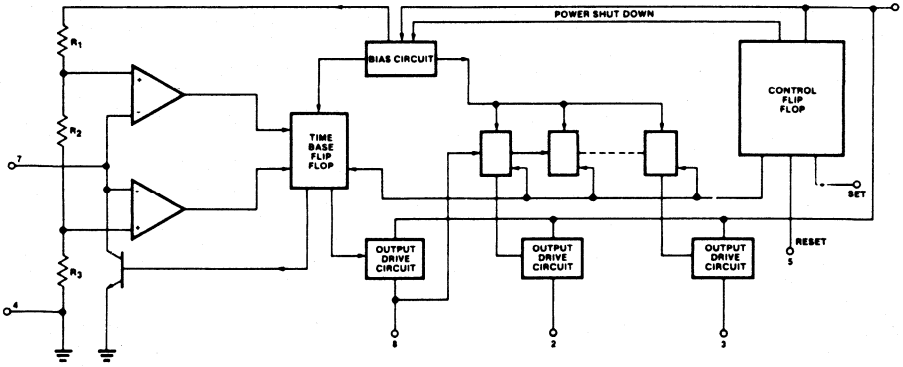


Figure 1. Simplified Circuit Schematic

of oscillation is determined by the external R and C values. The timing section is followed by an I^2L counter, which consists of eleven binary stages, with high current drive capability output stages from the first and the last. A third subsection of the circuit is the control logic circuit consisting of a flip-flop that is set and reset by Pins 6 and 5, respectively. This section controls the resetting of all counter stages, and starting the timing circuit upon application of a positive-going trigger pulse. The control logic also activates the power shut down circuit when a reset pulse is received, or when the timing cycle is completed. The power shut down circuit turns off the bias line to the time base and I^2L counters to reduce the standby power.

CONTROL FLIP-FLOP

The logic flip-flop circuit controls the time/counter, as well as the internal power, to reduce standby current consumption to approximately 100μA. Upon command, by a positive-going trigger pulse applied to Pin 6, the control logic circuit will first establish the upper and lower threshold voltages and then setup all internal current sources, biasing the time base and counter sections.

The circuit will automatically reset itself when power is first applied. Once triggered, the circuit is immune to additional trigger pulses until it is reset. A reset pin terminates the timing cycle by resetting the internal logic and shuts off the internal bias circuitry.

TIME BASE OSCILLATOR

The time base oscillator is a simple exponential ramp type timer circuit. The timing components, R and C, are external to the chip. The operation of such an oscillator can be described as follows: when the circuit is at rest the flip-flop is latched in its reset state, the discharge transistor is "off", and the external capacitor, C, is fully charged to a voltage approximately equal to V_{CC}. When the circuit is triggered, the flip-flop is unlatched and set, which causes the discharge transistor to turn "on" and discharge C rapidly. When the voltage across C discharges to the voltage level V_{th-}, the upper comparator changes state, resets the flip-flop and turns the discharge transistor "off". Then, C charges toward V_{CC} with a time constant set by the external R and C. When the voltage across it reaches the upper threshold, V_{th+}, the comparator changes state, sets the flip-flop again, and discharges C back to the lower threshold level, V_{th-}. In this manner, the circuit continues to oscillate with the voltage level across C exponentially rising to V_{th+}, then rapidly decaying to V_{th-} and then repeating this cycle until the timing period ends.

COUNTER SECTION (Pin 8)

The counter consists of eleven stages connected in a "ripple counter" configuration. The operating injector currents are set from a bus of 1.2 volts. This current is supply independent. Pin 8, which is time based o/p, is also the counter section input.

I^2L counters are D-type flip-flops with their $\overline{Q}$ output internally connected to their D input; basically, they form a divide by 2 block. With eleven stages, one could create delays of 1024 RC in a monostable mode of operation. The counters change state on the falling edge of the clock pulses.

When the trigger pulse is applied, the internal power line which is supplying voltage for I^2L circuitry (I^2LV_{CC}) is set up first, a Schmitt trigger circuit with a built in delay ensures the application of an internal set pulse, right after the power for the I^2 section is made available. The counters are all set to "1" and are ready to count with the incoming falling edges of clock impulses.

OUTPUT SECTIONS (Pins 2 and 3)

The output sections are designed such that they can handle 10mA load currents @ V_{OL} = 300mV. Both of the transistors in this section are operating in a non-saturated mode because of the clamping action. This ensures faster operation and also decreases the need of high base drive at full load operation. The two outputs of the XR-2243 contain 1KΩ pull up resistors.

The timing cycle for the circuit is initiated by applying a positive-going trigger to the set, or trigger pin, (Pin 6) of the device. The trigger pulse actuates the time base oscillator, enables the counter section, and sets the outputs to "low" state. The time base oscillator generates timing pulses with its period, T = 1RC. These timing or clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to the reset pin (Pin 5).

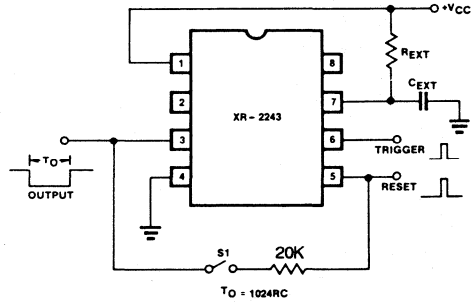


Figure 2. Typical Operation Diagram

ASTABLE AND MONOSTABLE MODE

Figure 2 shows the basic connection diagram for astable and monostable modes. When switch S_1 is open, the circuit is in its astable mode of operation. Upon the application of a trigger pulse, the time base oscillator resumes the timing cycles. Until the application of a reset pulse, the circuit will keep on working while generating a square wave at the last stage output, whose frequency is 1/2048 of the time base oscillator frequency. When switch S_1 is closed, the circuit is in its monostable mode of operation, with the last stage being connected to the reset input via an external resistor. This way, when a trigger pulse is applied, and the time base resumes its timing cycle, the last stage output will go low with the first pulse generated by the time

base generator, and will stay low for 1024 pulses. With the arrival of the 1024th pulse, the last output will go to a high state since it is coupled to the reset input (see Figure 3). When this stage goes high, the timing cycle is completed.

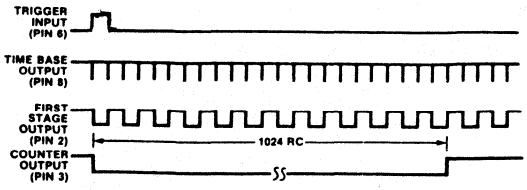


Figure 3. Timing Diagram of Output Waveforms

CASCADED MODE

The cascaded mode of operation allows the generation of ultra-long time delays. When several XR-2243 circuits are cascaded, such that their counter sections are connected in series, the total count available increases geometrically rather than arithmetically. Since one XR-2243 is capable of generating a total of 1024 RC time delay, where R and C are the external timing components, then when two such timers are cascaded, they will produce $(1024)^2$ RC and three will produce $(1024)^3$ RC time delay, and so on. Thus, one can easily achieve time delays in the range of days, months, or years, simply by cascading two or three such counter/timer circuits.

Figure 4 shows the basic connection for cascaded operation. Unit 2's time base is disabled by grounding Pin 7 to ground via 1 kΩ resistor. The last stage output of Unit 1 is connected to the input of the counter section of Unit 2. When the circuit is triggered, Unit 1 will resume generating a frequency whose period $T = R_{ext}C_{ext}$. The output of Unit 1 will change state every 1024 pulses. Since these pulses are supplied to Unit 2, the circuit will stop the timing cycle after 1024 pulses are generated by Unit 1. Therefore, a time delay of $(1024)^2$ RC is generated.

SEQUENTIAL TIMING APPLICATIONS

Figure 5 shows the basic connections for sequential timing applications. In this mode of operation, Unit 2's trigger input is connected to Unit 1's last output, while each unit's reset input is connected to their last output via external resistors. This way, Unit 1 will generate a time delay 1024 R_1C_1 upon the application of a trigger pulse. Once 1024 R_1C_1 seconds have elapsed, Unit 2 will be triggered, generating in its turn a delay equal to 1024 R_2C_2 seconds; therefore, resulting in an overall time delay of 1024 R_1C_1 + 1024 R_2C_2.

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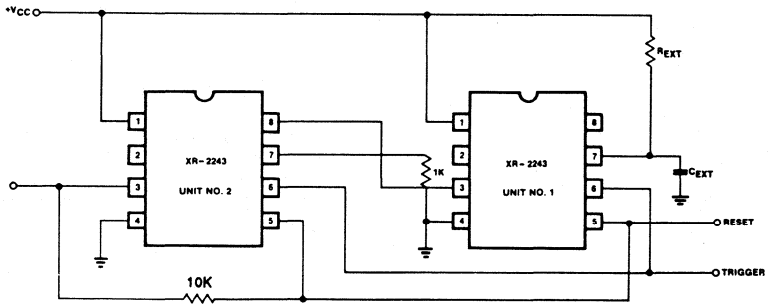


Figure 4. Cascaded Operation of Two XR-2243 Timer Circuits

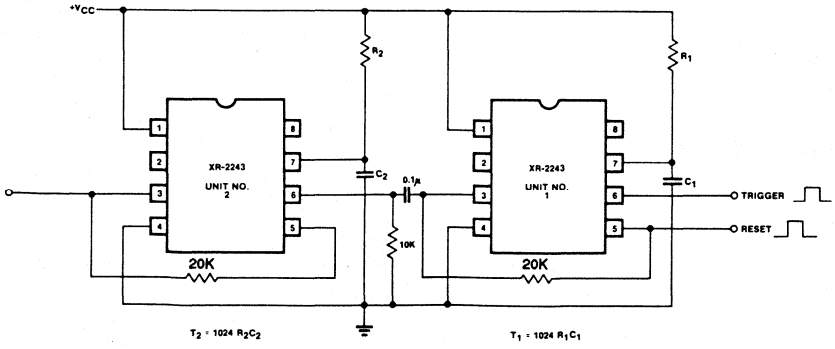


Figure 5. Sequential Timing Using XR-2243 Timer Circuits

Monolithic Timing Circuit

GENERAL DESCRIPTION

The XR-320 monolithic timing circuit is designed for use in instrumentation and digital communications equipment, and for a wide variety of industrial control and special testing applications. In many cases, this circuit provides a monolithic replacement for mechanical or electromechanical timing devices.

The XR-320 timing circuit generates precise timing pulses (or time delays) whose repetition rate (or length) is determined by an external timing resistor, R, and timing capacitor, C. The timing period is exactly equal to 2RC and can be continuously varied from 1 μsec to 1 hour. The circuits can be operated in a monostable or free-running (self-triggering) mode. They can be used for sequential timing and sweep generation, and also for pulse-position and pulse-width modulation.

The XR-320 integrated circuit is comprised of a stable internal bias reference, a precision current source, a voltage comparator, a flip-flop, a timing switch, and a pair of output logic drivers. The high current output at pin 12 can sink or source up to 100 milliamps of current.

FEATURES

Wide Timing Range: 1 μsec to 1 hour
High Accuracy: 1%
Excellent Temperature Stability: 100 ppm/°C
Wide Supply Voltage Range: 4.5V to 18V
Triggering with Positive or Negative-Going Pulses
Programmable
  Resistor Programming: 3 decades
  Capacitor Program: 9 decades
Logic Compatible Outputs
High Current Drive Capability: 100 mA

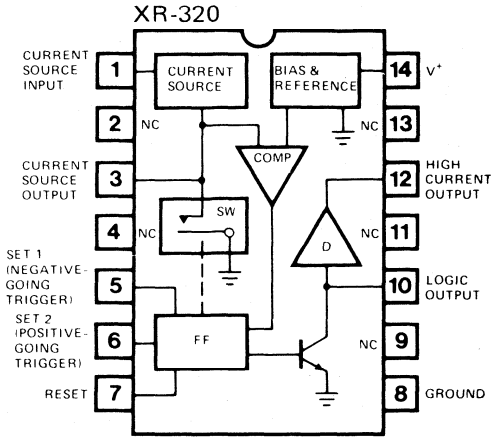
APPLICATIONS

Precision Timing
Time-Delay Generation
Sequential Timing
Pulse Generation/Shaping
Pulse-Position Modulation
Pulse-Width Modulation
Sweep Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Internal Power Dissipation	750 mW
Plastic Package:	625 mW
Derate above T_A = +25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-320P	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-320 is an extremely versatile monolithic timer capable of delays ranging from 1 μsec to 1 hour. It works with both positive and negative triggering, and features both normally high and normally low outputs. An on board current source, programmable by an external resistor, changes the timing capacitor. This produces a true ramp function and allows accurate timing intervals equal to 2 RC.

Positive going triggering is applied to Pin 6; negative triggering is applied to Pin 5. After a trigger pulse is applied, the open collector output (Pin 10) will go high and the high current output (Pin 12) switches into the current sink mode. At timeout, the open collector pulls low, and can sink 10 mA; the high current output goes high and can source 100 mA. Utilizing the high current output requires a pull-up resistor from Pin 10 to $+V_{CC}$. The resistor must limit current to no more than 10 mA; 1 mA is sufficient. Timing is interrupted and the device is reset when Pin 7 is grounded. Astable operation is attained by tying the negative going (falling) trigger (Pin 5) to the timing capacitor (Pin 3). In this configuration, the device will automatically retrigger itself upon completion of the timing interval.

ELECTRICAL CHARACTERISTICS

Test Conditions: Supply Voltage = 12V ±5%, Test Circuit of Figure 2, T_A = 25°C, unless otherwise specified.

PARAMETERS	XR-320 MIN	XR-320 TYP	XR-320 MAX	UNITS	CONDITIONS
Supply Voltage	4.5		18	V_{dc}	
Quiescent Supply Current					
V+ = 5V		2.0	3.5	mA	
V+ = 12V		6.0	7.0	mA	
V+ = 18V		10.0	12.5	mA	
Timing Cycle Supply Current					
V+ = 5V		2.5	4.0	mA	
V+ = 12V		6.5	8.0	mA	
V+ = 18V		12.0	14.0	mA	
Timing Accuracy					
V+ = 5V		1.0	5.0	%	
V+ = 12V		1.0	5.0	%	
V+ = 18V		1.0	5.0	%	
Temperature Drift		100		ppm/°C	
Timing vs. Supply Voltage		0.1	0.5	%/V	
Stand-by Voltage (Pin 3)		0.7		V	
Comparator Threshold Voltage (Pin 3)					
V+ = 5V		2.4		V	
V+ = 12V	4.5	5.2	6.0	V	
V+ = 18V		8.4		V	
Current Source Input Voltage (Pin 1)					
V+ = 5V		4.15		V	
V+ = 12V	9.0	9.75	10.6	V	
V+ = 18V		16.15		V	
Trigger Voltage					
Set (Pin 5)		1.0	1.5	V	See Figure 11
Set 2 (Pin 6)	0.5	1.4		V	See Figure 12
Reset (Pin 7)		0.7	1.5	V	
Trigger Current					
Set 1 (Pin 5)		10		μA	
Set 2 (Pin 6)		60		μA	
Reset (Pin 7)		30		μA	
Output 1 (Pin 10) (Normally low)					
"Low" Voltage		0.1		V	
"High" Voltage	4.0	5.0		V	
Rise Time		140		nsec	
Fall Time		50		nsec	
Output 2 (Pin 12) (Normally high)					
"High" Voltage		10.4		V	I_{source} = 100 mA
"Low" Voltage		1.5		V	I_{sink} = 100 mA
Rise Time		100		nsec	
Fall Time		40		nsec	

DEFINITIONS

Timing Accuracy: the timing error solely introduced by the XR-320, defined in per cent as:

$$100 \times \frac{\text{measured timing pulse length} - \text{2 RC based on actual component values}}{\text{2 RC based on actual component values}} \%$$

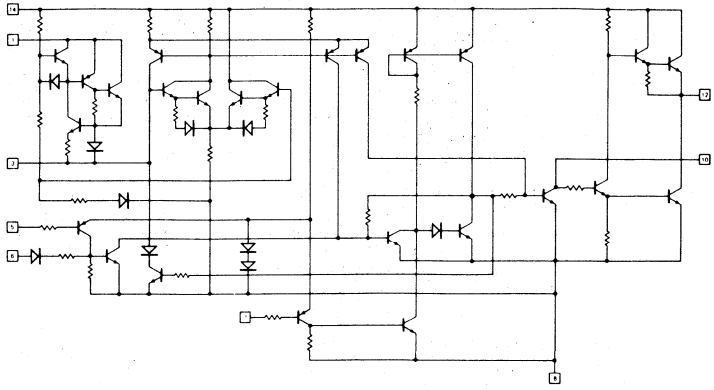
Timing vs Supply Voltage: the maximum timing drift over the power supply range of 5 to 18 volts referenced to 12 volt operation, defined in per cent per volt as:

$$\frac{100}{15} \times \frac{\text{max. timing pulse length over 5 to 18 volt supply} - \text{min. timing pulse length over 5 to 18 volt supply}}{\text{timing pulse length with 12 volt supply}} \%/V$$

Stand-by Voltage: the voltage between pin 3 and ground in reset condition.

Comparator Threshold Voltage (Pin 3): the voltage at which the internal comparator triggers the flip-flop and the timing capacitor discharges.

Trigger Voltage: the DC voltage level applied to each set or reset terminal which causes the output to change state.



EQUIVALENT SCHEMATIC DIAGRAM

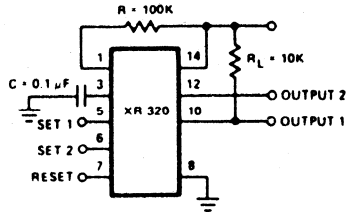


Figure 1. Test Circuit

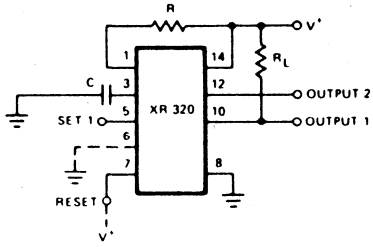


Figure 2. Monostable Operation, Negative Trigger

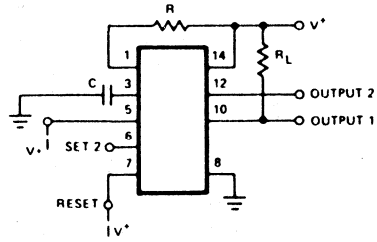


Figure 3. Monostable Operation, Positive Trigger

OPERATING INSTRUCTIONS

Figures 2 and 3 show typical connections for the XR-320. Only three external components are required for basic operation: the resistor R and capacitor C which determine the time delay (2RC); and an external load resistor, R_L. The circuit provides two independent logic outputs: a medium current output (up to 10 mA) at pin 10, and a high current output (up to 100 mA) at pin 12. The output at pin 10 is of the "bare-collector" type which requires an external pull-up resistor, R_L, connected between this terminal and V^+ for proper circuit operation.

With no trigger pulse applied, the output at pin 10 is in a low state near ground potential; and the output at pin 12 is in a high state, near V^+. The circuit is triggered by the application of a negative-going pulse to pin 5 or a positive-going pulse to pin 6. At that instant, the output levels change state such that pin 10 becomes high and pin 12 low. The outputs will remain in this (switched) state until the delay time, T = 2RC, expires, at which time the outputs will return to their original state. In this mode of operation, the trigger input can be activated repeatedly without further influencing the time cycle, i.e., once the circuit is triggered it becomes immune to subsequent triggering until the entire timing cycle is completed.

For reliable operation, the trigger pulse width must he shorter than the output pulse width. Although many units will function when this rule is not observed, proper operation cannot be guaranteed.

Figure 4 shows the waveforms at various circuit locations for a negative-going trigger applied to pin 5. A similar set of waveforms is displayed in Figure 5 for a positive-going pulse applied to pin 6. The timing cycle can be reset at any time by simply grounding pin 7.

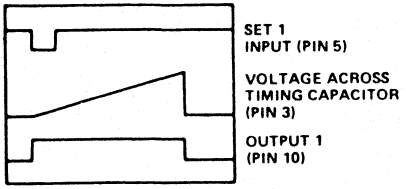


Figure 4. Waveforms for Negative-Going Trigger

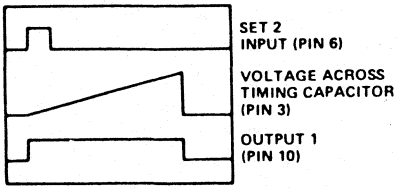


Figure 5. Waveforms for Positive-Going Trigger

DESCRIPTION OF CIRCUIT CONTROLS

TIMING RESISTOR (PIN 1)

Timing resistor, R, is connected between pin 1 and V+, pin 14. For maximum timing accuracy, R should be in the range 6 kΩ ≤ R ≤ 1 MΩ. See Figure 6 for the minimum and maximum values for R for various supply voltages.

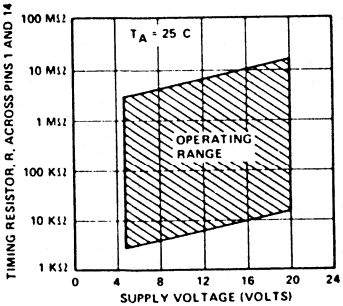


Figure 6. Operating Range as a Function of Timing Resistor and Supply Voltage

TIMING CAPACITOR (PIN 3)

Timing capacitor, C, is connected between pin 3 and ground. The time delay, T, is equal to 2RC in seconds. NOTE: A timing error can result due to the leakage current of the timing capacitor. When a capacitor with a relatively low insulation resistance (e.g. a high-valued electrolytic) is used as the timing capacitor, the resulting delay time will be much longer than 2RC because of the associated leakage current.

SET 1 — NEGATIVE TRIGGER (PIN 5)

A negative-going pulse applied to pin 5 will cause the outputs to change state. Output 1, pin 10, which is normally low will go high, Output 2, pin 12, which is normally high will go low. See Figure 11 for additional details. When not used, pin 5 should be connected to V+ to avoid false triggering.

By grounding or applying a negative pulse to the reset (Pin 7), the timing cycle is automatically interrupted and the outputs return to their original state. When the reset function is not in use, it is recommended that it be connected to V+ to avoid any possibility of false resetting.

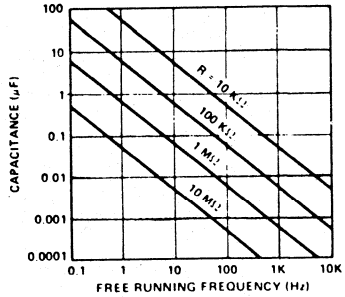
SET 2 — POSITIVE TRIGGER (PIN 6)

A positive-going pulse applied to pin 6 will cause the outputs to change state. The normally low output at pin 10 will go high, and the normally high output at pin 12 will go low. See Figure 12 for additional details. When not used, pin 6 should be grounded to avoid false triggering.

ADDITIONAL APPLICATIONS

FREE-RUNNING MODE

By shorting pins 3 and 5, the XR-320 will operate in a "free-running" or self-triggering mode. In this mode of operation, the circuit functions as a stable clock pulse generator with a repetition rate of approximately 1/(2RC). The circuit connection and free-running frequency in this application are shown in Figure 7. Note that one cycle is not precisely equal to 2RC because of capacitor discharge time. Typical waveforms for self-triggered operation are shown in Figure 8.



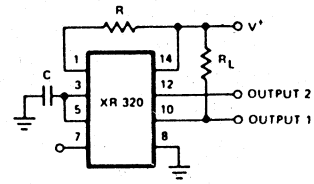


Figure 7. Free-Running Operation

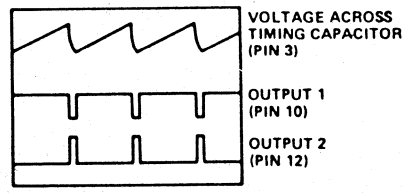


Figure 8. Waveforms for Self-Triggered Operation

SWEEP GENERATION

In self-triggered operation, the waveform across the timing capacitor (at pin 3) is a linear ramp as shown in Figure 8. The waveform at pin 3 can be used as a highly linear sweep voltage with a total nonlinearity of less than 1%.

PULSE-WIDTH MODULATION

For this application, the XR-320 should be connected as shown in Figure 9.

The modulation input is applied to pin 1 through coupling capacitor, C_C. The input signal modulates the current through the timing resistor, R, and, in turn, changes the width of the output timing pulses. The resistor R_M, in series with the signal source, is used to control the amount of modulation for a given input signal level.

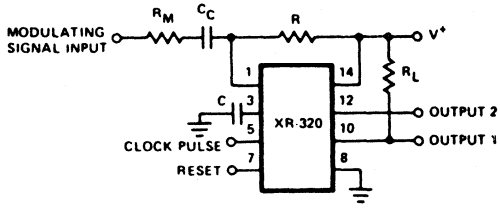


Figure 9. Circuit Connection for Pulse-width Modulation

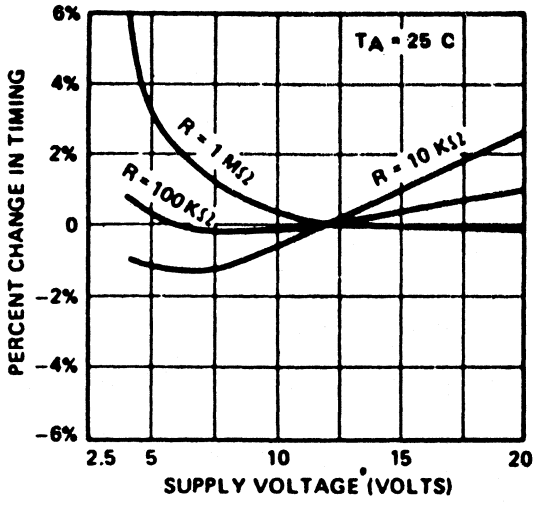


Figure 10. Change in Timing vs. Supply Voltage

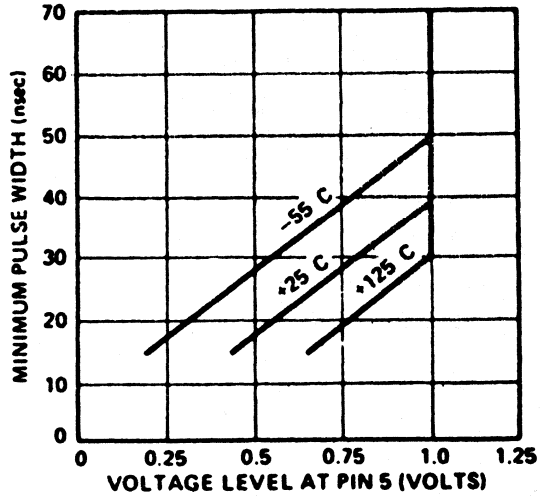


Figure 11. Minimum Pulse Width for Triggering at Pin 5

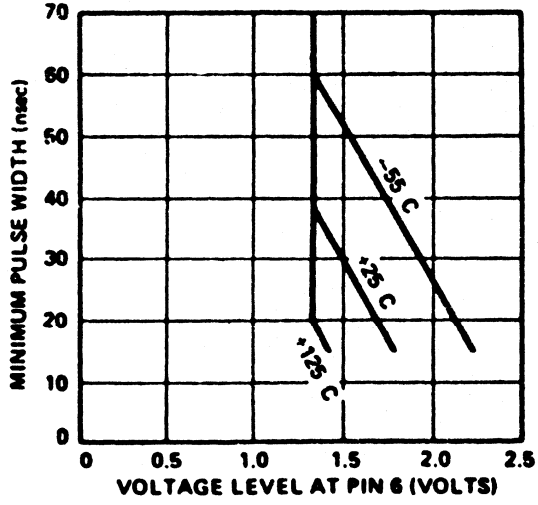


Figure 12. Minimum Pulse Width for Triggering at Pin 6

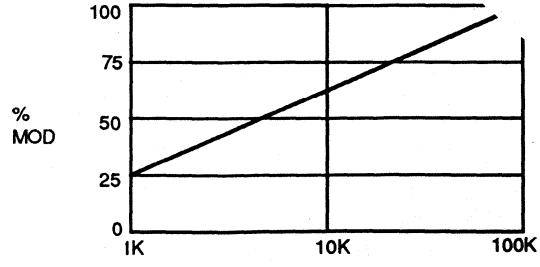


Figure 13. % MOD vs R_M

Micropower Timing Circuit

GENERAL DESCRIPTION

The XR-L555 is a stable micropower controller capable of producing accurate timing pulses. It is a direct replacement for the popular 555-timer for applications requiring very low power dissipation. The XR-L555 has approximately 1/15th the power dissipation of the standard 555-timer and can operate down to 2.7 volts without sacrificing such key features as timing accuracy and frequency stability. At 5-volt operation, typical power dissipation of the XR-L555 is 900 microwatts.

The circuit contains independent control terminals for triggering or resetting if desired. In the monostable mode of operation, the time delay is controlled by one external resistor and one capacitor. For astable operation as an oscillator the free-running frequency and the duty cycle are accurately controlled with two external resistors and one capacitor as shown in Figure 2. The XR-L555 is triggered or reset on falling waveforms. Its output can source up to 100 mA or drive TTL circuits.

Because of its temperature stability and low-voltage (2.7V) operation capability, the XR-L555 is ideally suited as a micropower clock oscillator or VCO for low-power CMOS systems. It can operate up to 1500 hours with only two 300 mA-Hr batteries.

FEATURES

Pin Compatible with Standard 555 Timer
Less than 1 mW Power Dissipation (V+ = 5V)
Timing from Microseconds to Minutes
Over 1000-Hour Operation with 2 Batteries
Low Voltage Operation (V+ = 2.7V)
Operates in Both Monostable and Astable Modes
CMOS TTL and DTL Compatible Outputs

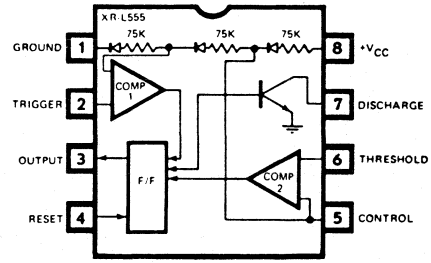
APPLICATIONS

Battery Operated Timing
Micropower Clock Generator
Pulse Shaping and Detection
Micropower PLL Design
Power-On Reset Controller
Micropower Oscillator
Sequential Timing
Pulse Width Modulation
Appliance Timing
Remote-Control Sequencer

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts

FUNCTIONAL BLOCK DIAGRAM



Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
SO-8	225 mW
Derate above +25°C	2.5 mW/°C
Storage Temperature	−65°C to +125°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-L555N	Ceramic	0°C to +70°C
XR-L555CN	Ceramic	0°C to +70°C
XR-L555CP	Plastic	0°C to +70°C
XR-L555MD	Japanese SOIC SO-8	0°C to +70°C

SYSTEM DESCRIPTION

The XR-L555 is a micropower timing circuit similar to the industry standard 555-type timer. It is not a direct replacement for a CMOS 555 timer. It is capable of both monostable and astable operation with timing intervals ranging from low microseconds up through several hours. Timing is independent of supply voltage which may range from 2.7 V to 15 V. The output stage can source 100mA.

In the monostable (one shot) mode, timing is determined by one resistor and capacitor. Astable operation (oscillation) requires an additional resistor, which controls duty cycle. An internal resistive divider provides a reference voltage of 2/3 V_{CC}, the interval is independent of supply voltage; however, for maximum accuracy, the user should ensure V_{CC} does not vary during timing.

The output of the XR-L555 is high during the timing interval. It is triggered and reset on falling waveforms. The control voltage input (Pin 5) may serve as a pulse width modulation point.

For applications requiring dual L555-type timers, see the XR-L556.

ELECTRICAL CHARACTERISTICS

Test Conditions: (T_A = 25°C, V_{CC} = +5V, unless otherwise specified.)

PARAMETERS	XR-L555N			XR-L555C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
Supply Voltage	2.7		15	2.7		15	V	
Supply Current		150	300		190	500	μA	Low State Output V_{CC} = 5V, R_L = ∞
Timing Error								R_A, R_B = 1 KΩ to 100 KΩ
Initial Accuracy		0.5	2.0		1.0		%	C = 0.1 μF
Drift with Temperature		30	100		50		ppm/°C	0°C ≤ T_T ≤ 70°C *
Drift with Supply Voltage		0.05			0.05		%/V	
Threshold Voltage		2/3			2/3		x V_{CC}	
Trigger Voltage	1.45 4.8	1.67 5.0	1.9 5.2		1.67 5.0		V V	V_{CC} = 5V V_{CC} = 15V
Trigger Current		0.5			0.5		μA	
Reset Voltage	0.4	0.7	1.0	0.4	0.7	1.0	V	
Reset Current		0.1			0.1		mA	
Threshold Current		0.1	0.25		0.1	0.25	μA	
Control Voltage Level	2.90 9.6	3.33 10.0	3.80 10.4	2.60 9.0	3.33 10.0	4.00 11.0	V	V_{CC} = 5V V_{CC} = 15V
Output Voltage Drop (Low)		0.1	0.3		0.25	0.35	V	I_{sink} = 1.5 mA
Output Voltage Drop (High)	3.0 13	3.3 13.3		2.75 12.75	3.3 13.3		V V	I_{source} = 10 mA V_{CC} = 5V V_{CC} = 15V
		12.5			12.5		V	I_{source} = 100 mA V_{CC} = 15V
Rise Time of Output		100			100		nsec	
Fall Time of Output		100			100		nsec	
Discharge Transistor Leakage		0.1			0.1		μA	

* These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

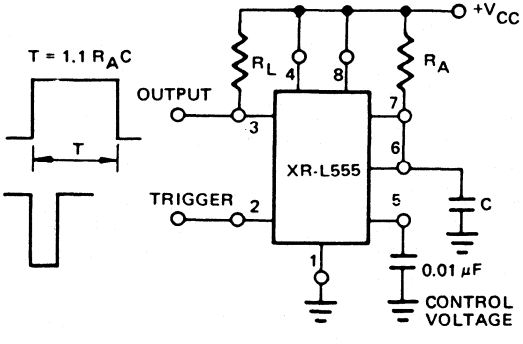


Figure 1. Monostable (One-Shot) Circuit

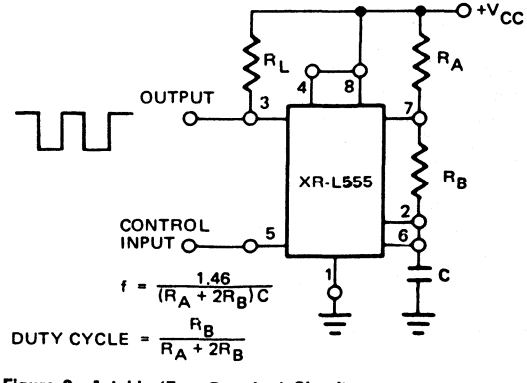


Figure 2. Astable (Free-Running) Circuit

GENERAL CHARACTERISTICS

CHARACTERISTIC CURVES

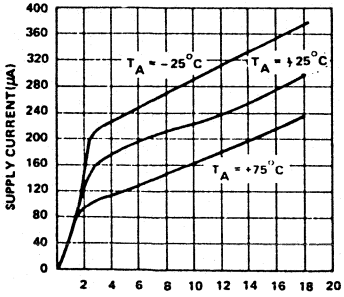


Figure 3. Supply Current as a Function of Supply Voltage

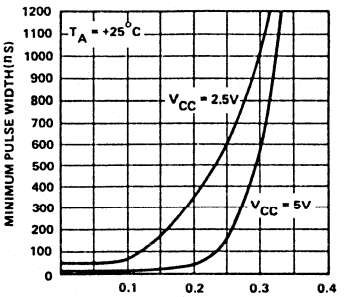


Figure 4. Minimum Pulse-Width Required for Triggering

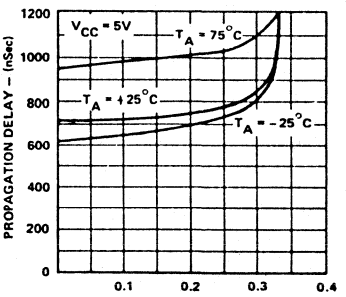


Figure 5. Propagation Delay as a Function of Voltage Level of Trigger Pulse

MONOSTABLE OPERATION

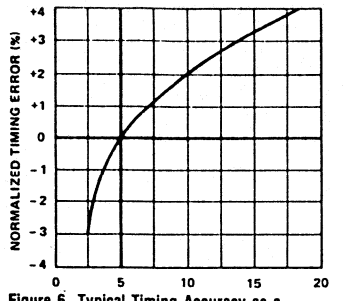


Figure 6. Typical Timing Accuracy as a Function of Supply Voltage

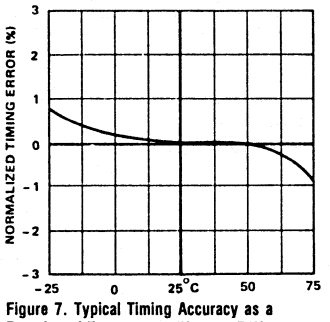


Figure 7. Typical Timing Accuracy as a Function of Temperature (V_{CC} = 51V, R_A = 100KΩ, C = 0.01 μF)

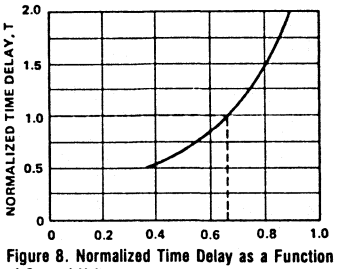


Figure 8. Normalized Time Delay as a Function of Control Voltage

ASTABLE OPERATION

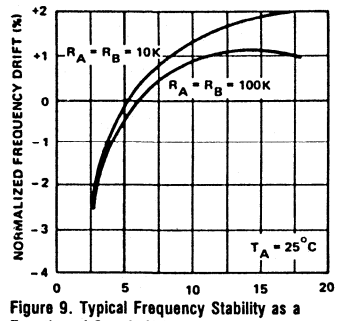


Figure 9. Typical Frequency Stability as a Function of Supply Voltage

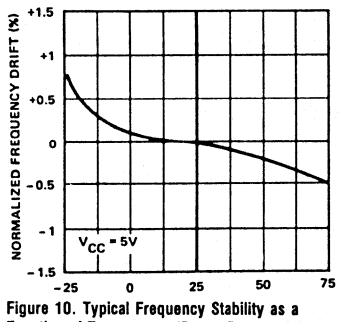


Figure 10. Typical Frequency Stability as a Function of Temperature (R_A = R_B = 10KΩ, C = 0.1 μF)

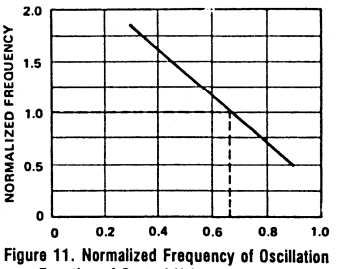


Figure 11. Normalized Frequency of Oscillation as a Function of Control Voltage

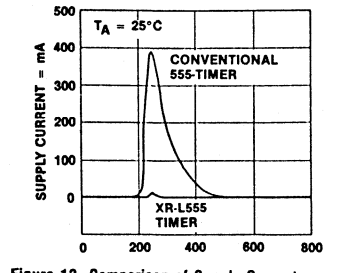


Figure 12. Comparison of Supply Current Transient of Conventional 555-Timer with XR-L555 Micropower Timer

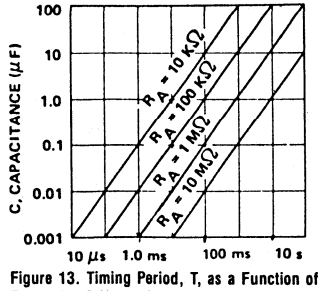


Figure 13. Timing Period, T, as a Function of External R-C Network

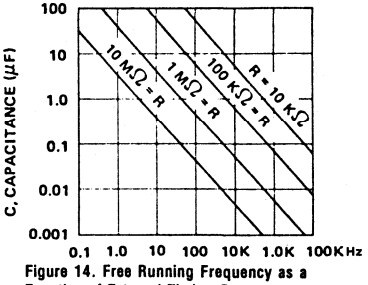


Figure 14. Free Running Frequency as a Function of External Timing Components (Note: R = R_A + 2R_B)

FEATURES OF XR-L555

The XR-L555 micropower timer is, in most instances, a direct pin-for-pin replacement for the conventional 555-type timer. However, compared to conventional 555-timer, it offers the following important performance features:

Reduced Power Dissipation: The current drain is 1/15th of the conventional 555-timer.

No Supply Current Transients: The conventional 555-timer can produce 300 to 400 mA of supply current spikes during switching. The XR-L555 is virtually transient-free as shown in Figure 12.

Low-Voltage Operation: The XR-L555 operates down to 2.7 volts of supply voltage, vs. 4.5V minimum operating voltage needed for conventional 555-timer. Thus, the XR-L555 can operate safely and reliably with two 1.5V batteries.

Proven Bipolar Technology: The XR-L555 is fabricated using conventional bipolar process technology. Thus, it is immune to electrostatic burn-out problems associated with low-power timers using CMOS technology.

APPLICATIONS INFORMATION

MONOSTABLE (ONE-SHOT) OPERATION

The circuit connection for monostable, or one-shot operation of the XR-L555 is shown in Figure 1. The internal flip-flop is triggered by lowering the trigger level at pin 2 to less than 1/3 of V_{CC}. The circuit triggers on a negative-going slope. Upon triggering, the flip-flop is set to one side, which releases the short circuit across the capacitor and also moves the output level at pin 3 toward V_{CC}. The voltage across the capacitor, therefore, starts increasing exponentially with a time constant $\tau = R_A C$. A high impedance comparator is referenced to 2/3 V_{CC} with the use of three equal internal resistors. When the voltage across the capacitor reaches this level, the flip-flop is reset, the capacitor is discharged rapidly, and the output level moves toward ground, and the timing cycle is completed.

The duration of the timing period, T, during which the output logic level is at a "high" state is given by the equation:

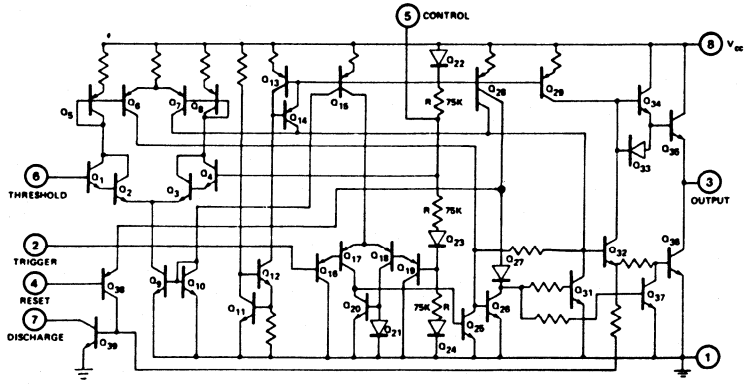
$$T = 1.1\ R_A C$$

The time delay varies linearly with the choice of R_A and C as shown by the timing curves of Figure 13. For proper operation of the circuit, the trigger pulse-width *must be* less than the timing period.

Once the circuit is triggered it is immune to additional trigger inputs until the present timing-period has been completed. The timing-cycle can be interrupted by using the reset control (pin 4). When the reset control is "low", the internal discharge transistor is turned "on" and prevents the capacitor from charging. As long as the reset voltage is applied, the digital output level will remain unchanged, i.e. "low". The reset pin should be connected to $+V_{CC}$ when not used to avoid the possibility of false triggering.

ASTABLE (SELF-TRIGGERING) OPERATION

For astable (or self-triggering) operation, the correct circuit connection is shown in Figure 2. The external capacitor charges to 2/3 V_{CC} through the **series** combination of R_A and R_B, and discharges to 1/3 V_{CC} through R_B. In this manner, the capacitor voltage oscillates between 1/3 V_{CC} and 2/3 V_{CC}, with an exponential waveform. The oscillations can be keyed "on" and "off" using the reset control. The frequency of oscillation can be readily calculated from the equations in Figure 2 and Figure 14.



EQUIVALENT SCHEMATIC DIAGRAM

Micropower Dual Timer

GENERAL DESCRIPTION

The XR-L556 dual timer contains two independent micropower timer sections on a monolithic chip. It is a direct replacement for the conventional 556-type dual timers, for applications requiring very low power dissipation. Each section of the XR-L556 dual timer is equivalent to Exar's XR-L555 micropower timer. The circuit dissipates only 1/15th of the stand-by power of conventional dual timers and can operate down to 2.5 volts without sacrificing such key features as timing accuracy and stability. At 5 volt operation, typical power dissipation of the dual-timer circuit is less than 2 mW; and it can operate in excess of 500 hours with only two 300 mA-Hr NiCd batteries.

The two timer sections of the circuit have separate controls and outputs, but share common supply and ground terminals. Each output can source up to 100 mA of output current or drive TTL circuits.

FEATURES

Replaces two XR-L555 Micropower Timers
Same Pinout as Standard 556-Type Dual Timer
Less than 1 mW Power Dissipation per Section (V_{CC} = 5V)
Timing from Microseconds to Minutes
Over 500-Hour Operation with 2 NiCd Batteries
Low Voltage Operation (V_{CC} = 2.7V)
Operates in Both Monostable and Astable Modes
CMOS TTL and DTL Compatible Outputs
Introduces No Switching Transients

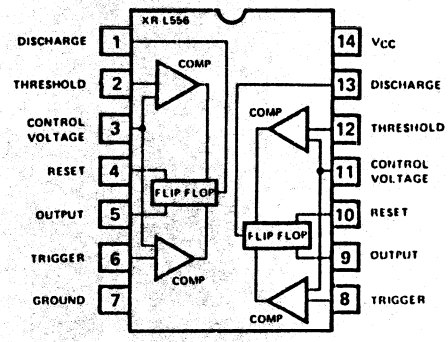
APPLICATIONS

Battery Operated Timing
Micropower Clock Generator
Pulse Shaping and Detection
Micropower PLL Design
Power-On Reset Controller
Micropower Oscillator
Sequential Timing
Pulse-Width Modulation
Appliance Timing
Remote-Control Sequencer

ABSOLUTE MAXIMUM RATINGS

Power Supply	18V
Power Dissipation	
Ceramic Dual-In-Line	750 mW
Derate above T_A = 25°C	6 mW/°C
Plastic Dual-In-Line	625 mW
Derate above T_A = 25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-L556 CN	Ceramic	0°C to +70°C
XR-L556 CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-L556 is a micropower version of the industry standard XR-556 timing circuit, capable of both monostable and astable operation with timing intervals ranging from low microseconds up through several hours. Timing is independent of supply voltage, which may range from 2.5 V to 15 V. The output stage can source 100 mA. Each timer section is fully independent and similar to the XR-L555. The XR-L556 is not a direct replacement for a CMOS 556, although the pinout is the same.

In the monostable (one shot) mode, timing is determined by one resistor and capacitor. Astable operation (oscillation) requires an additional resistor, which controls duty cycle. An internal resistive divider provides a reference voltage of 2/3 V_{CC}, which produces a timing interval of 1.1 RC. As the reference is related to V_{CC}, the interval is independent of supply voltage; however, for maximum accuracy, the user should ensure V_{CC} does not vary during timing.

The output of the XR-L556 is high during the timing interval. It is triggered and reset on falling waveforms. The control voltage inputs (Pins 3 and 11) may serve as pulse width modulation points.

XR-L556

ELELTRICAL CHARACTERISTICS

Test Conditions: (T_A = 25°DC, V_{CC} = +5V, unless otherwise specified)

PARAMETERS	XR-L556C MIN	XR-L556C TYP	XR-L556C MAX	UNITS	CONDITION
Supply Voltage	2.7		15	V	
Supply Current (Each Timer Section) Total Supply Current (Both Timer Sections)		200 400	500 1000	μA μA	Low State Output V_{CC} = 5V, R_L = ∞
Timing Error Initial Accuracy Drift with Temperature Drift with Supply Voltage		 1.0 50 0.5		 % ppm/°C %/V	R_A, R_B = 1 KΩ to 100 KΩ C = 0.1 μF 0°C ≤ T_T < 70°C * Monostable Operation
Threshold Voltage		2/3		X V_{CC}	
Trigger Voltage		1.67 5.0		V V	V_{CC} = 5V V_{CC} = 15V
Trigger Current		20		nA	
Reset Voltage	0.4	0.7	1.0	V	
Reset Curerent		10		μA	
Threshold Current		20	100	nA	
Control Voltage Level	2.60 9.0	3.33 10.0	4.00 11.0	V V	V_{CC} = 5V V_{CC} = 15V
Output Voltage Drop (Low)		0.15	0.35	V	I_{sink} = 1.5 mA
Output Voltage Drop (High)	 2.75 12.75	 3.3 13.3 12.5		 V V V	I_{source} = 10mA V_{CC} = 5V V_{CC} = 15V I_{source} = 100 mA V_{CC} = 15V
Rise Time of Output		200		nsec	
Fall Time of Output		100		nsec	
Discharge Transistor Leakage		0.1		μA	

*These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

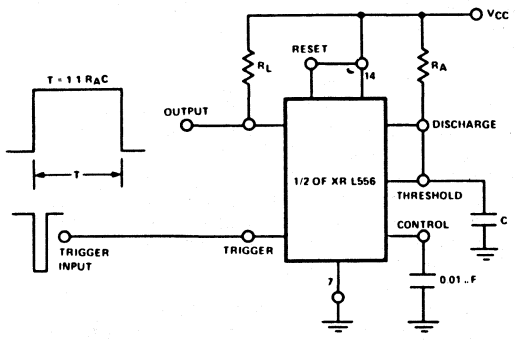


Figure 1. Monostable (One-Shot) Circuit

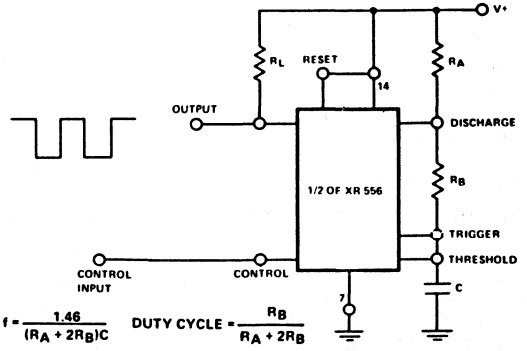


Figure 2. Astable (Free-Running) Circuit

CHARACTERISTIC CURVES

GENERAL CHARACTERISTICS

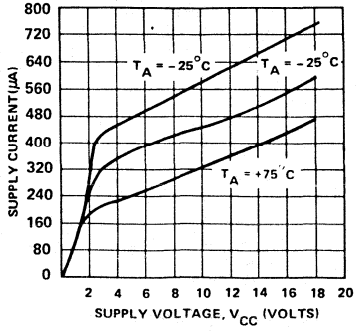


Figure 3. Total Supply Current as a Function of Supply Voltage

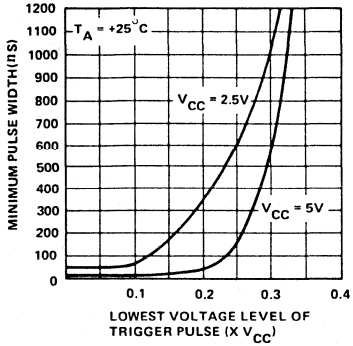


Figure 4. Minimum Pulse-Width Required for Triggering

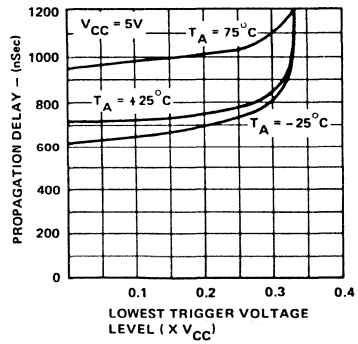


Figure 5. Propagation Delay as a Function of Voltage Level of Trigger Pulse

MONOSTABLE OPERATION

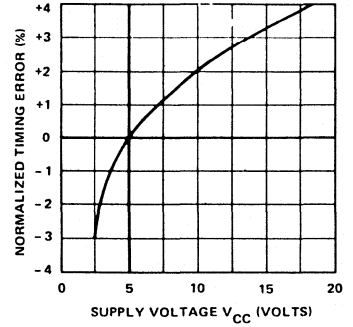


Figure 6. Typical Timing Accuracy as a Function of Supply Voltage

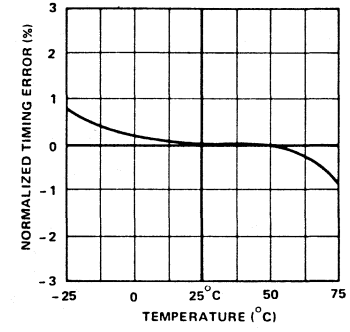


Figure 7. Typical Timing Accuracy as a Function of Temperature
(V_{CC} = 5V, R_A = 100KΩ, C = 0.01μF)

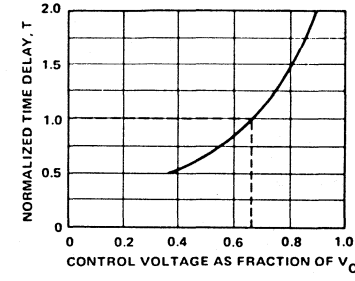


Figure 8. Normalized Time Delay as a Function of Control Voltage

ASTABLE OPERATION

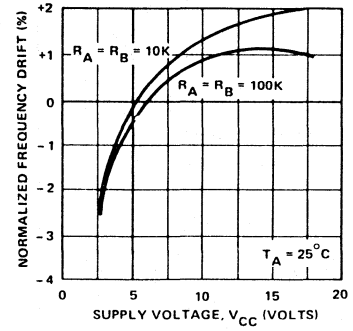


Figure 9. Typical Frequency Stability as a Function of Supply Voltage

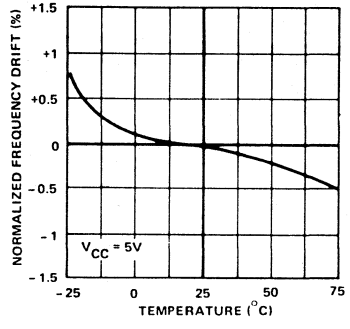


Figure 10. Typical Frequency Stability as a Function of Temperature
($R_A = R_B$ = 10KΩ, C = 0.1μF)

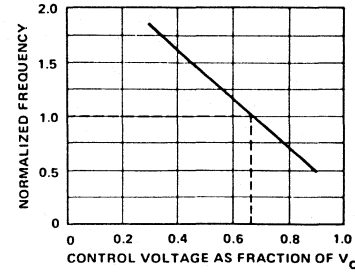


Figure 11. Normalized Frequency of Oscillation as a Function of Control Voltage

XR-L556

FEATURES OF XR-L556

The XR-L556 micropower dual timer is, in most instances, a direct pin-for-pin replacement for the conventional 556-type dual timer. However, compared to conventional 556-timer, it offers the following important performance features:

Reduced Power Dissipation: The current drain is 1/15th of the conventional 556-type dual timer.

No Supply Current Transients: The conventional 556-timer can produce 300 to 400 mA of supply current spikes during switching of either one of its timer sections. The XR-L556 is virtually transient-free as shown in Figure 12.

Low-Voltage Operation: The XR-L556 operates down to 2.7 volts of supply voltage, vs. 4.5V minimum operating voltage needed for conventional 556-timer. Thus, the XR-L556 can operate safely and reliably with two 1.5V NiCd batteries.

Proven Bipolar Technology: The XR-L556 is fabricated using conventional bipolar process technology. Thus, it is immune to electrostatic burn-out problems associated with low-power timers using CMOS technology.

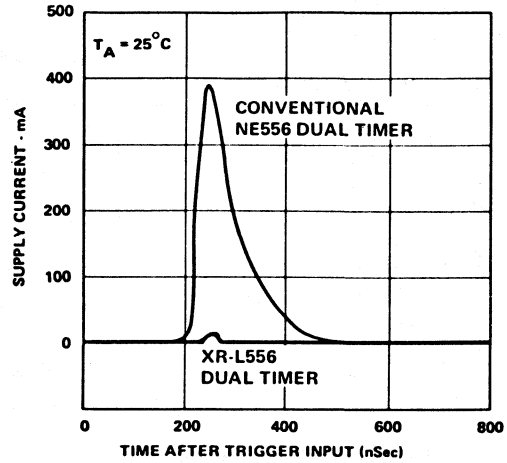


Figure 12. Comparison of Supply Current Transient of Conventional NE556 Dual Timer with XR-L556 Micropower Dual Timer

PRINCIPLES OF OPERATION

MONOSTABLE (ONE-SHOT) OPERATION

The circuit connection for monostable, or one-shot operation is one of the timer sections of the XR-L556 is shown in Figure 1. The internal flip-flop is triggered by lowering the trigger level to less than 1/3 of V_{CC}. The circuit triggers on a negative-going slope. Upon triggering, the flip-flop is set, which releases the short circuit across the capacitor and also moves the output level toward V_{CC}. The voltage across the capacitor, therefore, starts increasing exponentially with a time constant $\tau = R_AC$. A comparator is referenced to 2/3 V_{CC} with the use of three equal internal resistors. When the voltage across the capacity reaches this level, the flip-flop is reset, the capacitor is discharged rapidly, the output level moves toward ground and the timing cycle is completed. The duration of the timing period, T, during which the output logic level is at a "high" state is given by the equation:

$$T = 1.1\ R_AC$$

This time delay varies linearly with the choice of R_A and C as shown by the timing curves of Figure 13. For proper operation of the circuit, the trigger pulse-width *must be* less than the timing period.

Once the circuit is triggered it is immune to additional trigger inputs until the present period has been completed. The timing-cycle can be interrupted by using the reset control. When the reset control is "low", the internal discharge transistor is turned "on" and prevents the capacitor from charging. As long as the reset voltage is applied, the digital output level will remain unchanged i.e. "low". The reset pin should be connected to $+V_{CC}$ when not used to avoid the possibility of false triggering.

ASTABLE (SELF-TRIGGERING) OPERATION

For astable (or self-triggering) operation, the correct circuit connection is shown in Figure 2. The external capacitor charges to 2/3 V_{CC} through the series combination of R_A and R_B, and discharges to 1/3 V_{CC} through R_B. In this manner, the capacitor voltage oscillates between 1/3 V_{CC} and 2/3 V_{CC}, with an exponential waveform. The output level at pin 5 (or 9) is high during the charging cycle, and goes low during the discharge cycle. The charge and the discharge times are independent of supply voltage. The oscillations can be keyed "on" and "off" using the reset controls (pin 4 or 10).

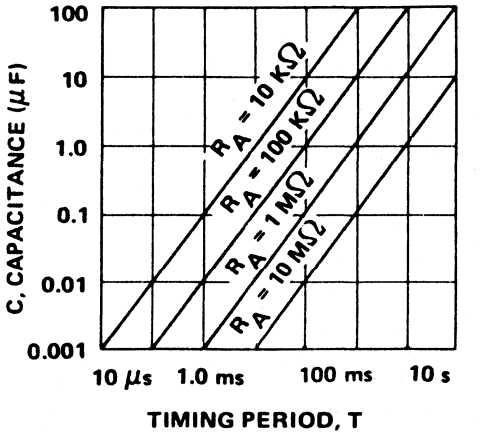


Figure 13. Timing Period, T, as a Function of External R-C Network

The charge time (output high) is given by:

$$t_1 = 0.695\ (R_A + R_B)C$$

The discharge time (output low) by:

$$t_2 = 0.695\ (R_B)C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.695\ ((R_A + 2R_B)C$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C} \text{ and}$$

may be easily found as shown in Figure 14.

The duty cycle D, is given by:

$$D = \frac{R_B}{R_A + 2R_B}$$

APPLICATIONS INFORMATION

INDEPENDENT TIME DELAYS

Each timer section of the XR-L556 can operate as an independent timer to generate a time delay, T, set by the respective external timing components. Figure 15 is a circuit connection where each section is used separately in the monostable mode to produce respective time delays of T_1 and T_2, where:

$$T_1 = 1.1\ R_1C_1 \text{ and } T_2 = 1.1\ R_2C_2$$

SEQUENTIAL TIMING (DELAYED ONE-SHOT)

In this application, the output of one timer section (Timer 1) is capacitively coupled to the trigger terminal of the second, as shown in Figure 16. When Timer 1 is triggered at pin 6, its output at pin 5 goes "high" for a time duration $T_1 = 1.1\ R_1C_1$. At the end of this timing cycle, pin 5 goes "low" and triggers Timer 2 through the capacitive coupling, C_C, between pins 5 thru 8. Then, the output at pin 9 goes "high" for a time duration

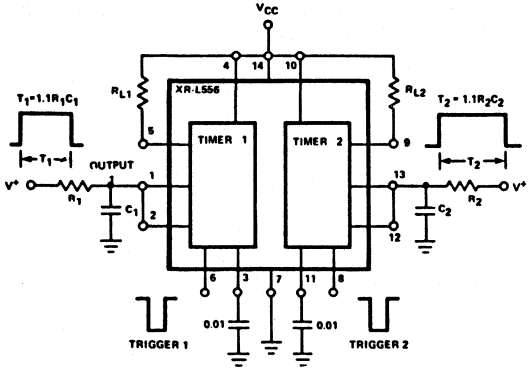


Figure 15. Generation of Two Independent Time Delays

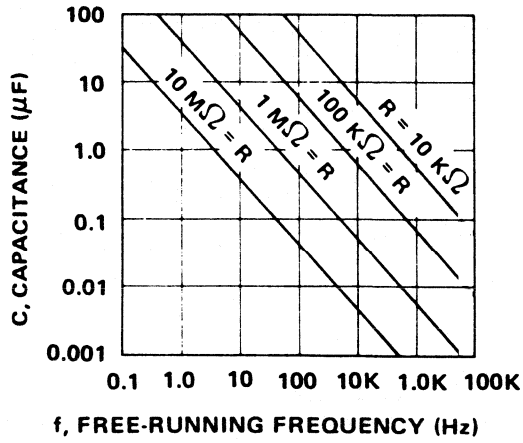


Figure 14. Free Running Frequency as a Functionof External Timing Components (Note: R = R_A + 2R_B)

$T_2 = 1.1\ R_2C_2$. In this manner, the unit behaves as a "delayed one-shot" where the output of Timer 2 is delayed from the initial trigger at pin 6 by a time delay of T_1

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KEYED OSCILLATOR

One of the timer sections of the XR-L556 can be operated in its free-running mode, and the other timer section can be used to key it "on" and "off". A recommended circuit connection is shown in Figure 17. Timer 2 is used as the oscillator section, and its frequency is set by the resistors R_A, R_B and the capacitor C_2. Timer 1 is operated as a monostable circuit, and its output is connected to the reset terminal (pin 10 of Timer 2).

When the circuit is at rest, the logic level at the output of Timer 1 is "low"; and the oscillations of Timer 2 are inhibited. Upon application of a trigger signal to Timer 1, the logic level at pin 1 goes "high" and the oscillator section (Timer 2) is keyed "on". Thus, the output of Timer 2 appears as a tone burst whose frequency is set by R_A, R_B and C_2, and whose duration is set by R_1 and C_1 of Figure 17.

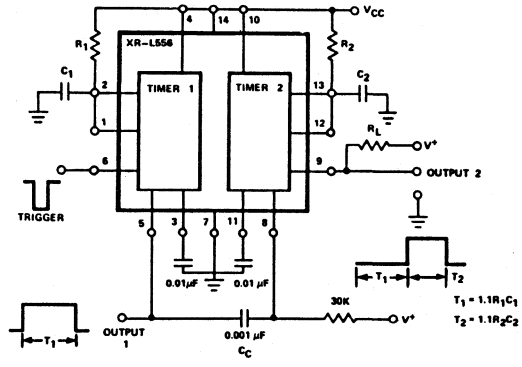


Figure 16. Sequential Timing

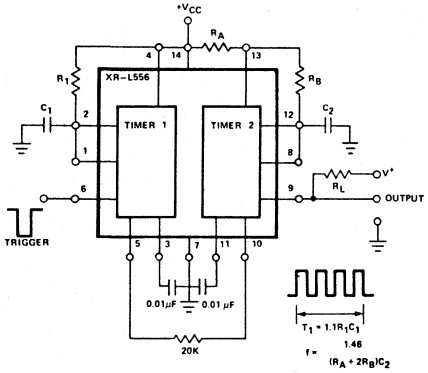


Figure 17. Keyed Oscillator

FREQUENCY DIVIDER AND PULSE SHAPER

If the frequency of the input is known, each timer section of the XR-L556 can be used as a frequency divider by adjusting the length of its timing cycle. If the timing interval T_1 (= 1.1 R_1C_1) is larger than the period of the input pulse trigger, then only those input pulses which are spaced more than 1.1 R_1C_1 will actually trigger the circuit.

The output frequency is equal to (1/N) times the input frequency. The division factor N is in the range:

$$\frac{T}{T_P} - 1 < N < \frac{T}{T_P}$$

where T_P is the period of the input pulse signal.

Since the two timer sections of the XR-L556 are electrically independent, each can be used as a frequency divider. Thus, if the trigger terminals of both timer sections are connected to a common input, the XR-L556 can produce two independent outputs at frequencies f_1 and f_2:

$$f_1 = f_2/N_1 \text{ and } f_2 = f_2 = f_S/N_2$$

Where N_1 and N_2 are the division factors for respective timer sections, set by external resistors and capacitors at pins (1, 2) and (12, 13).

Frequency division can be performed by 1/2 of the XR-L556. The remaining timer section can be used as a "pulse-shaper" to adjust the duty cycle of the output waveform. As seen in Figure 18, Timer 1 is used as the frequency divider section and Timer 2 is used as the pulse shaper.

The output of Timer 1 (pin 5) triggers Timer 2, which produces an output pulse whose frequency is the same as the output frequency of Timer 1, and whose duty cycle is controlled by the timing resistor and capacitor of Timer 2. The duty cycle of the output of Timer 2 (pin 9) can be adjusted from 1% to 99% by varying the value of R_2.

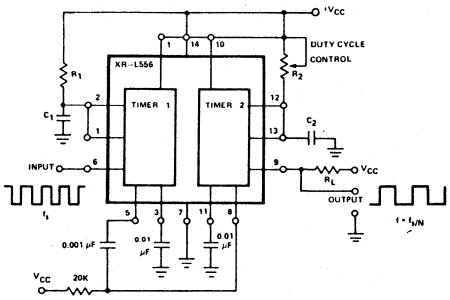


Figure 18. Frequency Divider and Pulse-Shaper

MICROPOWER OSCILLATOR WITH INDEPENDENT FREQUENCY AND DUTY CYCLE ADJUSTMENT

If Timer 1 is operated in its astable mode and Timer 2 is operated in its monostable mode, as shown in Figure 19, then an oscillator with fixed frequency and variable duty cycle results.

Timer 1 generates a basic periodic waveform that is then used to trigger Timer 2. If the time delay, T_2, of Timer 2 is chosen to be less than the period of oscillations of Timer 1, then the output at pin 9 has the same frequency as Timer 1, but has its duty cycle determined by the timing cycle of Timer 2. The output duty cycle can be adjusted over a wide range (from 1% to 99%) by adjusting R_2.

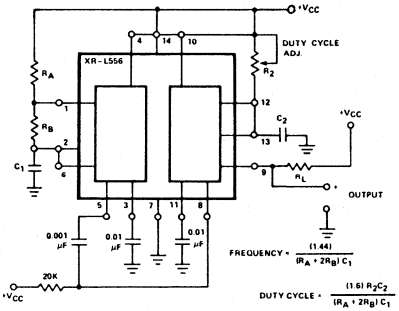
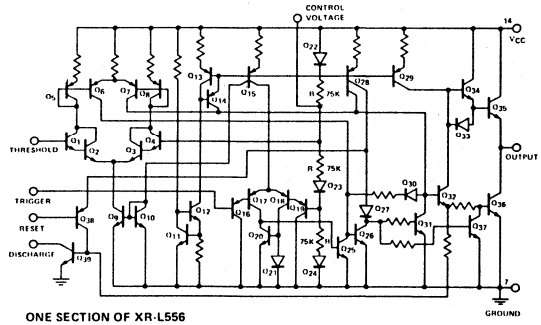


Figure 19. Micropower Oscillator with Fixed Frequency and Variable Duty-Cycle



EQUIVALENT SCHEMATIC DIAGRAM

Low Power JFET-Input Operational Diagram

General Description

The XR-062 low-power JFET-input operational amplifer is designed for low power consumption applications where high slew rate, low input bias and offset currents, and high input impedance are required. The XR-062 JFET input op amp is fabricated using ion-implanted bipolar JFET technology which combines well matched JFETs and high performance bipolar transistors on the same monolithic intergrated circuit.

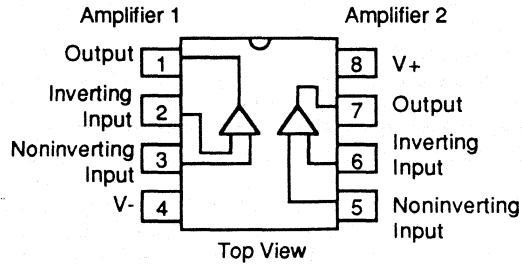
Features

Direct Replacement for TL062A/M
Low Power Dissipation-6mW/device
High-Impedance JFET Input Stage
Low Input Bias and Offset I's
High Slew Rate 3.5V/usec Typ.
Output Short-Circuit Protection
Latch-up-Free Operation
Internal Frequency Compensation

Applications

Instrumentation Amplifiers
Transimpedance Amplifiers
Buffer Amplifiers
Active Filters
Analog Computers
Microphone Preamplifier
Low Power Audio
Hearing Aids

Functional Block Diagram



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Ordering Information

Part Number	Package	Temperature
XR-062CD	JEDEC	0°C to 70°C
XR-062ACD	JEDEC	0°C to 70°C
XR-062BCD	JEDEC	0°C to 70°C
XR-062CP	Plastic	0°C to 70°C
XR-062ACP	Plastic	0°C to 70°C
XR-062BCP	Plastic	0°C to 70°C
XR-062CN	Ceramic	0°C to 70°C
XR-062MN	Ceramic	0°C to 70°C

Absolute Maximum Ratings

Supply Voltage	+/-18V
Differential I/P V	+/-30V
Input Voltage Range (Note 1)	+/-15V
O/P S.C. Duration (Note 2)	Indef.
Package Power Dissipation:	
Plastic Package	625mW
Derate Above Ta=+25°C	5mW/C
Ceramic Package	750mW
Derate Above Ta=+25°C	8mW/C
Storage Temp. Range	-65°C to +150°C

Single Supply Optimized Dual Operational Amplifiers

GENERAL DESCRIPTION

The XR-34072 family is a set of dual operational amplifiers for applications requiring fast slew rate (10V/µs typical) and fast settling time 1µS. The unity gain bandwidth of the XR-34072 is guaranteed to be greater than 3.5 MHz (at 25°C) and is typically 4.5 MHz. The XR-34072 family is in the industry standard dual operational amplifier configuration, allowing an upgrade to be performed in most established circuits.

The XR-34072 is a direct replacement for the MOTOROLA MC34072C. The XR-34072 marked with a white dot (JDEC SOIC package) is a direct replacement for the MC34072A.

The output structure of the XR-34072 allows the output to approach the VEE rail to within 0.3V. On the positive side, the output would be 1V below VCC. The XR-34072 family is fabricated in bipolar technology which provides the low input offset voltage characteristics and can operate with supplies up to 44 VDC single supply (± 22VDC dual supply).

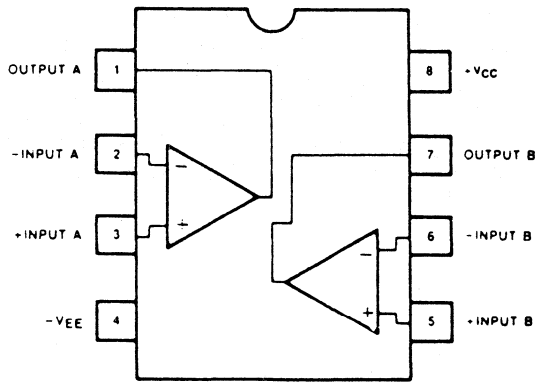
FEATURES

Wide Bandwidth: 4.5 MHz typical
High Slew Rate: 10V/µs typical
Wide Supply Voltage Operation: up to 44VDC single supply
Low Input Offset Voltage: 3.0 mV maximum with an A grade
Input Common Mode Voltage Range includes VEE
Low Total Harmonic Distortion
Direct Replacement for MC34072 and MC34072A

APPLICATIONS

Tape Head Amplifiers and Filters for Digital Signals
Output Stage for System Interface
Sampled Data Filters
Matched Component Applications (Stereo)
Battery Operated Amplifiers

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Power Supply V_{CC} Relative to V_{EE}	44 VDC
Power Dissipation (Package Limitation)	
Ceramic Package	500 mW
Derate above 25°C	5mW/°C
Plastic Package	450 mW
Derate above 25°C	7 mW/°C
Plastic JEDEC SOIC	300 mW
Derate above 25°C	5 mW/°C
Storage Temperature	-55°C to +150 °C
Input Common Mode Range (VEE-0.3).to (Vcc-0.3)V*	

*Note: Output phase reversal will occur with above input voltage range

ORDERING INFORMATION

XR-34072CP	Plastic	0°C to 70°C
XR-34072CN	Ceramic	0°C to 70°C
XR-34072CD	JEDEC SO	0°C to 70°C
XR-34072ACP	Plastic	0°C to 70°C
XR-34072ACN	Ceramic	0°C to 70°C
XR-34072ACD (White Dot)	JEDEC SO	0°C to 70°C

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +15 V_{DC} V_{EE} = -15 V_{DC}, R_{LOAD} = 2 kΩ, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	XR-34072A			XR-34072			UNITS	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO}	Input Offset		1.0	3.0		2.0	5.0	mV	
	Voltage		1.0	3.0		2.0	5.0		VCC = +5VDC VEE = 0VDC
I_{IB}	Input Bias Current		100	500		100	500	nA	
I_{IO}	Input Offset Current		6.0	50		6.0	75	nA	
A_{VOL}	Large Signal Voltage	50	100		25	100		V/mV	V_{OUT} = ± 10V
V_{OH}	Output Voltage Swing	3.7	4.0		3.7	4.0		V	V_{CC} = +5VDC V_{EE} = 0VDC
		13.6	14.0		13.6	14.0		V	R_L = 10 kΩ
V_{OL}	Output Voltage Swing		0.1	0.3		0.1	0.3	V	V_{CC} = 5VDC V_{EE} = 0VDC
			-14.7	-14.3		-14.7	-14.3	V	R_L = 10 kΩ
I_{SC}	Output Short Circuit	10	30		10	30		mA	Source, V_{IN}= 1V
	Current	20	30		20	30		mA	Sink, V_{IN} = -1V
CMRR	Common Mode Rejection Ratio	80	97		70	97		dB	V_{OUT} = 0, 10V
PSRR	Power Supply Rejection Ratio	80	97		70	97		dB	5V≤V_{CC} ≤15V -5V> V_{EE}> -15V
I_{CC}	Power Supply Current Per Amplifier		1.6	2.0		1.6	2.0	mA	V_{CC} = +5VDC V_{EE} = 0VDC No Load
			1.9	2.5		1.9	2.5	mA	No Load
*These parameters, although guaranteed over the recommended operating conditions, are not 100% tested.									
V_{IO}	Input Offset Voltage			5.0			7.0		T_A =0°C to 70°C
$V_{IO/\Delta t}$	Change in Input Offset Voltage over Temperature		10			10		µV/°C	T_A =0°C to 70°C
I_{IB}	Input Bias Current			700			700	nA	T_A=0°C to 70°C
I_{IO}	Input Offset Current			300			300	nA	T_A=0°C to 70°C
A_{VOL}	Large Signal Voltage	25			20			V/mV	T_A=0°C to 70°C
V_{OH}	Output Voltage Swing	13.4			13.4			V	T_A=0°C to 70°C
V_{OL}	Output Voltage Swing			-13.5			-13.5	V	T_A=0°C to 70°C
I_{CC}	Power Supply Current			2.8			2.8	mA	T_A =0°C to 70°C
AC ELECTRICAL CHARACTERISTICS									
SR	Slew Rate	8.0	10		8.0	10		V/µs	C_L=500pF, A_V =+1
			13			13		V/µs	C_L =500pF, A_V =-1
ts	Settling Time		1.1			1.1		µs	A_V=-1, 10 V step to 0.1%
			2.2			2.2		µs	A_V=-1, 10 V step to 0.01%
GBW	Gain Bandwidth Product	3.5	4.5		3.5	4.5		MHz	f_{IN}=100 kHz
e_n	Equivalent Input Noise		32			32		nv/√Hz	f = 1 kHz

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SYSTEM DESCRIPTION

The XR-34072 with its low input offset voltage, wide bandwidth, and high slew rate can be used in high gain applications where otherwise the resulting output offset voltage would be too large. The wide bandwidth characteristics of the dual operational amplifier allow it to be used in active filter applications where a single XR-34072 and some external passive components can be used to construct a fourth order filter to 450 kHz or higher if filter Q is less than 10.

PRINCIPLES OF OPERATION

The XR-34072 common mode range is achieved by its input stage. The PNP transistors Q12 and Q13 have their collectors tied directly to V_{EE} rather than to a current source. This prevents the collector base forward biasing that can occur with other input structures, where the collector of the input transistor is biased at a point approximately 1 V above V_{EE}.

The output stage does not use a complimentary pair which many times has substantial distortion. Instead, an inverter stage Q10 provides the reversed signal for the collector of Q11, the output drive transistor. Resistor R13 is for short circuit current limiting.

MARKING DESCRIPTION

The XR-34072 family of dual operational amplifiers are separated by maximum guaranteed input offset voltages. Due to the size of the 8 pin JEDEC SOIC package, a white dot is used instead of letters to denote the A grade. The XR-34072 with no dot notes a maximum input offset voltage of 5 mV maximum. The XR-34072 marked with a white dot notes a maximum input offset voltage of 3.0 mV. Other parameters also are different between the two grades and the electrical characteristics portion of the datasheet should be used as a guide.

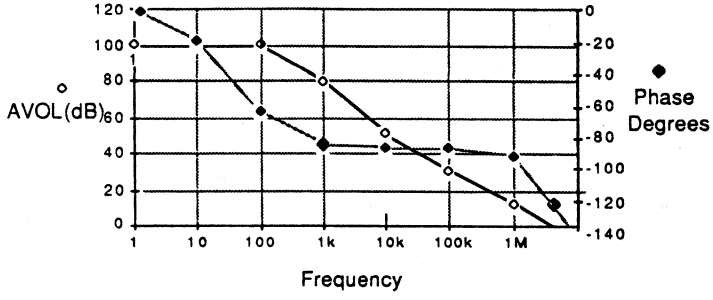


Figure 1. Open Loop Gain and Phase Response

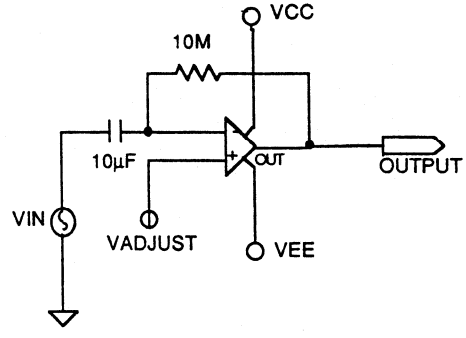
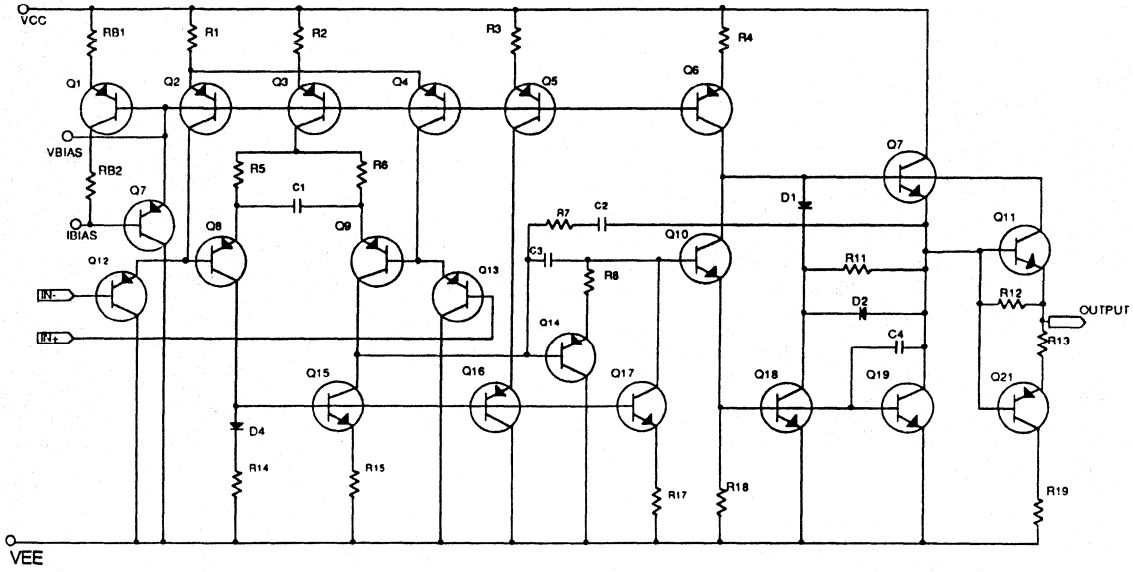


Figure 2. Test Circuit for Open Loop Gain and Phase Characteristics



Equivalent Schematic Diagram Each Op Amp of XR-34072

Quad High Performance Operational Amplifier

GENERAL DESCRIPTION

The XR-34074 and XR-34074A each contain 4 wide bandwidth, high slew rate operational amplifiers. The 13V/µs slew rate and 4.5 MHz gain-bandwidth product makes the XR-34074 ideal for pulsed signal applications where the accuracy of tracking the signal is of extreme importance. Although the XR-34074 and XR-34074A can be used in a split supply operation, their common mode input voltage includes VEE, allowing the device to be used in single supply applications without the degradation seen with typical operational amplifiers. The XR-34074A provides lower input offset voltages and a guaranteed minimum slew rate, and gain bandwidth product. These characteristics allow the use of the XR-34074A in applications where high gain and wide bandwidth is needed. In applications where low level signals need to be amplified by a large amount the XR-34074A is the device to use. Both devices are available in a 14-pin Plastic or Ceramic DIP as well as 14 pin JEDEC SO (SO-14) packages.

FEATURES

Wide Bandwidth: 4.5 MHz bandwidth, typical
High Slew Rate: 13V/µs, typical
Wide supply operating range: single supply operation up to 44 VDC
Low input offset voltage: 4.5mV/2mV for XR-34074/A
Large output voltage swing: within 1 V of supply rails
Large Capacitance drive Capability: up to 10 nF

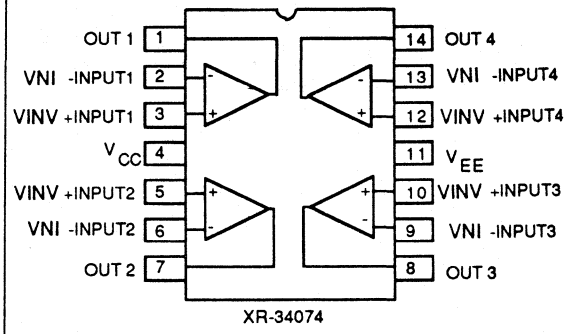
APPLICATIONS

Tape Head amplifiers and filters for digital signals
Output stage for system interface
Sampled Data Filters
Matched Component Applications (Stereo or Quadrophonic)

ABSOLUTE MAXIMUM RATINGS

Power Supply (V_{CC}-V_{EE})	44 V_{DC}
Power Dissipation (**Package Limitation**)	
Ceramic Package	750 mW
Derate above 25°C	5 mW/°C
Plastic Package	600 mW
Derate above 25°C	5 mW/°C
Storage Temperature	-65°C to +150°C
Input Common Mode Voltage Range	V_{EE} to (V_{CC} -1.8)V

PIN ASSIGNMENT



XR-34074

ORDERING INFORMATION

Part no.	Package	Operating Temp.
XR-34074 ACP	Plastic	0°C to 70°C
XR-34074ACN	Ceramic	0°C to 70°C
XR-34074CP	Plastic	0°C to 70°C
XR-34074CN	Ceramic	0°C to 70°C
XR-34074CD	Surface Mount	0°C to 70°C
XR-34074ACD	Surface Mount	0°C to 70°C

SYSTEM DESCRIPTION

The quad high performance XR-34074 and XR-34074A is an ideal replacement to designs using Norton Amplifiers (generally single supply applications). Its capacitance drive capability allows it to be used in continuous time filter applications with no problem with stability. The XR-34074 and XR-34074A has fast settling time (typically 0.1% in 1µs.) With its industry standard pin configuration the device also allows for a quick upgrade of circuits using older operational amplifier designs such as the LM747 or LM3900.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +15 V_{DC}, V_{EE} = -15 V_{DC}, R_{LOAD} = 2KΩ, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETERS	XR-34074A			XR-34074			UNIT	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO}	Input Offset Voltage		0.5	2.0		2.0	4.5	mV	
			0.5	2.5		2.5	5.0	mV	V_{CC} = +5V_{DC}, V_{EE} = 0V_{DC}
				4.0			6.5	mV	T_A = 0°C to 70°C ±15V
$V_{IO}/\Delta T$	Temperature Coefficient of Input Offset Voltage		10			10		µV/C	T_A = 0°C to 70°C
I_{IB}	Input Bias Current		200	500		200	500	nA	
				700			700	nA	T_A = 0°C to 70°C
I_{IO}	Input Offset Current		6.0	50		6.0	75	nA	
				300			300	nA	T_A = 0°C to 70°C
A_{VOL}	Large Signal Voltage Gain	50	100		25	100		V/mV	V_{OUT} =+/- 10V_{DC}
V_{OH}	Output Voltage Swing	3.7	4.0		3.7	4.0		V	V_{CC} = 5V_{DC}, V_{EE} = 0 V_{DC}
		13.7	14		13.7	14		V	R_{LOAD} = 10KΩ
		13.5			13.5			V	T_A = 0°C to 70°C
V_{OL}	Output Voltage Swing		-14.7	-14.4		-14.7	-14.4	V	R_{LOAD} = 10KΩ
				-13.8			-13.8	V	T_A = 0°C to 70°C
I_{SC}	Short Circuit Current								
	Source	10	30		10	30		mA	Output to ground
	Sink	20	47		20	47		mA	
C_{MRR}	Common Mode Rejection Ratio	80	97		70	97		dB	RS ≤ 10KΩ V_{IN}=0° to 10V_{DC}
P_{SRR}	Power Supply Rejection Ratio	80	97		70	97		dB	V Supply=±5V ±15V RS ≤ 100 ohms
I_{CC}	Power Supply Current		6.5	8.0		6.5	8.0	mA	V_{CC} = 5V_{DC}, V_{EE} = 0 V_{DC}
			7.5	10		7.5	10	mA	
				11			11	mA	T_A = 0°C to 70 °C

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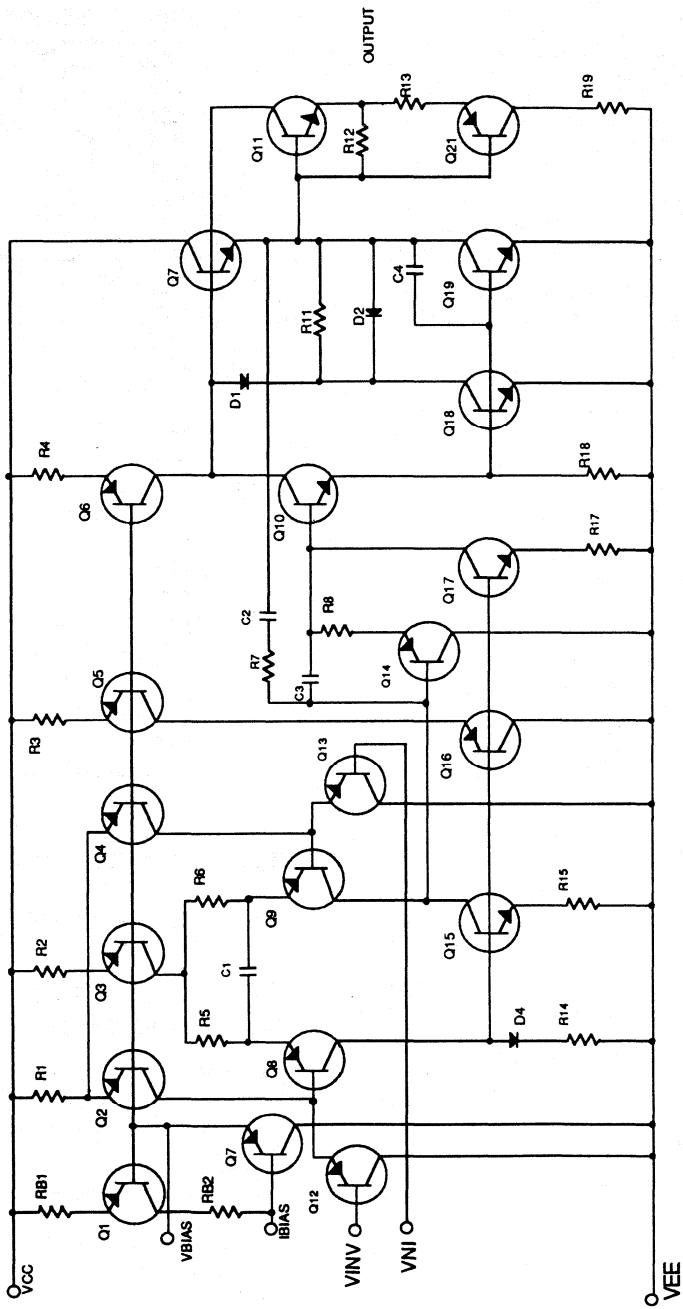
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	XR-34074A			XR-34074			UNITS	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
SR	Slew Rate	8.0	10			10		V/µs	Voltage follower configuration
			13			13		V/µs	Inverting and unity gain
t_S	Setting Time		1.1			1.1		µs	10V step to 0.10% Inverting and unity gain
			2.2			2.2		µs	10V step to 0.01% Inverting and unity gain
GPW	Gain Bandwidth Products	3.5	4.5			4.5		MHz	measured at 100kHz
en	Equivalent Input Noise		32			32		nv/$\sqrt{Hz}$	RS =100Ω, f = 1 kHz

PRINCIPLES OF OPERATION

The XR-34074 wide input common mode range is achieved by its input stage. The PNP transistors Q12 and Q13 have their collectors tied directly to V_{EE} rather than to a current source. This prevents the collector base forward biasing that can occur with other input structures, where the collector of the input transistor is biased at a point approximately 1V above V_{EE}.

The output stage does not use a complimentary pair which many times has substantial distortion. Instead, an inverter stage Q10 provides the reversed signal for the collector of Q11, the output drive transistor. Resistor R13 is for short circuit current limiting. For additional information on the operation of operational amplifiers, the book "Analysis and Design of Analog Integrated Circuit", by Paul R. Gray and Robert G. Meyer is recommended. The publisher is Wiley.



Equivalent Schematic Diagram Each Op Amp of XR-34074

Programmable Quad Operational Amplifiers

GENERAL DESCRIPTION

The XR-146 family of quad operational amplifiers contain four independent high-gain, low-power, programmable op-amps on a monolithic chip. The use of external bias setting resistors permit the user to program gain-bandwidth product, supply current, input bias current, input offset current, input noise and the slew rate.

The basic XR-146 family of circuits offer partitioned programming of the internal op-amps where one setting resistor is used to set the bias levels in the three op-amps, and a second bias setting is used for the remaining op-amp. Its modified version, the XR-346-2 provides a separate bias setting resistor for each of the two op-amp pairs.

FEATURES

Programmable
Micropower operation
Low noise
Wide power supply range
Class AB output
Ideal pin out for biquad active filters
Overload protection for input and output
Internal frequency compensation

APPLICATIONS

Total Supply Current = 1.4 mA (I_{SET}/10 μA)
Gain Bandwidth Product = 1 MHz (I_{SET}/10μA)
Slew Rate = 0.4V/μs (I_{SET}/10 μA)
Input Bias Current $\cong$50 nA (I_{SET}/10 μA)

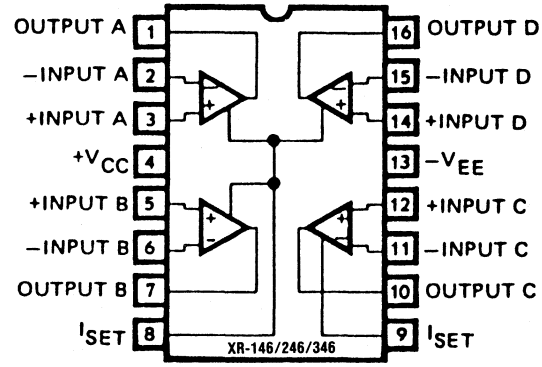
I_{SET} = Current into pin 8, pin 9 (see schematic)

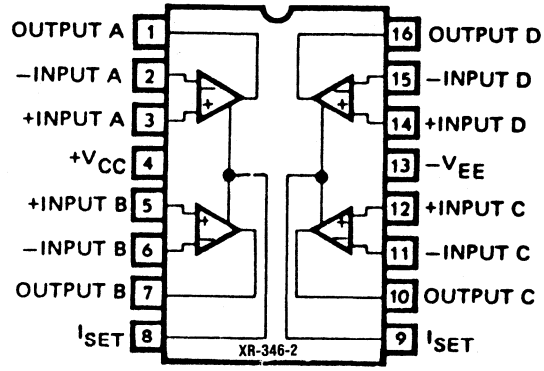
$$I_{SET} = \frac{V+ - V- - 0.6V}{R_{SET}}$$

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
XR-146	±22V
XR-246/346	±18V
Differential Input Voltage (Note 1)	
XR-146/246/346	±30V
Common Mode Input Voltage (Note 1)	
XR-146/246/346	±15V
Power Dissipation (Note 2) (Package Limitation)	
XR-146CN	900 mW
XR-246/346CN	500 mW
Output Short Circuit Duration (Note 3)	
XR-146/246/346	Indefinite
Maximum Junction Temperature	
XR146	150°C
XR-246	110°C
XR-346	100°C

FUNCTIONAL BLOCK DIAGRAMS





ABSOLUTE MAXIMUM RATINGS (continued)

Storage Temperature Range	
XR-146/246/346	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-146M	Ceramic	−55°C to +125°C
XR-246N	Ceramic	−25°C to +85°C
XR-246P	Plastic	−25°C to +85°C
XR-346/ 346-2CN	Ceramic	0°C to +70°C
XR-346/ 346-2CP	Plastic	0°C to +70°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_S = ±15V, I_{SET} = 10 μA)

PARAMETERS	XR-146			XR-246/346			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
Input Offset Voltage		0.5	5		0.5	6	mV	V_{CM} = 0V, $R_S \leq 50\Omega$
Input Offset Current		2	20		2	100	nA	V_{CM} = 0V
Input Bias Current		50	100		50	250	nA	V_{CM} = 0V
Supply Current (4 Op-Amps)		1.4	2.0		1.4	2.5	mA	
Large Signal Voltage Gain	100	1000		50	1000		V/mV	R_L = 10 kΩ, ΔV_{OUT} = ±10V
Input CM Range	±13.5	±14		±13.5	±14		V	
CM Rejection Ratio	80	100		70	100		dB	$R_S \leq 10$ kΩ
Power Supply Rejection Ratio	80	100		74	100		dB	$R_S \leq 10$ kΩ
Output Voltage Swing	±12	±14		±12	±14		V	$R_L \leq 10$ kΩ
Short-Circuit Current	5	20	30	5	20	30	mA	
Gain Bandwidth Product	0.8	1.2		0.5	1.2		MHz	
Phase Margin		60			60		Deg	
Slew Rate		0.4			0.4		V/μs	
Input Noise Voltage		28			28		nV/√Hz	f = 1 kHz
Channel Separation		120			120		dB	R_L = 10 kΩ, ΔV_{OUT} = 0V to +12V
Input Resistance		1.0			1.0		MΩ	
Input Capacitance		2.0			2.0		pF	

The following specifications apply over the maximum operating temperature range, for the XR-246 and the XR-346 the specifications are not tested in production.

Input Offset Voltage		0.5	6		0.5	7.5	mV	V_{CM} = 0V, $R_S \leq 50\Omega$
Input Offset Current		2	25		2	100	nA	V_{CM} = 0V
Input Bias Current		50	100		50	250	nA	V_{CM} = 0V
Supply Current (4 Op-Amps)		1.5	2.0		1.5	2.5	mA	
Large Signal Voltage Gain	50	1000		25	1000		V/mV	R_L = 10 kΩ, ΔV_{OUT} = ±10V
Input CM Range	±13.5	±14		±13.5	±14		V	
CM Rejection Ratio	70	100		70	100		dB	$R_S \leq 50\Omega$
Power Supply Rejection Ratio	76	100		74	100		dB	$R_S \leq 50\Omega$
Output Voltage Swing	±12	±14		±12	±14		V	$R_L \geq 10$ kΩ

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±15V, I_{SET} = 1 μA)

Input Offset Voltage		0.5	5		0.5	6	mV	V_{CM} = 0V, $R_S \leq 50\Omega$
Input Bias Current		7.5	20		7.5	100	nA	V_{CM} = 0V
Supply Current (4 Op-Amps)		140	250		140	300	μA	
Gain Bandwidth Product	80	100		50	100		kHz	

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_S = ±1.5V, I_{SET} = 10 μA)

Input Offset Voltage		0.5	5		0.5	7	mV	V_{CM} = 0V, $R_S \leq 50\Omega$
Input CM Range	±0.7			±0.7			V	
CM Rejection Ratio		80			80		dB	$R_S \leq 50\Omega$
Output Voltage Swing	±0.6			±0.6			V	$R_L \geq 10\ k\Omega$

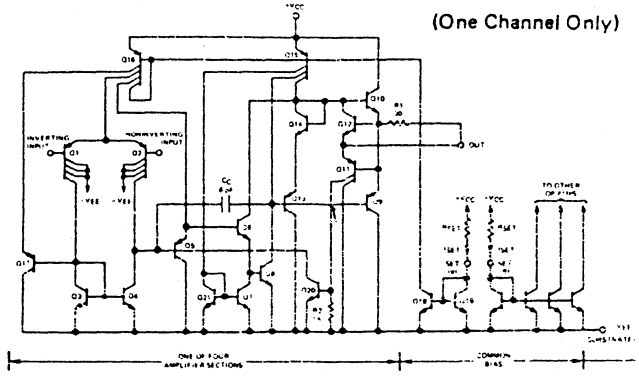
Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θjA, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta jA$ or the 25°C P_{dMAX}, whichever is less.

Note 3: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should be simultaneously shorted as the maximum junction temperature will be exceeded.

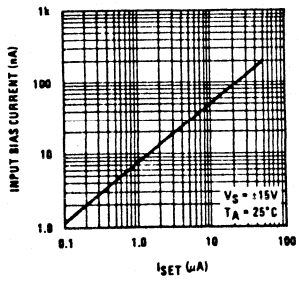
EQUIVALENT SCHEMATIC DIAGRAM

(One Channel Only)

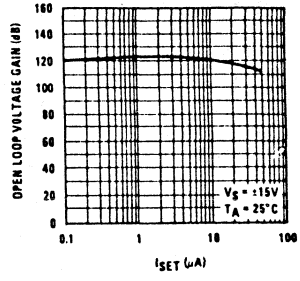


TYPICAL PERFORMANCE CHARACTERISTICS

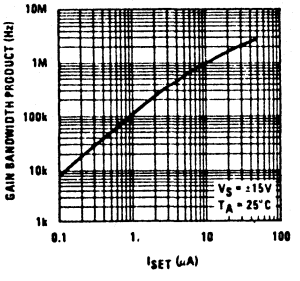
Input Bias Current vs I_{SET}



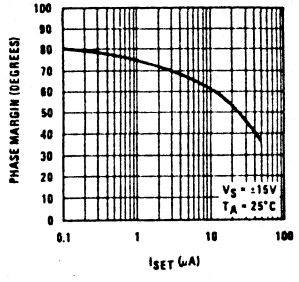
Open Loop Voltage Gain vs I_{SET}



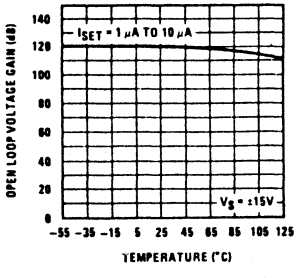
Gain Bandwidth Product vs I_{SET}



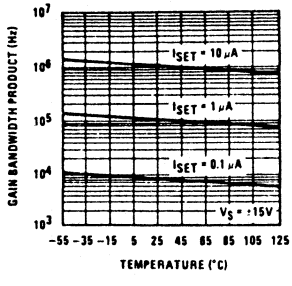
Phase Margin vs I_{SET}



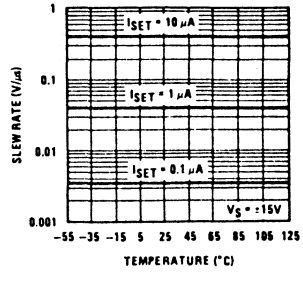
Open Loop Voltage Gain vs Temperature



Gain Bandwidth Product vs Temperature

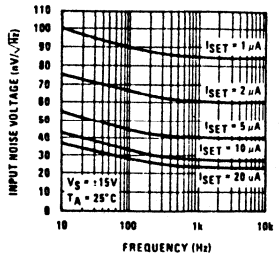


Slew Rate vs Temperature

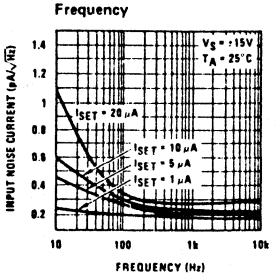


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

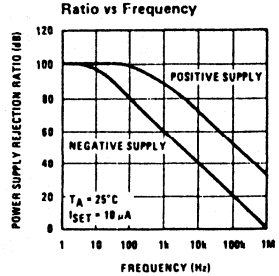
Input Noise Voltage vs Frequency



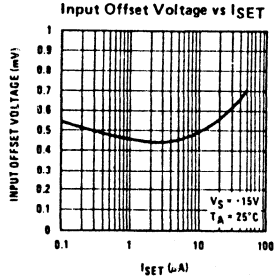
Input Noise Current vs Frequency



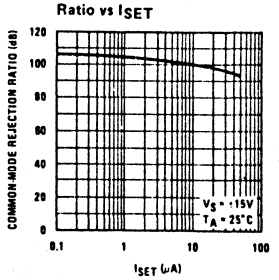
Power Supply Rejection Ratio vs Frequency



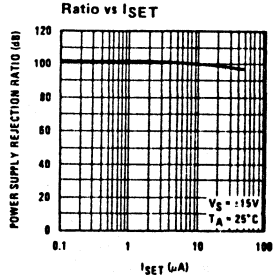
Input Offset Voltage vs I_{SET}



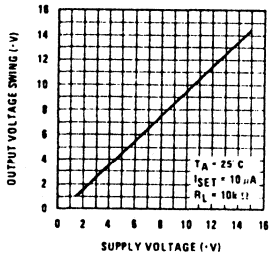
Common-Mode Rejection Ratio vs I_{SET}



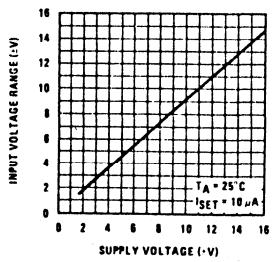
Power Supply Rejection Ratio vs I_{SET}



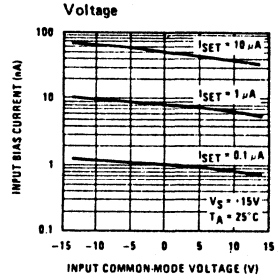
Output Voltage Swing vs Supply Voltage



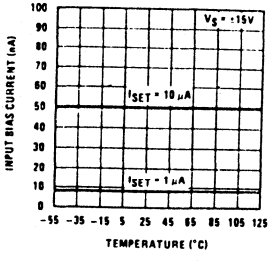
Input Voltage Range vs Supply Voltage



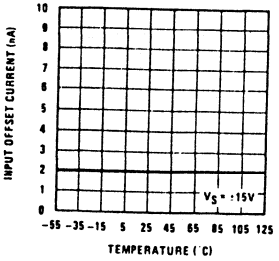
Input Bias Current vs Input Common-Mode Voltage



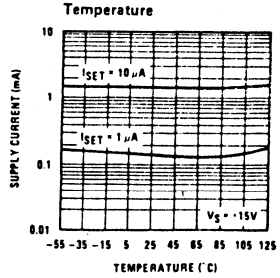
Input Bias Current vs Temperature



Input Offset Current vs Temperature



Supply Current vs Temperature



Quad Operational Amplifier

GENERAL DESCRIPTION

The XR-4136 is an array of four independent internally compensated operational amplifiers on a single silicon chip, each similar to the popular 741. Good thermal tracking and matched gain-bandwidth products make **these Quad Op-amps useful for active filter and signal conditioning applications.**

FEATURES

Direct Pin-for-Pin Replacement for RC4136 and RM4136
Output Short-Circuit Protection
Internal Frequency Compensation
No Latch-Up
Wide Common-Mode and Differential Voltage Ranges
Matched Gain-Bandwidth within a Package

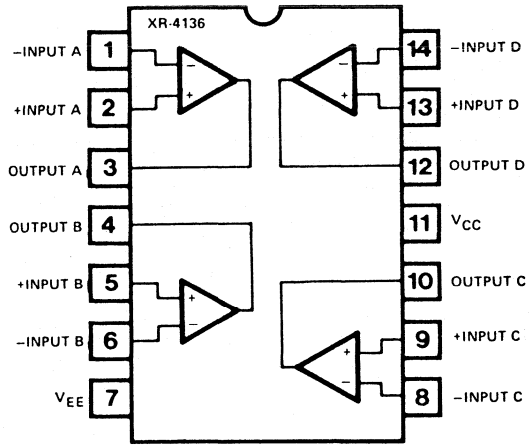
APPLICATIONS

Buffer Amplifiers
Summing/Differencing Amplifiers
Instrumentation Amplifiers
Active Filters
Signal Processing
Sample and Differencing
I to V Converters
Integrators
Simulated Components
Analog Computers; Neural Networks

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
XR-4136M	±22V
XR-4136C	±18V
Common Mode	
Voltage Range	V_{EE} to V_{CC}
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	±30V
Internal Power Dissipation	
Ceramic Package:	750 mW
Derate above T_A = +25°C	6 mW/°C
Plastic Package:	625 mW
Derate above T_A = +25°C	5 mW/°C
Storage Temperature Range:	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-4136M	Ceramic	−55°C to +125°C
XR-4136CN	Ceramic	0°C to +70°C
XR-4136CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-4136 is a quad operational amplifier featuring similar characteristics to standard 741-type devices. As all four are monolithic, they have matched characteristics, including thermal tracking and gain bandwidth products.

ELECTRICAL CHARACTERISTICS

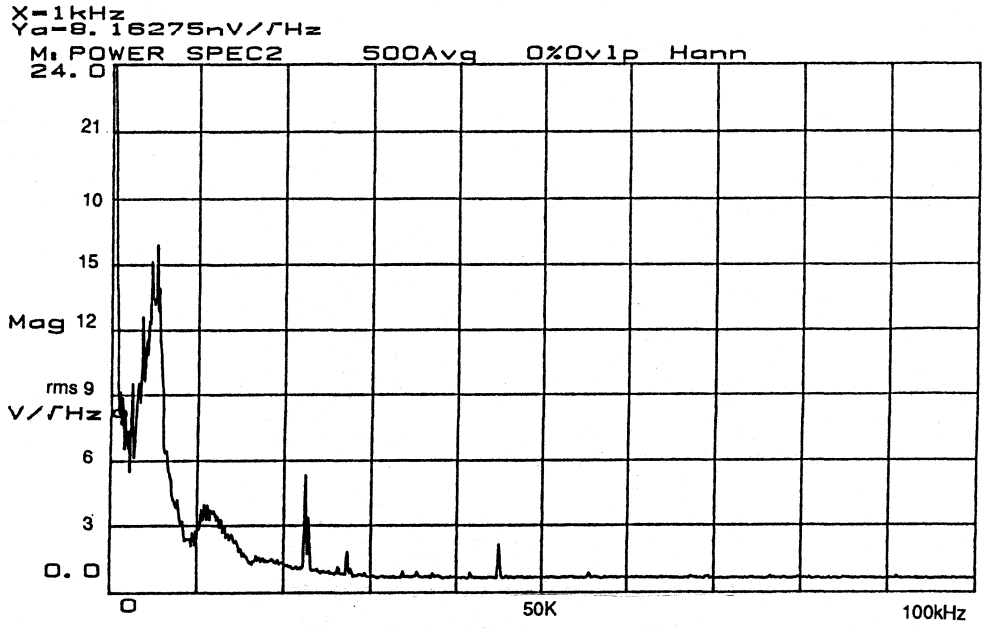
Test Conditions: $T_A = +25°C$, $V_S = \pm 15V$, unless otherwise specified.

SYMBOLS	PARAMETERS	XR4136M MIN	XR4136M TYP	XR4136M MAX	XR4136C MIN	XR4136C TYP	XR4136C MAX	UNITS	CONDITIONS
$\|V_{io}\|$	Input Offset Voltage		.5	5.0		.5	6.0	mV	$R_S \leq 10$ KΩ
$\|I_{io}\|$	Input Offset Current		5.0	200		5.0	200	nA	
$\|I_b\|$	Input Bias Current		40	500		40	500	nA	
R_{in}	Input Resistance	0.3	5.0		0.3	5.0		MΩ	
A_{VOL}	Large Signal Voltage Gain	50	300		20	300		V/mV	$R_L \geq 2$ KΩ $V_{out} = \pm 10V$
V_{out}	Output Voltage Swing	±12	±14		±12	±14		V	$R_L \geq 10$ KΩ
V_{out}		±10	±13		±10	±13		V	$R_L \geq 2$ KΩ
V_{iCM}	Input Voltage range	±12	±14.0		±12	±14.0		V	
CMRR	Common Mode Rejection Ratio	70	105		70	105		dB	$R_S \leq 10$ KΩ
PSRR	Supply Voltage Rejection Ratio		10	150		10	150	μV/V	$R_S \leq 10$ KΩ
P_i	Power Consumption		210	340		210	340	mW	
t_r t_o	Transient Response (unity gain) Risetime Overshoot		.13 5.0			.13 5.0		μs %	$V_{in} = 20$ mV $R_L = 2$ KΩ $C_L \leq 100$ pF
BW	Unity Gain Bandwidth	2.0	3.0			3.0		MHz	
dV_{out}/dt	Slew Rate (unity gain)		1.5			1		V/μs	$R_L \geq 2$ KΩ
	Channel Separation (open loop)		105			105		dB	f = 10 KHz $R_S = 1$ KΩ
	(Gain of 100)		105			105		dB	f = 10 KHz $R_S = 1$ KΩ
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for XR-4136M: $0°C \leq T_A \leq +70°C$ for XR-4136C									
$\|V_{io}\|$	Input Offset Voltage			6.0			7.5	mV	$R_S \leq 10$ KΩ
$\|I_{io}\|$	Input Offset Current			500			300	nA	
I_b	Input Bias Current			1500			800	nA	
A_{VOL}	Large-Signal Voltage Gain	25			15			V/mV	$R_L \geq 2$ KΩ $V_{out} = \pm 10V$
V_{out}	Output Voltage Swing	±10			±10			V	$R_L \geq 2$ KΩ
P_i P_i	Power Consumption		180 240	300 400		100 240	300 400	mW mW	$V_S = \pm 15V$ T_A = High T_A = Low
I_{SC}	Output Short-Circuit Current		45			45		mA	

TYPICAL PARAMETER MATCHING:

Test Conditions: $T_A = +25°C$, $V_S = \pm 15V$ unless otherwise noted

SYMBOLS	PARAMETERS	XR4136M TYP	XR4136C TYP	UNITS	CONDITIONS
$\|V_{io}\|$	Input Offset Voltage	±1.0	±2.0	mV	$R_S \geq 10$ KΩ
$\|I_{io}\|$	Input Offset Current	±7.5	±7.5	nA	
I_b	Input Bias Current	±15	±15	nA	
A_{VOL}	Voltage Gain	±0.5	±1.0	dB	$R_S \geq 2$ KΩ


X=1kHz
Ya=8.16275nV/√Hz
M1 POWER SPEC2
500Avg
0%Ovlp
Hann
24.0
21
10
15
Mag 12
rms 9
V/√Hz
6
3
0.0
0
50K
100kHz

Dual Low-Noise Operational Amplifier

GENERAL DESCRIPTION

The XR-5532 dual low-noise operational amplifier is especially designed for applications in high quality professional audio equipment. The low-noise, wide bandwidth and output drive capability make it ideally suited for instrumentation and control circuits as well as active filter design.

The XR-5532A is the specially screened version of the XR-5532, with guaranteed noise characteristics.

FEATURES

Pin for Pin Replacement for Signetics NE 5532
Wide Small-Signal Bandwidth: 10 MHz
High-Current Drive Capability
(10V rms into 600Ω at VS = ±18V)
High Slew Rate: 9 V/μs
Wind Power-Bandwidth: 140 kHz
Very Low Input Noise: 5 nV/√Hz
Wide Supply Range: ±3V to ±20V

APPLICATIONS

High Quality Audio Amplification
Telephone Channel Amplifier
Servo Control Systems
Low-Level Signal Detection
Active Filter Design

ABSOLUTE MAXIMUM RATINGS

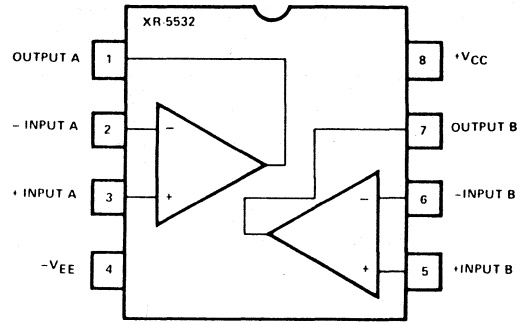
Power Supply	±22V
Input Common-Mode Range	$-V_{EE}$ to $+V_{CC}$
Differential Input Voltage (Note 1)	±0.5V
Power Dissipation (Package Limitation)	
Ceramic Package 8-Pin	600 mW
Derate Above TA = 25°C	8 mW/°C
Storage Temperature	−60°C to +150°C

Note 1: Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ± 10 mA.

Note 2: Output may be shorted to ground at $V_{CC} = |V_{EE}| =$ 15V, T_A = 25°C. Temperature and/or voltages must be limited to ensure dissipation rating is not exceeded.

Note 3: Operation near the absolute maximum ratings will exceed the power dissipation of the package.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-5532N	Ceramic	0°C to +70°C
XR-5532P	Plastic	0°C to +70°C
XR-5532AN	Ceramic	0°C to +70°C
XR-5532AP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-5532 and XR-5532A are dual monolithic operational amplifiers featuring low noise and very large gain bandwidth products. The devices have low output resistance and can drive 10 Vrms into 600Ω. Input noise is 100% tested on the XR-5532A, and is typically only 5 nV/√Hz. The small signal bandwidth is 10 MHz and slew rate exceeds 9 V/μS. Supply voltage may range from ± 3V to ± 18V.

XR-5532/5532A

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{CC} = $|V_{EE}|$ = 15V unless otherwise specified.

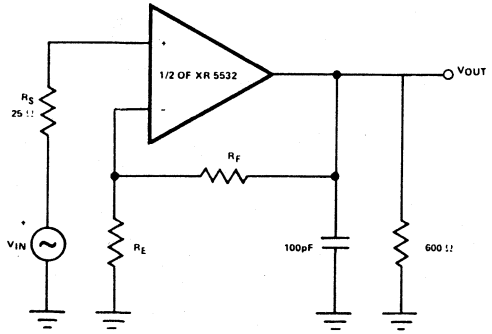
PARAMETERS	XR-5532A MIN	XR-5532A TYP	XR-5532A MAX	XR-5532 MIN	XR-5532 TYP	XR-5532 MAX	UNITS	SYMBOL	CONDITIONS
DC CHARACTERISTICS									
Input Offset Voltage		0.5	4 5		0.5	4 5	mV mV	V_{OS}	T_A = 25°C T_T = Full Range *
Input Offset Current		10	150 200		10	150 200	nA nA	I_{OS}	T_A = 25°C T_T = Full Range *
Input Bias Current		200	800 1000		200	800 1000	nA nA	I_B	T_A = 25°C T_T = Full Range *
Large Signal Voltage Gain	25 15	100		25 15	100		V/mV V/mV	A_{VOL}	$R_L \geq 600\Omega$, $V_O = \pm 10V$ T_A = 25°C T_T = Full Range *
Supply Current		8	16		8	16	mA	I_{CC}	R_L = Open
Output Swing	±12 ±15	±13 ±16		±12 ±15	±13 ±16		V V	V_{OUT}	$R_L \geq 600\Omega$ $V_{CC} = V_{EE}$ = 15V $V_{CC} = V_{EE}$ = 18V
Output Short Circuit Current		38			38		mA	I_{SC}	(Note 2)
Input Resistance	30	300		30	300		kΩ	R_{IN}	
Common-Mode Range	±12	±13		±12	±13		V	V_{iCM}	
Common-Mode Rejection	70	100		70	100		dB	CMRR	
Power Supply Rejection		10	100		10	100	μV/V	PSRR	
Channel Separation		110			110		dB		f = 1 kHz, R_S = 5 KΩ
AC CHARACTERISTICS									
Transient Response Rise Time Overshoot		 20 10			 20 10		 nsec %	 t_r t_0	Voltage Follower R_L = 600Ω V_{IN} 100 MV_{pp}, C_L = 100 pF
AC Gain		2.2			2.2		V/mV		f = 10 kHz
Unity-Gain Bandwidth		10			10		MHz	BW	C_L = 100 pF
Slew Rate		9			9		V/μsec		
Power Bandwidth		140			140		kHz	f_p	$V_{OUT} = \pm 10V$ RL = 600Ω
Output Resistance		.3			.3		Ω	R_{OUT}	A_V = 30 dB Closed loop f = 10 kHz R_L = 600Ω
NOISE CHARACTERISTICS									
Input Noise Voltage		8 5	10 6		8 5		nV/√Hz nV/√Hz	e_n	f_0 = 30 Hz f_0 = 1 kHz
Input Noise Current		2.7 .7			2.7 .7		pA/√Hz pA/√Hz	i_n	f_0 = 30 Hz f_0 = 1 kHz

*These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

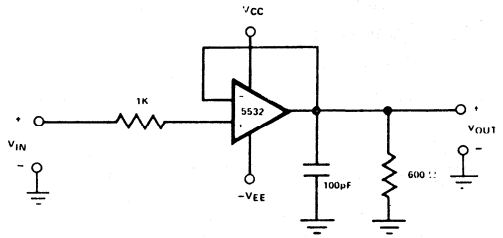
5

TEST CIRCUITS

CLOSED LOOP FREQUENCY RESPONSE

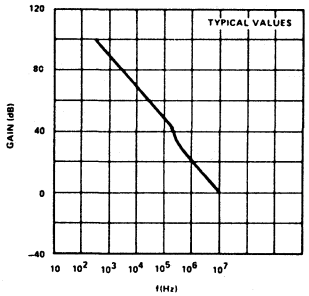


VOLTAGE FOLLOWER

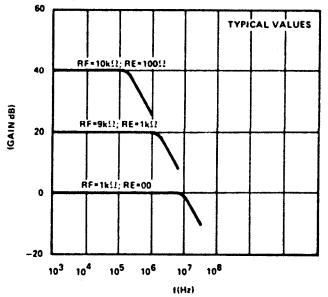


TYPICAL PERFORMANCE CHARACTERISTICS

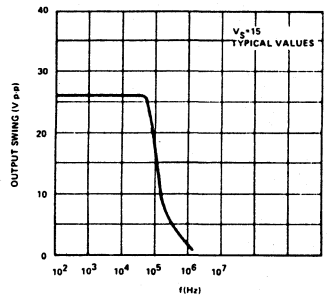
OPEN LOOP FREQUENCY RESPONSE



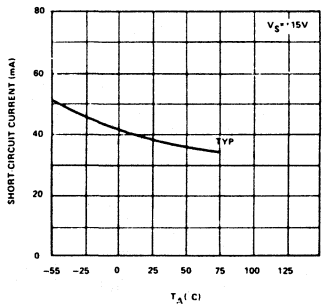
CLOSED LOOP FREQUENCY RESPONSE



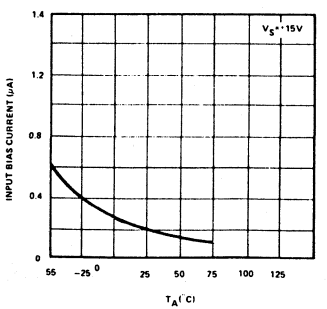
LARGE-SIGNAL FREQUENCY RESPONSE



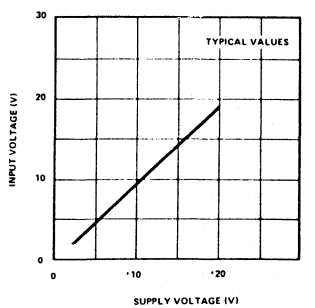
OUTPUT SHORT-CIRCUIT CURRENT



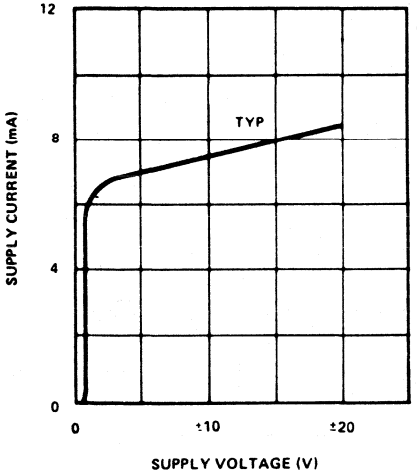
INPUT BIAS CURRENT



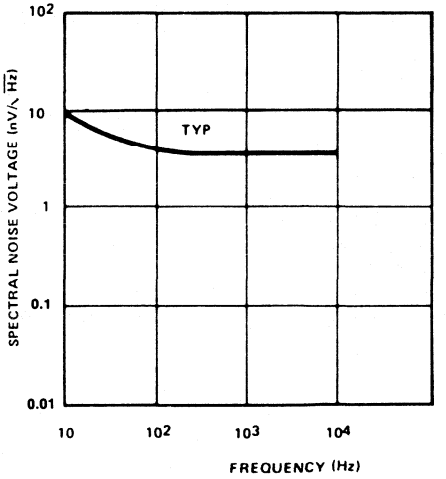
INPUT COMMON MODE VOLTAGE RANGE



SUPPLY CURRENT



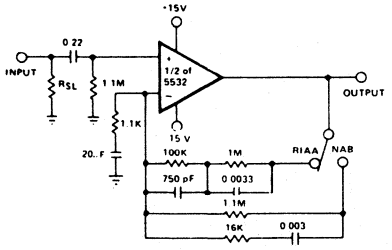
INPUT NOISE VOLTAGE DENSITY



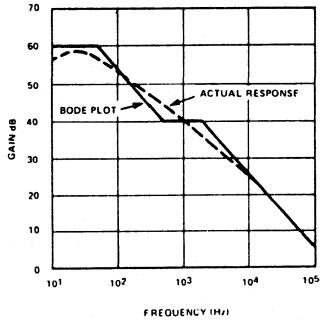
5

TYPICAL APPLICATION

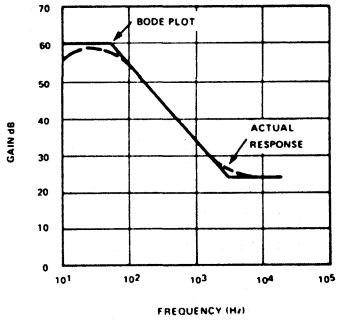
PREAMPLIFIER–RIAA/NAB COMPENSATION



*SELECT TO PROVIDE SPECIFIED TRANSDUCER LOADING
OUTPUT NOISE 0 8 mV r m s (WITH INPUT SHORTED)
ALL RESISTOR VALUES ARE IN OHMS

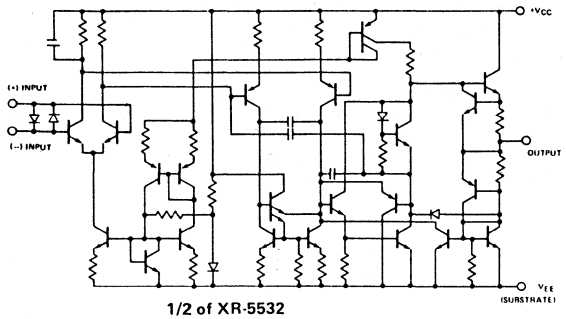


BODE PLOT OF RIAA EQUALIZATION AND THE RESPONSE REALIZED IN AN ACTUAL CIRCUIT USING THE XR 5533

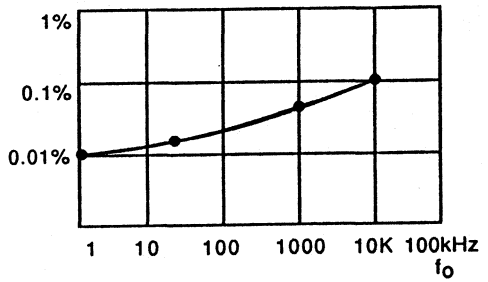


BODE PLOT OF NAB EQUALIZATION AND THE RESPONSE REALIZED IN THE ACTUAL CIRCUIT USING THE XR 5533

EQUIVALENT SCHEMATIC DIAGRAM



1/2 of XR-5532



Total Harmonic Distortion vs Frequency

$V_{IN} = 1 V_{PP}$

Low-Noise Operational Amplifier

GENERAL DESCRIPTION

The XR-5534 is a high performance low-noise operational amplifier especially designed for application in high quality and professional audio equipment. It offers five-fold improvement in noise characteristics, output drive capability and full-power bandwidth over conventional 741-type op amps. The op amp is internally compensated for gain equal to, or higher than, three. The frequency response can be optimzed with an external compensation capacitor for various applications such as operating in unity gain mode or driving capacitive loads.

The XR-5534A is a specially-screened version of the XR-5534, with guaranteed noise specifications.

FEATURES

Direct Replacement for Signetics NE/SE 5534
Wide Small-Signal Bandwidth: 10 MHz
High-Current Drive Capability
(10V rms into 600Ω at $V_S = \pm 18V$)
High Slew Rate: 13 V/μs
Wide Power-Bandwidth: 200 kHz typ.
Very Low Input Noise: 4 nV/√Hz typ.

APPLICATIONS

High Quality Audio Amplification
Telephone Channel Amplifiers
Servo Control Systems
Low-Level Signal Detection
Active Filter Design

ABSOLUTE MAXIMUM RATINGS

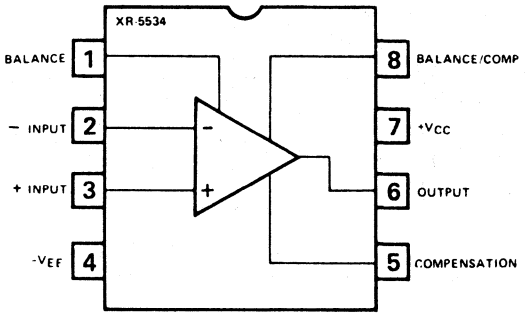
Power Supply	±22 V
Input Common-Mode Voltage	$+V_{CC}$ to $-V_{EE}$
Differential Input Voltage (Note 1)	±0.5 V
Power Dissipation (Package Limitation)	
Ceramic Package	750 mW
Plastic Package	625 mW
Derate Above +24°C	2.5 mW/°C
Short Circuit Duration (Note 2)	Indefinite
Storage Temperature	−60°C to +150°C

Note 1: Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ± 10 mA.

Note 2: Output may be shorted to ground at $V_S = \pm 15V$, T_A = 25°C. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

Note 3: Operation near the absolute maximum ratings will exceed the power dissipation rating of the package.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
5534AM	Ceramic	−55°C to +125°C
5534M	Ceramic	−55°C to +125°C
5534ACN	Ceramic	0°C to +70°C
5534CN	Ceramic	0°C to +70°C
5534ACP	Plastic	0°C to +70°C
5534CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-5534 and XR-5534A are monolithic operational amplifiers featuring low noise and a very large gain bandwidth product. The devices offer low output resistance and can drive 10 Vrms into 600Ω. Input noise is 100% tested on the XR-5534A, and is typically only 4 nV/√Hz. The small signal bandwidth is 10 MHz and slew rate exceeds 13 V/μS.

Reverse parallel diodes provide input protection; maximum differential input voltage is 0.7 V. Balance pins are provided to zero offset voltage. The device is internally compensated for gains ≥3 and provides external compensation pins for unity gain applications. Supply voltage may range from ±3V to ±20V.

For driving capacitive loads, an adjustment of the compensation can be made. The slew rate vs. compensation capacitor graph should be referenced. Slew rate has a large effect on op amp stability when driving capacitor loads.

XR-5534/5534A

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{CC} = $|V_{EE}|$ = 15V, unless otherwise specified.

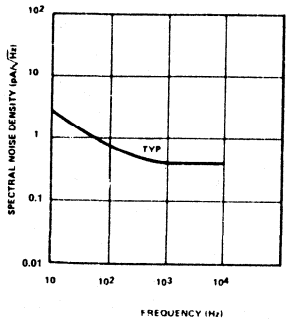
PARAMETERS	XR-5534M/5534AM			XR-5534AC/XR-5534C			UNITS	SYMBOL	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX			
DC CHARACTERISTICS									
Input Offset Voltage		0.5	2 3		0.5	4 5	mV mV	V_{OS}	T_A = 25°C T_T = Full Range *
Input Offset Current		10	200 500		20	300 400	nA nA	I_{OS}	T_A = 25°C T_T = Full Range *
Input Bias Current		400	800 1500		500	1500 2000	nA nA	I_B	T_A = 25°C T_T = Full Range *
Large Signal Voltage Gain	50 25	100		25 15	100		V/mV V/mV	A_{VOL}	$R_L \geq 600\Omega$, $V_O = \pm 10V$ T_A = 25°C T_T = Full Range *
Supply Current		4	6.5		4	8	mA	I_{CC}	R_L = Open
Output Swing	±12 ±15	±13 ±16		±12 ±15	±13 ±16		V V	V_{OUT}	$R_L \geq 600\Omega$ $V_{CC} = V_{EE}$ = 15V $V_{CC} = V_{EE}$ = 18V
Output Short Circuit Current		38			38		mA	I_{SC}	(Note 2)
Input Resistance	50	100		30	100		kΩ	R_{IN}	
Common-Mode Range	±12	±13		±12	±13		V	V_{iCM}	
Common-Mode Rejection	80	100		70	100		dB	CMRR	
Power Supply Rejection		10	50		10	100	μV/V	PSRR	
AC CHARACTERISTICS									
Transient Response									Voltage Follower
Rise Time		20			20		nSec	t_r	$R_L \geq 600\Omega$, C_C = 22 pF
Overshoot		20			20		%	t_0	C_L = 100 pF
AC Gain		6 2.2			6 2.2		6 2.2	V/mV V/mV	f = 10 kHz C_C = 0 C_C = 22 pF
Unity-Gain Bandwidth		10			10		MHz	BW	C_C = 22 pF, C_L = 100 pF
Slew Rate		13 6			13 6		V/μsec V/μsec		C_C = 0 C_C = 22 pF
Power Bandwidth		95 200			95 200		kHz kHz	f_p	$V_{OUT} = \pm 10V$, C_C = 22 pF C_C = 0

PARAMETERS	XR-5534A			XR-5534			UNITS	SYMBOL	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX			
NOISE CHARACTERISTICS									
Input Noise Voltage		5.5 3.5	7 4.5		7 4		nV/√Hz nV/√Hz	e_n	f_0 = 30 Hz f_0 = 1 kHz
Input Noise Current		1.5 0.4			2.5 0.6		pA/√Hz pA/√Hz	i_n	f_0 = 30 Hz f_0 = 1 kHz
Broadband Noise Figure		0.9					dB	F_N	R_S = 5 kΩ f = 10 Hz to 20 kHz

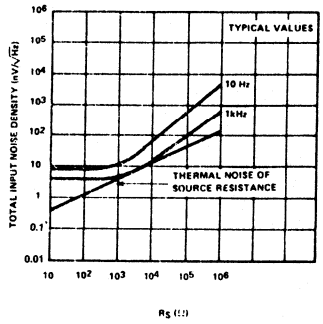
*These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

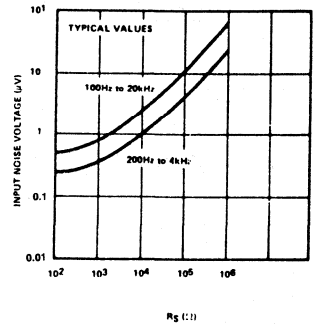
INPUT NOISE CURRENT DENSITY



TOTAL INPUT NOISE DENSITY

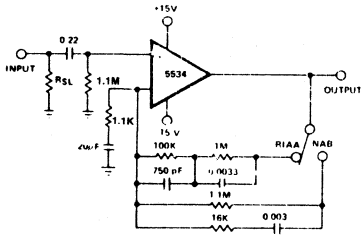


BROADBAND INPUT NOISE VOLTAGE

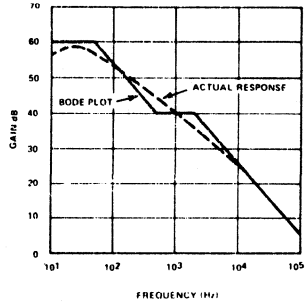


TYPICAL APPLICATION

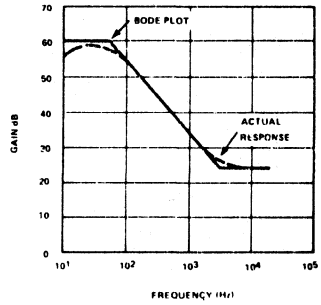
PREAMPLIFIER–RIAA/NAB COMPENSATION



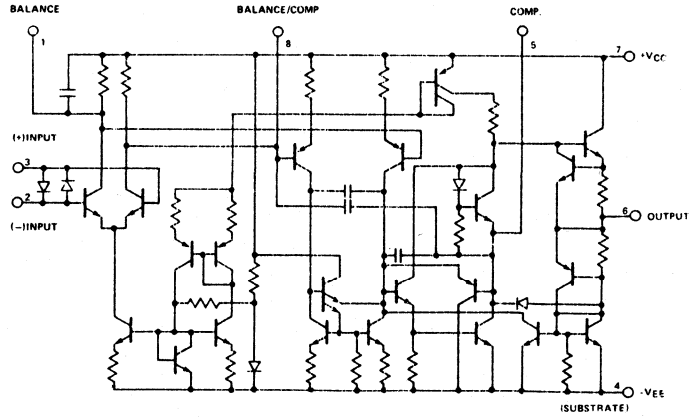
*SELECT TO PROVIDE SPECIFIED TRANSDUCER LOADING
OUTPUT NOISE 0.8 mV rms (WITH INPUT SHORTED)
ALL RESISTOR VALUES ARE IN OHMS



BODE PLOT OF RIAA EQUALIZATION AND THE RESPONSE REALIZED IN AN ACTUAL CIRCUIT USING THE XR–5534.



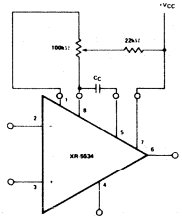
BODE PLOT OF NAB EQUALIZATION AND THE RESPONSE REALIZED IN THE ACTUAL CIRCUIT USING THE XR–5534.



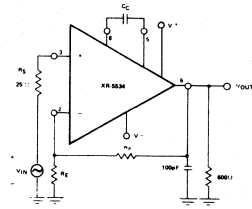
EQUIVALENT SCHEMATIC DIAGRAM

TEST CIRCUITS

FREQUENCY COMPENSATION AND OFFSET VOLTAGE ADJUSTMENT CIRCUIT

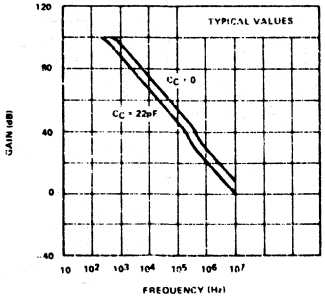


CLOSED LOOP FREQUENCY RESPONSE

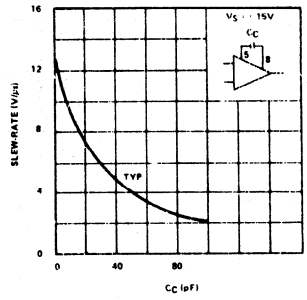


TYPICAL PERFORMANCE CHARACTERISTICS

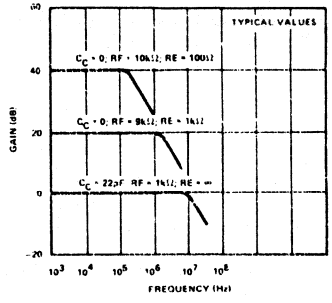
OPEN LOOP FREQUENCY RESPONSE



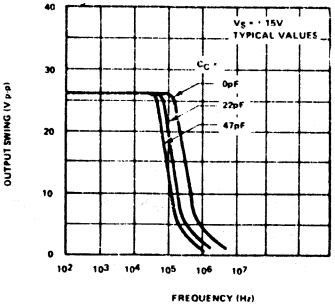
SLEW-RATE AS A FUNCTION OF COMPENSATION CAPACITANCE



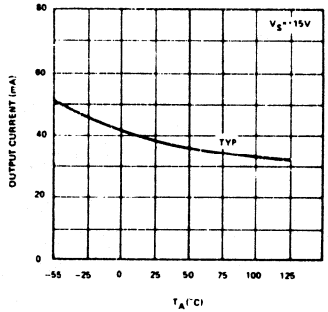
CLOSED LOOP FREQUENCY RESPONSE



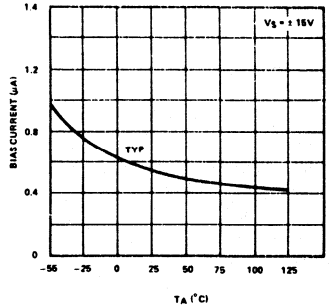
LARGE-SIGNAL FREQUENCY RESPONSE



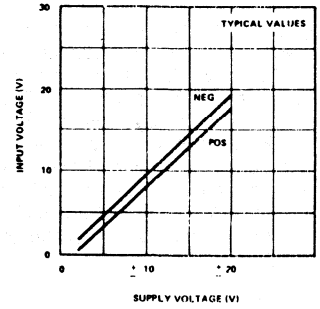
OUTPUT SHORT-CIRCUIT CURRENT



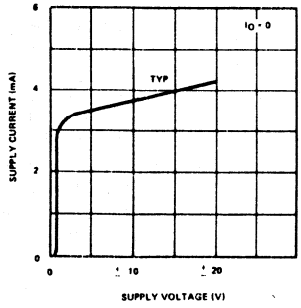
INPUT BIAS CURRENT



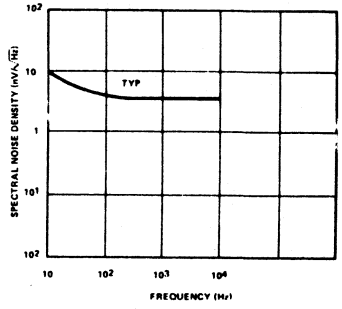
INPUT COMMON MODE VOLTAGE RANGE



SUPPLY CURRENT



INPUT NOISE VOLTAGE DENSITY



5

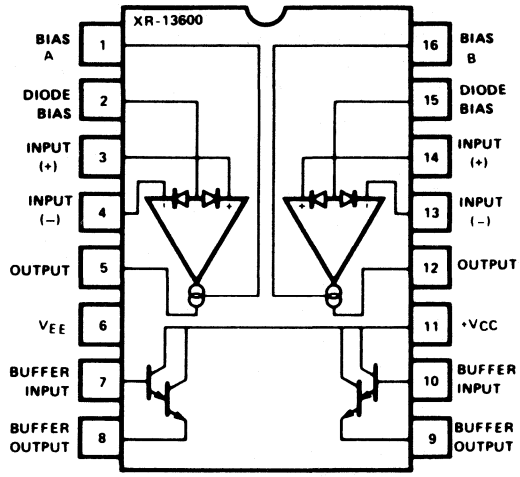
Dual Operational Transconductance Amplifier

GENERAL DESCRIPTION

The XR-13600 is a dual operational transconductance (Norton) amplifier with predistortion diodes and non-committed Darlington buffer outputs.

The device is especially suitable for electronically controllable gain amplifiers, controlled frequency filters, an other applications requiring current or voltage adjustments.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for LM-13600 and LM-13600 A
Transconductance Adjustable Over 4 Decades
Excellent Transconductance-Control Linearity
Uncommitted Darlington Output Buffers
On-Chip Predistortion Diodes
Excellent Matching Between Amplifiers
Wide Supply Range: ±2V to ±18V

APPLICATIONS

Current-Controlled Amplifiers
Current-Controlled Impedances
Current-Controlled Filters
Current-Controlled Oscillators
Multipliers/Attenuators
Sample and Hold Circuits
Electronic Music Synthesis

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-13600AP	Plastic	0°C to + 70°C
XR-13600CP	Plastic	0°C to + 70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (See Note 1)	±22 V
Power Dissipation (T_A = 25°C, see Note 2)	625 mW
Derate Above 25°C	5 mW/°C
DC Input Voltage	$+V_{CC}$ to $-V_{EE}$
Differential Input Voltage	±5 V
Diode Bias Current (I_D)	2 mA
Amplifier Bias Current (I_B)	2 mA
Output Short Circuit Duration	Indefinite
Buffer Output Current (Note 3)	20 mA
Storage Temperature Range	−65°C to +150°C

SYSTEM DESCRIPTION

The XR-13600 consists of two programmable transconductance amplifiers with high input impedance and push-pull outputs. The two amplifiers share common supplies but otherwise operate independently. Each amplifier's transconductance is directly proportional to its applied bias current. To improve signal-to-noise performance, predistortion diodes are included on the inputs; the use of these diodes results in a 10 dB improvement referenced to 0.5% THD. Independent Darlington emitter followers are included to buffer the outputs.

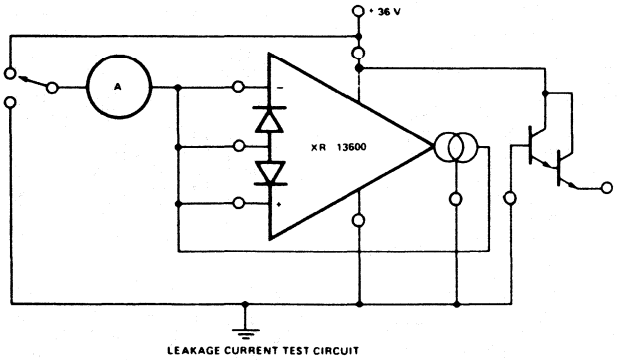
XR-13600

ELECTRICAL CHARACTERISTICS

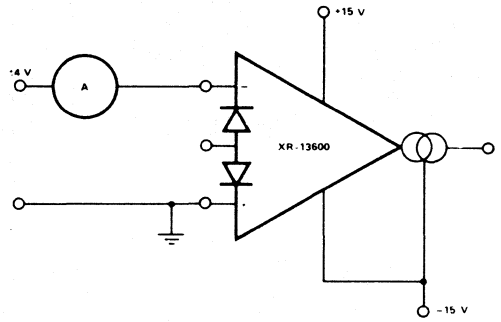
Test Conditions: T_A = +25°C, Supply Voltage = ±15V, unless otherwise specified.

PARAMETERS	XR-13600A			XR-13600C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
Input Offset Voltage (V_{OS})		0.4	2		0.4	5	mV	
			5				mV	Over Temperature Range
		0.3	2		0.3	5	mV	I_B = 5μA
V_{OS} Including Diodes		0.5	2		0.5	5	mV	Diode Bias Current (I_D) = 500 μA
Input Offset Change		0.1	3		0.1		mV	5μA ≤ I_B ≤ 500μA
Input Offset Current		0.1	0.6		0.1	0.6	μA	
Input Bias Current		0.4	5		0.4	5	μA	T_A = 25°C
		1	7		1	8	μA	Over Temperature Range
Forward Transconductance (g_m)	7700	9600	12000	6700	9600	13000	μmho	T_A = 25°C
	4000			5400			μmho	Over Temperature Range
g_m Tracking		0.3			0.3		dB	
Peak Output Current	3	5	7		5		μA	RL = 0, I_B = 5μA
	350	500	650	350	500	650	μA	RL = 0, I_B = 500μA
	300			300			μA	RL = 0, Over Specified Temp Range
Peak Output Voltage								
Positive	+12	+14.2		+12	+14.2		V	RL = ∞, 5 μA ≤ I_B ≤ 500 μA
Negative	−12	−14.4		−12	−14.4		V	RL = ∞, 5 μA ≤ I_B ≤ 500 μA
Supply Current		2.6			2.6		mA	I_B = 500 μA, Both Channels
V_{OS} Sensitivity								
Positive		20	150		20	150	μV/V	Δ V_{OS}/Δ V +
Negative		20	150		20	150	μV/V	Δ V_{OS}/Δ V −
CMRR	80	110		80	110		dB	
Common Mode Range	±12	±13.5		±12	±13.5		V	Referred to Input (Note 5)
Channel Separation		100			100		dB	20 Hz < f < 20 KHz
Diff. Input Current		0.02	10		0.02	100	nA	I_B = 0, Input = ±4 V
Leakage Current		0.2	5		0.2	100	nA	I_B = 0 (refer To Test Circuit)
Input Resistance	10	26		10	26		KΩ	
Open Loop Bandwidth		2			2		MHz	
Slew Rate		50			50		V/μSec	Unity Gain Compensated
Buff. Input Current		0.4	5		0.4	5	μA	(Note 5)
Peak Buffer Output Voltage	10			10			V	(Note 5)

TEST CIRCUITS



LEAKAGE CURRENT TEST CIRCUIT



DIFFERENTIAL INPUT CURRENT TEST CIRCUIT

Note 1. For selections to a supply voltage above ±22 V, contact factory.

Note 2. For operating at high temperatures, the device may be derated based on a 150°C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.

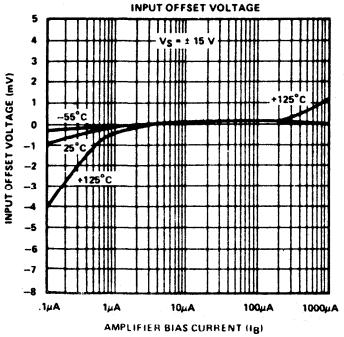
Note 3. Buffer output current should be limited so as to not exceed package dissipation.

Note 4. These specifications apply for V_{CC} = V_{EE} = 15V, T_A = 25°C, amplifier bias current (I_B) = 500 μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

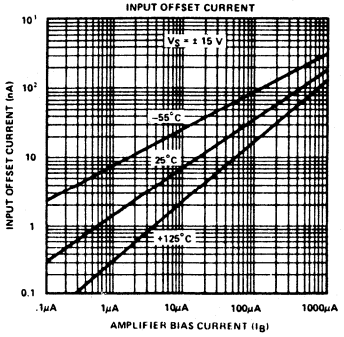
Note 5. These specifications apply for V_{CC} = V_{EE} = 15 V, I_B = 500 μA, R_{OUT} = 5 kΩ connected from the buffer output to $-V_{EE}$ and the input of the buffer is connected to the transconductance amplifier output.

TYPICAL PERFORMANCE CHARACTERISTICS

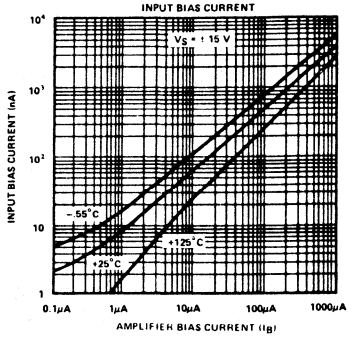
INPUT OFFSET VOLTAGE



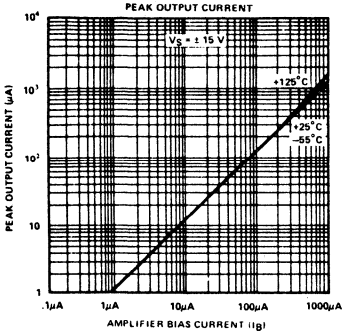
INPUT OFFSET CURRENT



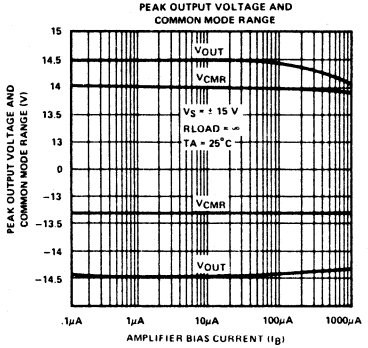
INPUT BIAS CURRENT



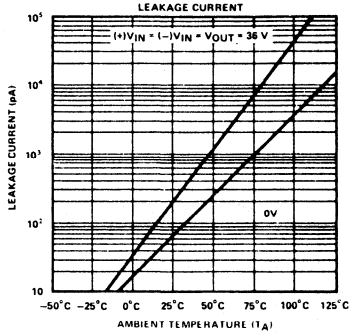
PEAK OUTPUT CURRENT



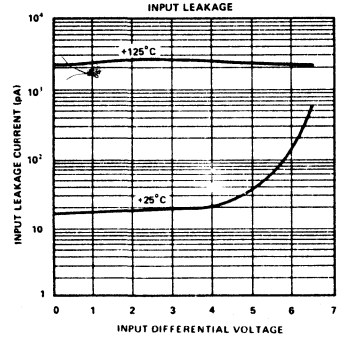
PEAK OUTPUT VOLTAGE AND COMMON MODE RANGE



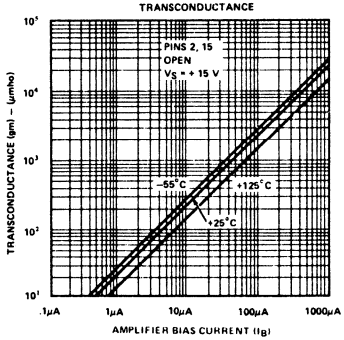
LEAKAGE CURRENT



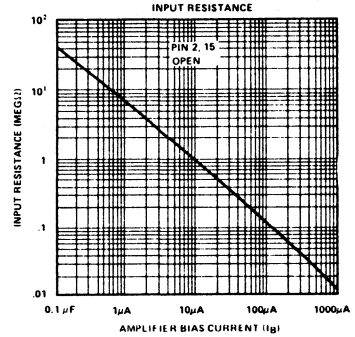
INPUT LEAKAGE



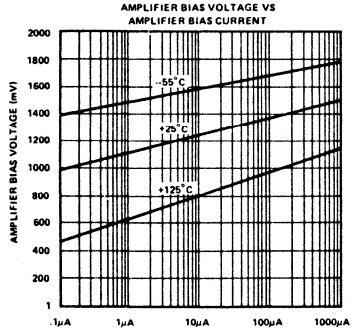
TRANSCONDUCTANCE



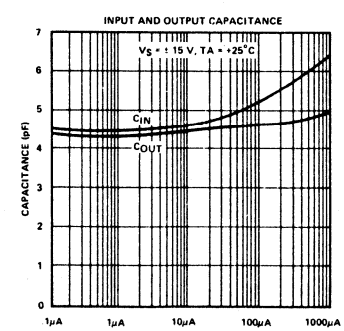
INPUT RESISTANCE



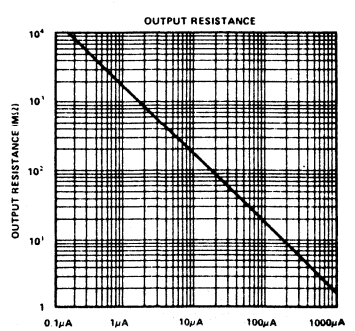
AMPLIFIER BIAS VOLTAGE VS AMPLIFIER BIAS CURRENT



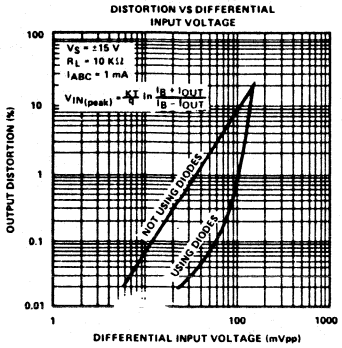
INPUT AND OUTPUT CAPACITANCE

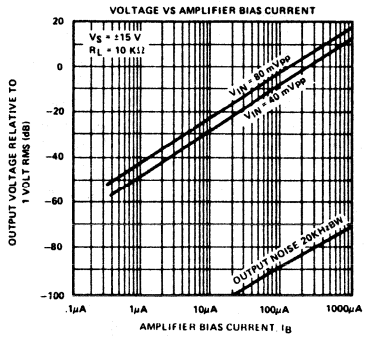


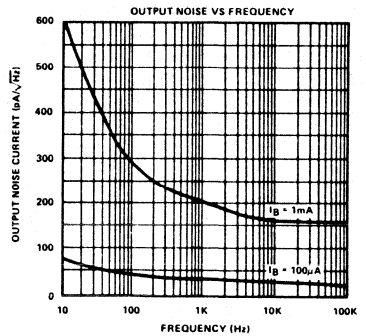
OUTPUT RESISTANCE



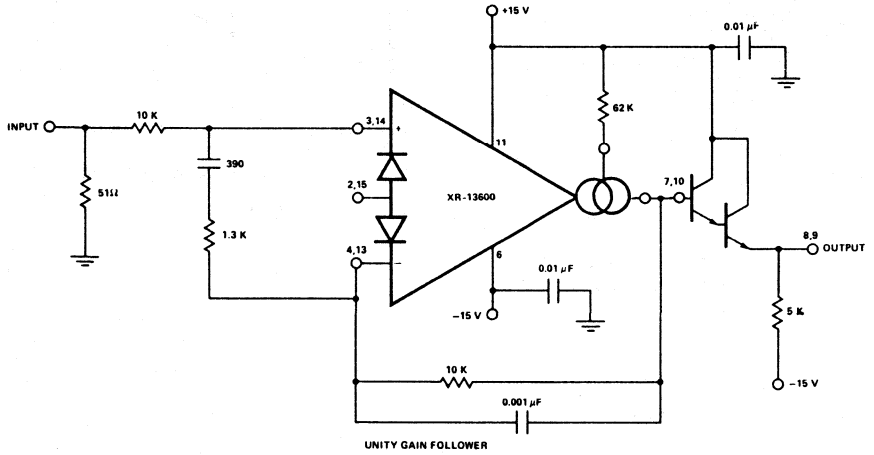
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)







TYPICAL CIRCUIT CONNECTION



CIRCUIT DESCRIPTION

The differential transistor pair Q_4 and Q_5 form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \qquad (1)$$

where V_{IN} is the differential input voltage, KT/q is approximately 26 mV at 25° C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_3 and Q_{13}, all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_B;

$$I_4 + I_5 = I_B \qquad (2)$$

where I_B is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the ln function can be approximated as:

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \qquad (3)$$

$$I_4 \approx I_5 \approx \frac{I_B}{2}$$

$$V_{IN}\left[\frac{(I_B)(q)}{2KT}\right] = I_5 - I_4 \qquad (4)$$

Collector currents I_4 and I_5 are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

$$V_{IN}\left[\frac{(I_B)(q)}{2KT}\right] = I_{OUT} \qquad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_B.

LINEARIZING DIODES

For differential voltages greater than a few millivolts, Equation 3 is no longer accurate, and the transconductance becomes increasingly nonlinear. Figure 1 demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is the form of current I_S. Since the sum of I_4 and I_5 is I_B and the difference is I_{OUT}, currents I_4 and I_5 can be written as follows:

$$I_4 = \frac{I_B}{2} - \frac{I_{OUT}}{2}, \quad I_5 = \frac{I_B}{2} + \frac{I_{OUT}}{2}$$

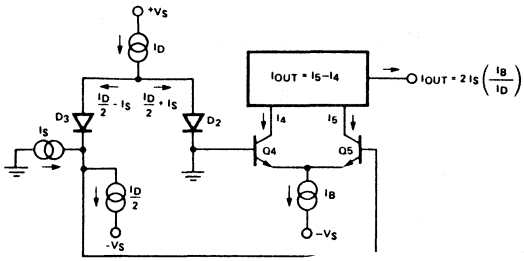


Figure 1. Linearizing Diodes

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\frac{KT}{q} 1n \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} 1n \frac{\frac{I_B}{2} + \frac{I_{out}}{2}}{\frac{I_B}{2} - \frac{I_{out}}{2}}$$

$$\therefore I_{out} = I_S \left(\frac{2I_B}{I_D}\right) \text{ for } |I_S| < \frac{I_D}{2} \qquad (6)$$

Notice that in deriving Equation 6, no approximations have been made and there are no temperature dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

CONTROLLED IMPEDANCE BUFFERS

The upper limit of transconductance is defined by the maximum value of I_B (2 mA). The lowest value of I_B for which the amplifier will function therefore determines the overall dynamic range. At very low values of I_B, a buffer which has very low input bias current is desirable. A FET follower satisfies the low input current requirement, but is some what non-linear for large voltage wing. The controlled impedance buffer is a Darlington which modifies its input bias current to suit the need. For low values of I_B, the buffer's input current is minimal. At higher levels of I_B, transistor Q_3 biases up to Q_{12} with a current proportional to I_B for fast slew rate.

APPLICATIONS

VOLTAGE CONTROLLED AMPLIFIERS (VCA)

Figure 2 shows how the linearizing diodes can be used in a voltage controlled amplifier. To understand the input biasing, it is best to consider the 13 KΩ resistor as a current source and use a Therenin equivalent circuit as shown in Figure 3. This circuit is similar to Figure 1 and operates the same. The potentiometer in Figure 2 is adjusted to minimize the effects of the control signal at the output.

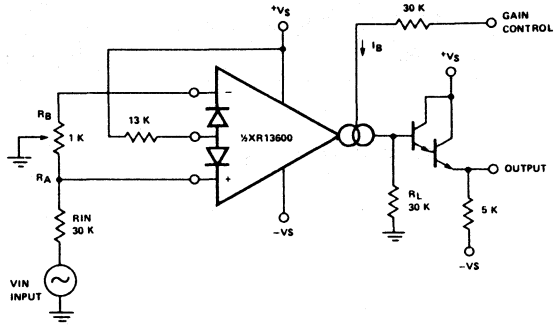


Figure 2. Voltage Controlled Amplifier (VCA) Circuit

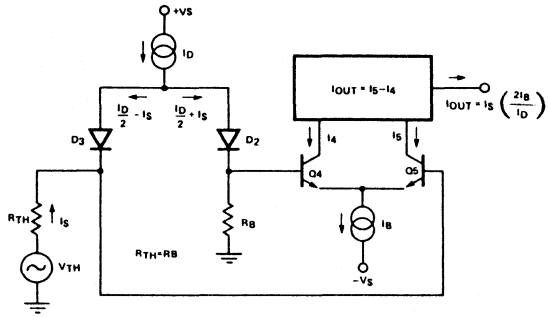


Figure 3. Equivalent VCA Input Circuit

For optimum signal-to-noise performance, I_B should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via R_{IN} (Figure 2) until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting R_L.

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, I_D should be as large as possible. This minimizes the dynamic junction resistance of the diodes (r_e) and maximizes their linearizing action when balanced against R_{IN}. A value of 1 mA is recommended for I_D unless the specific application demands otherwise.

XR-13600
STEREO VOLUME CONTROL

The circuit of Figure 4 uses the excellent matching of the two XR-13600 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. Rp is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived from Figure 2 as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_B \text{ (mA)}$$

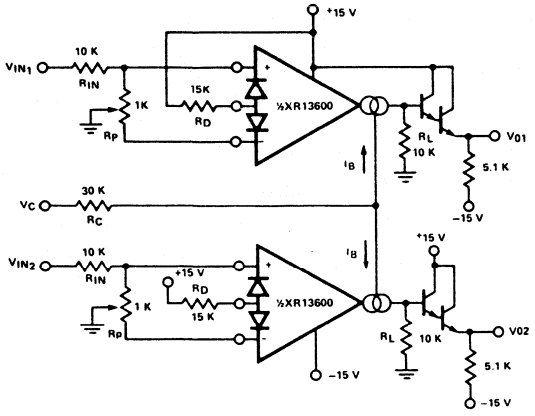


Figure 4. Stereo Volume Control

If V_C is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in Figure 5, where:

$$I_O = \frac{-2I_S}{I_D}(I_B) = \frac{-2I_S}{I_D}\frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D}\frac{(V = 1.4V)}{R_C}$$

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C/2(V + 1.4\ V)$ into I_O. The circuit of Figure 6 adds R_M to provide this current, resulting in a four-quadrant multiplier where R_C is trimmed such that V_O = OV for V_{IN2} = OV. R_M also serves as the load resistor for I_O.

Noting that the gain of the XR-13600 amplifier of Figure 3 may be controlled by varying the linearizing diode current I_D as well as by varying I_B, Figure 7 shows an AGC Amplifier using this approach. As V_O reaches a high enough amplitude ($3V_{BE}$) to turn on the Darlington transistors and the linearizing diodes, the increase in I_D reduces the amplifier gain so as to hold V_O at that level.

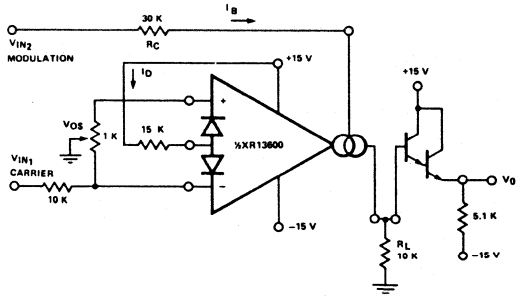


Figure 5. Amplitude Modulator

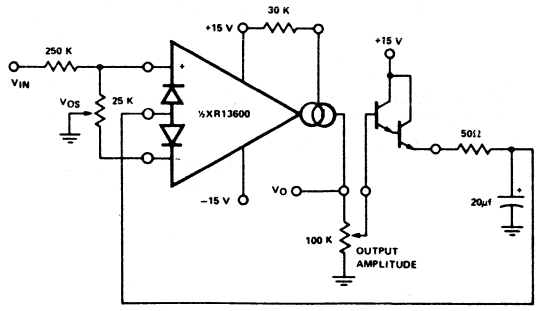


Figure 6. Four-Quadrant Multiplier

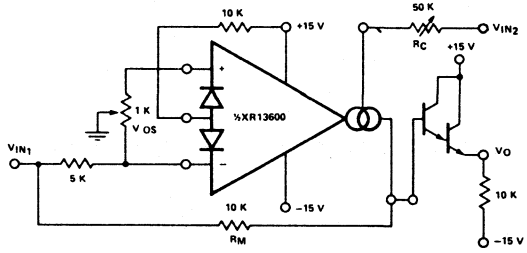


Figure 7. AGC Amplifier

VOLTAGE CONTROLLED RESISTORS (VCR)

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in Figure 8. A signal voltage applied at R_X generates a V_{IN} to the XR-13600 which is then multiplied by the gm of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m R_A}$$

where $g_m \approx 19.2\ I_B$ at 25°C. Note that the attenuation of V_O by R and R_A is necessary to maintain V_{IN} within the linear range of the XR-13600 input.

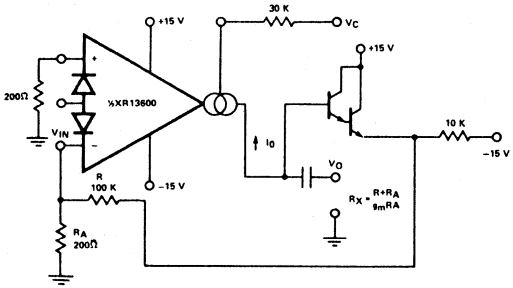


Figure 8. Voltage Controlled Resistor, Single-Ended

Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the nose performance of the resistor. A floating VCR is shown in Figure 10, where each "end" of the "resistor" may be at any voltage within the output voltage range of the XR-13600.

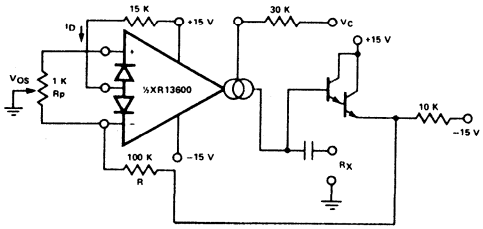


Figure 9. Voltage Controlled Resistor with Linearizing Diodes

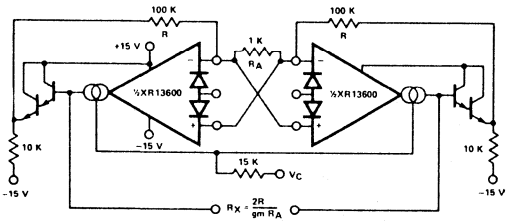


Figure 10. Floating Voltage Controlled Resistor

VOLTAGE CONTROLLED FILTERS

OTA's are extremely useful for implementing voltage controlled filters, with the XR-13600 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of Figure 11 performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which X_C/g_m equals the closed-loop gain of (R/R_A). At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a −3 dB point defined by the given equation, where g_m is again 19.2 × I_B at room temperature.

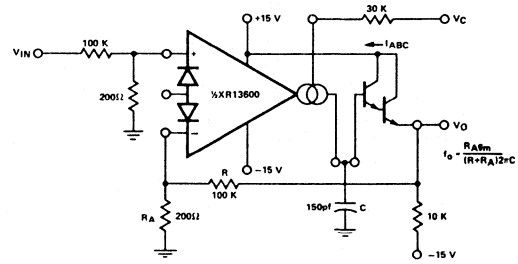


Figure 11. Voltage Controlled Low-Pass Filter

Figure 12 shows a voltage controlled high-pass filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

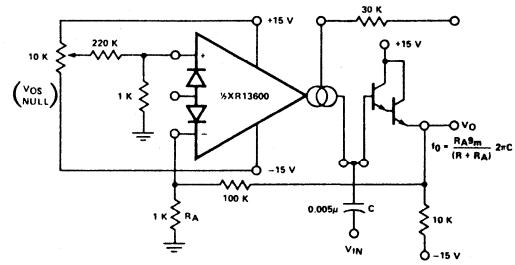


Figure 12. Voltage Controlled High-Pass Filter

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth lowpass filter of Figure 13 and the state variable filter of Figure 14. Due to the excellent g_m tracking of the two amplifiers and the varied bias of the buffer Darlingtons, these filters perform well over several decades of frequency.

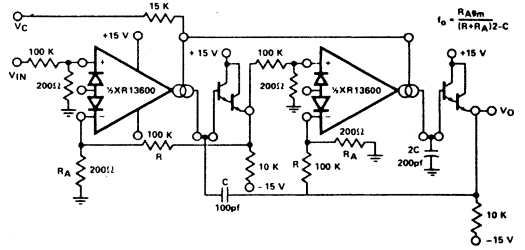


Figure 13. Voltage Controlled 2-Pole Butterworth Low-Pass Filter

VOLTAGE CONTROLLED OSCILLATORS (VCO)

The classic Triangular/Square Wave VCO of Figure 15 is one of a variety of Voltage Controlled Oscillators which may be built utilizing the XR-13600. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as I_C is varied from 1mA to 10nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5 volts to prevent zenering the inputs.

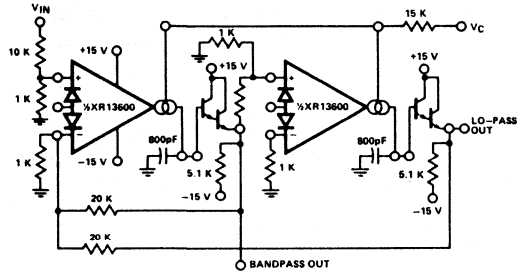


Figure 14. Voltage Controlled State Variable Filter

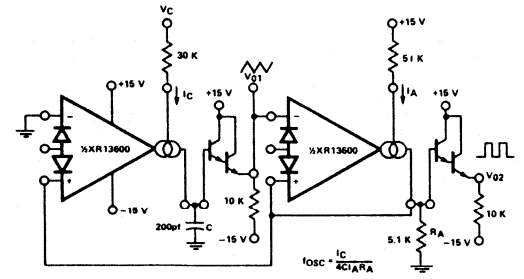


Figure 15. Triangular/Square-Wave VCO

A few modifications to this circuit produce the ramp/pulse VCO of Figure 16. When V_{O2} is high, I_F is added to I_C to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When V_{O2} is low, I_F goes to zero and the capacitor discharge current is set by I_C.

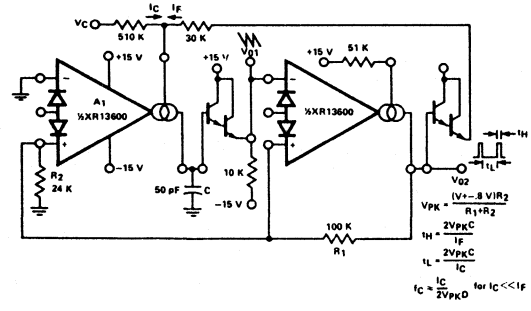


Figure 16. Ramp/Pulse VCO

The voltage-controlled low-pass filter of Figure 11 may be used to design a high-quality sinusoidal VCO. The circuit of Figure 17 employs two XR-13600 packages, with three of the amplifiers configured as low-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

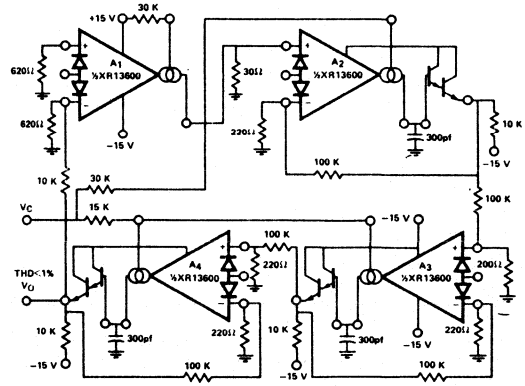


Figure 17. Sinusoidal VCO Using Two XR-13600 Circuits

Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

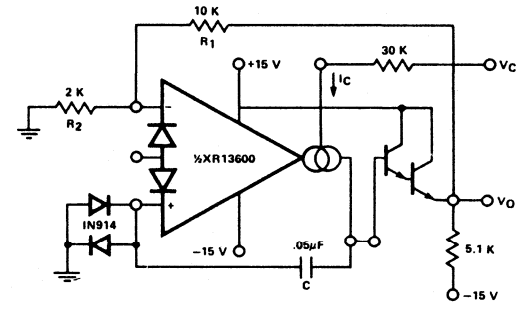


Figure 18. Single Amplifier VCO

ADDITIONAL APPLICATIONS

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through R_B and pulls the non-inverting input high. The amplifier regenerates and latches it output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is speeded up by shorting the diode bias pin to the inverting input so that an additional discharge current flows through D_1 when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_O, can perform another function and draw zero stand-by power as well.

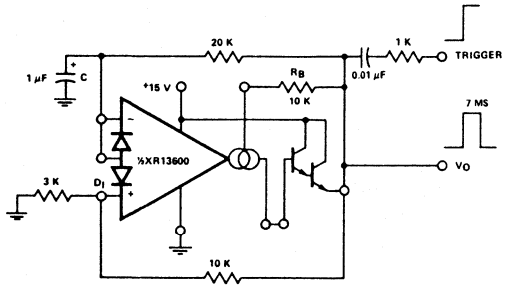


Figure 19. Timer With Zero Stand-By Power

The operation of the multiplexer of Figure 20 is very straight-forward. When A_1 is turned on it holds V_O equal to V_{IN1} and when A_2 is supplied with bias current then it controls V_O. C_C and R_C serve to stabilize the unity-gain configuration of amplifiers A_1 and A_2. The maximum clock rate is limited to about 200 kHz by the XR-13600 slew rate into 150 pF when the $(V_{IN1} - V_{IN2})$ differential is at its maximum allowable value of 5 volts.

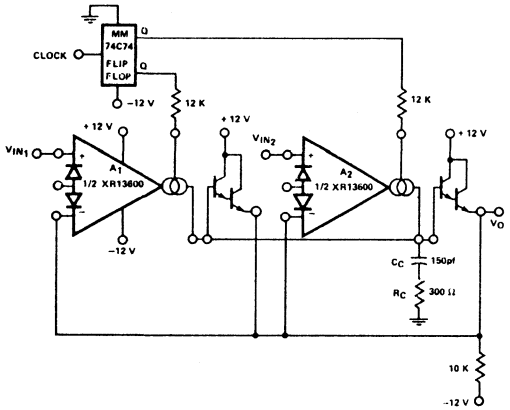


Figure 20. Multiplexer

The phase-locked loop of Figure 21 uses the four-quadrant multiplier of Figure 6 and the VCO of Figure 18 to produce a PLL with a ±5% hold-in range and an input sensitivity of about 300 mV.

The Schmitt trigger of Figure 22 uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$ will produce a Schmitt trigger with variable hysteresis.

Figure 23 shows a tachometer or frequency-to-voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H - V_L)\ C_t$ is sourced into C_f and R_t. This once per cycle charge is then balanced by the current of V_O/R_t. The maximum F_{IN} is limited by the amount of time required to charge C_t from V_L to V_H with a current of I_B, where V_L and V_H

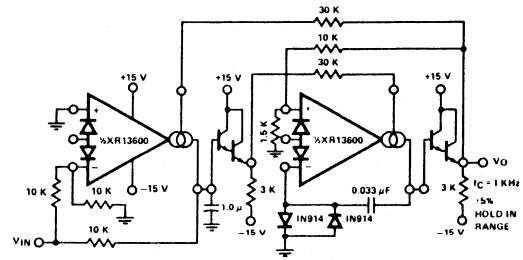


Figure 21. Phase-Locked Loop

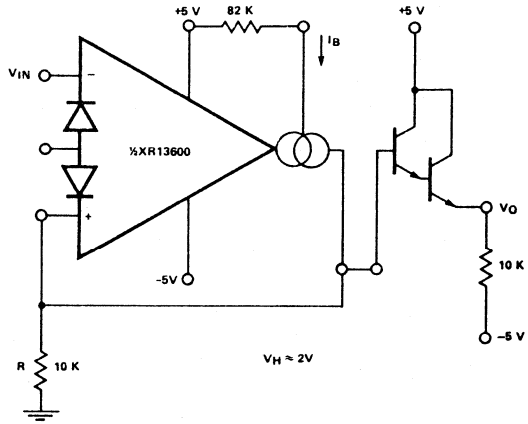


Figure 22. Schmitt Trigger

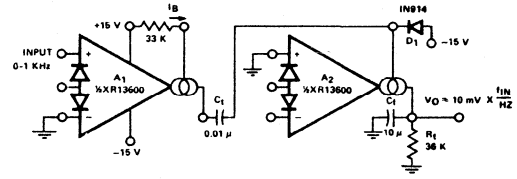


Figure 23. Tachometer

represent the maximum low and maximum high output voltage swing of the XR-13600. D1 added to provide a discharge path for C_t and A_1 switches low.

The sample-hold circuit of Figure 24 also requires that the Darlington buffer used be from the other (A_2) half of the package and that the corresponding amplifier be biased on continuously.

The peak detector of Figure 25 uses A_2 to turn on A_1 whenever V_{IN} becomes more positive than V_O. A1 then charges storage capacitor C to hold V_O equal to V_{IN} PK. One precaution to observe when using this circuit: the Darlington transistor used must be on the same side of the package as A_2 since the A_1 Darlington will be turned on and off with A_1. Pulling the output of A_2 low through D_1 serves to turn off A_1 so that V_O remains constant.

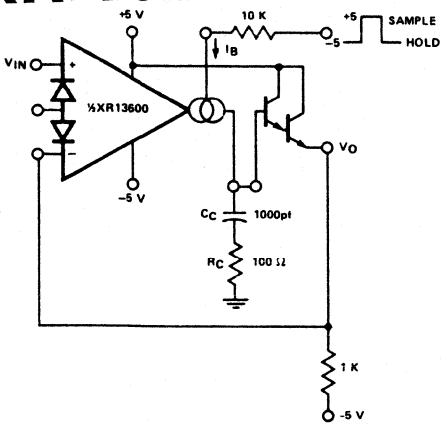


Figure 24. Sample-Hold Circuit

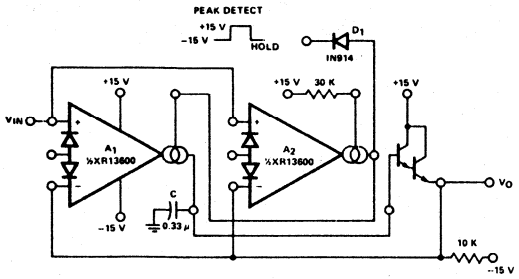


Figure 25. Peak Detector and Hold Circuit

The ramp-and-hold of Figure 26 sources I_B into capacitor C whenever the input to A_1 is brought high, giving a ramp-rate of about IV/ms for the component values shown.

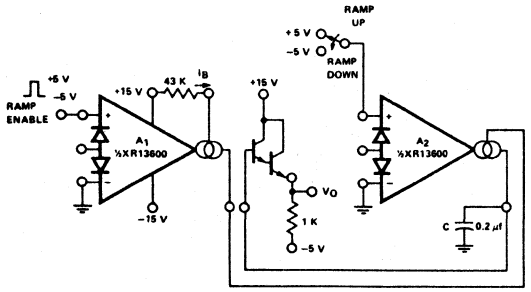


Figure 26. Ramp and Hold Circuit

The true RMS converter of Figure 27 is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A_1 is constant. The output power of amplifier A_1 is monitored by squaring amplifier A_2 and the average compared to a reference voltage with amplifier A_3. The output of A_3 provides bias current to the diodes of A_1 to attenuate the input signal. Because the output power of A_1 is held constant, the RMS value is constant and the attenuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A_4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A_4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that V_O reads directly in RMS volts.

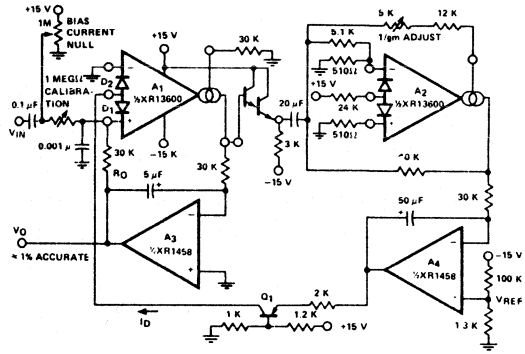


Figure 27. True RMS Converter Circuit

The circuit of Figure 28 is a voltage reference of variable Temperature Coefficient. The 100 KΩ potentiometer adjusts the output voltage which has a positive TC above 1.2 volts, zero TC at about 1.2 volts and negative TC below 1.2 volts. This is accomplished by balancing the TC of the A_2 transfer function against the complementary TC of D_1.

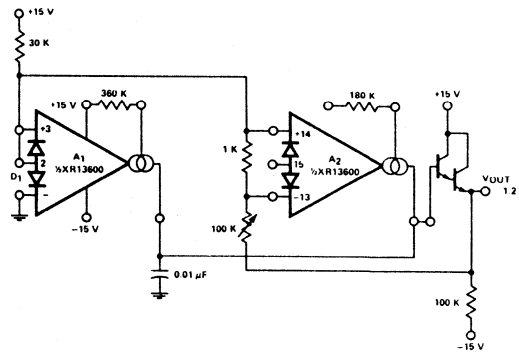


Figure 28. Delta V_{BE} Reference

The log amplifier of Figure 29 responds to the ratio of current thru buffer transistors Q_3 and Q_4. Zero temperature dependence for V_{OUT} is ensured in that the TC of the A_2 transfer function is equal and opposite to the TC of the logging transistors Q_3 and Q_4.

The wide dynamic range of the XR-13600 allows easy control of the output pulse width in the pulse-width modulator of Figure 30.

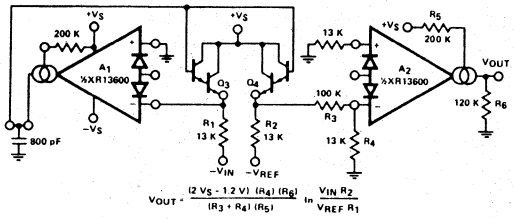


Figure 29. Log Amplifier

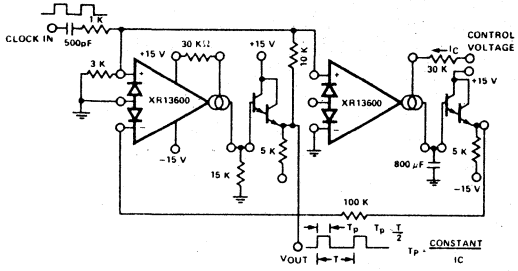


Figure 30. Pulse Width Modulator

For generating I_B over a range of 4 to 6 decades of current, the system of Figure 31 provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A_2 is held equal to O_V, the output current of A_1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q_1 and Q_2 is attenuated by the R_1, R_2 network so that A_1 may be assumed to be operating within its linear range. From equation (5), the input voltage to A_1 is:

$$V_{IN1} = \frac{-2KTI_3}{qI_2} = \frac{2KTV_C}{qI_2R_C}$$

The voltage on the base of Q1 is then

$$V_{B1} = \frac{(R_1 + R_2)\,V_{IN1}}{R_1}$$

The ratio of the Q1 to Q2 collector currents is defined by:

$$V_{B1} = \frac{KT}{q} 1n \frac{I_{C2}}{I_{C1}} \approx \frac{KT}{q} 1n \frac{I_B}{I_1}$$

Combining and solving for I_B yields:

$$I_B = (I_1) \exp\left[\frac{2(R_1 + R_2)\,V_C}{I_2R_1R_C}\right]$$

This logarithmic current can be used to bias the circuit of Figure 4 to provide temperature independent stereo attenuation characteristic.

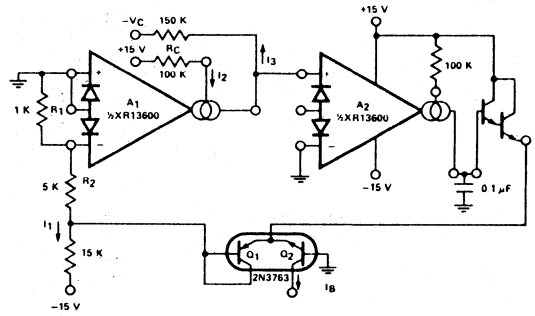
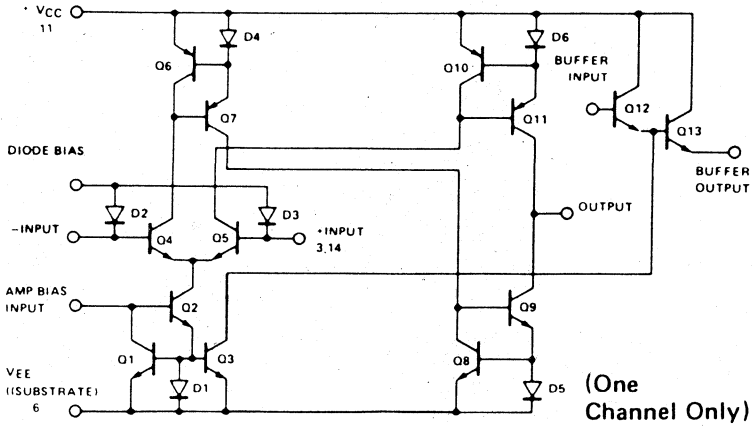


Figure 31. Logarithmic Current Source



EQUIVALENT SCHEMATIC DIAGRAM

Pulse-Width Modulating Regulator

GENERAL DESCRIPTION

The XR-1524 family of monolithic integrated circuits contain all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The XR-1524 is specified for operation over the full military temperature range of -55°C to +125°C, while the XR-2524 is specified to operate from -25°C to +85°C. The XR-3524 are designed for commercial applications of 0°C to +70°C.

FEATURES

Pin-for-Pin Replacement for SG-1524/2524/3524
Complete PWM power control circuitry
Single ended or push-pull outputs
Line and load regulation of 0.2%
1% maximum temperature variation
Total supply current less than 10 mA
Operation beyond 100 kHz

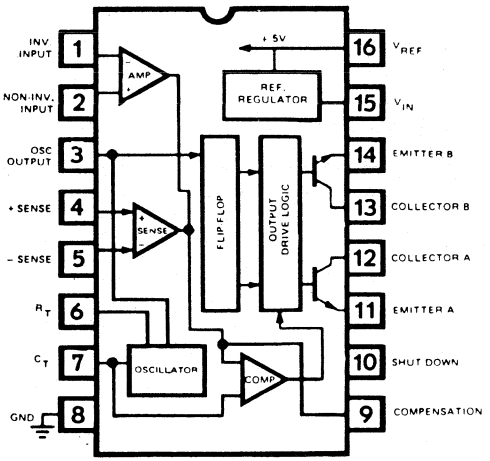
APPLICATIONS

Switching Regulators
Pulse-width Modulated Power Control Systems

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Output Current (each output)	100 mA
Reference Output Current	50 mA
Oscillator Charging Current	5 mA
Power Dissipation	
Ceramic Package	1000 mW
Derate above +25°C	8 mW/°C
Plastic Package	625 mW/°C
Derate above +25°C	5 mW/°C
Japanese SO	**500 mW**
Derate above 25°C	**5 mW/°C**
Operating Temperature Range	
XR-1524	−55°C to +125°C
XR-2524/XR-3524	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1524M	Ceramic	−55°C to +125°C
XR-2524N	Ceramic	−25°C to +85°C
XR-2524P	Plastic	−25°C to +85°C
XR-3524CN	Ceramic	0°C to +70°C
XR-3524CP	Plastic	0°C to +70°C
XR-3524MD	**Japanese Dimension SO-16**	**0°C to +70°C**

SYSTEM DESCRIPTION

The XR-1524/2524/3524 pulse width modulating regulator is a complete monolithic switching regulator. An internal 5V reference, capable of supplying up to 50 mA to external loads, provides an on board operating standard. The oscillator frequency and duty cycle are adjusted by an external RC network. Regulation is controlled by an error amplifier which, combined with the sense amplifier, also allows current limiting and remote shutdown functions. The outputs of the XR-1524/2524/3524 are two identical NPN transistors with both emitters and collectors uncommitted. Each output transistor has antisaturation circuitry for fast response and local current limiting set at 100 mA.

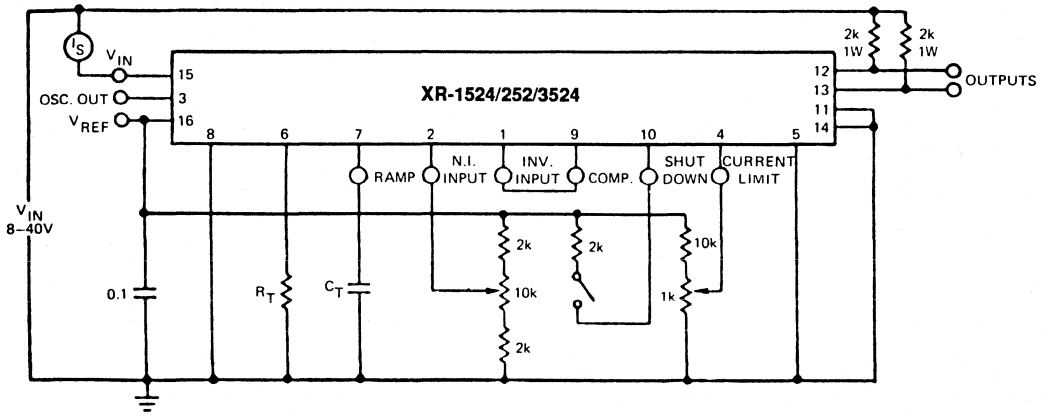
ELECTRICAL SPECIFICATIONS

Test Conditions: T_A = **25°C** V_{IN} = 20V, and f = 20 kHz, unless specified otherwise.

PARAMETERS	XR-1524/ XR-2524 MIN	XR-1524/ XR-2524 TYP	XR-1524/ XR-2524 MAX	XR-3524 MIN	XR-3524 TYP	XR-3524 MAX	UNITS	CONDITIONS
REFERENCE SECTION								
Output Voltage	4.8	5.0	5.2	4.6	5.0	5.4	V	
Line Regulation		10	20		10	30	mV	V_{IN} = 8 to 40 Volts
Load Regulation		20	50		20	50	mV	I_L = 0 to 20 mA
Ripple Rejection		66			66		dB	f = 120 Hz, T_A = 25°C
Short Circuit Current Limit		100	**150**		100		mA	V_{REF} = 0, T_A = 25°C
Temperature Stability		1.0	2		0.3	1	%	Over Operating Temperature Range*
Long Term Stability		20			20		mV/khr	T_A = 25°C
OSCILLATOR SECTION								
Maximum Frequency		300			300		kHz	C_T = .001 μF, R_T = 2 KΩ
Initial Accuracy		5			5		%	R_T and C_T constant
Voltage Stability			1			1	%	V_{IN} = 8 to 40 Volts, T_A = 25°C
Temperature Stability			2		2		%	Over Operating Temperature Range*
Output Amplitude		3.5			3.5		V	Pin3, T_A = 25°C
Output Pulse Width		0.5			0.5		μS	C_T = .01 mfd, T_A = 25°C
ERROR AMPLIFIER SECTION								
Input Offset Current			2		2		μA	
Input Offset Voltage		0.5	5		2	10	mV	V_{CM} = 2.5 Volts
Input Bias Current		2	10		2	10	μA	V_{CM} = 2.5 Volts
Open Loop Voltage Gain	72	80		60	80		dB	
Common Mode Voltage	1.8		3.4	1.8		3.4	V	T_A = 25°C
Common Mode Rejection Ratio	**46**	70			70		dB	T_A = 25°C
Small Signal Bandwidth		3			3		MHz	A_V = 0 dB, T_A = 25°C
Output Voltage	0.5		3.8	0.5		3.8	V	T_A = 25°C
COMPARATOR SECTION								
Duty Cycle	0		45	0		45	%	% Each Output On
Input Threshold		1			1		V	Zero Duty Cycle
Input Threshold		3.5			3.5		V	Max. Duty Cycle
Input Bias Current		1			1		μA	
CURRENT LIMITING SECTION								Pin 9 = 2V with Error Amplifier
Sense Voltage	190	200	210	180	200	220	mV	Set for Max. Out, T_A = 25°C
Sense Voltage Temp. Coef.		0.2			0.2		mV/°C	
Common Mode Voltage	−0.3		+0.3	−0.3		+0.3	V	
OUTPUT SECTION (Each Output)								
Max. Collector-Emitter Voltage	40			40			V	
Collector Leakage Current		0.1	50		0.1	50	μA	V_{CE} = 40V
Saturation Voltage		1	2		1	2	V	I_C = 50 mA
Emitter Output Voltage	17	18		17	18		V	V_{IN} = 20V
Rise Time		0.2			0.2		μS	R_C = 2 KΩ, T_A = 25°C
Fall Time		0.1			0.1		μS	R_C = 2 KΩ, T_A = 25°C
TOTAL STANDBY CURRENT (Excluding oscillator charging current, error and current limit dividers, and with outputs open)		8	10		8	10	mA	V_{IN} = 40V

* These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

OPEN LOOP TEST CIRCUIT



DESCRIPTION OF CIRCUIT OPERATION

VOLTAGE REFERENCE SECTION

The internal voltage reference and regulator section provides a 5-volt reference output at pin 16. This voltage also serves as a regulated voltage source for the internal timing and control circuitry. This regulator may be bypassed for operation from a fixed 5-volt supply by connecting pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0 volts.

This reference regulator may be used as a 5-volt source for other circuitry. It will provide up to 50 mA of current itself and can easily be expanded to higher currents with an external PNP as shown in Figure 2.

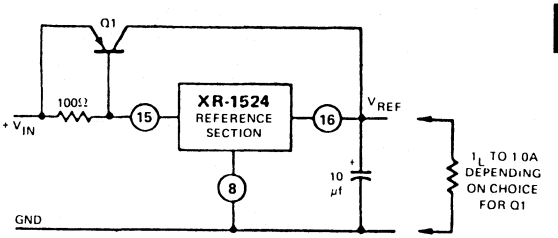


Figure 2. Using the Internal Regulator as 5V Power Supply for External Circuitry

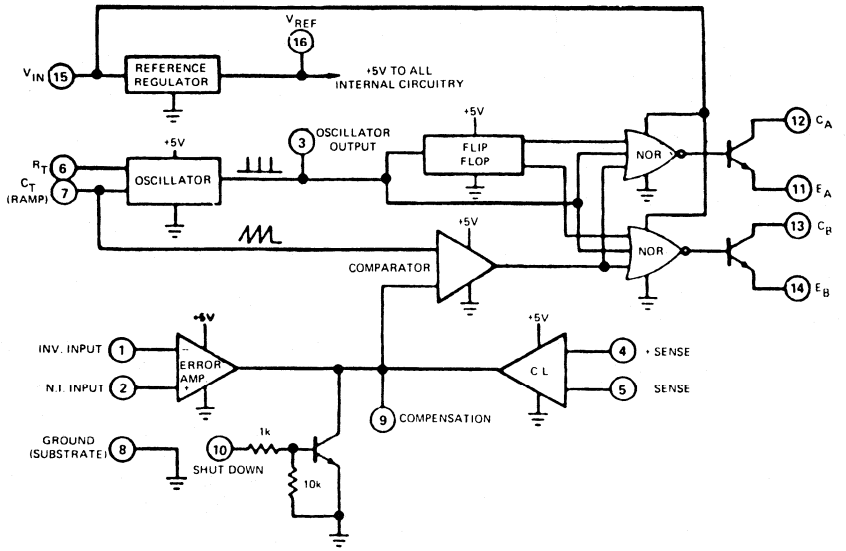


Figure 1. Detailed System Block Diagram of XR-1524

OSCILLATOR SECTION

The oscillator section in the XR-1524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to 3.6V ÷ R_T and should be kept within the range of approximately 30 μA to 2 mA, i.e., 1.8K < R_T < 100K.

The oscillator period is approximately $T = R_T C_T$ where T is in microseconds when R_T = ohms and C_T = microfarads.

The use of Figure 3 allows the selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0 - 90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each output's duty cycle is 0 - 45% and the overall frequency is 1/2 that of the oscillator.

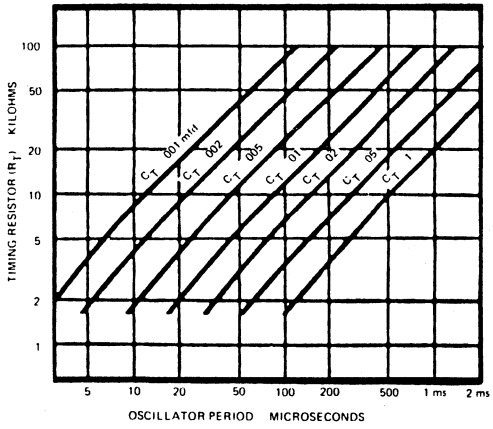


Figure 3. Oscillator Period as a Function of R_T and C_T

The range of values for C_T also has limits as the discharge time of C_T determines the pulse width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 4. A pulse width below approximately 0.5 microseconds may allow false triggering of one output by removing the blanking pulse prior to the flip-flop's reaching a stable state. If small values of C_T must be used, the pulse width may still be expanded by adding a shunt capacitance (≈ 100 pF) to ground at the oscillator output. (Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the **blanking pulse width slightly.) The upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between .001 and 0.1μF.**

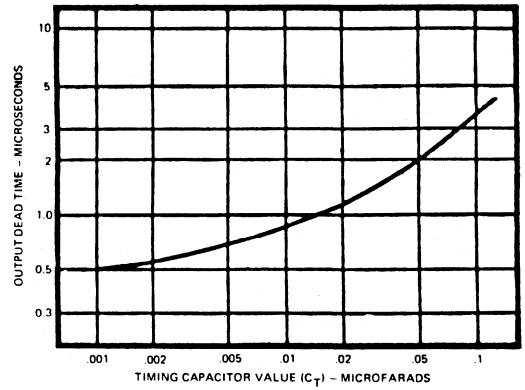


Figure 4. Output Stage Dead Time as a Function of the Timing Capacitor Value

If it is desired to synchronize the XR-1524 to an external clock, a pulse of ≈ +3 volts may be applied to the oscillator output terminal with $R_T C_T$ set slightly greater than the clock period. The same considerations of pulse width apply. The impedance to ground at this point is approximately 2K ohms.

If two or more XR-1524 circuits must be synchronized together, one must be designated as master with its $R_T C_T$ set for the correct period. The slaves should each have an $R_T C_T$ set for approximately 10% longer period than the master with the added requirement that C_T (slave) = 1/2 C_T (master). Then connecting pin 3 on all units together will insure that the master output pulse – which occurs first and has a wider pulse width – will reset the slave units.

ERROR AMPLIFIER SECTION

The error amplifier is a simple differential-input, transconductance amplifier. The output is the compensation terminal, pin 9, which is a high-impedance node ($R_L \approx 5$ MΩ). The gain is

$$A_V = g_m R_L = \frac{8\, I_C\, R_L}{2kT} \approx .002\, R_L$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from pin 9 to ground, as shown in Figure 5.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 5 show the uncompensated amplifier with a single pole at approximately 200 Hz and a unity gain cross-over at 5 MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series R-C combination between pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50 KΩ plus .001 μF.

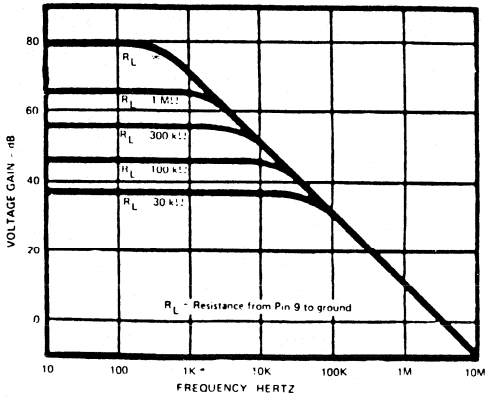


Figure 5. Error Amplifier Frequency Response as a Function of External Resistor, R_L, at Pin 9

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200 μA can pull this point to ground, thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5-volt reference voltage must be divided down as shown in Figure 6. The error amplifier may also be used in fixed duty cycle applications by using the unit gain configuration shown in the open loop test circuit.

CURRENT LIMITING CONTROLS

The current limiting circuitry of the XR-1524 is shown in Figure 7.

By matching the base-emitter voltages of Q1 and Q2, and assuming negligible voltage drop across R_1,

$$\text{Threshold} = V_{BE}(Q1) + I_1 R_2 - V_{BE}(Q2) = I_1 R_2 \approx 200 \text{ mV}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ± 1 volt common mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R_1C_1 and Q1 provides a roll-off pole at approximately 300 Hertz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

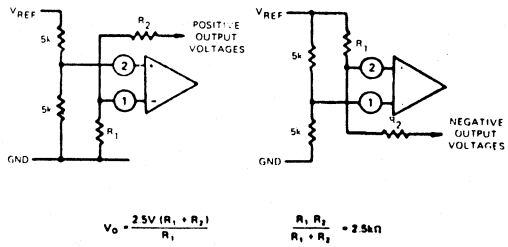


Figure 6. Error Amplifier Biasing Circuits. *(Note: Change in Input Connections for Opposite Polarity Outputs)*

In addition to constant current limiting, pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur. (Refer to Figure 15.) Another application is to ground pin 5 and use pin 4 as an additional shutdown terminal, i.e., the output will be off with pin 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 8. This circuit can reduce the short-

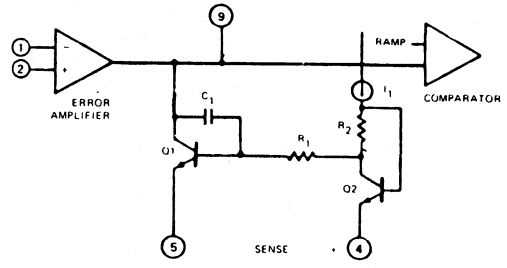


Figure 7. Current Limiting Circuitry of the XR-1524

circuit current (I_{SC}) to approximately one-third the maximum available output current (I_{MAX}).

The shutdown Pin (Pin 10) should be grounded whenever the shutdown circuitry is not used. If the shutdown function is used, Pin 10 should be driven from a low impedance source to prevent noise pickup.

OUTPUT CIRCUITS

The outputs of the XR-1524 are two identical NPN transistors with both collectors and emitters uncommitted. Each output transistor has antisaturation circuitry for fast response, and current limiting set for a maximum output current of approximately 100 mA. The availability of both collectors and emitters allows maximum versatility to enable driving either NPN or PNP external transistors.

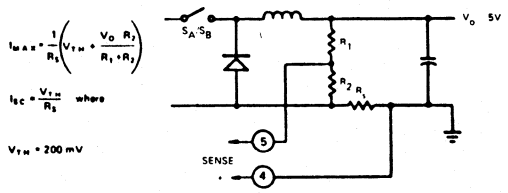


Figure 8. Foldback Current Limiting Can Be Used to Reduce Power Dissipation Under Shorted Output Conditions

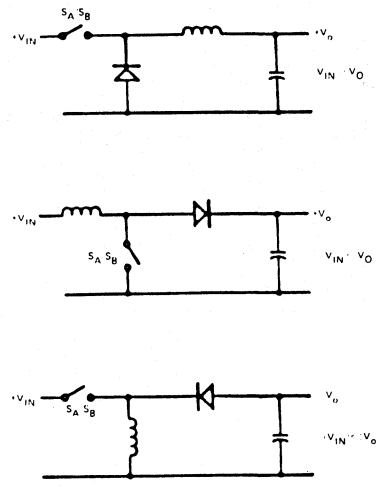


Figure 10. Single-ended Inductor Circuits Where the Two Outputs of the XR-1524 are Connected in Parallel

In considering the application of the XR-1524 to voltage regulator circuitry, there are a multitude of output configurations possible. In general, however, they fall into three basic classifications:

1. Capacitor-diode coupled voltage multipliers
2. Inductor-capacitor single-ended circuits
3. Transformer-coupled circuits

Examples of each category are shown in Figures 9, 10 and 11. In each case, the switches indicated can be either the output transistors in the XR-1524 or added external transistors according to the load current requirements.

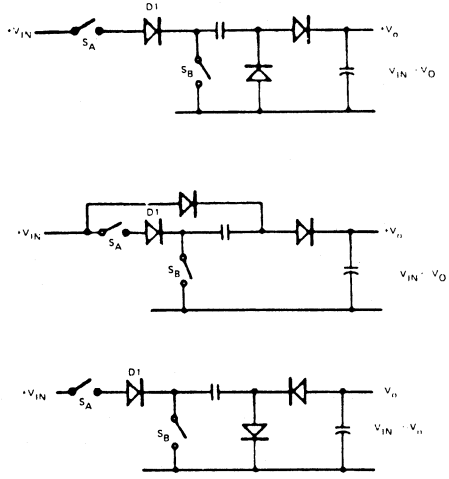


Figure 9. Capacitor-Diode Coupled Voltage Multiplier Output Stages. *(Note: Diode D1 is Necessary to Prevent Reverse Emitter-Base Breakdown of Transistor Switch S_A)*

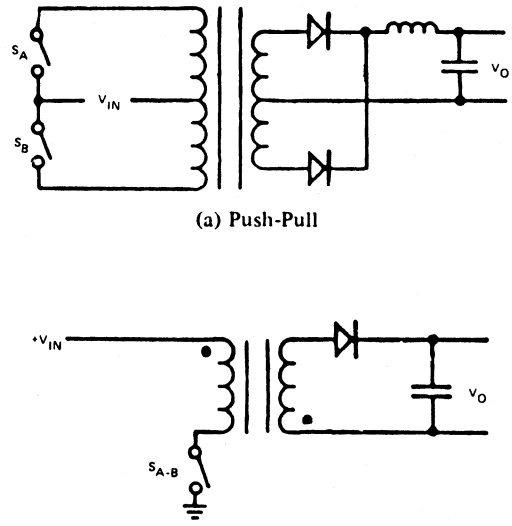


Figure 11. Push-Pull and Flyback Connections for Transformer-Coupled Outputs

DEADBAND CONTROL

The XR-1524 pulse width modulating regulator provides two outputs which alternate in turning on for push-pull inverter applications. The internal oscillator sends a momentary blanking pulse to both outputs at the end of each period to provide a deadband so that there cannot be a condition when both outputs are on at the same time. The amount of deadband is determined by the width of the blanking pulse appearing on pin 3 and can be controlled by any one of the four techniques described below:

Method 1: For 0.2 to 2.0 microseconds, the deadband is controlled by the timing capacitor, C_T, on pin 7. The relationship between C_T and deadband is shown in Figure 4. Of course, since C_T also helps determine the operating frequency, the range of control is somewhat limited.

Method 2: For 0.5 to 5.0 microseconds, the blanking pulse may be extended by adding a small capacitor from pin 3 to ground. The value of the capacitor must be less than 1000 pF or triggering will become unreliable.

Method 3: For longer and more well-controlled blanking pulses, a simple one-shot latch similar to the circuit shown in Figure 12 should be used.

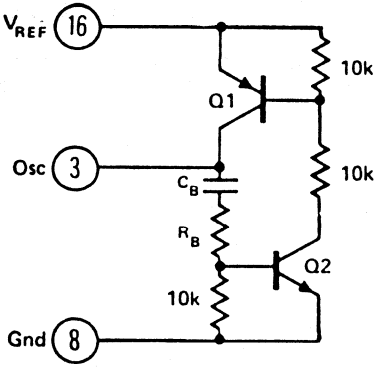


Figure 12. Recommended External Circuitry for Long Duration Blanking Pulse Generation (Method 3 of Deadband Control. *Note: For 5 μsec blanking, choose C_B = 200 pF, R_B = 10 KΩ)*

When this circuit is triggered by the oscillator output pulse, it will latch for a period determined by C_BR_B providing a well-defined deadband.

Another use for this circuit is as a buffer when several other circuits are to be synchronized to one master oscillator. This one-shot latch will provide an adequate signal to insure that all the slave circuits are completely reset before allowing the next timing period to begin.

Note that with this circuit, the blanking pulse holds off the oscillator so its width must be subtracted from the overall period when selecting R_T and C_T

Method 4: Another way of providing greater deadband is just to limit the maximum pulse width. This can be done by using a clamp to limit the output voltage from the error amplifier. A simple way of achieving this clamp is with the circuit shown in Figure 13.

This circuit will limit the error amplifier's voltage range since its current source output will only supply 200 μA. Additionally, this circuit will not affect the operating frequency.

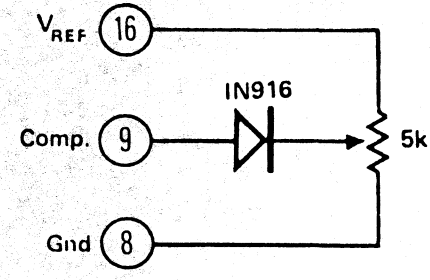


Figure 13. Using a Clamp Diode to Control Deadband (Method 4 of Deadband Control)

APPLICATIONS INFORMATION

POLARITY CONVERTING REGULATOR

The XR-1524 pulse width modulating regulator can be interconnected as shown in Figure 14. The component values shown in the figure are chosen to generate a -5 volt regulated supply voltage from a +15 volt input. This circuit is useful for an output current of up to 20 mA with no additional boost transistors required. Since the output transistors are current limited, no additional protection is necessary. Also, the lack of an inductor allows the circuit to be stabilized with only the output capacitor.

FLYBACK CONVERTER

Figure 15 shows the application of XR-1524 in a low-current DC-DC converter, using the flyback converter principle (see Figure 11b). The particular values given in the figure are chosen to generate ±15 volts at 20 mA from a +5 volt regulated line. The reference generator in the XR-1524 is unused. The reference is provided by the input voltage. Current limiting in a flyback converter is difficult and is accomplished here by sensing current in the primary line and resetting a soft-start circuit.

SINGLE ENDED REGULATOR

The XR-1524 operates as an efficient single-ended pulse width modulating regulator, using the circuit connection shown in Figure 16. In this configuration, the two output transistors of the circuit are connected in parallel by shorting pins (12, 13) and (11, 14) together, respectively, to provide for effective 0 – 90% duty-cycle modulation. The use of an output inductance requires an R-C phase compensation on pin 9, as shown in the figure.

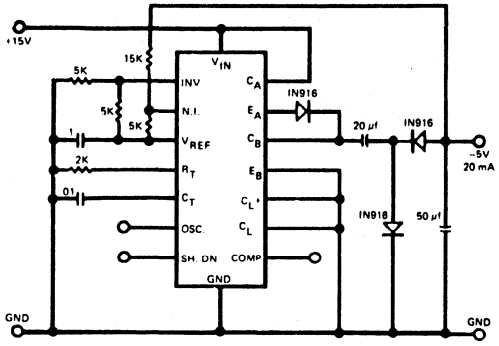


Figure 14. Circuit Connection for Polarity Converting Regulator (V_{in} = +15V, V_{out} = −5V)

PUSH-PULL CONVERTER

The circuit of Figure 17 shows the use of XR-1524 in a transformer-coupled DC-DC converter with push-pull outputs (see Figure 11a). Note that the oscillator must be set at twice the desired output frequency as the XR-1524's internal flip-flop divides the frequency by 2 as it switches the P.W.M. signal from one output to the other. Current limiting is done in the primary. This causes the pulse/width to be reduced automatically if the transformer saturation occurs.

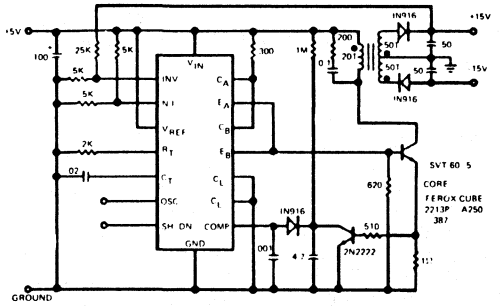


Figure 15. A Low-Current DC-DC Converter Using Flyback Principle (V_{out} = ±15V, V_{in} = +5V, I_L ≤ 20 mA)

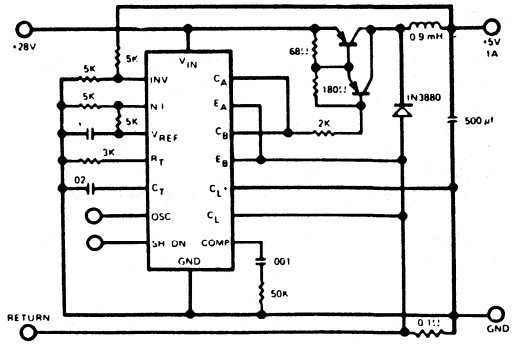


Figure 16. Conventional Single-Ended Regulator Connection (V_{in} = +28V, V_0 = +5V, I_{out} ≤ 1 Amp)

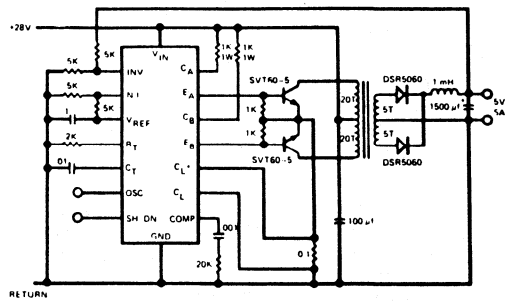


Figure 17. A High-Current DC-DC Converter with Push-Pull Outputs (V_{in} = +28V, V_0 = +5V, I_0 ≤ 5A)

Power Supply Output Supervisory Circuit

GENERAL DESCRIPTION

The XR-1543/2543/3543 are monolithic integrated circuits that contain all the functions necessary to monitor and control the output of a power supply system. Included in the 16-Pin dual-in-line package is a voltage reference, an operational amplifier, voltage comparators, and a high-current SCR trigger circuit. The functions performed by this device include over-voltage sensing, under-voltage sensing and current limiting, with provisions for triggering an external SCR "crowbar."

The internal voltage reference on the XR-1543 and XR-2543 is guaranteed for an accuracy of ±1% to eliminate the need for external potentiometers. The entire circuit may be powered from either the output that is being monitored or from a separate bias voltage.

FEATURES

Over-Voltage Sensing Capability	
Under-Voltage Sensing Capability	
Current Limiting Capability	
Reference Voltage Trimmed	±1%
SCR "Crowbar" Drive	300 mA
Programmable Time Delays	
Open Collector Outputs and Remote Activation Capability	
Total Standby current	Less than 10 mA

APPLICATIONS

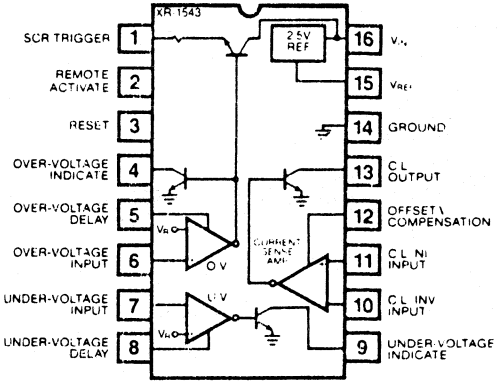
DC/DC Converters
Switch Mode Power Supplies
Power Line Monitors
Linear Power Supplies

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{IN}	40V
Sense Inputs	V_{IN}
SCR Trigger Current (Note 1)	300 mA
Indicator Output Voltage	40V
Indicator Output Sink Current	50 mA
Power Dissipation (Ceramic)	1000 mW
Derate Above T_A = +25°C	8 mW/°C
Power Dissipation (Plastic)	625 mW
Derate Above T_A = +25°C	5 mW/°C
Operating Junction Temperature (T_J)	+150°C
Storage Temperature Range	−65°C to +150°C

Note 1: At higher input voltages, a dissipation limiting resistor, R_G, is required.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1543M	Ceramic	−55°C to +125°C
XR-2543N	Ceramic	−25°C to +85°C
XR-3543CN	Ceramic	0°C to +70°C
XR-3543CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

An output supervisory circuit, such as the XR-1543, is used to control and monitor the performance of a power supply. In many systems, it is crucial that the supply voltage is always within some minimum and maximum level, to guarantee proper performance, and to prevent damage to the system. If the supply voltage is out of tolerance, it is often desirable to shut down the system or to have some form of indication to the operator or system controller. As well as protecting the system, the power supply sometimes needs to be protected under short circuit and current overload situations. By providing an SCR "crowbar" on the output of a power supply, it can be shut off under certain fault conditions as well.

The over-voltage sensing circuit (O.V.) can be used to monitor the output of a power supply and provide triggering of an SCR, when the output goes above the prescribed voltage level. The under-voltage sensing circuit (U.V.) can be used to monitor either the output of a power supply or the input line voltage.

5

XR-15/25/3543

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{IN} = 10V, T_A = 25°C unless otherwise specified. Refer to Figure 9 for component designation.

PARAMETERS	XR-1543/2543			XR-3543			UNIT	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
Input Voltage Range	4.5		40	4.5		40	V	T_A = 25°C
Input Voltage Range	4.7		40	4.7		40	V	T_T = min to max *
Supply Current		7	10		7	10	mA	T_A = 25°C, V_{IN} = 40V
REFERENCE VOLTAGE SECTION (Pins 15 and 16)								
Output Voltage	2.48	2.50	2.52	2.45	2.50	2.55	V	T_A = 25°C
Output Voltage	2.45		2.55	2.40		2.60	V	T_T = min to max *
Line Regulation		1	5		1	5	mV	V_{IN} = 5 to 30V
Load Regulation		1	10		1	10	mV	I_{ref} = 0 to 10 mA
Short Circuit Current		15			15		mA	V_{ref} = 0V
Temperature Stability		50			50		ppm/°C	
SCR TRIGGER SECTION (Pins 1, 2, and 3)								
Peak Output Current	100	200	400	100	200	400	mA	V_{IN} = 5V, R_G = 0Ω, V_O = 0
Peak Output Voltage	12	13		12	13		V	V_{IN} = 15V, I_O = 100 mA
Output OFF Voltage		0	0.1		0	0.1	V	V_{IN} = 40V
Remote Activate Current		0.4	0.8		0.4	0.8	mA	Pin 2 = GND
Remote Activate Voltage		2	6		2	6	V	Pin 2 = Open
Reset Current		0.4	0.8		0.4	0.8	mA	Pin 2 = GND, Pin 3 = GND
Reset Voltage		2	6		2	6	V	Pin 2 = GND, Pin 3 = Open
Output Current Slew Rate		400			400		mA/μs	T_J = 25°C, R_L = 50Ω, C_D = 0
Propagation Delay Time (From Pin 2)		300			300		nsec	T_J = 25°C, R_L = 50Ω C_D = 0, Pin 2 = 0.4V
Propagation Delay Time (From Pin 6)		500			500		nsec	T_J = 25°C, R_L = 50Ω, C_D = 0, Pin 6 = 2.7V
COMPARATOR SECTIONS (Pins 4, 5, 6, 7, 8, and 9)								
Input Threshold (Input Voltage Rising on Pin 6 and	2.45	2.50	2.55	2.40	2.50	2.60	V	T_T = min to max *
Falling on Pin 7)	2.40		2.60	2.35		2.65	V	T_J = 25°C
Input Hysteresis		25			25		mV	
Input Bias Current		0.3	1.0		0.3	1.0	μA	Sense input = 0V
Delay Saturation		0.2	0.5		0.2	0.5	V	
Delay High Level		6	7		6	7	V	
Delay Charging Current	200	250	300	200	250	300	μA	V_D = 0V
Indicate Saturation Voltage		0.2	0.5		0.2	0.5	V	I_L = 10 mA
Indicate Leakage Current		0.01	1.0		0.01	1.0	μA	V_{out} = 40V
Propagation Delay Time		400			400		nsec	C_D = 0 Pin 6 = 2.7V Pin 7 = 2.3V
Propagation Delay Time		10			10		msec	C_D = 1 μF T_J = 25°C
CURRENT LIMIT AMPLIFIER SECTION (Pins 10, 11, 12, and 13)								
Input Voltage Range	0		V_{IN} − 3V	0		V_{IN} − 3V	V	
Input Bias Current		0.3	1.0		0.3	1.0	μA	Pin 12 = Open, V_{CM} = 0V
Input Offset Voltage		0	10		0	15	mV	Pin 12 = Open, V_{CM} = 0V
Input Offset Voltage	80	100	120	70	100	130	mV	Pin 12 = 10 kΩ to GND
Common Mode Rejection Ratio	60	70		60	70		dB	V_{IN} = 15V, 0 ≤ V_{CM} ≤ 12V
Open Loop Gain	72	80		72	80		dB	V_{CM} = 0V, Pin 12 = Open
Output Saturation Voltage		0.2	0.5		0.2	0.5	V	I_L = 10 mA
Output Leakage Current		0.01	1.0		0.01	1.0	μA	V_{out} = 40V
Small Signal Bandwidth		5			5		MHz	T_J = 25°C, Av = 0 dB
Propagation Delay Time		200			200		nsec	T_J = 25°C, $V_{overdrive}$ = 100 mV

* These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production for XR-3543.

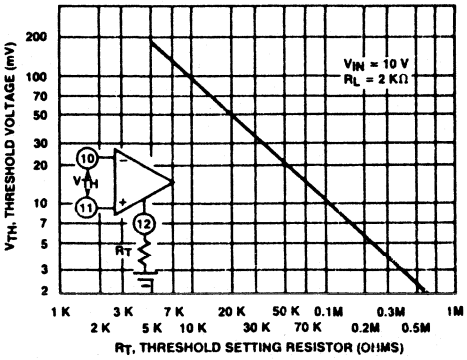


Figure 1. Typical Current Threshold (V_{TH}) vs. Threshold Setting Resistor (R_T)

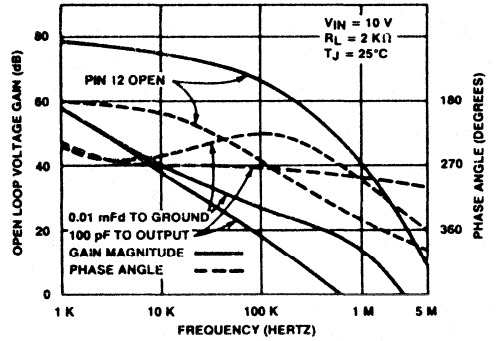


Figure 2. Current Limiting Amplifier—Frequency Response

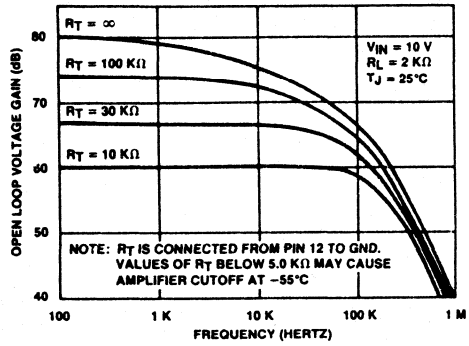


Figure 3. Current Limiting Amplifier Gain vs. Threshold Setting Resistor (R_T

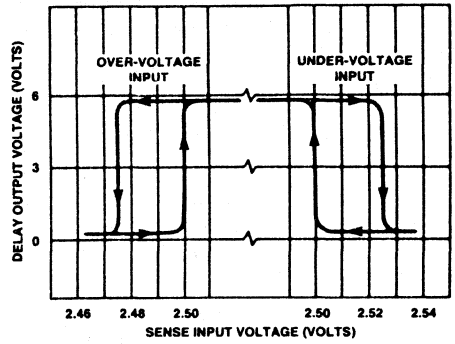


Figure 4. Over-Voltage and Under-Voltage Comparator Hysteresis

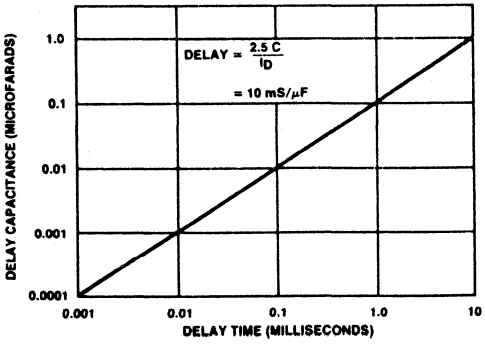


Figure 5. Comparator Activation Delay vs. Capacitor Value

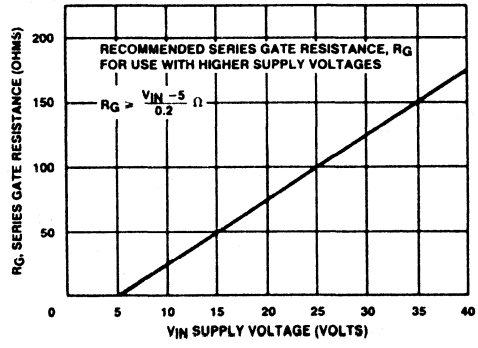


Figure 6. SCR Trigger—Series Gate Resistance (R_G) vs. Input Voltage

PRINCIPLES OF OPERATION

The internal control blocks of the XR-1543 operate as follows:

Voltage Reference Section

The internal voltage reference circuit of the XR-1543 is based on the well-known "band-gap reference" with a nominal output voltage of 2.50 volts, internally trimmed to give an accuracy of ± 1% at 25°C. It is capable of providing a stable output voltage over a wide input voltage range. Furthermore, its performance is guaranteed for changes in line and load conditions. The accuracy of the output voltage is guaranteed to ± 2% maximum for the XR-1543/2543, and ± 4% maximum for the XR-3543, over the entire operating temperature range.

The output of the reference circuit is capable of providing up to 10 mA of current for use as a reference for external circuitry. The primary function of this circuit is to provide a very accurate and stable reference input for the under-voltage and over-voltage comparators, thereby enabling very precise monitoring of line and output voltages without potentiometers.

Comparator Section

The under-voltage and over-voltage sensing comparators of the XR-1543 are identical except for the input polarities. Each section is made up of two comparators in series whose inputs are referenced to 2.50 volts. The delay terminal between the comparators requires an external capacitor to ground for programmable time delays on the output.

When an out-of-tolerance situation occurs, the first comparator activates a current source which then charges the external capacitor at a constant rate. This ramp voltage is then compared to the reference voltage by the second comparator which activates the output indicating circuit. With no external capacitor, the overall time delay from sense input to output is approximately 0.5 μsec. The charging current for the capacitor, C_D, is approximately 250 μA which results in the following relationship:

$$\text{Time delay} = 10\ C_D\ (\text{msec})$$

where C_D is in μF.

The output npn transistors are capable of sinking 10 mA with saturation voltage of less than 0.4 volts. The outputs can be "wired OR'd" to provide a single output indicator. The maximum recommended R_4 pull up resistor volume is 1K so when pulled up to $+5V_{DC}$.

Current Sensing Amplifier

The operational amplifier used in the XR-1543 is a high-gain, externally compensated amplifier with open collector outputs. The pnp input stage provides for a wide input common mode range extending from ground to approximately 3 volts below the positive supply. With a 2 kΩ pull-up resistor, the open-loop voltage gain is 72 dB minimum with a unity gain bandwidth beyond 5 MHz. The operational amplifier may be used as a comparator or, if linear amplification is required, external compensation may be added for stable performance over a wide frequency range.

The input offset voltage of this amplifier is specified for 10 mV maximum; however, it may be programmed externally for thresholds up to 200 mV. By connecting a resistor, R_T, from Pin 12 to ground, the input threshold voltage can be varied. For most current sensing applications, the required threshold polarity calls for a positive voltage on the inverting input. Reducing the impedance on Pin 12 also lowers the overall voltage gain of the amplifier, which makes this pin a convenient point to apply frequency compensation. This can be accomplished by either connecting C_1 to the output, or C_2 to ground as shown in Figure 8. The diode, D_1, and the resistor, R_C, are used only if it is necessary to increase the frequency response by operating the output at a higher current and/or isolating the load from R_C and C_1, when the amplifier is off.

SCR Trigger Section

The SCR trigger section of the XR-1543 is connected to the output of the over-voltage comparator and is capable of handling 300 mA. The circuit also provides for remote activation of the output as well as a reset terminal. When an over-voltage situation occurs, the output of the sensing comparator goes low, turning "on" the over-voltage indicate transistor. At the same time, the comparator drives an npn Darlington pair which provides 300 mA to activate an external SCR crowbar.

A remote activation circuit is included to allow the user to activate the SCR crowbar in other than an over-voltage situation. When this terminal, Pin 2, is grounded, it forces the output of the comparator low which activates the output circuitry in the same manner as the over-voltage comparator does. Figure 9 and 11 shows one possible SCR application. RG is dependent upon the V_{SUPPLY} to prevent>300 mA of current flow and to prevent exceeding the power dissipation rating of the XR-1543/2543/3543.

Another function of this circuit is to provide the capability to latch the O.V. indicate and SCR trigger outputs "on", after a fault is sensed. This is done by connecting the remote activate terminal (Pin 2) to the O.V. indicating terminal (Pin 4). When an O.V. condition occurs, Pin 2 is pulled low, which in turn holds the outputs in the "on" condition until the reset terminal is externally grounded, removing the latch and turning "off" the outputs. If the external connection is not made, the high current output will be activated only as long as a fault condition exists. When the fault condition disappears, the outputs will be disabled. The thresholds for both remote activation and reset terminals are approximately 1.2 volts.

EQUIVALENT SCHEMATIC DIAGRAM

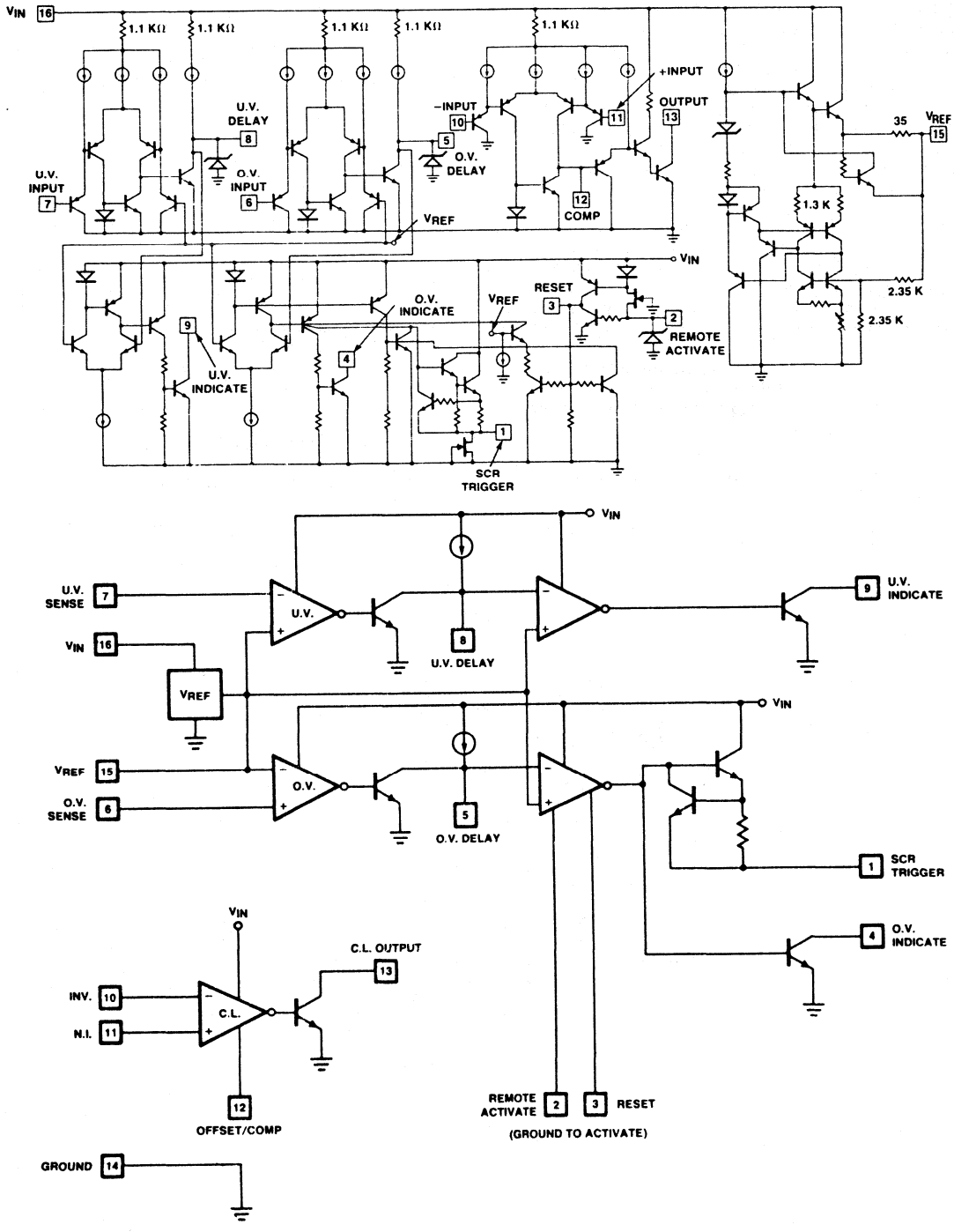


Figure 7. XR-1543 Block Diagram

APPLICATIONS INFORMATION

A typical application of the XR-1543 is to monitor a single power supply output voltage as shown in Figure 9. In this circuit, both over- and under-voltage sensing and current-limiting functions are performed. The circuit shown is powered from an external bias capable of supplying 10 mA in addition to the activation current for the SCR trigger. With Pin 2 tied to Pin 4, a latch has been provided such that when an over-voltage situation occurs, the o.v. indicator and SCR trigger are activated and held until the reset terminal is externally grounded.

In powering an SCR from supply voltages greater than 5 volts, an external resistor, R_G, is required on Pin 1 to limit the power dissipation for the XR-1543. Although the XR-1543 is capable of handling 300 mA of current, its power dissipation must be kept below the absolute maximum ratings.

In this circuit, current-limiting is performed by sensing the voltage drop across the resistor, R_{SC}, in the positive supply line. The threshold for the amplifier is externally set by the resistor, R_T

The values of the external components used in Figure 9 are calculated as follows:

1. Current limiting threshold, $V_{TH} \approx \frac{1000}{R_T}$
2. C_1 is determined by the loop dynamics.
3. Peak current to load,

$$I_p \approx \frac{V_{TH}}{R_{SC}} + \frac{V_O}{R_{SC}}\left(\frac{R_2}{R_2 + R_3}\right)$$

4. Short circuit current,

$$I_{SC} = \frac{V_{TH}}{R_{SC}}$$

5. Low output voltage limit,

$$V_O \text{ (low)} = \frac{2.5(R_4 + R_5 + R_6)}{R_5 + R_6}$$

6. High output voltage limit,

$$V_O \text{ (high)} = \frac{2.5(R_4 + R_5 + R_6)}{R_6}$$

7. Voltage sensing delay, $T_D = 10{,}000\ C_D$
8. SCR trigger power limiting resistor,

$$R_G > \frac{V_{IN} - 5}{0.2}$$

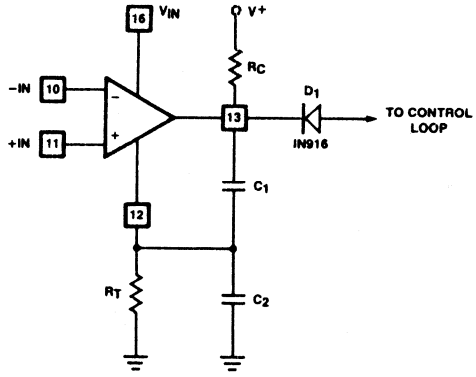


Figure 8. Current Limiting Amplifier Connections for Threshold Control and Frequency Compensation

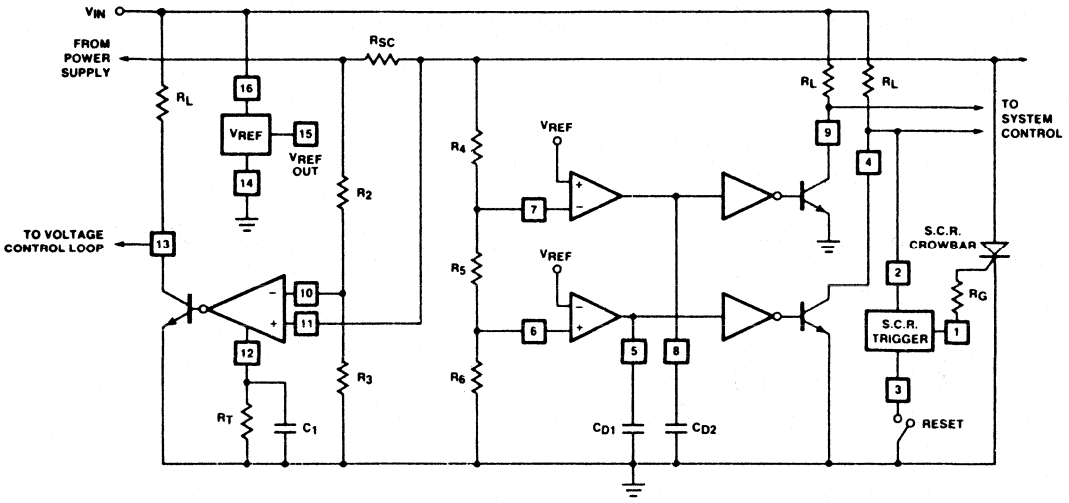


Figure 9. Typical Connection for Linear Foldback Current Limiting as well as Over-Voltage and Under-Voltage Protection.

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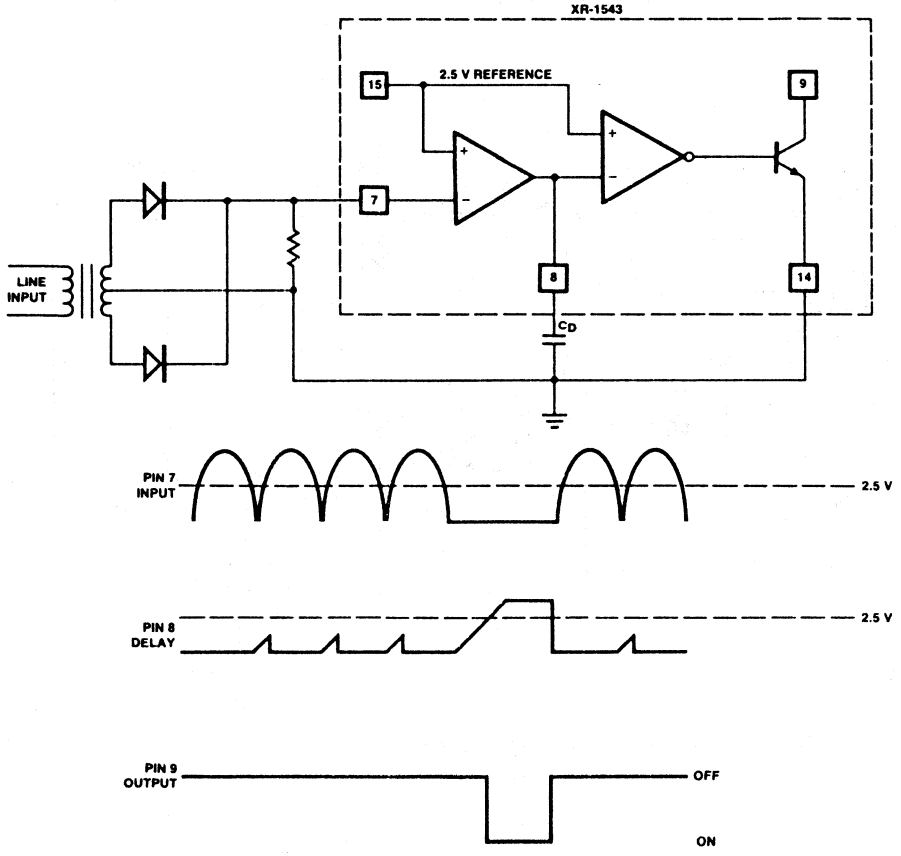


Figure 10. XR-1543—Input Line Monitor Circuit

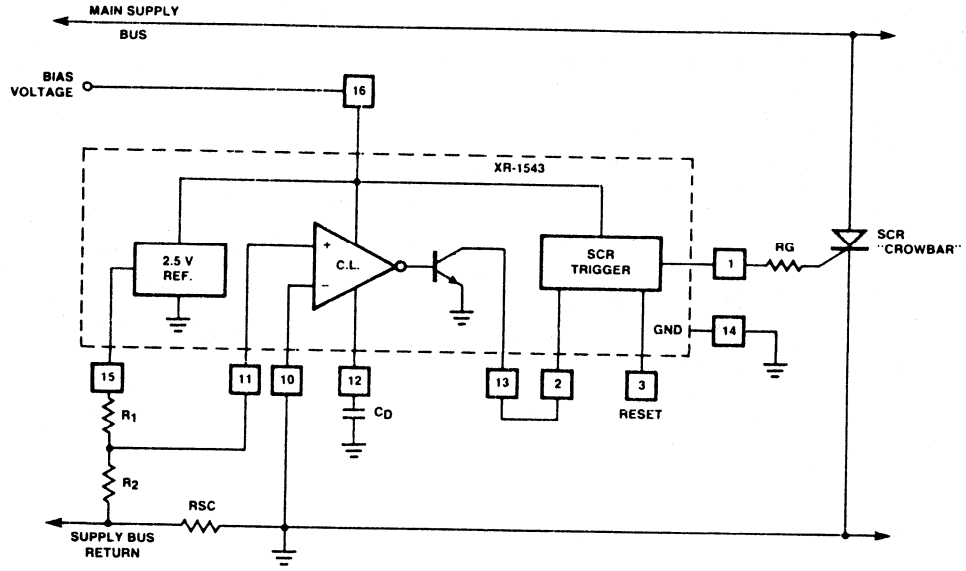


Figure 11. XR-1543—Over Current Shutdown Circuitry

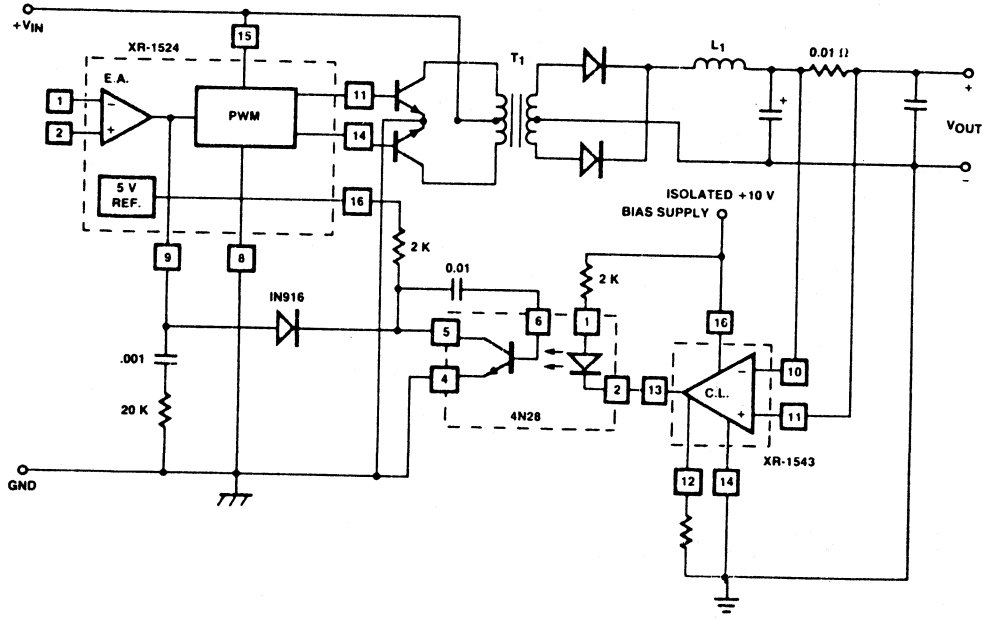


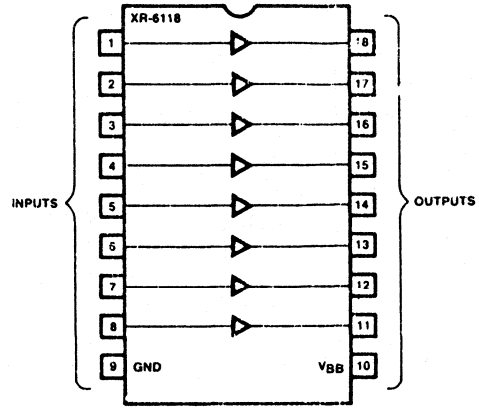
Figure 12. XR-1543 - DC Converter with Isolated Current Limiting

Fluorescent Display Drivers

GENERAL DESCRIPTION

The XR-6118 is a high-voltage display driver array which is designed to interface between low-level digital logic and vacuum fluorescent displays. The circuit consists of eight independent signal channels comprised of Darlington output stages and common-emitter type inputs. All stages on the chip share common power supply and ground connections. The device is capable of driving digits and/or segments of fluorescent displays, and all of the eight outputs can be activated simultaneously.

PIN ASSIGNMENT



FEATURES

Direct Replacement for Sprague UDN-6118A, and UDN-6118P-2 (60V)
Digit or Segment Drive Capability
Low Input Current
Integral Output Pulldown Resistors
Low Power
High Output Breakdown Voltage

ORDERING INFORMATION

Part Number	Package	Operating Temp
XR-6118P	Plastic	0°C to +70°C
XR-6118P-2	Plastic	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{BB}	85V
Output Voltage, V_{OUT}	85V
Input Voltage, VIN	20V
Output Current, I_{OUT}	40 mA
Power Dissipation, ($T_A \leq 25°C$)	1 W
Derate Above 25°C	8 mW/°C
Operating Temperature	0°C to +85°C
Storage Temperature	-55°C to +150°C

SYSTEM DESCRIPTION

The XR-6118 is a fluorescent display driver which can switch up to 85V and 40mA. Inputs are protected to 20V. The XR-6118 is compatible with TTL, Schottky TTL, DTL and 5 Volt CMOS logic families. The output load is activated when the inputs are pulled toward positive supply. Output pulldown resistors are included on the die.

ELECTRICAL CHARACTERISTICS

Test Conditions: (T_A = 25°C, V_{BB} = 80V) Full Temp. Range 0°C to +70°C, XR-6118A only. V_{BB} = 60V for XR-6118 P-2.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
ICEX	Output Leakage Current			15	µA	V_{IN} = 0.4V
VOUT	Output ON Voltage	77			V	I_{OUT} = 25 mA V_{IN} = 2.4 V (XR-6118)
	Input ON Voltage	2.4		15	V	I_{OUT} = 25 mA
	Input ON Current			650	µA	V_{IN} = 5V (XR-6118)
I_{BB} (OFF)	Supply Current OFF Condition			100	µA	All Inputs Open
I_{BB} (ON)	ON Condition			9	mA	V_{IN} = 2.4V (XR-6118) (All Inputs)
I_{OUT}	Output Pulldown			1100	µA	All Inputs Open V_{OUT} = 80V

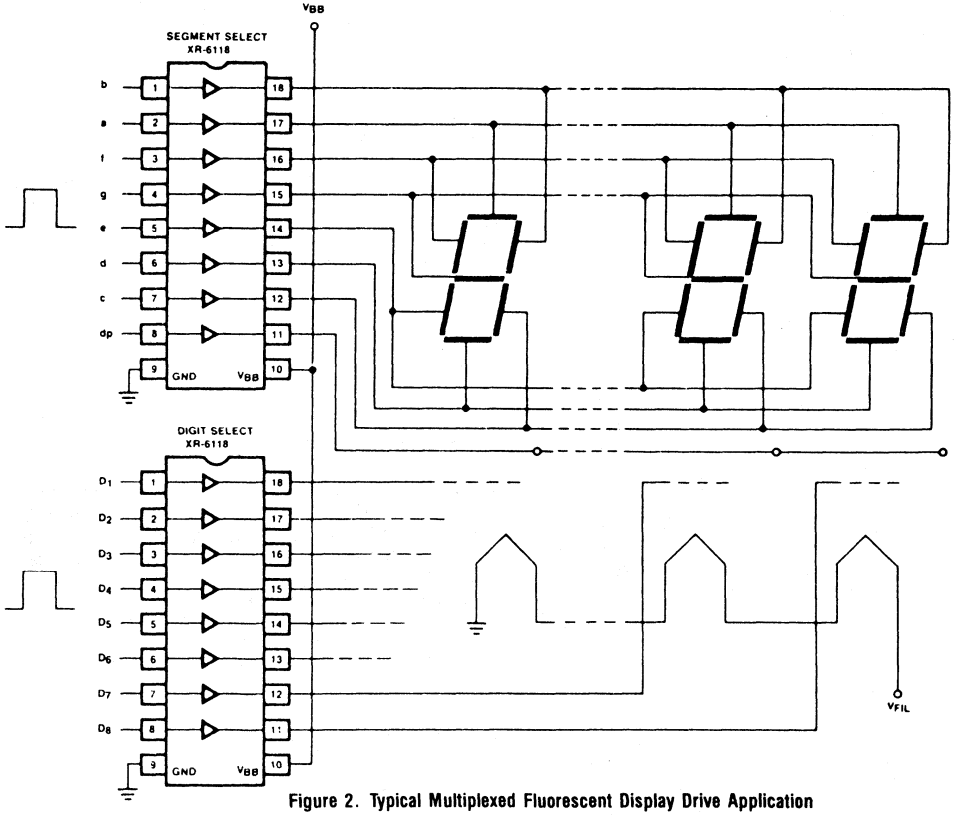
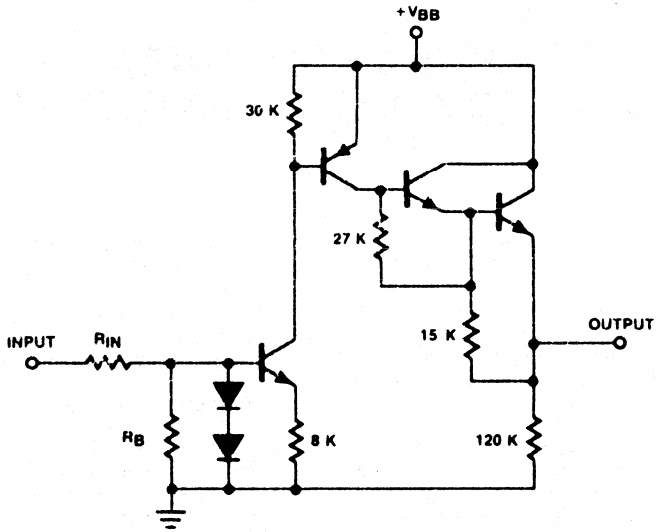


Figure 2. Typical Multiplexed Fluorescent Display Drive Application



One of Eight Stages

R_{IN} = 10 K, R_B = 30 K

EQUIVALENT SCHEMATIC DIAGRAM

Stable FSK Modems featuring the XR-2207, XR-2206 and XR-2211

INTRODUCTION

Frequency-shift keying (FSK) is the most commonly used method for transmitting digital data over telecommunications links. In order to use FSK, a modulator/demodulator (modem) is needed to translate digital 1's and 0's into their respective frequencies and back again. This application note describes the design of a modem using state-of-the-art Exar devices specifically intended for modem application.

The devices featured in this application note are the XR-2206 and XR-2207 FSK Modulators, and the XR-2211 FSK demodulator with carrier detect capability. Because of the superior frequency stability of these devices (typically 20 ppm/°C), a properly designed modem will be virtually free of the temperature and voltage-dependent drift problems associated with many other designs. In addition, the demodulator performance is independent of incoming signal strength variation over a 60 dB dynamic range. Because bias voltages are generated internally, the external parts count is much lower than in most other designs. The modem designs shown in this application note can be used with mark and space frequencies, anywhere from several Hz to 100 kHz.

PRINCIPLES OF OPERATION

THE XR-2206 FSK MODULATOR

FEATURES

Typically 20 ppm/°C Temperature Stability
Choice of 0.5% THD Sine Wave, Triangle, or Square Wave Output
Phase-Continuous FSK Output
Inputs are TTL and CMOS Compatible
Low-Power Supply Sensitivity (0.01%)

Low-Power Supply Sensitivity (0.01%/V)
Split or Single Supply Operation
Low External Parts Count

The XR-2206 is ideal for FSK applications requiring the spectral purity of a sinusoidal output waveform. It offers TTL and CMOS compatibility, excellent frequency stability, and ease of application. The XR-2206 can typically provide a 3-volt p-p sine wave output. Total harmonic distortion can be trimmed to 0.5%. If left untrimmed, it is approximately 2.5%.

The circuit connection for the XR-2206 FSK Generator is shown in Figure 1. The data input is applied to Pin 9. A high-level signal selects the frequency ($1/R_6C_3$) Hz; a low level signal selects the frequency ($1/R_7C_3$) Hz, (resistors in ohms and capacitors in farads). For optimum stability, R_6 and R_7 should be within the range of 10 kΩ to 100 kΩ. The voltage applied to Pin 9 should be selected to fall between ground and V+.

Note: Over and under voltage may damage the device.

Potentiometers, R_8 and R_9, should be adjusted for minimum total harmonic distortion. In applications where minimal distortion is unnecessary, Pins 15 and 16 may be left open-circuited and R_8 may be replaced by a fixed 200Ω resistor.

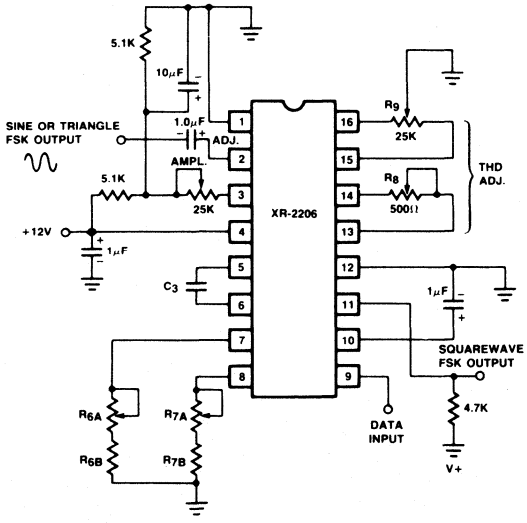


Figure 1. The XR-2206 Sinusoidal FSK Generator.

In applications where a triangular output waveform is satisfactory, Pins 13 through 16 may be left open-circuited.

The output impedance at Pin 2 is about 600Ω, with ac coupling normally being used, in single supply operation.

THE XR-2207 FSK MODULATOR

FEATURES

Typically 20 ppm/°C Temperature Stability
Phase-Continuous FSK Output
Provides Both Triangle and Square Wave Outputs
Operates Single-Channel or Two-Channel Multiplex
Inputs are TTL and CMOS Compatible
Split- or Single-Power Supply Operation
Low-Power Supply Sensitivity (0.15%/V)
Low External Parts Count

The XR-2207 is a stable FSK generator which is designed for those applications where only a triangle or square wave output is required. It is capable of either single-channel or two-channel multiplex operation, and can be used easily with either split- or single-power supplies.

Figure 2 shows the XR-2207 using a single-supply and Figure 3 shows split-supply operation. When used as an FSK modulator, Pin 8 and 9 provide the digital inputs. When the 2207 is used with a split-supply, the threshold at these pins is approximately +2 volts, which is a level that is compatible with both TTL and CMOS logic forms. When used with a single-supply, the threshold is near mid-supply and is CMOS compatible. Table 1 shows how to select the timing resistors, R_1 through R_4, to determine the output frequency based on the logic levels applied to Pin 8 and 9. For optimum stability, the values of R_1 and R_3 should be selected to fall between 10 kΩ and 100 kΩ.

With Pin 8 grounded, Pin 9 serves as the data input. A high-level signal applied to Pin 8 will disable the oscillator. When used in this manner, Pin 8 of the XR-2207 serves as the channel select input. For two-channel multiplex operation, Pin 4 and 5 should be connected as shown by the dotted lines. (For single channel operation, Pin 4 and 5 should be left open-circuited.)

The XR-2207 provides two outputs: a square wave at Pin 13 and a triangle wave at Pin 14. (For safe operation, current into Pin 13 should be limited to 20 mA.) When used with a split-supply, the triangle wave peak-to-peak amplitude is equal to V^- and the dc level is near ground. Direct coupling is usually used. With a single-supply, the peak-to-peak amplitude is approximately equal to one-half/V^+, the dc level is approximately at mid-supply, and ac coupling is usually necessary. In either case, the output impedance is typically 10Ω and is internally protected against short circuits.

The square wave output has an npn open-collector configuration. When connected as shown in Figure 2 and 3, this output voltage will swing between V^+ and the voltage at Pin 12.

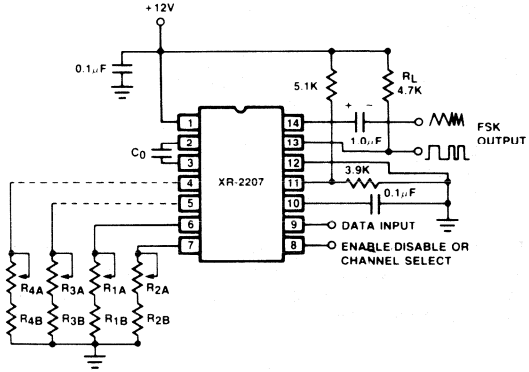


Figure 2. The XR-2207 FSK Modulator Single-Supply Operation.

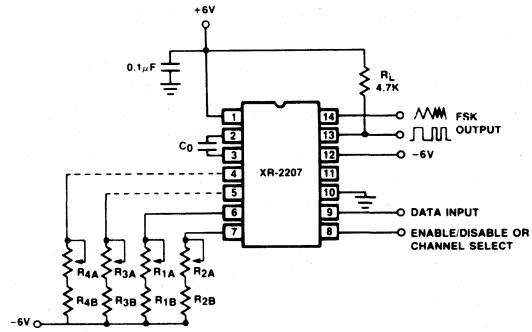


Figure 3. The XR-2207 FSK Modulator Split-Supply Operation.

Table 1.
XR-2207 FSK Input Control Logic

Logic Level		Active Timing Resistor	Output Frequency
Pin 8	Pin 9		
L	L	Pin 6	$\frac{1}{C_0R_1}$
L	H	Pins 6 and 7	$\frac{1}{C_0R_1} + \frac{1}{C_0R_2}$
H	L	Pin 5	$\frac{1}{C_0R_3}$
H	H	Pin 4 and 5	$\frac{1}{C_0R_3} + \frac{1}{C_0R_4}$

Units: Resistors — Ohms; Capacitors — Farads; Frequency — Hz

The XR-2211 FSK DEMODULATOR

FEATURES

Typically 20 ppm/°C Temperature Stability
Simultaneous FSK and Carrier-Detect Output
Outputs are TTL and CMOS Compatible
Wide Dynamic Range (2 mV to 3V rms)
Split or Single Supply Operation
Low-Power Supply Sensitivity (0.05%/V)
Low External Parts Count

The XR-2211 is an FSK demodulator which operates on the phase-locked loop principle. Its performance is virtually independent of input signal strength variations, over the range of 2 mV to 3V rms.

Figure 4 shows the circuit connection for the XR-2211. The center frequency is determined by $f_0 = (1/C_1R_4)$ Hz, where capacitance is in farads and resistance is in ohms. Calculation for f_0 should fall mid-way between the mark and space frequencies.

The tracking range ($\pm\Delta f$) is the range of frequencies over which the phase-locked loop can retain lock with a swept input signal. This range is determined by the formula: $\Delta f = (R_4 f_0/R_5)$ Hz. Δf should be made equal to, or slightly less than, the difference between the mark and space frequencies. For optimum stability, choose an R_4 between 10 kΩ and 100 kΩ.

The capture range ($\pm\Delta f_C$) is the range of frequencies over which the phase-locked loop can acquire lock. It is always less than the tracking range. The capture range is limited by C_2, which, in conjunction with R_5, forms the loop filter time constant. In most modem applications, Δf_C = (80%—99%) Δf.

The loop-damping factor (ζ) determines the amount of overshoot, undershoot, or ringing present in the phase-locked loop's response to a step change in frequency. it is determined by $\zeta = 1/4\sqrt{C_1/C_2}$. For most modem applications, choose $\zeta \approx 1/2$.

The FSK output filter time constant (τ_F) removes chatter from the FSK output. The formula is: $\tau_F = R_F C_F$. Normally calculate τ_F to be approximately equal to [3/(baud rate)] seconds.

The lock-detect filter capacitor (C_D) removes chatter from the lock-detect output. With R_D = 510 kΩ, the minimum value of C_D can be determined by: $C_D(\mu f) \approx$ 16/capture range in Hz.

Note: Excessive values of C_D will unnecessarily slow the lock-detect response time.

The XR-2211 has three npn open-collector outputs, each of which is capable of sinking up to 5 mA. Pin 7 is the FSK data output, Pin 5 is the Q lock-detect output which goes low when a carrier is detected, and Pin 6 is the Q lock-detect output which goes high when lock is detected. If Pin 6 and 7 are wired together, the output signal from these terminals will provide data when FSK is applied, and will be LOW when no carrier is present.

If the lock-detect feature is not required, Pins 3, 5 and 6 may be left open-circuited.

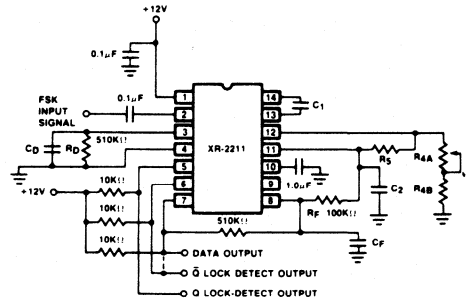
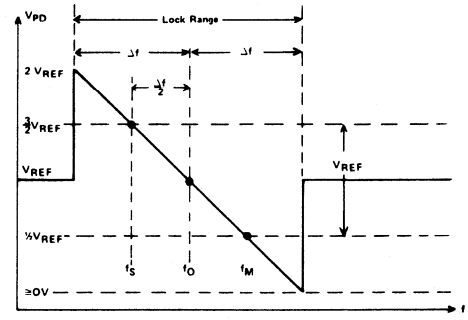


Figure 4: The XR-2211 FSK Demodulator with Carrier Detect



XR-2211 TRACKING CHARACTERISTICS

As seen above, the XR-2211 produces at its phase detector output a voltage V_{PD}, which has a peak to peak value equal to about V_{REF} for a frequency swing from f_M (mark) to F_S (space). The DC level V_{PD} will be about $V_{REF}\left(\frac{V+}{2} - .65\right)$.

CIRCUIT DESIGN

Table 2 shows recommended component values for the three most commonly used FSK bands. In many instances, system constraints dictate the use of some non-standard FSK bands. The XR-2206/XR-2207/XR-2211 combination is suitable for any range of frequencies from several Hertz to 100 kiloHertz.

Here are several guidelines to use when calculating non-standard frequencies:

- For maximum baud rate, choose the highest upper frequency that is consistent with the system bandwidth.
- The lower frequency must be at least 55% of the upper frequency (less than a 2:1 ratio).
- For minimum demodulated output pulse-width jitter, select an FSK band whose mark and space frequencies are both high, compared to the baud rate. (i.e., for a 300 baud channel, mark and space frequencies of 2025 Hz and 2225 Hz would result in significantly less pulse-width jitter than 300 Hz and 550 Hz).
- For any given pair of mark and space frequencies, there is a limit to the baud rate that can be achieved. When maximum spacing between the mark and space frequencies is used (where the ratio is close to 2:1) the relationship

$$\frac{\text{mark-space frequency difference (Hz)}}{\text{maximum data rate (baud)}} \geq 83\%$$

should be observed.

For narrower spacing, the minimum ratio should be **about 67%. As spacing is reduced, tuning difficulties (of the XR-2211) increase. Signal-to-noise performance will be degraded as well.**

The values shown in Table 2 may be scaled proportionately for mark and space frequencies, maximum baud rate, and (inversely) capacitor value. It is best to retain (approximately) the resistor values shown.

DESIGN EXAMPLES

I. Design a modem to handle a 10 kilobaud data rate, using the minimum necessary bandwidth.

A. Frequency Calculation
Because we want to use the minimum possible bandwidth (lowest possible upper frequency) we will use a 55:100 frequency ratio. The frequency difference, or 45% of the upper frequency, will be 83% of 10,000. We therefore chose an upper frequency:

$$\frac{83 \times 10{,}000}{45} = 18.444 \text{ kHz} \approx 18.5 \text{ kHz}.$$

and the lower frequency:

$$0.55 \times 18.5 \text{ kHz} = 10.175 \text{ kHz}.$$

B. Component Selection
1. For the XR-2207 FSK modulator, set $R_1 \approx 30$ kΩ. Now, select a value of C_o to generate 10.175 kHz with R_1:

$$10.175 \text{ kHz} = 1/(C_o \times 30{,}000);\ C_o = 3300\text{pF}.$$

To choose R_2:

$$18.500 \text{ khz} - 10.175 \text{ kHz} = 8.325 \text{ kHz} = 1/C_oR_2;\ R_2 = 36 \text{ k}\Omega.$$

A good choice would be to use 10 kΩ potentiometers for R_{1A} and R_{2A}, and to set $R_{1B} = 24$ kΩ and $R_{2B} = 30$ kΩ.

2. For the XR-2206, we can make R_7 equal to R_1, and C_3 equal to C_0 above. To determine R_6:

$$18.5 \text{ kHz} = 1/R_6C_3;\ R_6 = 16 \text{ k}\Omega$$

Use at 10 kΩ potentiometer for R_{6A} and set $R_{6B} = 13$ kΩ.

5

Table 2.
Recommended Component Values for Typical FSK Bands VCC = 12 VDC VEE = 0V

FSK Band			XR-2207					XR-2206					XR-2211						
Baud Rate	f_L	f_H	R_{1A} R_{3A}	R_{1B} R_{3B}	R_{2A} R_{4A}	R_{2B} R_{4B}	C_0	R_{6A}	R_{6B}	R_{7A}	R_{7B}	C_3	R_{4A}	R_{4B}	R_5	C_1	C_2	C_F	C_D
300	1070	1270	10	20	100	100	.039	10	18	10	20	.039	10	18	100	.039	.01	.005	.05
300	2025	2225	10	18	150	160	.022	10	16	10	18	.022	10	18	200	.022	.0047	.005	.05
1200	1200	2200	20	30	20	36	.022	10	16	20	30	.022	10	18	30	.027	.0033	.0022	.01

Units: Frequency — Hz; Resistors — kΩ; Capacitors — μF

3. For the XR-2211 demodulator, we need to first determine R_4 and C_1. First, $f_o = (f_L + f_H)/2 = (10.175 + 18.500)/2 = 14.338$ kHz. If we make $R_4 = 25$ kΩ, then $1/(C_1 \times 25{,}000) = 14{,}338$; $C_1 = 2790$ pF ≈2700 pF. With that value of C_1, the precise value of R_4 is now 25.8 kΩ. Select $R_{4B} = 18$ kΩ and use a 10 kΩ for R_{4A}.

C. Frequency Component Selection
1. To calculate R_5, we first need our Δf, which is 18,500 — 10.175, or 8.325 kHz:

$$8325 = (25{,}800 \times 14{,}338)/R_5$$
$$R_5 = 44.4\ k\Omega \approx 47\ k\Omega.$$

2. To determine C_2 use $\zeta = 1/2 = 1/4\ \ C_1/C_2$. Then, $C_2 = 1/4C_1$; $C_2 = 670$ pF:

3. To select C_F, we use τ_F = [0.3/(baud rate)] seconds:

$$\tau_F = 3/10{,}000 = 30\ \mu sec.$$

with

$$R_F = 100\ k\Omega,\ C_F = 300\ pF$$

D. Lock Range Selection
To select C_D, let us start with the actual lock range:

$$\Delta f = R_4 f_o / R_5\ Hz = 7870\ Hz$$

If we assume a capture range of 80%:

$$\Delta f_C = 6296\ Hz$$

therefore, our total capture range of $\pm\Delta f_C$ is 12,592 Hz. Our minimum value for C_D is (16/12,592) μf or 0.0013 μf.

E. Completed Circuit Example
See Figure 5.

II. Design a 3 kilobaud modem to operate with low output jitter. The bandwidth available is 13 kHz.

For this modem, we can take the values from two for the 300 baud modem operating at 1070 Hz and 1270 Hz, multiply our baud rate and mark and space frequencies by ten, and divide all capacitor values on the table by ten. Resistor values should be left as they are.

III. Design a 2 channel multiplex FSK modulator to operate at the following pairs of mark and space frequencies: 600 Hz and 900 Hz, and 1400 and 1700 Hz (each of these channels could handle about 400 baud).

For this task, we will use the XR-2207. The only real consideration here is that, if possible, we want to keep the following resistances all between 10 kΩ and 100 kΩ: R_1, R_1/R_2, R_3 and R_3/R_4. The ratio between the maximum and minimum frequencies is less than 3:1, so we should have no trouble meeting this criterion. If we set our maximum frequency with an R of about 20 kΩ, we have: $1700 = 1/(C_o \times 20{,}000)$; $C_o = 0.029$ μf which is approximately equal to 0.033 μf.

Calculating R_1 using 600 Hz and 0.033 μf, we get $R_1 = 50{,}5$ kΩ. We can use $R_{1B} = 47$ kΩ and $R_{1A} = 10$ kΩ. For R_2, we get 101 kΩ. Use $R_{2B} = 91$ kΩ and $R_{2A} = 20$ kΩ. To determine R_3, use: $1400 = 1/R_3C_o$, which gives us $R_3 = 21.6$ kΩ. Use $R_{3B} = 18$ kΩ and $R_{3A} = 5$ kΩ. R_4 must generate a 300 Hz shift in frequency, the same as R_2. Therefore, set R_4 equal to R_2.

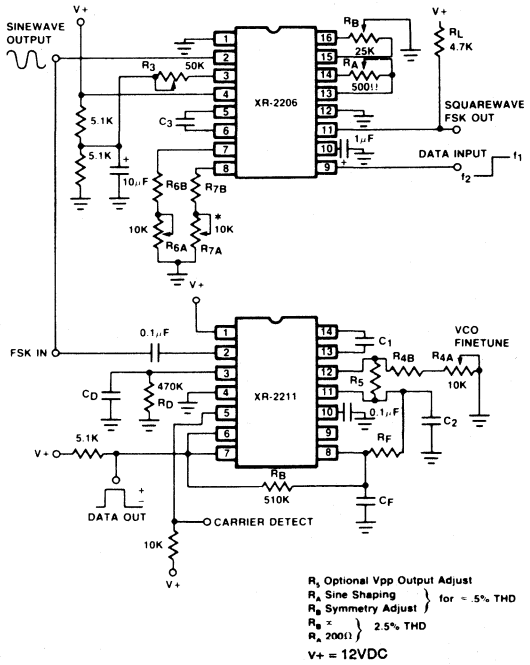


Figure 5: Full Duplex FSK Modem Using XR-2206 and XR-2211. (See Table 2 for Component Values.)

For 5VDC single supply operation of the XR-2211 R_S should be within the range 100kΩ≤ R_S ≤ 1MΩ. Timing capacitor C1 and loop damping capacitor C2; as well as timing resistors $R4_A$ and $R4_B$ should be adjusted as needed by recalculating their values.

Adjustment Procedure

The only adjustments that are required with any of the circuits in this application note are those for frequency fine tuning. Although these adjustments are fairly simple and straightforward, there are a couple of recommendations that should be followed.

The XR-2207: Always adjust the lower frequency first with R_{1B} or R_{3B} and a low level on Pin 9. Then with a high level on Pin 9, adjust the high frequency using R_{2B} or R_{4B}. The second adjustment affects only the high-frequency, whereas the first adjustment affects both the low- and the high-frequencies.

The XR-2206: The upper and lower frequency adjustments are independent, and the sequence is not important.

The XR-2211: With the input open-circuited, the loop-phase detector output voltage is essentially undefined and VCO frequency may be anywhere within the lock range. There are several ways that f_o can be monitored:

1. **Apply an alternating mark and space frequency pattern and adjust until an alternating pattern is obtained.**
2. Short Pin 2 to Pin 10 and measure f_o at Pin 3 with C_D disconnect; or
3. Open R_5 and monitor Pin 13 or 14 with a high-impedance probe

Note: Do NOT adjust the center frequency of the XR-2211 by monitoring the timing capacitor frequency with everything connected and no input signal applied.

For further information regarding the use of the XR-2207, XR-2206 and XR-2211 refer to the individual product data sheets.

Active Filter Design with IC OP Amps

INTRODUCTION

This application note will assist the designer in selecting the optimum filter for his application. It begins with a table of transfer functions, and network defining equations, for the high-pass, low-pass, bandpass, and band-reject filters. A guide to the three types of filter responses will be presented, along with illustrations of several filter realizations, with their respective merits and limitations. Finally, the entire contents are brought together, to provide the designer a complete working schematic of an active filter in a modem configuration, utilizing the XR-346 Quad Programmable Operational Amplifier, along with the XR-2206 Waveform generator, and the XR-2211 Precision Tone Decoder.

PRINCIPLES OF OPERATION

The XR-346 Quad Programmable Operational Amplifier is a basic building block for active filters, and is ideally suited for most filter applications. The XR-346 provides the user the flexibility to externally program the gain-bandwidth product, the supply current, the input bias current, the input offset current, the input noise, and the slew rate. The user, therefore, can trade-off bandwidth for supply current or optimize the noise figure. Likewise, other amplifier characteristics can be programmed for a specific need.

Since the operational amplifier plays such a key role in the active filter, its characteristics are of prime importance. By using operational amplifiers as the basic gain stage of the active filter, problems previously encountered due to low-input impedance, high-output impedance and low-gain are virtually eliminated. Operational amplifiers provide the required response for various filter types. Some of the more popular filters are multiple feedback, state variable, bi-quad and Sallen Key, which can be used to obtain high-pass, bandpass and low-pass filter functions. They are capable of giving the designer all of the standard filter responses, i.e., Butterworth, Chebychev, and Bessel.

There are many single, dual, and quad operational amplifiers that can be used to implement the filters discussed. Table 1 lists some standard operational amplifiers and compares their important typical characteristics. Table 2 gives the designer a brief review of the basic transfer functions and network defining equations. Note that a family of curves exists for all filters except first order low-pass and high-pass. This is due to the presence of loop damping. This point will be expanded upon in the next section on filter responses.

Table 1.

DEVICE CHARACTERISTICS	XR-062	XR-346	XR-34074	XR-34072	741	UNITS
Slew Rate	3.5	0.4	10	10	.5	v/μS
Gain-Bandwidth Product	1	1.2	4.5	4.5	1	MHz
Input Offset Voltage	3	0.5	2.0	0.5	7.5	mV
Input Offset Current	0.05	2	6	6	20	nA
Input Bias Current	0.03	50	100	100	80	nA
Supply Current (max)	0.5	2.5	10	5.7	2.8	mA

Table 2.
Transfer Functions and Equations

Low Pass

$$H(s) = \frac{H_0\omega_0}{s + \omega_0}$$

$$[H(j\omega)] = \left[\frac{H_0{}^2\omega_0}{\omega^2 + \omega_0{}^2}\right]^{1/2}$$

$$\phi = \text{Tan}^{-1}\frac{\omega}{\omega_0}$$

High Pass

$$H(s) = \frac{H_0 s}{s + \omega_0}$$

$$[H(j\omega)] = \left[\frac{H_0{}^2\omega_0{}^2}{\omega^2 + \omega_0{}^2}\right]$$

$$\phi = \frac{\pi}{2} - \text{Tan}^{-1}\frac{\omega}{\omega_0}$$

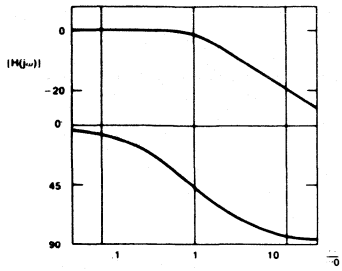
Band Pass

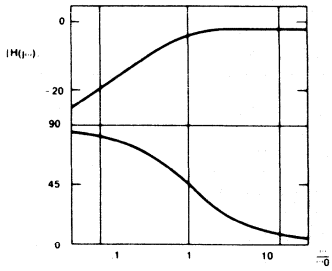
$$H(s) = \frac{H_0\ \alpha\ \omega_0 s}{s^2 + \alpha\omega_0 s + \omega_0{}^2}$$

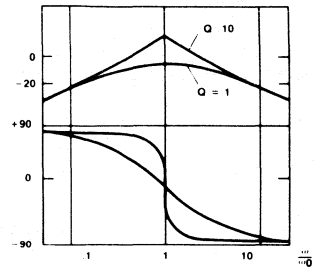
$$[H(j\omega)] = \left[\frac{H_0{}^2\alpha^2\omega_0{}^2\omega^2}{\omega A + \omega^2\omega_0{}^2(\alpha^2 - 2) + \omega_0{}^2}\right]$$

$$\phi = \frac{\pi}{2} - \text{Tan}^{-1}\left(\frac{2Q\omega}{\omega_0} + \sqrt{4Q^2 - 1}\right)$$

$$-\text{Tan}^{-1}\left(\frac{2Q\omega}{\omega_0} - \sqrt{4Q^2 - 1}\right)$$







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Low Pass Second Order

$$H(s) = \frac{H_0\omega_0{}^2}{s^2 + \alpha\omega_0 s + \omega_0{}^2}$$

$$[H(j\omega)] = \left[\frac{Ha^2\omega_0{}^4}{\omega^4 + \omega^2\omega_0{}^2(\alpha^2 - 2) + \omega_0 A}\right]$$

$$\phi = -\text{Tan}^{-1}\left[\frac{1}{\alpha}\ 2\frac{\omega}{\omega_0} + \sqrt{4 - \alpha^2}\right]$$

$$-\text{Tan}^{-1}\left[\tfrac{1}{2}\frac{2\omega}{\omega_0} + \sqrt{4 - \alpha^2}\right]$$

High Pass Second Order

$$H(s) = \frac{H_0 s^2}{s^2 + \alpha\omega_0 s + \omega_0{}^2}$$

$$[H(j\omega)] = \left[\frac{H_0{}^2\omega^4}{\omega^4 + \omega^2\omega_0{}^2(\alpha^2 - 2) + \omega_0 A}\right]$$

$$\phi = \pi - \text{Tan}^{-1}\left[\frac{1}{\alpha}\left(2\frac{\omega}{\omega_0} + \sqrt{4 - \alpha^2}\right)\right]$$

$$-\text{Tan}^{-1}\left[\frac{1}{\alpha}2\left(\frac{\omega}{\omega_0} - \sqrt{4 - \alpha^2}\right)\right]$$

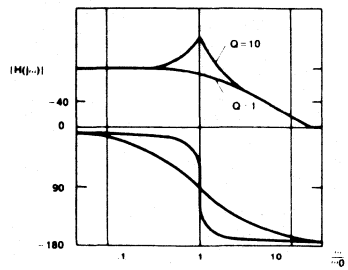
Band Reject

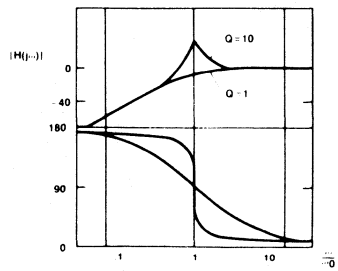
$$H(s) = \frac{(s^2 + \omega_0{}^2)H_0}{s^2 + \alpha\omega_0 s + \omega_0{}^2}$$

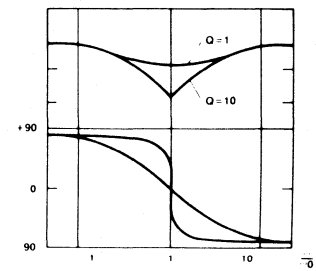
$$[H(j\omega)] = \left[\frac{H_0{}^2\omega^4 + \omega_0{}^4}{\omega^4 + \omega^2\omega_0(\alpha^2 - 2) + \omega_0{}^4}\right]$$

$$\phi = \frac{\pi}{2} - \text{Tan}^{-1}\ \frac{2Q\omega}{\omega_0} + \sqrt{4Q^2 - 1}$$

$$-\text{Tan}^{-1}\left(\frac{2Q\omega}{\omega_0} - \sqrt{4Q^2 - 1}\right)$$







Definition of terms:

ω_0 = Cutoff frequency $2\pi f_0$
α = Loop damping
$s = \sigma + j\omega$ complex frequency

ω_c = Center frequency
ω_1 = Lower cutoff frequency
ω_2 = Upper cutoff frequency

$Q = 1/\alpha = \frac{\omega c}{\omega_2 - \omega_1}$
ϕ = Phase
$[H(j\omega)]$ = Magnitude response
$H(s)$ = Transfer function

Filter Responses

Once the transfer function has been determined, the next step in filter design is to decide upon the desired response. As previously mentioned, the damping of the filter determines its characteristics near cutoff. There are three basic types of responses which are depicted in Table 3, along with their characteristics. In the case of Butterworth and Bessel, the response has been fixed. However, for the Chebychev the α is chosen for the particular response desired. This is done by using a nomograph such as the one shown in Figure 1. To use a nomograph the information required is: A_{max} (maximum ripple in the passband), A_{min} (minimum attenuation in the stop band), and Ω_s (ratio of the A_{min} bandwidth to the A_{max} bandwidth). These terms are illustrated in Figure 2. Once these terms are known, the nomograph is used by locating A_{max}, and drawing a straight line through A_{min} to the left-hand side of the graph. From this point, a horizontal line is drawn to the intersection of Ω_s. The minimum order of the transfer function will be the number of the curve passing above this point. Once this is done, the α and ω_o for each stage is found by consulting the Chebychev network parameter tables for the desired passband ripple, and the number of poles. Such tables can be found in standard filter handbooks.

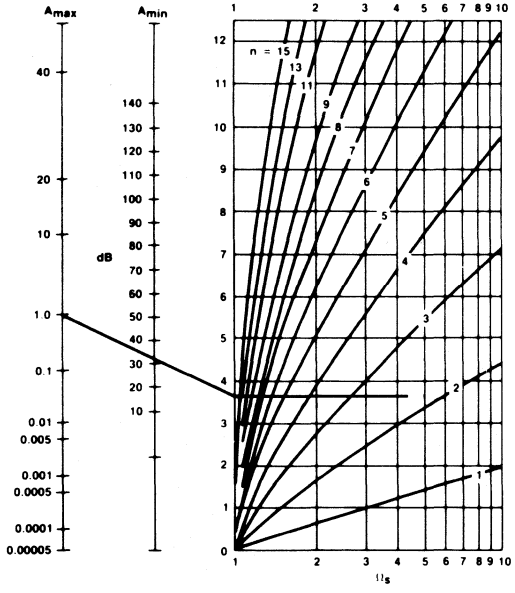


Figure 1. Nomograph to Select Desired Response.

Filter Realizations

There are numerous ways of realizing the transfer functions discussed. Each method has its own relative merit. The configuration selected depends primarily on the specific application and the desired sensitivity parameters. Sensitivity parameters are a means of relating the resultant change in a transfer function, due to an element change. Although these parameters are only directly applicable to an infinitesimal change, they are easily used to evaluate performance for 1% changes, and many times are used for element changes up to 10%. Examples will be given later in this section that will help clarify this parameter.

Table 3.

FILTER TYPE	α	BASIC FEATURES	AMP. RESPONSE
Bessel	$\sqrt{3}$	Best time delay Smoothest phase response	
Butterworth	$\sqrt{2}$	Maximally flat amplitude response	
Chebychev	Can Vary	Passband ripple Fast cutoff slope	

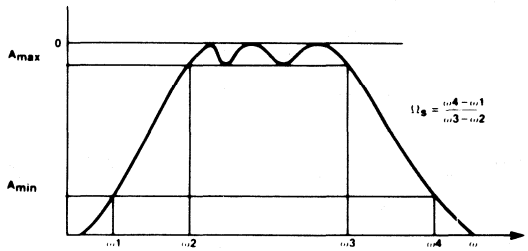


Figure 2. Ratio of A_{min} Bandwidth to A_{max} Bandwidth.

The filter realizations presented here are to be used as a basic guide to help the designer become more adept at designing filters. State-variable and multiple feedback filters will be discussed, and the relative merits of each will be given. It will also be shown that many of the commonly used filters are actually specific cases for the filters mentioned.

Figure 3 illustrates a typical multiple feedback connection with the non-inverting input grounded. To minimize offset, this point should be returned to ground via a resistor whose value is equal to the impedance at the inverting input. The transfer function for this circuit is given by Eq. 1. Each element represents a single resistor or capacitor. To realize the transfer function, each admittance parameter is replaced by 1/R for a resistor and SC for a capacitor. An example will help to clarify this point. If the desired response is a high pass, the form of the characteristic equation is given in Table 2. To transform Eq. 1 into the high-pass characteristic, then Y_1, Y_3, and Y_4 become capacitors and Y_2 and Y_5 resistors. (It should be obvious that a low-pass function could have been fabricated by letting Y_2 and Y_5 be capacitors, and similarly, a bandpass function could have been realized by making Y_3 and Y_4 capacitors.) The terms of the network function, for the high-pass filter shown in Figure 4, are given in Table 4 along with their sensitivity parameters. The transfer function for Figure 4 is given by Eq. 2.

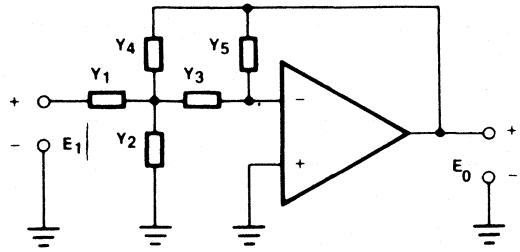


Figure 3. Multiple Feedback Connection with Noninverting Input Grounded.

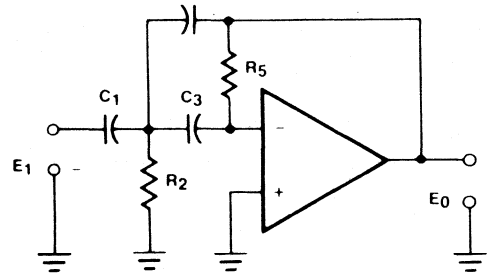


Figure 4. Network Function for the High-Pass Filter.

Eq. 1

$$\frac{E_0}{E_1}(s) = \frac{-Y_1Y_3}{Y_5(Y_1 + Y_2 + Y_3 + Y_4) + Y_3Y_4}$$

Eq. 2

$$\frac{E_0}{E_1}(s) = \frac{-(C_1/C_4)s^2}{s^2 + s(1/R_5)(C_1/C_3C_4 + 1/C_4 + 1/C_3) + 1/R_2R_5C_3C_4}$$

As can be seen from the sensitivity parameters, there is a high degree of circuit sensitivity due to the component tolerances. Due to the interaction of components, the tuning of this circuit may be rather involved. However, with tight component tolerances, these circuits give the designer very predictable results. Due to the high input impedance and low-output impedance, several of these stages may easily be cascaded to achieve a higher order function. What is desired is to have a lower sensitivity to component tolerances. The most commonly used filter for this purpose is the state-variable.

The state-variable synthesis approach is used in most present day Universal Active Filters (UAF). With this method, the actual n^{th} order polynominal of the transfer function is simulated as it would be with an analog computer. When using the state-variable approach, all three outputs (high-pass, low-pass, and bandpass) are available simultaneously. The sensitivities, with respect to component tolerances, are typically less than or equal to one, and the sensitivity of Q, with respect to amplifier gain, can equal zero with high amplifier gain. Because of the high amplifier gain requirement, these filters tend to be limited to the audio range. The cost of reducing the circuit element sensitivities is the need to use n + 2 operational amplifiers to synthesize an n^{th} order transfer function. For this reason, this type of configuration may not be cost effective in the synthesis of low-Q, high-pass, and low-pass filters.

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Table 4.

Parameter	Defining Equation	Sensitivity	
H_0	$= \frac{C_1}{C_4}$	$S_{C_1}^{H_0} = -S_{C_4}^{H_0} = 1$	
α	$= \sqrt{\frac{R_2}{R_5}}\left(\frac{C_1}{\sqrt{C_3C_4}} + \sqrt{\frac{C_3}{C_4}} + \sqrt{\frac{C_4}{C_3}}\right)$	$S_{C_3}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha\omega_0R_5C_3}\left(\frac{C_1}{C3} + 1\right)$ $S_{C_4}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha\omega_0R_5C_4}\left(\frac{C_1}{C3} + 1\right)$ $S_{C_1}^{\alpha} = \frac{1}{\alpha\omega_0R_5}\frac{C_1}{C_3C_4}$ $S_{R_2}^{\alpha} = -S_{R_5}^{\alpha} = \frac{1}{2}$	Note: The sensitivity of H_0 with this implies that if C_1 changes by 1% H_0 will also change by 1%. The defining equation for a sensitivity parameter is: $S_xY = \frac{xdY}{Ydx}$
ω_o	$= \left(\frac{1}{R_2R_5C_3C_4}\right)^{1/2}$	$S_{R_2}^{\omega 0} = S_{R_5}^{\omega 0} = S_{C_3}^{\omega 0} = S_{C_4}^{\omega 0} = -\frac{1}{2}$	

Table 5.

Output	Parameters	Defining Equation	Sensitivity
Low Pass Eq. 3	H_0	$\frac{1 + R_3/R_4}{1 + R_1/R_2}$	$S_{R_1}^{H_0} = -S_{R_2}^{H_0} = -1/(1 + R_2/R_1)$ $S_{R_3}^{H_0} = -S_{R_4}^{H_0} = \frac{1}{H_0}\left(\frac{R_3/R_4}{1 + R_1/R_2}\right)$
	ω_0	$\left(\frac{R_4}{R_3R_5R_6C_1C_2}\right)^{1/2}$	$S_{R_3}^{\omega_0} = S_{R_5}^{\omega_0} = S_{R_6}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -S_{C_4}^{\omega_0} = -1/2$
	α	$\frac{1 + R_4/R_3}{1 + R_2/R_1}\left(\frac{R_3R_6C_2}{R_4R_5C_1}\right)^{1/2}$	$S_{R_4}^{\alpha} = -S_{R_3}^{\alpha} = -1/2 + \frac{R_4/R_3}{R_5C_1\,\alpha\omega_0(1 + R_2/R_1)}$ $S_{R_1}^{\alpha} = -S_{R_3}^{\alpha} = \frac{1}{1 + R_1R_2}$ $S_{R_6}^{\alpha} = S_{C_2}^{\alpha} = -S_{R_5}^{\alpha} = -S_{C_1}^{\alpha} = 1/2$
High Pass Eq. 4	H_0	$\frac{1 + R_4/R_3}{1 + R_1/R_2}$	$S_{R_1}^{H_0} = -S_{R_2}^{H_0} = -1/(1 + R_2/R_1$ $S_{R_3}^{H_0} = -S_{R_4}^{H_0} = \frac{1}{H_0}\left(\frac{R_4/R_3}{1 + R_1/R_2}\right)$
	ω_0	SAME AS LOW PASS	
	α	$\left(\frac{1 + R_4/R_3}{1 + R_2/R_1}\right)\left(\frac{R_3R_6C_2}{R_4R_5C_1}\right)^{1/2}$	$S_{R_4}^{\alpha} = -S_{R_3}^{\alpha} = -1/2 + \frac{R_4/R_3}{R_5C_1\,\alpha\omega_0(1 + R_2/R_1)}$ $S_{R_1}^{\alpha} = -S_{R_2}^{\alpha} = \frac{1}{1 + R_1R_2}$ $S_{R_6}^{\alpha} = S_{C_2}^{\alpha} = -S_{R_5}^{\alpha} = -S_{C_1}^{\alpha} = 1/2$
Band Pass Eq. 5	H_0	$\frac{R_2}{R_1}$	$S_{R_1}^{H_0} = -S_{R_2}^{H_0} = -1$
	ω_0	SAME AS LOW PASS	
	$Q = 1/\alpha$	$\left(\frac{1 + R_2/R_1}{1 + R_4/R_3}\right)\left(\frac{R_4R_5C_1}{R_3R_6C_2}\right)^{1/2}$	$S_{R_5}^{Q} = S_{C_1}^{Q} = -S_{R_6}^{Q} = -S_{C_2}^{Q} = 1/2$ $S_{R_4}^{Q} = S_{R_3}^{Q} = 1/2 - \frac{R_4/R_3}{R_5C_1\,\alpha\omega_0(1 + R_2/R_1)}$ $S_{R_2}^{Q} = -S_{R_1}^{Q} = \frac{1}{1 + R_1/R_2}$

Figure 5 shows a typical state-variable configuration whose characteristic equations are given by Eq. 3, Eq. 4, and Eq. 5. These equations all have the same denominator, and the numerator is determined by the point at which the output is taken. This form may also be used to simulate a band-reject function by summing the high-pass and low-pass outputs. The defining equations and sensitivity parameters are given in Table 5. It is noted here that the bi-quad is actually a slight variation of a second order state-variable.

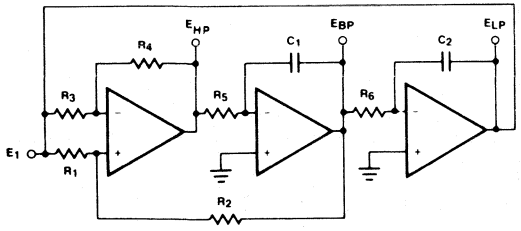


Figure 5. Typical State-Variable Configuration.

Eq. 3

$$\frac{E_{LP}}{E_i} = \frac{\left(\frac{1}{R_5R_6C_1C_2}\right)\left(\frac{1 + R_4/R_3}{1 + R_1/R_2}\right)}{s^2 + s\left(\frac{1}{R_5C_1}\right)\left(\frac{1 + R_4/R_3}{1 + R_2/R_1}\right) + \frac{R_4}{R_3}\left(\frac{1}{R_5R_6C_1C_2}\right)}$$

Eq. 4

$$\frac{E_{HP}}{E_i} = \frac{s^2\left(\frac{1 + R_4/R_3}{1 + R_1/R_2}\right)}{s^2 + s\left(\frac{1}{R_5C_1}\right)\left(\frac{1 + R_4/R_3}{1 + R_2/R_1}\right) + \frac{R_4}{R_3}\left(\frac{1}{R_5R_6C_1C_2}\right)}$$

Eq. 5

$$\frac{E_{BP}}{E_i} = \frac{-s\left(\frac{1}{R_5C_1}\right)\left(\frac{1 + R_4/R_3}{1 + R_1/R_2}\right)}{s^2 + s\left(\frac{1}{R_5C_1}\right)\left(\frac{1 + R_4/R_3}{1 + R_2/R_1}\right) + \frac{R_4}{R_3}\left(\frac{1}{R_5R_6C_1C_2}\right)}$$

Modem Filter

A typical application for an active filter is the input stage of a frequency demodulator. Any noise or spurious signals at this point would affect the overall quality of the output. A more specific example can be cited by considering the FSK system shown in Figure 6. (Frequency-shift keying is a means of transmitting digital information, primarily through telecommunications links.) This type of system is thoroughly covered in Exar's Application Note, AN-01, and will only be briefly discussed here.

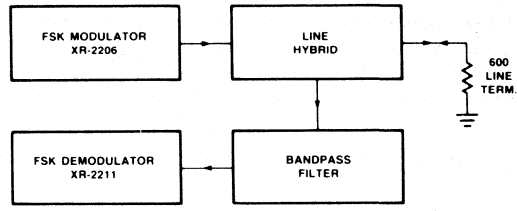


Figure 6. FSK System.

In this system, the digital data to be transmitted is used to key the XR-2206. The frequency-shift keyed output of the XR-2206 is then sent through the hybrid and out onto the line. (The hybrid is used to obtain isolation between data transmitted and data received, and may also be used to amplify the received signal.) In full duplex operation, this system must be able to receive and transmit, simultaneously. Due to line losses, the received signal may range from −12 dBm to −48 dBm. The output level of the transmitter is typically −6 dBm (allowing for a 6 dB loss in the hybrid). Due to line mismatch, the hybrid may only provide 10 dB of isolation to the filter. Therefore, the levels at the input of the filter, assuming a gain of 6 dB from the line through the hybrid, is −6 and −42 dBm for the desired signal, and −16 dBm from the local oscillator. This means that in a worst case situation, the input level of the received signal is −42 dBm, with the level of the local oscillator 26 dB above this. For the XR-2211 to operate with a low-bit error rate at 300 bps the input should be 6 dB higher than the interfering signal. This implies that the stopband, A_{min}, from Figure 2 is 32 dB. The XR-2211 has an internal preamplifier with a dynamic range of greater than 60 dB, and requires a minimun input level of -38 dBm to cause limiting. If we choose a filter to have a passband ripple of 1 dB, and an overall gain of 5 dB, the input conditions of the XR-2211 will be satisfied. The filters introduce a phase shift that is only linear for approximately 1/2 to 1/3 of the passband; therefore a bandwidth of 400 Hz is used for the filter. The general shape of the filter is shown in Figure 7.

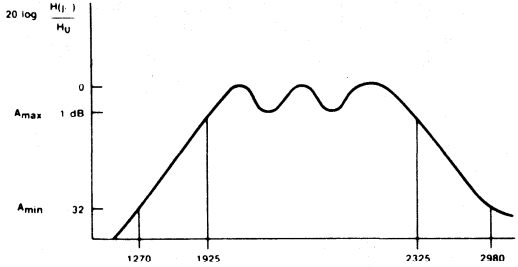


Figure 7. General Filter Shape.

Note: The values used in this filter are based on a modem using an XR-2206 as the modulator, and XR-2211 as the demodulator. If digital techniques are used, the filter parameters may be different, due to the harmonics generated by digital synthesis of a sine wave, and higher signal-to-noise requirements of the demodulator.

To find the minimum number of poles required for this response, the nomograph in Figure 1 is used. The point falls between a 2- and 3-pole filter. The values of $\omega_o + \alpha$ are determined from the tables, for a 3rd order Chebychev response with 1 dB ripple.

From the tables:

$\omega_0 = .997098$
$\alpha = .495609$ complex pole
$\omega_0 = .494171$ – real pole.

The geometric center is $\omega_0 = \sqrt{\omega_3\omega_2}$ or $\sqrt{f_3 f_2 = f_0}$

The filter $Q_0 = \dfrac{f_0}{f_3 - f_2} = \dfrac{\sqrt{(1925)(2325)}}{2325 - 1925} = 5.28892$

The Q of each section of the filter is determined by Equation 6.

Eq. 6

$$Q_A = \frac{\left(\frac{\omega_1}{Q_0}\right)^2 + 4 + \sqrt{\left[\left(\frac{\omega_1}{Q_0}\right)^2 + 4\right]^2 - 4\left(\frac{\alpha_1\omega}{Q_0}\right)^2}}{2\frac{\alpha_1\omega_1}{Q_0}^2}$$

$Q_1 = 21.49 = Q_2$. Section two is a reflection of section one, about f_0. The center frequencies are found by Eq. 7.

Eq. 7

$$M = \frac{\alpha\omega_1 Q_1}{2Q_0} + \sqrt{\left(\frac{\alpha\omega_1 Q_1}{2Q_0}\right)^2 - 1}$$

Where $M = \dfrac{\omega_1}{\omega_0} = \dfrac{\omega_0}{\omega_2} = \dfrac{f_1}{f_0} = \dfrac{f_0}{f_2}$

$M = 1.0955$
$f_1 = 2317.6$
$f_2 = 1931.1$

for Section 3 the real pole is transformed into a complex pole pair.

$$Q_3 = \frac{2Q_0}{\alpha\omega_B} = 10.7$$

and $f_3 = f_0$.

The 3 filter stages are now defined:

$f_1 = 2317.6$ $Q_1 = 21.49$
$f_2 = 1931.1$ $Q_2 = 21.49$
$f_3 = 2115.56$ $Q_3 = 10.7$

In this example, the multiple feedback approach is used since 3-pole pairs can be generated with 3 op amps, 6 capacitors, and 9 resistors; an equivalent filter could have been designed with the state-variable, but this would have required 9 op amps to realize. The actual filter is shown in Figure 8. All capacitor values are chosen to be .01 μF (5%), and all resistors are 1%. The values for this filter and a low-band filter are shown in Table 6.

Figure 9 shows a complete Originate or Answer modem. The values for the XR-2206 and XR-2211 are given

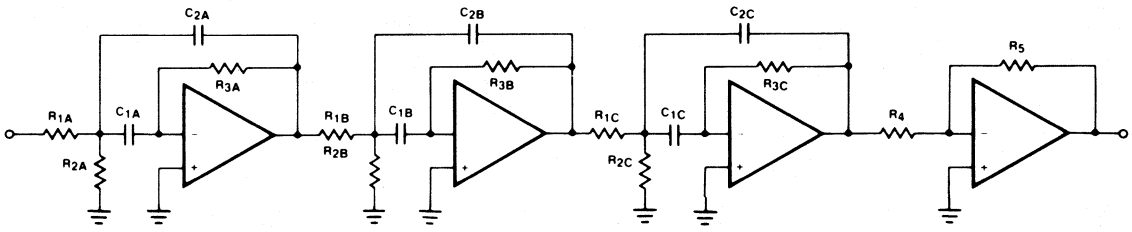


Figure 8. Modem Filter.

Table 6.

		f_0	ω_0	Q_0	R_1	R_2	R_2	C_1	C_2	H_0
Originate	A	1931.1	12.1335K	21.49	88.6K	192	354K	.01	.01	2
	B	2317.6	14.562K	21.49	74K	160	295K	.01	.01	2
	C	2115.6	13.293K	10.7	40K	355	161K	.01	.01	2
Answer	A	1362.26	10.115K	11.827	58.5K	421	234K	.01	.01	2
	B	975.51	6129.3	11.827	96.5K	421	386K	.01	.01	2
	C	1152.78	7.243K	5.832	40.3K	1219.5	161K	.01	.01	2

in Table 7. For an originate modem, the transmitting frequencies are 1070 and 1270, and the receiving frequencies are 2025 and 2225, for a space and mark, respectively.

The first op-amp is connected as an active hybrid which should supply a minimum of 10 dB isolation, from transmit to receive, while adding 6 dB from the line to the receiver.

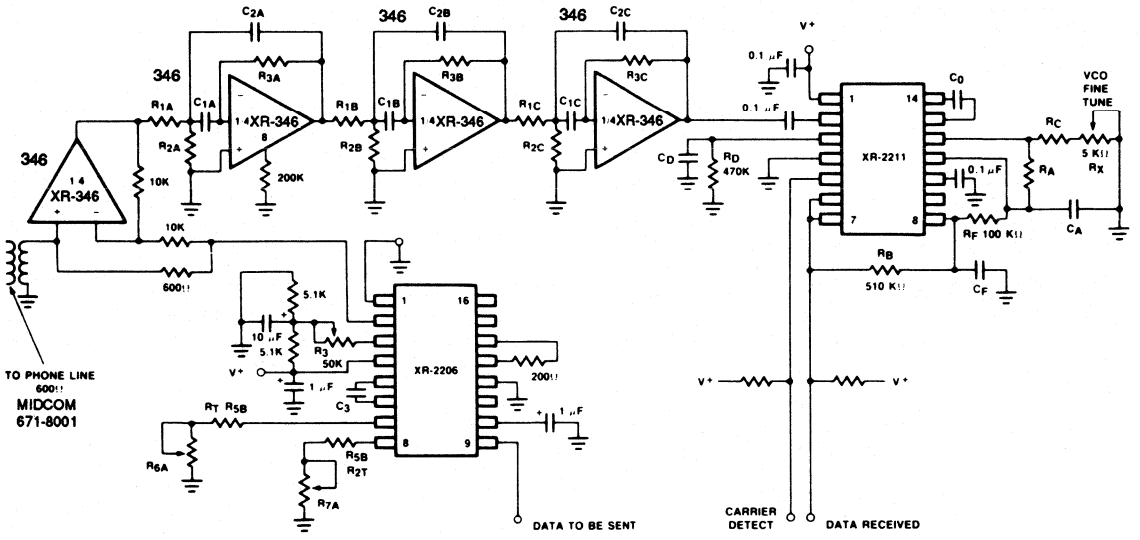


Figure 9. Originate or Answer Modem.

Table 7. Recommended Component Values for Typical FSK Bands

FSK Band			Component Values											
			XR-2206					XR-2211						
Baud Rate	f_L	f_H	R_{6A}	R_{6B}	R_{7A}	R_{7B}	C_3	R_X	R_C	R_A	C_0	C_A	C_F	C_D
Originate	1070	1270	10	18	10	20	.039	10	18	100	.039	.01	.005	.05
Answer	2025	2225	10	16	10	18	.022	10	18	200	.022	.0047	.005	.05

Units: Frequency — Hz; Resistors — kΩ; Capacitors — μF.

Three-State FSK Modem Design using XR-2207 and XR-2211

INTRODUCTION

This application note describes the design principle, and the operation of three-state frequency-shift keyed (FSK) modems for industrial process control systems. Compared to conventional bi-state modems, which utilize only the mark and space frequencies, the three-state modems utilize a third frequency, the carrier signal, for additional command and control functions. This carrier-control feature allows each modem system connected to a central processor (CPU) to be interrogated or activated, one at a time, without interference from the other modem transmitters or receivers within the same system.

The design and operation of conventional bi-state FSK modems using the XR-2206 modulator, and the XR-2211 demodulator, are covered in Exar's Application Note, AN-01. This application note extends these basic concepts to the design of FSK modulators or demodulators with three-state operation capability.

PRINCIPLES OF OPERATION

In a wide variety of industrial process control applications, it is necessary to have a number of separate sensors and controllers activated by a centralized computer or processing unit (CPU). This can be achieved by operating a number of separate FSK modulator/demodulator (modem) stations over a common set of telephone lines, and address them one at a time from the CPU. The simplified block diagram of such a process controlled system is shown in Figure 1. In many such cases, such a process control system also makes use of the distributed-intelligence concept by employing a separate data acquisition system at each control station. Such an intelligent data acquisition system is normally made up of a microprocessor, along with its A/D and D/A converter circuitry, which will interface with the sensors and the control machinery. An FSK modem will interface with the telephone wires going back to the central command unit, the CPU.

In the conventional operation of FSK modems, they operate in their bi-state mode, i.e., the information to be transmitted or received is available in two states, corresponding to either a mark or a space frequency. In a complex process control system, such as the one shown in Figure 1, the versatility of the system can be greatly enhanced by operating the FSK modulator/demodulator in three-state mode, where the information to be transmitted or received is available in three states, i.e., a mark or space frequency, or a carrier signal, which is normally a tone having a frequency halfway between the mark and space frequencies.

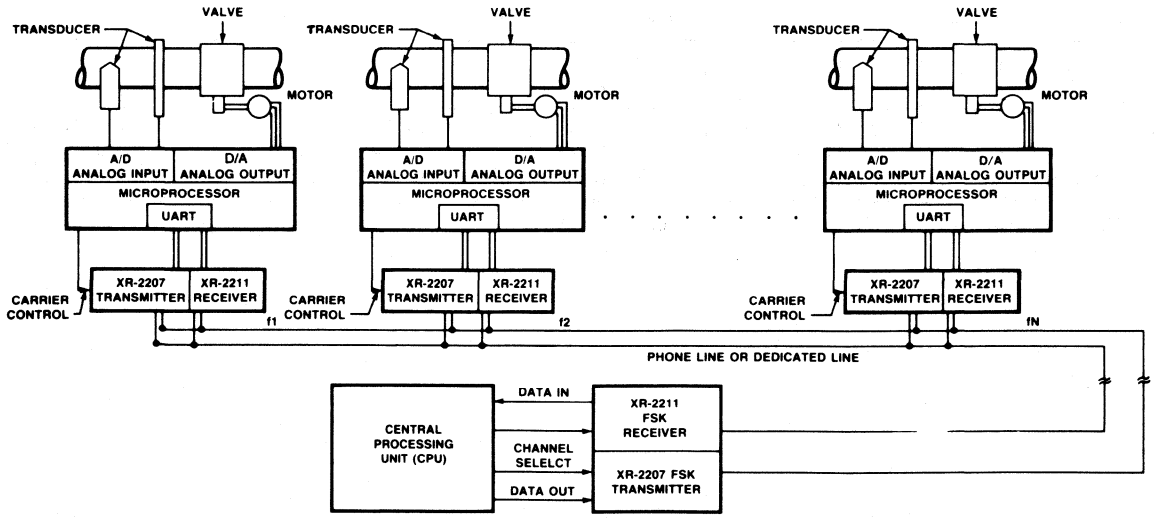


Figure 1. Simplified Block Diagram of a Complex Process Control System with Multiple FSK Modems.

Figure 2 shows a detailed block diagram of a complete three-state FSK modem system. The system is made up of five blocks:

(a) FSK transmitter or encoder which converts the input data or logic signals into transmitted mark, space, and carrier tones.

(b) FSK receiver or decoder which converts the frequency signals sent over the telephone lines into binary logic signals.

(c) Transmitter bandpass filter which band-limits the frequency output of the transmitter to the allocated transmitter bandwidth.

(d) Receiver bandpass filter which limits the incoming signals to those frequencies which fall within the allocated receiver bandwidth.

(e) A line hybrid, or a 4-wire to 2-wire transformer, which isolates or decouples the transmitter output from the receiver input.

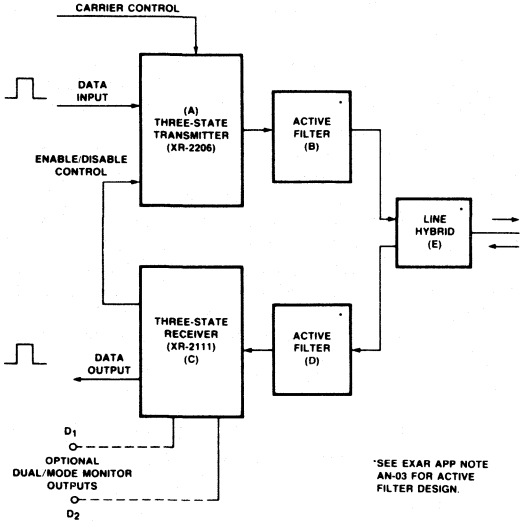


Figure 2. Block Diagram of a Three-State FSK Modem System.

The first 2 blocks, the FSK transmitter and the receiver, are the essential part of the modem system. The remaining three blocks, namely the active filters and the line-hybrid, are support circuits, depending on the frequency-band requirements or the necessary telephone line interconnections. Detailed descriptions and design examples for these active filters are given in Exar's Application Note, AN-03. **Switched capacitor filters, such as the XR-1010 can be used as well.**

The three-state modem is designed to operate in two separate frequency bands: A transmit-band for the transmitted data, and a receive-band for the incoming frequencies. In certain operating modes, such as the half-duplex operation, these frequency bands may be one and the same. In its most general case, the frequency information associated with the three-state modem system (Figure 2) is concentrated in three discrete frequencies in each of the transmit- and receive-bands. These are:

Transmit-Band (transmitter output):

f_{T1} = Transmitter mark frequency

f_{T2} = Transmitter space frequency

f_{T0} = Transmitter carrier or center frequency

Receive-Band (receiver input):

f_{R1} = Receiver mark frequency

f_{R2} = Receiver space frequency

f_{R0} = Receiver carrier or center frequency

Normally, the mark and space frequencies are chosen to be near the opposite edges of the receive- or transmit-band, and the carrier frequency is chosen to be at the center of the corresponding band.

When activated by the enable/disable control, the three-state transmitter generates either the FSK mark/space frequencies, f_{T1} and f_{T2}, or the carrier frequency, f_{T0}. The carrier frequency is activated by the carrier control input, and can override the input data.

The three-state receiver provides two outputs: A binary data output, when activated by the input mark/space frequencies, f_{R1} and f_{R2}, and a logic signal, to control or enable the transmitter when the receiver-carrier frequency, f_{R0}, is present. As an option, it may have a dual-mode operation capability which can provide serial data outputs for half-bandwidth deviations of the input signal, i.e., for FSK signals comprised of center-to-mark or center-to-space frequency shifts. The data outputs corresponding to this mode of operation are shown as outputs, D_1 and D_2 of Figure 2.

CIRCUIT OPERATION

The generalized three-state modem system of Figure 2 can operate in a multiplicity of modes. Some of these are outlined below:

Answerback Under CPU Control

The modem will be in a standby mode with the transmitter disabled, and the receiver in a standby condition with its data output disabled. It will be activated only when an interrogate tone at the receiver center frequency, f_{R0}, is transmitted by the control modem unit associated with the CPU (see Figure 1). This tone is detected by the receiver; it activates the transmitter via its enable/disable control, and instructs the local microprocessor to transmit its status information via the local transmitter. This data is transmitted as an FSK signal made up of the transmit mark and space frequencies f_{T1} and f_{T2}. When the information transmission is complete, or when the interrogate tone is discontinued, the entire modem system again reverts back to its standby mode.

Receive Under CPU Control

In this mode of operation, the transmitter remains disabled, the receiver is at its standby mode with its data output disabled. When the FSK data is sent by the CPU modem transmitter, at the mark/space frequencies, f_{R1} and f_{R2}, the data output is enabled, and the decoded binary data is fed into the local microprocessor. Since the center receive-frequency, f_{R0}, is not transmitted, the transmitter remains disabled.

Priority-Transmit Request

In an emergency situation, the local transmitter can be activated by its carrier-control input, which causes it to transmit a tone, f_{T0}, at its center frequency. When this tone is received by the CPU, it will be treated as a priority request to transmit information; the CPU will immediately interrogate the corresponding local modem by sending out its address tone at frequency, f_{R0}.

Dual-Channel Receive

As an option, the receiver can provide serial data outputs, through separate terminals, D_1 and D_2 of Figure 2, for half-bandwidth deviations of the input FSK signals. In this mode, the input data will be in the form of center-to-mark frequency shifts for one channel, and center-to-space shifts for the other. This mode of operation allows two separate sets of data or control instructions to be transmitted within the same channel bandwidth, provided that only one of these channels is used at any one time.

Dual-Channel Transmit

As an option, the transmitter can also transmit two separate channels, using half-bandwidth deviations of the transmit signal. In this case, the outgoing data will be encoded with center-to-mark transitions of the transmitter frequency in one of the channels, and center-to-space transitions in the other. However, similar to the case of the receiver, only one or the other, and not both, of these half-bandwidth channels can be on at a given time.

XR-2207 As A Three-State FSK Transmitter

The XR-2207 is a monolithic voltage-controlled oscillator (VCO) circuit with excellent temperature stability. It provides simultaneous triangle and square wave outputs, and can be keyed to any one of four preprogrammed frequencies by means of external logic signals. These four discrete frequencies are preprogrammed by the choice of four external timing resistors.

Figure 3 shows a functional block diagram of the XR-2207 monolithic FSK generator chip. The circuit is comprised of four functional blocks: A variable-frequency oscillator which generates the basic periodic waveforms; four current switches actuated by binary keying inputs, and buffer amplifiers for both the triangle and square wave outputs. The internal current switches transfer the oscillator current to any of four external timing resistors, to produce four discrete frequencies which are selected according to the binary logic levels at the keying terminals.

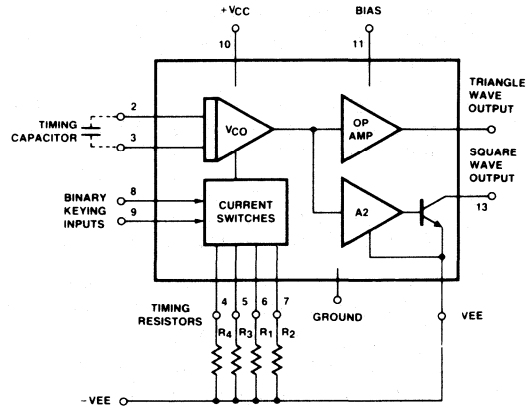


Figure 3. Functional Diagram of XR-2207 Monolithic FSK Generator.

The frequency of oscillation is set by an external timing capacitor, and by the combination of one or more of the external timing resistors, R_1 through R_4. The keying terminals switch these external resistors in and out of the circuit and thus control the operating frequency. Table 1 shows the four discrete frequencies which can be obtained as a function of four logic states at Pin 8 and 9. It should be noted that the frequency is inversely proportional to the timing resistor connected to the activated timing pin. For example, if only one of the timing pins, say Pin 5, is activated and its associated resistor, R_3, is left open-circuited (i.e., $R_3 = \infty$) the oscillator will be keyed OFF since this corresponds to a zero-frequency state.

Table 1.
Output Frequency of the XR-2207 as a Function of the Keying Logic.

Logic Level		Active Timing Resistor	Output Frequency
Pin 8	Pin 9		
L	L	Pin 6	$\frac{1}{C_0R_1}$
L	H	Pin 6 and 7	$\frac{1}{C_0R_1} + \frac{1}{C_0R_2}$
H	L	Pin 5	$\frac{1}{C_0R_3}$
H	H	Pin 4 and 5	$\frac{1}{C_0R_3} + \frac{1}{C_0R_4}$

(* Frequency in Hz, R in Ohms and C in Farads.)

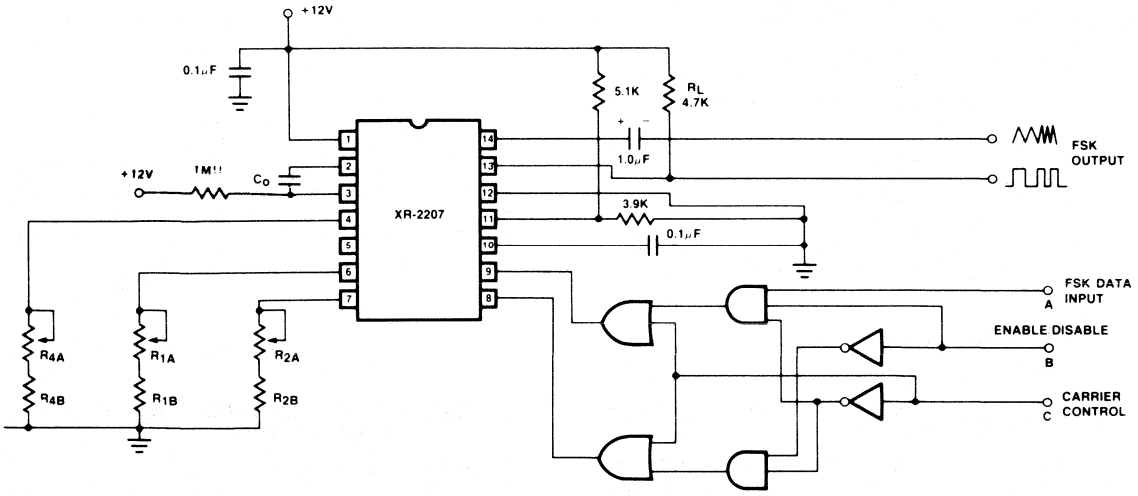


Figure 4. Three-State FSK Transmitter Using the XR-2207.

Figure 4 shows the recommended circuit connection of the XR-2207, for its operation as a three-state FSK transmitter. The three resistors, R_1, R_2 and R_4, are used to set the three discrete frequencies to be transmitted in accordance with the frequency expressions given in Table 1, where:

$$f_{T1} = \frac{1}{C_0R_1} \quad f_{T2} = \frac{1}{C_0R_1} + \frac{1}{C_0R_2} \quad f_{T0} = \frac{1}{C_0R_4}$$

It should be noted that Pin 5 is left open circuited (i.e., $R_3 = \infty$). This allows the circuit to be keyed OFF, or disabled, by applying a high-logic state to Pin 8, and a low-logic state to Pin 9 (see Table 1).

The functions of the three control terminals can be described as follows:

a. **FSK Data Input:** The serial binary data is applied to this terminal. With the carrier control at low- and enable/disable control at high-state, the binary data causes the transmitter to generate the mark and space frequencies, f_{T1} and f_{T2}.

b. **Enable/Disable Control:** When this input is at low-state, the transmitter is disabled.

c. **Carrier-Control:** When this terminal is at high-state, the transmitter generates a continuous tone at frequency, f_{T0}.

With the external logic circuitry shown in Figure 4, carrier-control can override both the enable/disable or the FSK data inputs. A detailed truth-table of the circuit outputs is given in Table 2, for various states of the three control inputs.

Table 2.
Three-State Transmitter Operating Modes as a Function of Control Inputs

Control Input States			Level at Pin 9	Level at Pin 9	Transmitter Output Frequency	Transmitter Operating Mode
A	B	C				
L	L	L	L	H	OFF	Transmitter Off
H	L	L	L	H	OFF	
L	H	L	L	L	f_{T1}	Transmit Data
H	H	L	H	L	f_{T2}	
L	L	H	H	H	f_{T0}	Transmit Carrier Only
L	H	H	H	H	f_{T0}	
H	H	H	H	H	f_{T0}	

XR-2211 As A Three-State Receiver

The XR-2211 is a monolithic FSK demodulator which operates on the phase-locked loop principle. In addition to the basic PLL system, the monolithic chip also contains a quadrature-detector circuit which produces a logic signal when a carrier signal, or tone, is present within the capture range of the PLL. A simplified functional block diagram of the circuit is shown in Figure 5.

Basic Bi-State Operation

The basic operation of the XR-2211, in conventional bi-state modems, is described in detail in Exar's Application Note, AN-01. It will be briefly reviewed below.

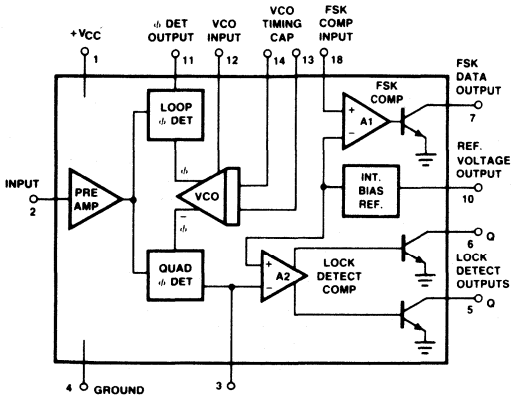


Figure 5. Functional Block Diagram of XR-2211 FSK and Tone Detector.

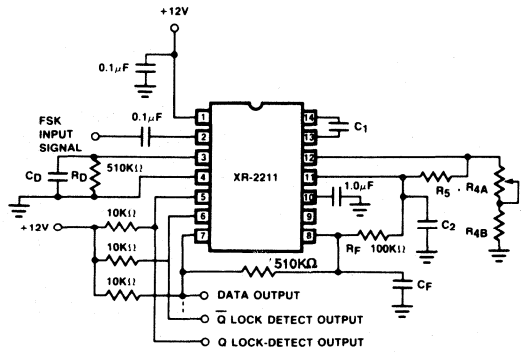


Figure 6. XR-2211 as a Bi-State Receiver with Tone-Detection Capability.

The basic circuit connection for the XR-2211 for bi-state FSK detection is shown in Figure 6. The center frequency is determined by $f_0 = (1/C_1R_4)$ Hz, where capacitance is in farads and resistance is in ohms. Calculations for f_0 should fall midway between the mark and space frequencies.

The tracking range ($\pm\Delta f$) is the range of frequencies over which the phase-locked loop can retain a lock with a swept input signal. This range is determined by the formula:

$$\Delta f = (R_4 f_0/R_5)\ \text{Hz}.$$

Δf should be made equal to, or slightly less than, the difference between the mark and space frequencies. For optimum stability, the recommended range of values for R_4 is between 10 kΩ and 100 kΩ.

The capture range ($\pm\Delta f_C$) is the range of frequencies over which the phase-locked loop can acquire lock. It is always less than the tracking range. The capture range is limited by C_2, which, in conjunction with R_5, forms the loop-filter time constant. In most modern applications, Δf_C is chosen to be ≈80% to 95% of the tracking range, Δf.

The bi-state FSK data filter, made up of R_F and C_F, removes the jitter from the demodulated FSK signal. Similarly, the lock-detect filter capacitor (C_D) removes chatter from the lock-detect output. With R_D = 510 kΩ, the minimum value of C_D can be determined by: $C_D(\mu f)$ ≈ 16/capture range in Hz. The XR-2211 has three npn open-collector outputs, each of which is capable of sinking up to 5 mA. Pin 7 is the FSK data output, Pin 5 is the Q lock-detect output which goes low when a carrier is detected, and Pin 6 is the Q lock-detect output which goes high when lock is detected. If Pin 6 and 7 are wired together, the output signal from these terminals will provide data when FSK is applied, and will be low when no carrier is present.

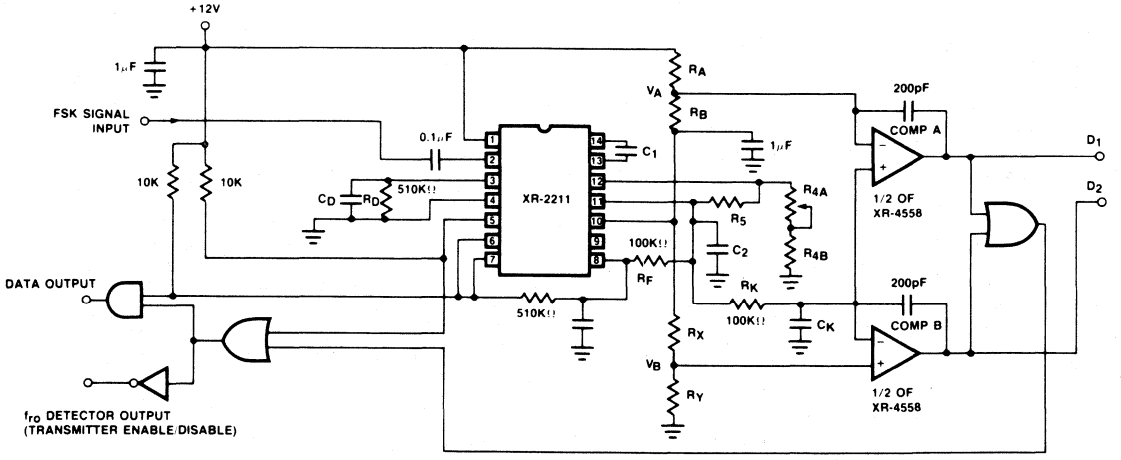


Figure 7. Circuit Connection for Operating XR-2211 as a Three-State FSK Receiver.

Three-State Operation

The XR-2211 FSK demodulator circuit can be made to operate as a three-state receiver (see Block C of Figure 2), using the circuit configuration shown in Figure 7. With reference to the Figure, the basic operation of the circuit can be described as follows: The basic FSK decoding function, converting the incoming mark and space signals at frequencies f_{R1} and f_{R2}, is performed in the same manner as in the bi-state case, and the resulting output is available at Pin 7 of XR-2211. Pin 7 is connected to the tone-detect output, and then gated by the complement of the carrier-detect output. Thus, the data output terminal will be enabled only when the mark and space frequencies are present, but not when the receive-carrier, f_{R0}, is present.

The external voltage comparators shown in Figure 7 are added to the circuit to distinguish PLL output voltage levels corresponding to various input frequencies. The function of the XR-2211 frequency-to-voltage transfer characteristics can be understood by referring to Pin 11 in Figure 8. The voltage levels and polarities shown are relative to the XR-2211 internal reference voltage, V_{10}, at Pin 10. The mark and space frequencies, f_{R1} and f_{R2}, generate the maximum dc level shifts. V_{R1} and V_{R2}, sensed by the internal FSK comparator (see Figure 5) which is internally biased from the reference voltage, V_{10}.

The external comparators, Comp. A and Comp. B of Figure 7, are biased at voltage levels, V_A and V_B, approximately halfway between V_{R1} and V_{R2}, to trip at frequencies f_A and f_B, which are halfway between mark-to-center and space-to-center frequency shifts. This biasing is achieved with the external resistive dividers, R_A, R_B, R_X, and R_Y of Figure 7, which generate the reference voltage levels, V_A and V_B, with respect to the XR-2211 internal reference at Pin 10. It should be noted that the value of the resistors (R_A + R_B) and (R_X + R_Y) must be as large as possible (typically in excess of 100 kΩ) to avoid disturbing the voltage level at Pin 10.

The output of Pin 11 is filtered by R_K and C_K, and is used to drive the external voltage comparators. The outputs of these comparators are then connected through the external logic gates, to produce the carrier-detect or the enable/disable signal. The resulting logic output will be noramlly at a low state, and will go high only when the carrier signal, f_{R0}, is present. This logic signal is normally used for transmitter enable/disable control, as shown in Figure 2.

The logic level changes, at the external comparator outputs, correspond to mark-to-carrier or space-to-carrier frequency shifts (see Figure 8); thus, these outputs can be utilized as optional dual-mode monitor outputs, D_1 and D_2 of Figure 2.

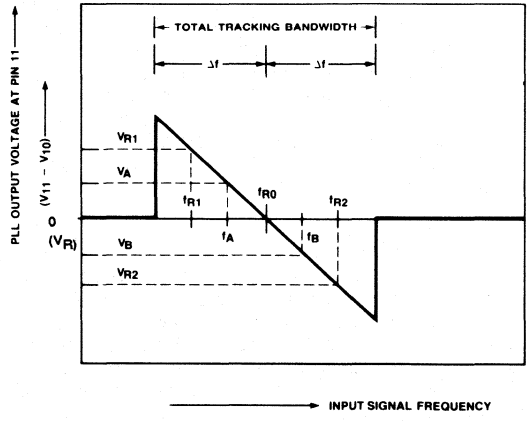


Figure 8. XR-2211 Frequency-to-Voltage Transfer Characteristics. (Note: V_{11} and V_{10} are the dc voltage levels at Pins 11 and 10, respectively.)

Master-Slave Operation

If a common 2 wire line is desired between each modem, a repeater arrangement is needed for the line hybrid interface.

Precision PLL System using the XR-2207 and the XR-2208

INTRODUCTION

The phase-locked loop (PLL) is a versatile system block, suitable for a wide range of applications in data communications and signal conditioning. In most of these applications, the PLL is required to have a highly stable and predictable center frequency and a well-controlled bandwidth. Presently available monolithic PLL circuits often lack the frequency stability and the versatility required in these applications.

This application note describes the design and the application of two-chip PLL system using the XR-2207 and the XR-2208 monolithic circuits. The XR-2207 is a precision voltage controlled oscillator (VCO) circuit with excellent temperature stability (±20 ppm/°C, typical) and linear sweep capability. The XR-2208 is an operational multiplier which combines a four quadrant multiplier and a high gain operational amplifier in the same package. Both circuits are designed to interface directly with each other with a minimum number of external components. Their combination functions as a high performance PLL, with the XR-2207 forming the VCO section of the loop, and the XR-2208 serving as the phase-detector and loop amplifier.

As compared with the presently available single-chip PLL circuits such as the XR-210 or the Harris HI-2820, the two-chip PLL system described in this paper offers approximately a factor of 10 improvement in temperature stability and center frequency accuracy. The system can operate from 0.01 Hz to 100 kHz, and its performance characteristics can be tailored to given design requirements with the choice of only four external components.

DEFINITIONS OF PLL PARAMETERS

The phase-locked loop (PLL) is a unique and versatile feedback system that provides frequency selective tuning and filtering without the need for coils or inductors. It consists of three basic functional blocks; phase comparator, low-pass filter, and voltage-controlled oscillator, interconnected as shown in Figure 1. With no input signal applied to the system, the error voltage, V_d, is equal to zero. The VCO operates at a set "free-running" frequency, f_o. If an input signal is applied to the system, the phase comparator compares the phase and frequency of the input signal with the VCO frequency and generates an error voltage, $V_e(t)$, that is related to the phase and frequency difference between the two signals. This error voltage is then filtered and applied to the control terminal of the VCO. If the input signal frequency, f_S, is sufficiently close to f_o, feedback causes

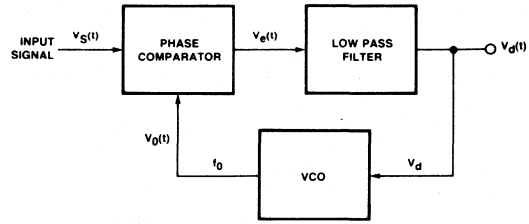


Figure 1. Block Diagram of a Phase-Locked Loop.

the VCO to synchronize or "lock" with the incoming signal. Once in lock, the VCO frequency is identical to the input signal, except for a finite phase difference.

Two key parameters of a phase-locked loop system are its "lock" and "capture" ranges. These can be defined as follows:

Lock Range = The band of frequencies in the vicinity of f_o over which the PLL can *maintain lock* with an input signal. It is also known as the "tracking" or "holding" range. Lock range increases as the overall loop gain of the PLL is increased.

Capture Range = The band of frequencies in the vicinity of f_o where the PLL can *establish* or *acquire lock* with an input signal. It is also known as the "acquisition" range. The capture is always smaller than the lock range. It is related to the low pass filter bandwidth and decreases as the low pass filter time constant increased.

The PLL responds to only those input signals sufficiently close to the VCO frequency, f_0, to fall within the "lock" or "capture" ranges of the system. Its performance characteristics, therefore, offer a high degree of frequency selectivity, with the selectivity characteristics centered about f_0. Figure 2 shows the typical frequency-to-voltage transfer characteristics of the PLL. The input is assumed to be a sine wave whose frequency is swept slowly, over a broad frequency range covering both the "lock" and the "capture" ranges of the PLL. The vertical scale corresponds to the filtered loop error voltage, V_d, appearing at the VCO control terminal.

As the input frequency, f_S, is swept up (Figure 2(a)) the system does not respond to the input signal until the input frequency reaches the lower end of capture range, f_{CL}. Then, the loop suddenly locks on the input signal, causing a positive jump in the error voltage V_d. Next, V_d varies at a slope equal to the reciprocal of VCO

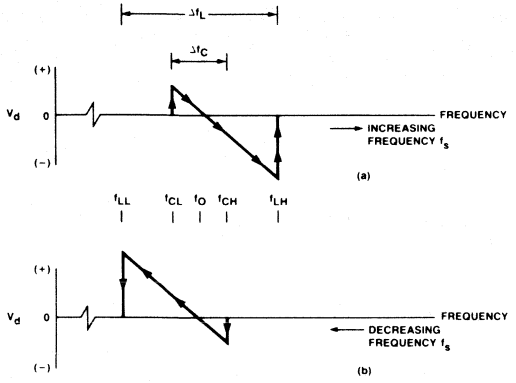


Figure 2. Frequency to Voltage Transfer Characteristics of a PLL System; (a) Increasing Input Frequency; (b) Decreasing Input Frequency.

voltage-to-frequency conversion gain, (K_V), and goes through zero at $f_S = f_0$. The loop tracks the input frequency until f_S reaches the upper edge of the lock range, f_{LH}. Then the PLL loses lock, and the error voltage drops to zero. If the input frequency is swept back slowly, from high towards low frequencies the cycle repeats itself, with the characteristics shown in Figure 2(b). The loop captures the signal at the upper edge of the capture range, f_{CH}, and tracks it down the lower edge of the lock range, f_{LL}. With reference to the figure, the "lock" and the "capture" ranges can be defined as:

$$\text{Lock Range} = \Delta f_L = f_{LH} - f_{LL}$$
$$\text{Capture Range} = \Delta f_C = f_{CH} - f_{CL}$$

The gain parameters associated with the PLL are defined as follows:

Phase Detector Gain, $K\phi$: Phase detector output per unit of phase difference between the two signals appearing at the phase detector inputs. It is normally measured in volts per radian.

VCO Conversion Gain, K_V: VCO frequency change per unit of input voltage. It is normally measured in radians/sec./volt.

Loop Gain, K_L: Total d_C gain around the feedback loop. It is equal to the product of $K\phi$ and K_V.

Loop Damping Factor, ζ: Defines the response of the loop error voltage V_d, to a step change in frequency. If $\zeta < 1$, the loop is underdamped; and the error voltage V_d will exhibit an underdamped response for a step change of signal frequency.

The lock range of the phase-locked loop is controlled by the loop gain, K_L. The capture range and the damping factor are controlled by both the loop gain and the low pass filter.

PRECISION PLL USING XR-2207 AND XR-2208

The XR-2207 VCO and the XR-2208 operational multiplier can be inter-connected as shown in Figure 3, to form a highly stable PLL system. The circuit of Figure 3 operates with supply voltages in the range of +12V to +26V; and over a frequency range of 0.01 Hz to 100 kHz. In the PLL system of Figure 3, all the basic performance characteristics of the PLL can be controlled and adjusted by the choice the choice of 4 external components identified as resistors R_0 and R_1 and capacitors C_0 and C_1. C_0 and R_0 control the VCO center frequency : R1 and C1 determine the tracking range and the low pass filter characteristics. The two-chip PLL system can be readily converted to split supply operation by interconnecting the circuit as shown in Figure 4. The PLL circuit of Figure 4 operators over a supply voltage range of ±6 volts to ±13 volts.

For best results, the timing resistor R_0 should be in the range of 5k to 100k, and $R_1 > R_0$. Under these conditions, the basic parameters of the PLL can be easily calculated from the design equations listed in Table 1.

Design Example

As an example, consider the design of a PLL system using the circuit of Figure 3, to meet the following nominal performance specifications:

a) Center Frequency = 10 kHz
b) Tracking Range = 20% (9 kHz to 11 kHz)
c) Capture Range = 10% (9.5 kHz to 10.5 kHz)

Solution:

a) Set Center Frequency:
Choose R_0 = 10k (Arbitrary choice for $5k < R_0 < 100k$)

Then, from equation 1 of Table 1:

$$C_0 = (1/f_0 R_0) = 0.01\ \mu F$$

b) Set Lock Range:
From equation 2 of Table 1:

$$R_1 = (0.45)\ R_0 = 45k$$

c) Set Capture Range:
Since capture range is significantly smaller than Lock range, equation 8(a) applies.

Solving equation 8(a) for C_1, one obtains:

$$C_1 = 0.032\ \mu F$$

PRECISION SINE WAVE OUTPUT PLL USING XR-2208 AND XR-2206

The interconnection of the XR-2208 and XR-2206 as shown in Figure 5 forms a precision phase-locked loop system with a sine wave output. The phase-locked loop

characteristics are adjusted with the same four external components as previously described. Equation 2 in Table 1 is modified to:

(2) Lock Range $(\Delta f_L/f_0) = (0.5)(R_0/R_1)$

This change is because the reference of the XR-2206 is internally set. The clamp network with Q_1 has been added to adjust the swing to the VCO to compensate for this reference. The sine wave characteristics are adjusted by R_4 and R_5, which adjust sine-shaping and symmetry respectively. Sine wave distortion levels are typically 2.5% unadjusted with $R_4 = 200\Omega$ and R_5 open, and 0.5% adjusted using R_4 and R_5. Sine wave amplitude is adjusted by R_3 with the conversion gain equalling typically:

$$\frac{60mV_{P\text{-}P}}{K\Omega \text{ of } R_3}$$

The phase-locked loop input characteristics allow locking to input signal levels of 50 mV RMS to 2V RMS.

Table 1
Phase-Locked Loop Design Equations*

(1) Center Frequency: $f_0 = \frac{1}{R_0C_0}$ Hz	(7) Loop Damping: $= \frac{1}{2\sqrt{\tau K_L}} = \sqrt{\frac{2\,C_0}{C_1}}$
(2) Lock Range: $(\Delta f_L/f_0) = (0.9)(R_0/R_1)$	(8) Capture Range:
(3) Phase Detector Gain: $K\phi = 0.5\ V_{CC}$ volts/radian Where $V_{CC} = V^+$ for split supply; $V_{CC} = V^+/2$ for single supply.	a) Underdamped Loop ($\zeta < 1/2$): $(\Delta f_C/f_0) = \frac{0.8R_0}{R_1}\ \frac{C_0}{C_1}$
(4) VCO Conversion Gain: $K_V = \frac{1}{2\ V_{CC}C_0R_1}$ rad/sec/volt	b) Overdamped Loop ($\zeta > 1$): $(\Delta f_C/f_0) = 0.8(R_0/R_1)$
(5) Loop Gain: $K_L = K\phi K_V = \frac{0.25}{C_0R_1}$ sec^{-1}	*See Figures 3 and 4 for component designation.
(6) Low Pass Filter Time Constant: $\tau = \frac{C_1R_1}{2}$ sec.	

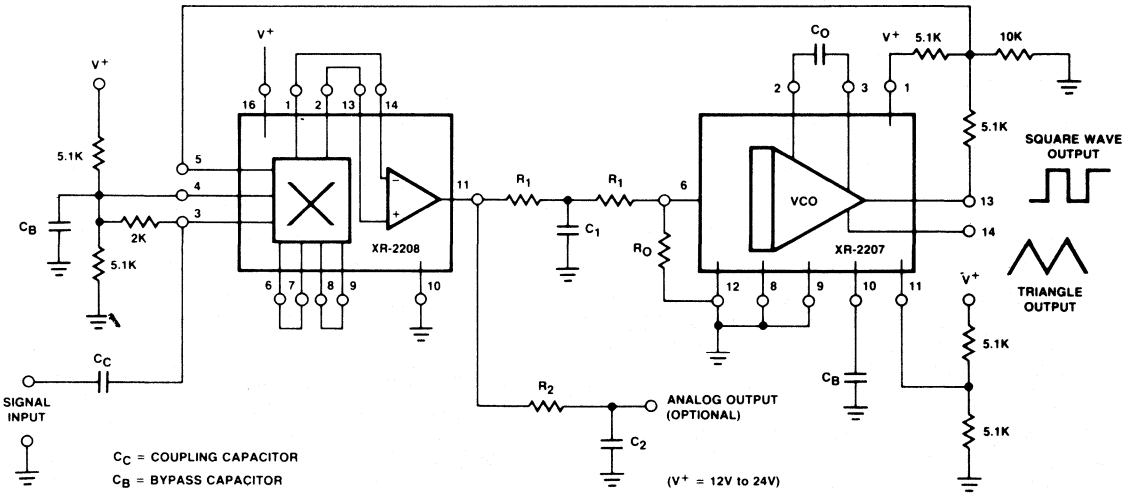


Figure 3. Circuit Interconnections for Single Supply Operation.

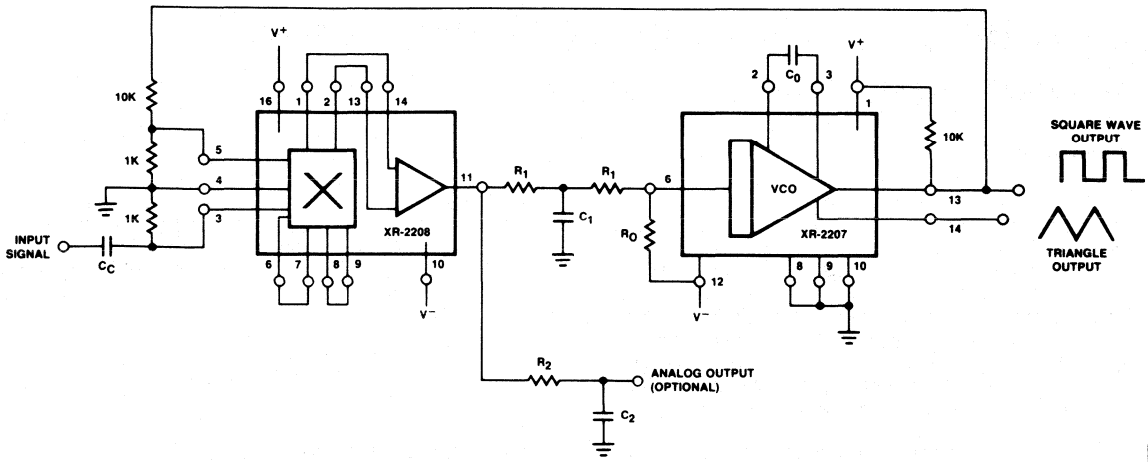


Figure 4. Circuit Interconnections for the Precision PLL System using the XR-2207 and the XR-2208 Monolithic Circuits. (Split-Supply operation, ±6V to ±13V.

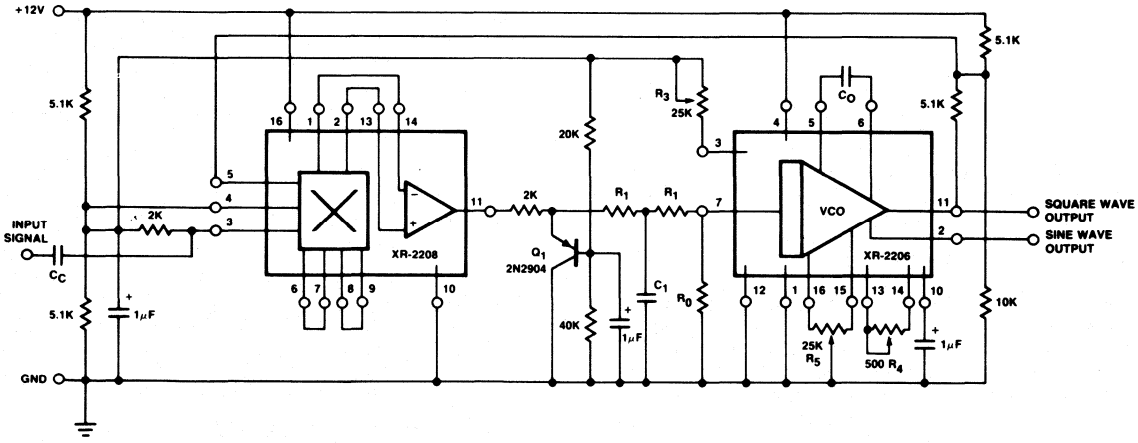


Figure 5.

Single-Chip Frequency Synthesizer Employing the XR-2240

INTRODUCTION

The XR-2240 monolithic timer/counter contains an 8-bit programmable binary counter and a stable time-base oscillator in a single 16-pin IC package. Although the circuit was originally designed as a long-delay timer capable of generating time delays from microseconds to weeks, it also offers a wide range of other applications beyond simple time-delay generation. One such unique application is its use as a single-chip, frequency synthesizer, where it can generate over 2,500 discrete frequencies from a single reference frequency input.

The operation of the XR-2240 as a frequency synthesizer is possible because of the ability of the circuit to both *multiply* and *divide* the input frequency reference. It can, simultaneously, multiply the input frequency by a factor, "M," and divide it by a factor "N + 1," where both M and N are adjustable integer values. Therefore, the circuit can produce an output frequency, f_O, related to the input reference frequency f_R as:

$$f_O = f_R \frac{M}{1 + N}$$

Figure 1 shows the circuit connection for operating the XR-2240 timer/counter as a self-contained frequency synthesizer. The integer values M and N can be externally adjusted over a broad range:

$$1 \leq M \leq 10 \quad 1 \leq N \leq 225$$

The multiplication factor M is obtained by locking on the harmonics of the input frequency. The division factor N is determined by the pre-programmed count in the binary counter section. The principle of operation of the circuit can be best understood by briefly examining its capabilities for frequency division and multiplication separately.

Frequency Division by (1 + N):

When there is no external reference input, f_R, the time-base oscillator section of the XR-2240 free-runs at its set frquency, f_S (f_S = 1/RC), where R and C are the external components at pin 13. The 8-bit binary counter can be programmed to divide the time-base frequency by an integer count, N, and generate an output pulse train whose frequency is:

$$f_O = f_S \frac{1}{1 + N}$$

Frequency Multiplication by "M":

Frequency multiplication is achieved by synchronizing the time-base oscillator with the *harmonics* of the input sync or reference signal. Thus, if the time-base oscillator is made to free-run at "M" times the input frequency, it can be made to synchronize the "M"th harmonic of the input reference signal. Typical capture range of the circuit is better than ±3%, for integer values of $1 \leq M \leq 10$; and since the time-base is accurate to within ± 0.5% of the external R-C setting, lock-up does not present a problem for a given harmonic lock setting.

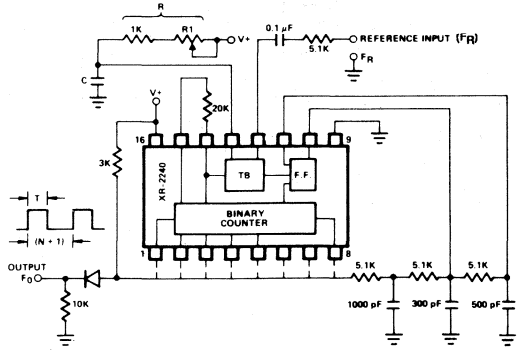


Figure 1. XR-2240 Frequency Synthesizer.

Circuit Operation:

With reference to Figure 1, the operation of the synthesizer circuit can be briefly explained as follows: The reference input frequency, f_R, is applied to the time-base sync terminal (pin 12) through a 5.1 KΩ series resistance and a coupling capacitor. The recommended waveform for the input frequency, f_R, is a 3 Vpp pulse train with a pulse width in the range of 30% to 80% of the time-base period, T. The multiplication factor M is chosen by the potentiometer R_1 which sets the time-base period T (T = RC). If no external reference is used, then M is automatically equal to 1.

The divider modulus, N, is chosen by shorting various counter outputs to a 3K common pull-up resistor. The output waveform is a pulse train with a fixed pulse width, T = RC, and a period T_O = (N + 1)RC.

The external R-C network between the output and the trigger and reset terminals of the XR-2240 is a non-critical delay network which resets and re-triggers the circuit to maintain a periodic output waveform. For the component values shown in Figure 1, the circuit can operate with the timing components R and C in the range of:

$$0.005\ \mu F \leq C \leq .1\ \mu F;\ 1\ K\Omega \leq R \leq\ 1\ M\Omega$$

The XR-2240 is a low-frequency circuit. Therefore, the maximum output frequency is limited to ≈200 kHz, by the frequency capability of the internal time base oscillator.

A particularly useful application of the simple synthesizer circuit of Figure 1 is to generate stable clock frequencies which are synchronized to an external reference, such as the 60 Hz line frequency. For example, one can generate a 100 Hz reference synchronized to 60 Hz line frequency simply by setting M = 5 and N = 2 such that:

$$f_O = f_R \frac{M}{1 + N} = (60)\frac{5}{1 + 2} = 100\ Hz$$

5

Dual Tone Decoding with XR-567 and XR-2567

INTRODUCTION

Two integrated tone decoders, XR-567 units, can be connected (as shown in Figure 1A) to permit decoding of simultaneous or sequential tones. Both units must be on before an output is given. R_1C_1 and $R'_1C'_1$ are chosen, respectively, for Tones 1 and 2. If sequential tones (1 followed by 2) are to be decoded, then C_3 is made very large to delay turn-off of Unit 1 until Unit 2 has turned on and the NOR gate is activated. Note that the wrong sequence (2 followed by 1) will not provide an output since Unit 2 will turn off before Unit 1 comes on. Figure 1B shows a circuit variation which eliminates the NOR gate. The output is taken from Unit 2, but the Unit 2 output stage is biased off by R_2 and CR_1 until activated by Tone 1. A further variation is given in Figure 1C. Here, Unit 2 is turned on by the Unit 1 output when Tone 1 appears, reducing the standby power to half. Thus, when Unit 2 is on, Tone 1 is or was present. If Tone 2 is now present, Unit 2 comes on also and an output is given. Since a transient output pulse may appear

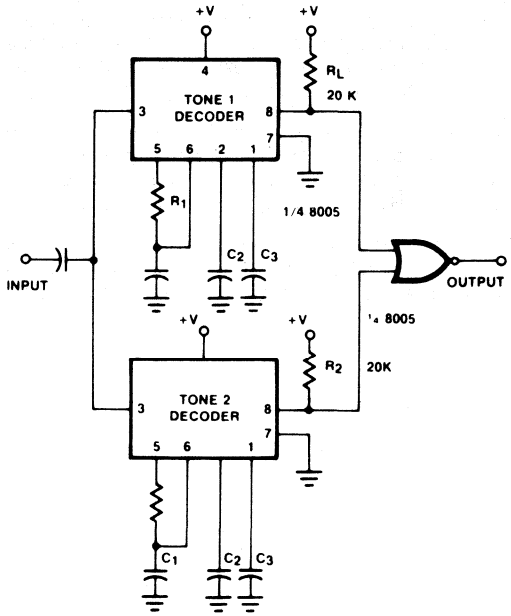


Figure 1A. Detection of Two Simultaneous or Sequential Tones

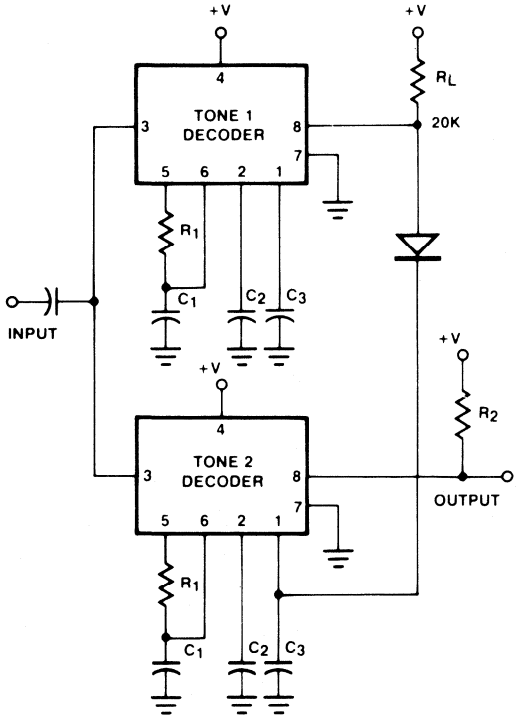


Figure 1B

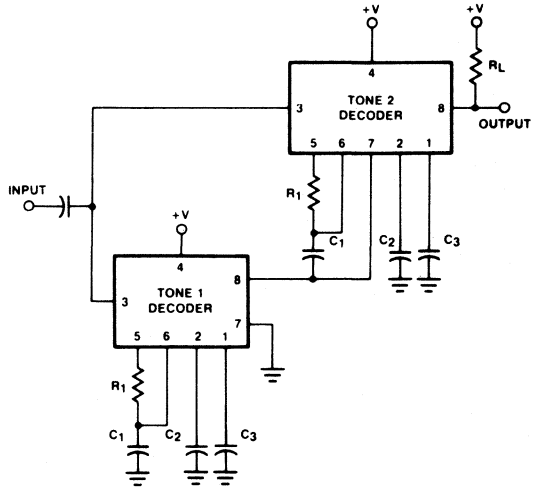
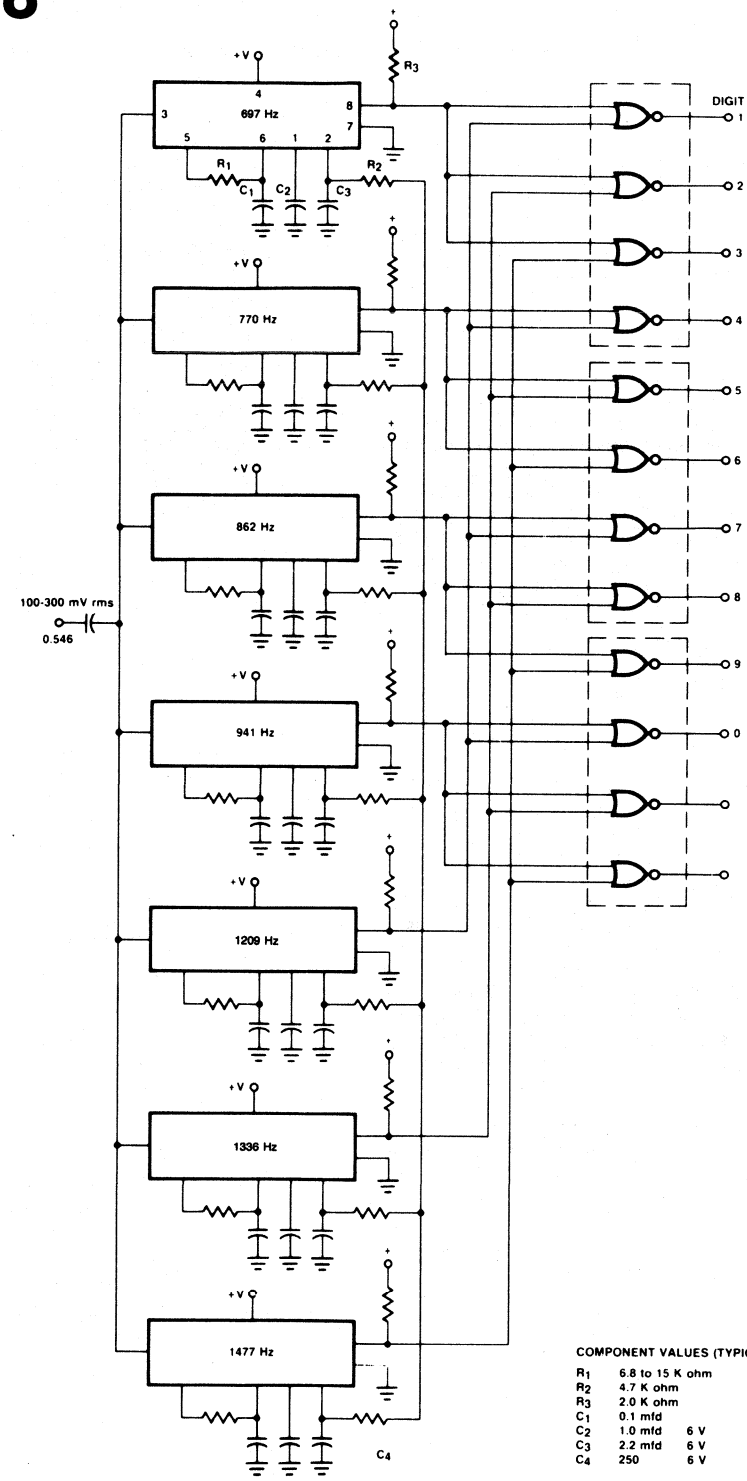


Figure 1C



COMPONENT VALUES (TYPICAL)

R_1	6.8 to 15 K ohm	
R_2	4.7 K ohm	
R_3	2.0 K ohm	
C_1	0.1 mfd	
C_2	1.0 mfd	6 V
C_3	2.2 mfd	6 V
C_4	250	6 V

Figure 2. Low-Cost Touch Tone® Decoder

during Unit 1 turn-on, even if Tone 2 is not present, the load must be slow in response to avoid a false output due to Tone 1 alone.

The XR-2567 Dual Tone Decoder can replace two integrated tone decoders in this application.

HIGH SPEED, NARROW BAND TONE DECODER

The circuit of Figure 1 may be used to obtain a fast, narrow band tone decoder. The detection bandwidth is achieved by overlapping the detection bands of the two tone decoders. Thus, only a tone within the overlap portion will result in an output. The input amplitude should be greater than 70 mV rms at all times to prevent detection band shrinkage and C_2 should be between $130/f_0$ and $1300/f_0$ mfd where f_0 is the nominal detection frequency. The small value of C_2 allows operation at the maximum speed so that worst-case output delay is only about 14 cycles.

TOUCH-TONE DECODER

Touch-Tone decoding is of great interest since all sorts of remote control applications are possible if you make use of the encoder (the push-button dial) that will ultimately be part of every tone. A low-cost decoder can be made as shown in Figure 2. Seven 567 tone decoders, their inputs connected in common to a phone line or acoustical coupler, drive three integrated NOR gate packages. Each tone decoder is tuned, by means of R_1 and C_1, to one of the seven tones. The R_2 resistor reduces the bandwidth to about 8% of 100 mV and 5% at 50 mV rms. Capacitor C_4 decouples the seven units. If you are willing to settle for a somewhat slower response at low input voltages (50 to 10 mV rms), the bandwidth can be controlled in the normal manner by selecting C_2, thereby eliminating the seven R_2 resistors and C_4. In this case, C_2 would be 4.7 mfd for the three lower frequencies or 2.2 mfd for the four higher frequencies.

The only unusual feature of this circuit is the means of bandwidth reduction using the R_2 resistors. As shown in the 567 data sheet under Alternate Method of Bandwidth Reduction, the external resistor R_A can be used to reduce the loop gain and, therefore, the bandwidth. Resistor R_2 serves the same function as R_A except that instead of going to a voltage divider for dc bias it goes to a common point with the six other R_2 resistors. In effect, the five 567's which are not being activated during the decoding process serve bias voltage sources for the R_2 resistors of the two 567's which are being activated. Capacitor C_4 (optional) decouples the ac currents at the common point.

LOW COST FREQUENCY INDICATOR

Figure 3 shows how two tone decoders set up with overlapping detection bands can be used for a go/no/go frequency meter. Unit 1 is set 6% above the desired sensing frequency and Unit 2 is set 6% below the desired frequency. Now, if the incoming frequency is within 13% of the desired frequency, either Unit 1 or Unit 2 will give an output. If both units are on, it means that the incoming frequency is within 1% of the desired frequency. Three light bulbs and a transistor allow low cost read-out.

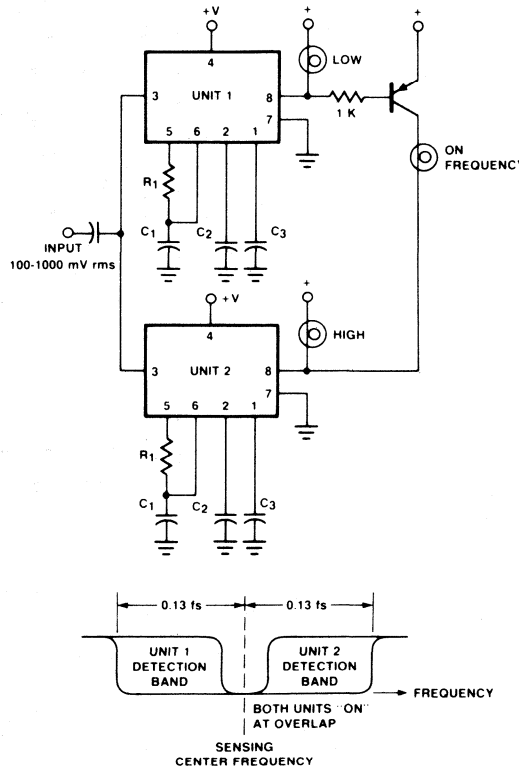


Figure 3. Frequency Meter with Low-Cost Lamp Readout

Sinusoidal Output from XR-215 Monolithic PLL Circuit

INTRODUCTION

In a wide range of communication or signal conditioning applications, it is necessary to obtain a sinusoidal output signal which is synchronized to a desired reference or clock input. This can be achieved by using the XR-215 type monolithic PLL circuit and an additional sine-shaping network.

When a periodic input signal is present within the capture range of the XR-215 PLL, the system will lock on the input; and the VCO section of the PLL will synchronize with the input frequency. The output of the oscillator section of the PLL can then be converted to a low distortion sine wave by a relatively simple sine-shaping circuit.

GENERAL DESCRIPTION

Figure 1 contains a functional block diagram of the XR-215 monolithic PLL system. The circuit consists of a balanced phase comparator, a highly stable voltage-controlled oscillator (VCO) and high speed operational amplifier. The phase comparator outputs are internally connected to the VCO inputs and to the non-inverting input of the operational amplifier. A self-contained PLL system is formed by simply ac coupling the VCO output to either of the phase comparator inputs and adding a low-pass filter to the phase comparator output terminals. The XR-215 can operate over a large choice of power supply voltages ranging from 5 volts to 26 volts and a wide frequency band of 0.5 Hz to 35 MHz. It can accommodate analog signals between 300 microvolts and 3 volts and can interface with conventional DTL, TTL and ECL logic families.

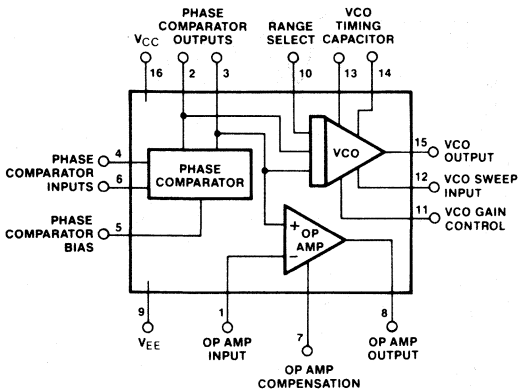


Figure 1. Functional Block Diagram of XR-215 Monolithic PLL Circuit

Figure 2 shows the simplified circuit schematic of the XR-215 phase-locked loop IC. The VCO part of XR-215, shown in the center section of Figure 2, is an emitter-coupled multivibrator circuit, whose frequency is set by an external capacitor, C_0, connected across the timing terminals (Pins 13 and 14). In this type of an oscillator, the differential voltage waveform across the timing capacitor, C_0, is a linear triangle, with a peak-to-peak amplitude of 1.4 volts. This output amplitude across the timing capacitor is independent of supply voltage.

This triangular waveform can be shaped into a low distortion sine wave by passing it through a simple differential gain stage, as shown in Figure 3. By adjusting the potentiometer R_g of Figure 3, the input transistors T_1 and T_2 of the differential stage can be brought to the verge of cutoff at the positive and the negative extremities of the input triangle wave. This causes the peaks of the triangle waveform to be rounded, resulting in a nearly sinusoidal output waveform from the differential stage. If the transistor characteristics and the current levels in the differential gain stage are well matched, one can reduce the total harmonic distortion (THD) of the sinusoidal output waveform to less than 3%.

The sine-shaper circuit of Figure 3 can be designed by using the XR-D101 NPN transistor array, which provides five identical NPN transistors in a single IC package. Figure 4 shows the package diagram of XR-D101 chip, in terms of its 16-pin DIP package.

The five independent transistors contained in the XR-D101 transistor array can be interconnected, as shown in Figure 5, to form the differential sine wave-shaping circuit of Figure 3. The inputs of the sine-shaper can be directly connected to the timing capacitor terminals (Pins 13 and 14) of the XR-215 PLL.

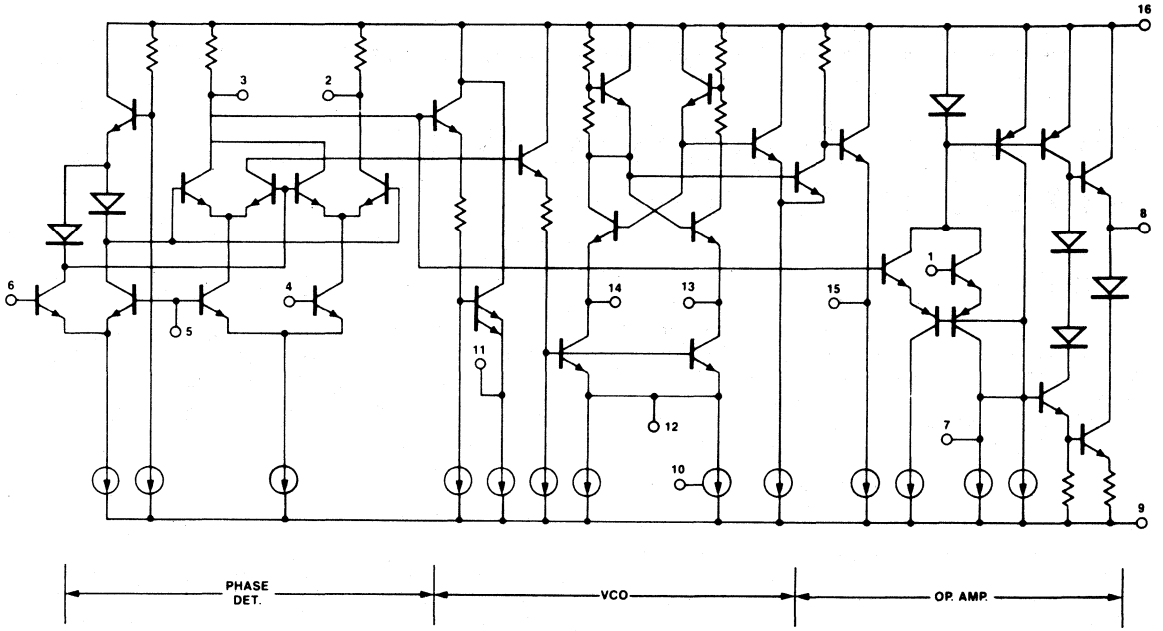


Figure 2. Simplified Schematic of XR-215

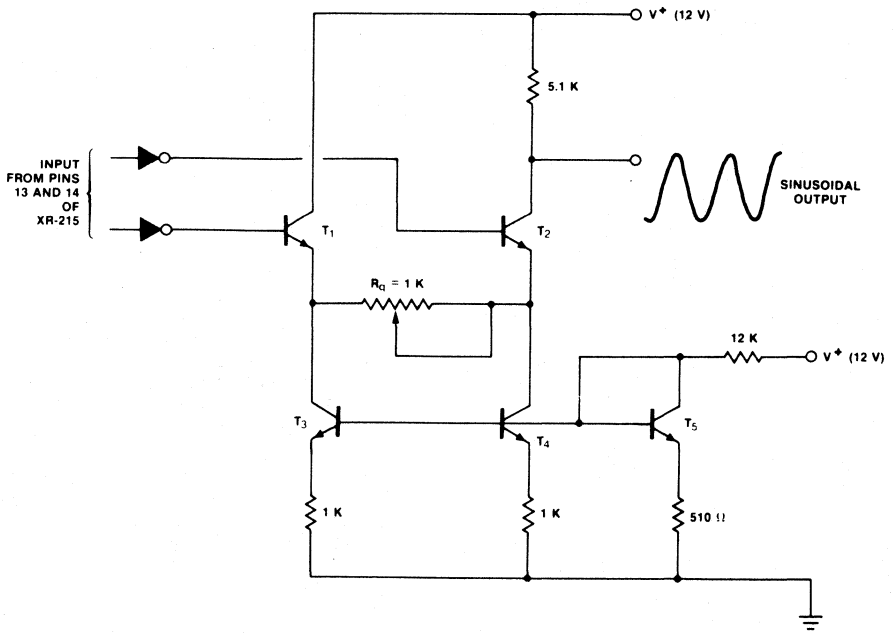


Figure 3. A Simple Triangle-to-Sine Wave Converter Using a Differential Gain Stage

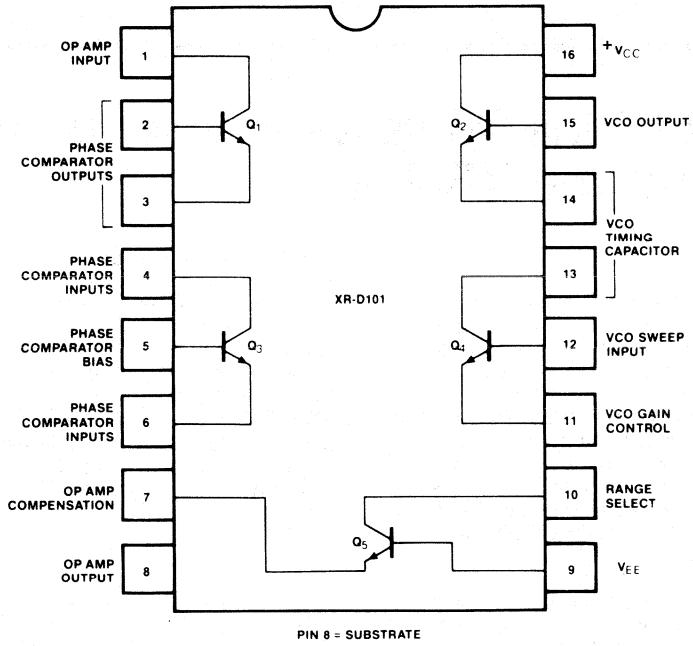
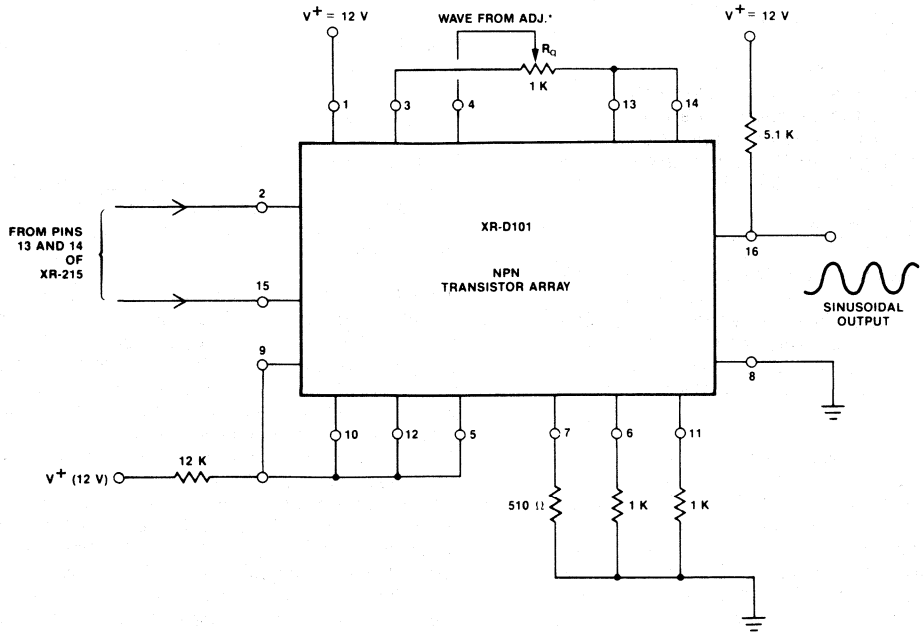


Figure 4. Package Diagram for XR-D101 Matched NPN Transistor Array



*ADJUST R_Q FOR MINIMUM HARMONIC DISTORTION.

Figure 5. Use of XR-D101 Transistor Array to Obtain Sinusoidal Output from XR-215 PLL

A Universal Sine Wave Converter using the XR-2208 and the XR-2211

INTRODUCTION

A universal sine wave converter is a system block which can convert *any* periodic input signal waveform to a low-distortion sine wave, whose frequency is identical to the repetition rate of the periodic input signal. Such universal sine wave converters find applications in communications and telemetry systems. They are particularly useful for converting transducer output waveforms, or pulses, into clean sine wave signals over a band of frequencies. This conversion to sine wave is often necessary to reduce the required system bandwidth for signal transmission by eliminating the harmonic frequencies of the signal.

In the cases where the input frequency is known, and does not change, the universal sine wave converter can be replaced by a simple high-Q filter, tuned to the input frequency. However, in many cases the input frquency, or the repetition rate, is *not* constant, but varies as a function of time or input data. In such cases a fixed-frequency filter is not feasible, and one is forced to use a universal sine wave converter which is essentially a *"tracking regenerative filter"*.

In this application note, the design principle and the performance characteristics of a regenerative sine wave converter circuit is described. The circuit operates on the phase-locked loop (PLL) principle and can be implemented using the XR-2211 monolithic PLL tone decoder and the XR-2208 multiplier IC.

PRINCIPLES OF OPERATION

Figure 1 shows the functional block diagram of a regenerative sine wave converter system, comprised of four functional blocks: (1) a phase-locked loop (PLL), (2) a sine-shaper, (3) a keyed amplifier, and (4) a lock-detect circuit. With reference to the figure, the principle of operation of the entire system can be briefly explained as follows:

When a periodic input signal is present at the input, within the tracking range of the PLL, the circuit would "lock" to the input signal; and the output of the voltage-controlled oscillator (VCO) section of the PLL will duplicate the frequency of the input signal. However, the VCO output waveform will have a fixed wave shape (normally a triangle wave) independent of the input waveform or amplitude. The output of the oscillator section then can be connected to a triangle-to-sine wave converter which converts it to a low-distortion sine wave. The output of the triangle-to-sine converter is then applied to a variable-gain amplifier which sets the desired output amplitude. Since the oscillator section of the PLL is always running, the circuit also contains a "lock-detect" section which *enables* the output amplifier only when there is an input signal. Thus, with no input signal present within the bandwidth of the PLL, the lock-detect section will keep the output amplifier in the "off" state, and the circuit will not produce an output signal.

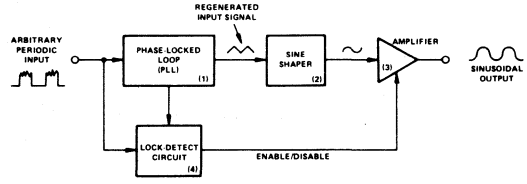


Figure 1. Basic Concept of a Regenerative Sinewave Converter.

CIRCUIT DESIGN

The basic regenerative sine wave converter system of Figure 1 can be easily implemented using the XR-2211 monolithic tone decoder and the XR-2208 monolithic multiplier IC's, with only a minimum number of external components.

The XR-2211 is a monolithic PLL circuit especially designed for FSK and tone detection. Thus, it contains the complete PLL and lock-detect sections (Blocks 1 and 4 of Figure 1) on the same chip. Its overall block diagram is shown in Figure 2. The circuit is packaged in a 14-pin dual-in-line package; and the functions of the circuit terminals are given in Figure 3 in terms of the monolithic IC package. In the sine wave converter application, the FSK detector portion of the circuit is not used; only the basic phase-locked loop and the lock-detector sections are utilized. Figure 4 illustrates the necessary external components for its application in the sine wave converter system. The oscillator section of the XR-2211 is an emitter–coupled multivibrator which oscillates by charging and discharging the external timing capacitor,

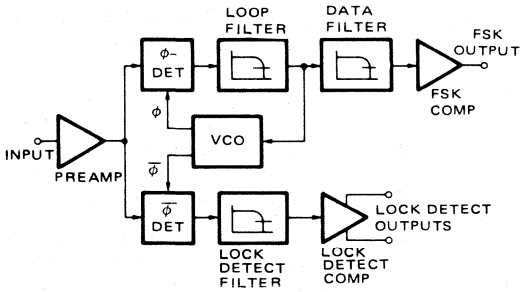


Figure 2. Block Diagram of XR-2211 Phase-Locked Loop FSK and Tone Decoder IC.

C_O, (connected across pins 13 and 14) through internal constant-current stages. Thus, the output waveform, taken differentially across the timing capacitor, is a linear triangle wave. This waveform can then be converted to a low-distortion sine wave by the XR-2208 multiplier.

The XR-2208 is a monolithic multiplier circuit which contains a four-quadrant analog multiplier, an op amp, and a unity-gain buffer amplifier in a 16-pin dual-in-line package. Its functional block diagram and equivalent circuit schematic are given in Figures 5 and 6, respectively.

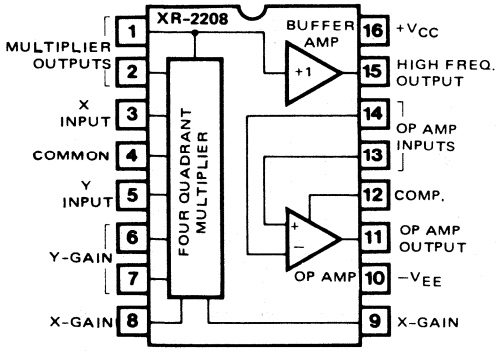


Figure 5. Diagram of XR-2208 Operational Multiplier.

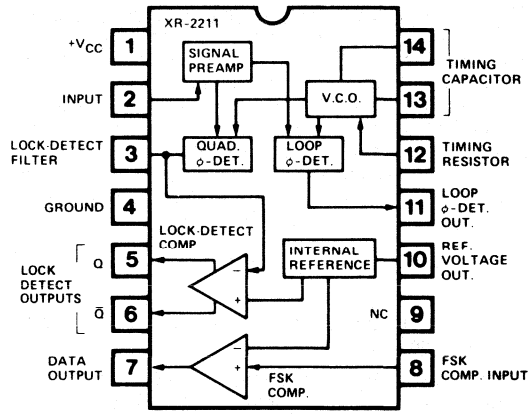


Figure 3. Package Diagram of XR-2211 PLL Circuit.

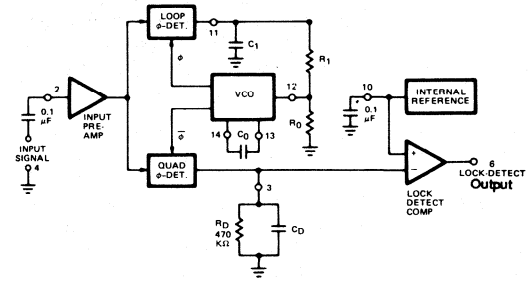


Figure 4. External Circuit Connections for XR-2211 for Sine-wave Converter Application.

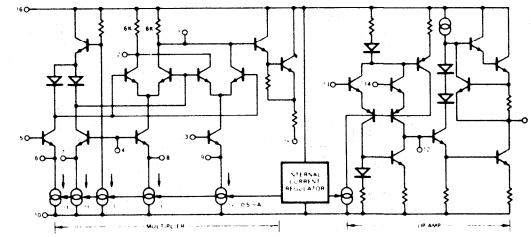


Figure 6. Simplified Circuit Schematic of the XR-2208 Operational Multiplier.

Figure 7 shows the recommended circuit connection of the XR-2211 and the XR-2208 to form a universal sine wave converter circuit. In the figure, a non-crital zener diode ($V_Z \approx$ 6V to 7V) is used to reduce the supply voltage applied to XR-2211, to facilitate DC coupling between the two chips. The frequency of the VCO section of the XR-2211 is set by the timing components R_O and C_O. In this application, a fixed value of R_O = 10KΩ is recommended, giving a center frequency, f_O value of:

$$f_O = \frac{100}{C_O\ (\mu F)} \text{ Hz}$$

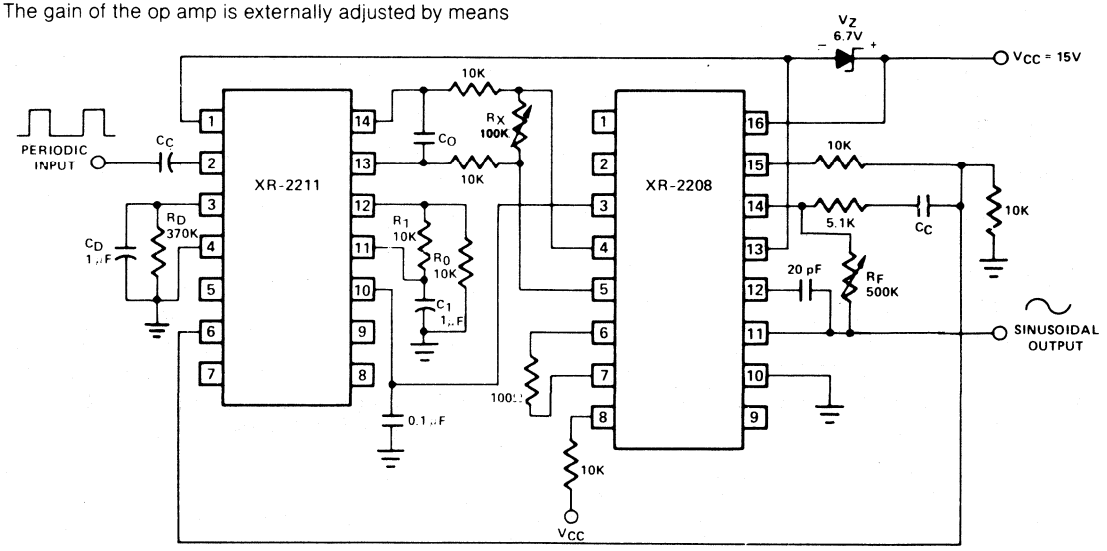
If a R_O value greater than 10KΩ is used, the VCO may not oscillate.

The triangle wave oscillator output of the XR-2211 PLL is attenuated through a resistive divider made up of two 10KΩ resistors, and a variable 10KΩ potentiometer, R_X. The attenuated triangle wave across R_X is then applied differentially to the X-input (pins 4 and 5) of the XR-2208. The 100Ω external resistor across Y-gain setting terminals (pins 6 and 7) causes the Y-input of the multiplier to be slightly overdriven, and thus causes the peaks of the triangle input rounded into a low-distortion sine wave.

The distortion of the sine wave is minimized by adjusting R_X, which sets the traingle wave amplitude. The output is available at the unity-gain buffer terminal (pin 15) of the XR-2208. This output is then level-shifted toward ground, through two 10KΩ resistors, and is AC coupled to the inverting input of the op amp section of XR-2208. The gain of the op amp is externally adjusted by means of the 500 kΩ potentiometer, R_F. The DC voltage level of the op amp output is set at the reduced supply voltage (i.e., $V_{CC} - V_Z$).

The lock-detect output of the XR-2211 (pin 6) is shorted to the mid-point of the resistive divider at pin 15 of the XR-2208. With no input signal present at the input within the lock range of the XR-2211, pin 6 is at a "low" state. Thus it acts as a shorting switch to ground and disables the op amp section of the XR-2208. When a periodic input signal appears at the circuit input and the XR-2211 establishes lock with the signal; the lock-detect output at pin 6 goes to a "high" or nonconducting state and enables the output op amp of the XR-2208; and a low-distortion sine wave output is obtained at the output (pin 11 of XR-2208).

The circuit of Figure 7 can operate as a sine wave converter, over a frequency band between two frequencies f_H and f_L corresponding to the upper and lower lock ranges of the PLL. With the components shown in the figure, this corresponds to approximately ±30% bandwidth around the center frequency, f_O, for inputs with close to 50% duty cycle. For periodic inputs with less than 50% duty cycle, this lock range is reduced further. For example, for inputs with 20% duty cycle, this bandwidth drops to about ±10% of center frequency. The operation of the circuit with input signals having less than 10% (or more than 90%) duty cycle is not practical. The minimum input level required for circuit operation is 10 mV rms. The circuit can generate a nearly sinusoidal output with input signals from very low



R_X = Distortion Adj. Potentiometer
R_F = Output Amplitude Adj. Pot.

C_C = Coupling Capacitor ($\geq 0.1\ \mu F$)

Figure 7. Recommended Circuit Connection for the Regenerative Sinewave Converter.

frequencies up to 100 kHz. Typical distortion characteristics of the output are shown in Figure 8, as a function of frequency of operation. Figure 9 shows a typical example of input and output waveforms for sine converter circuit of Figure 7, operating at 1 kHz input repetition rate, with a noisy input signal.

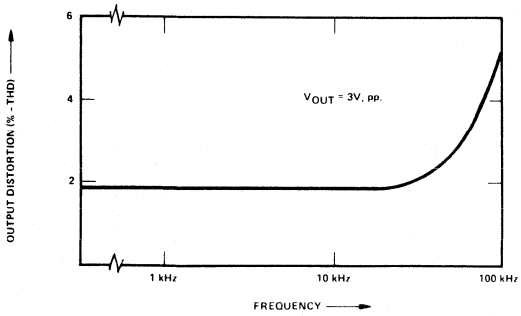


Figure 8. Output Distortion vs Frequency.

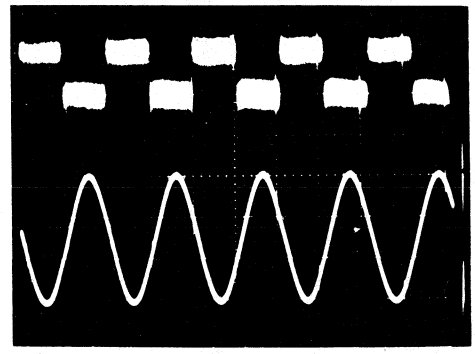


Figure 9. Typical Input-Output Waveforms.

(Top: Noisy Input Signal; Bottom: Sinusoidal Output.)
Scale: Vertical: 1 Volt/Div.
Horizontal: 1 m Sec./Div.

5

Designing High-Frequency Phase-Locked Loop Carrier-Detector Circuits

INTRODUCTION

The phase-locked loop (PLL) system can be converted to a frequency-selective tone- or carrier-detection system by the addition of a quadrature detector section to the basic PLL. Such a carrier-detect system serves as a lock indicator for the PLL and produces a logic signal at its output when there is a tone or a carrier signal present within the lock range of the phase-locked loop.

A number of monolithic tone-decoder ICs have been developed which implement the quadrature-detection technique for detection of low frequency tones, such as those used for telephone dialing or ultrasonic remote control. However, because of the particular PLL designs used in these monolithic detectors, their applications are limited to frequencies below 100 kHz. This application note describes a circuit approach, using the XR-210 or the XR-215 high frequency PLLs, along with the XR-2228 monolithic multiplier/detector, which extends phase-locked loop tone detection capabilities to frequencies up to 20 MHz.

PRINCIPLES OF OPERATION

The basic block diagram of a phase-locked loop tone detector system is shown in Figure 1. Such a detector system produces a logic-level signal at its output, when the PLL is locked on an input signal. It is made up of two main sections:

1. A PLL section which synchronizes or locks on the input signal.

2. A quadrature detector section made up of a phase-detector, a low-pass filter and a voltage-comparator.

The principle of operation can be briefly described as follows: When the PLL is locked on an input signal, its voltage-controlled oscillator (VCO) section produces a set of input signals, Φ_1 and Φ_1, which are 90° apart in phase, but have the same frequency as the input signal to be detected. One of these signals, Φ_1, is used to drive the PLL phase detector; the other output, which is called the "quadrature output" is used to drive a quadrature phase-detector, as shown in Figure 1. If the PLL is locked on the input signal, then the input signal and the VCO signal applied to the quadrature phase-detector are coherent in phase and frequency. This causes a DC level shift at the low-pass filtered output of the quadrature phase-detector and makes the voltage comparator output change its output logic state. Thus, an output logic signal is produced indicating the lock condition of the PLL.

This type of tone detection technique is a special case of the synchronous AM detection principle, discussed in detail in Exar's Application Note AN-13. The key difference between the tone detection and the synchronous AM detection application is that, in the case of the tone detection, a binary logic output is produced, corresponding to the *presence* or the *absence* of the desired input tone, rather than an analog demodulated signal.

XR-210 and XR-215 HIGH FREQUENCY PLL CIRCUITS

The XR-210 and the XR-215 are high frequency phase-locked loop detector and demodulator circuits. Their functional block diagrams are shown in Figures 2 and 3. Both circuits are packaged in 16-pin dual-in-line packages and contain high frequency VCO and phase-detector sections. The XR-215 chip also contains an operational amplifier. In the case of the XR-210, this op amp section is replaced by a high-gain voltage comparator which drives an open-collector type logic output. The XR-210 is particularly intended for FSK demodulation and can operate up to 20 MHz. The XR-215 is designed for linear FM detection and is suitable for frequencies up to 35 MHz. Except for the frequency capability of the VCO, the oscillator and the phase-comparator sections of both circuits are quite similar.

The VCO section of the XR-210 or the XR-215 does not provide a separate quadrature output, which is 90° phase-shifted with respect to the basic VCO output (Pin 15). However, the triangular output available across the VCO timing capacitor terminals (Pins 13 and 14) can

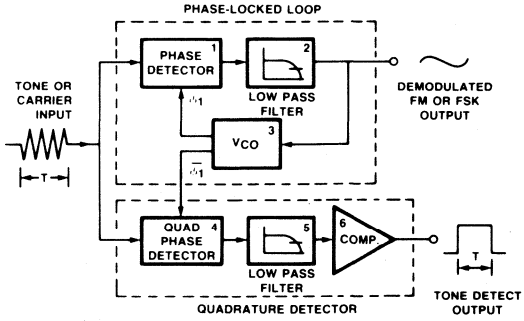


Figure 1. Functional Block Diagram of a PLL Tone- or Carrier-Detector System.

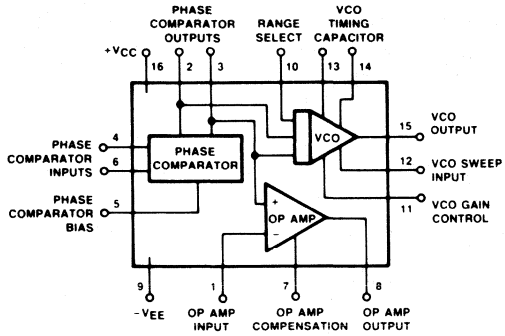


Figure 2. Functional Block Diagram of XR-210 High-Frequency FSK Modulator/Demodulator.

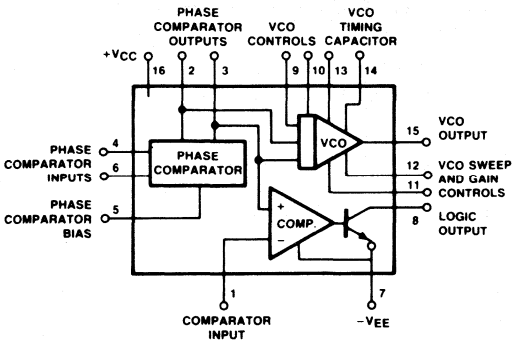


Figure 3. Functional Block Diagram of XR-215 High-Frequency Phase-Locked Loop.

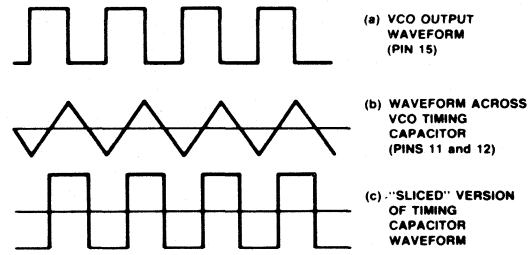


Figure 4. Timing Diagram of VCO Output Waveforms Available from XR-210 or XR-215 High-Frequency PLL Circuits.

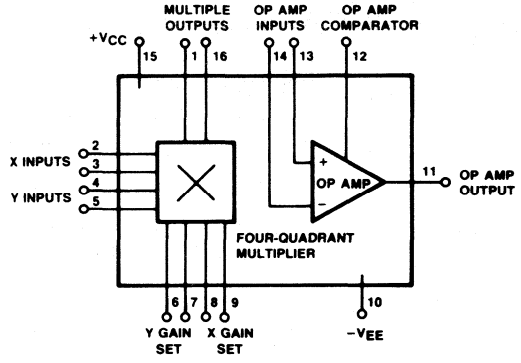


Figure 5. Functional Block Diagram of XR-2228 Multiplier/Detector.

serve as such a quadrature output if it is amplified and "sliced" externally, as shown in the timing diagram of Figure 4.

XR-2228 MULTIPLIER/DETECTOR CIRCUIT

The XR-2228 is comprised of a four-quadrant multiplier and a high-gain op amp on a single monolithic chip. It is packaged in a 16-pin dual-in-line package and has the functional block diagram shown in Figure 5. It contains independent and fully differential X- and Y-inputs which makes it easy to interface with the XR-210 or the XR-215 type PLL circuit for carrier-detection applications. In the tone- or carrier-detect application, the multiplier section of the XR-2228 is used as the quadrature phase-detector section of the block diagram of Figure 1. The op amp is used as a high-gain voltage comparator which converts the differential voltage level changes at the multiplier outputs into logic level output signals.

CIRCUIT OPERATION

Figure 6 shows the generalized circuit connection of the XR-2228, along with either the XR-210 or the XR-215 high frequency PLL IC, for tone- or carrier-detection application. Since the external connections for the XR-210 or the XR-215 are the same as those given in their respective data sheets, only the external circuitry associated with the XR-2228 is shown in the figure. The circuit, as shown, can operate with a single power supply, from 10 V to 20 V, or with split supplies in the range of ± 5 V to ± 10 V. In the case of split power supplies, the resistor string biasing the input terminals of the XR-2228 is not necessary and can be eliminated by connecting node A of Figure 6 to ground.

The input signal is AC coupled, with separate coupling capacitors, both to the input of the particular PLL circuit to be used, and to the X-input terminal (Pin 2) of the XR-2228.

The Y-inputs (Pins 4 and 5) are driven differentially from the VCO timing capacitor signal (available at Pins 13 and 14 of the PLL IC) which is AC coupled to Pins 4 and 5 of the XR-2228 multiplier input. The multiplier input stage "slices" this signal to produce the quadrature frequency waveform shown in Figure 4(c).

The differential DC voltage level at the multiplier output terminals (Pins 1 and 6) is offset by means of an external resistor, R_A, as shown in Figure 6. This initial offset causes the op amp output of the XR-2228 to settle to a known state when there is no carrier or tone signal to be detected. With the op amp input connections as shown in Figure 6, the op amp output (Pin 11) would be

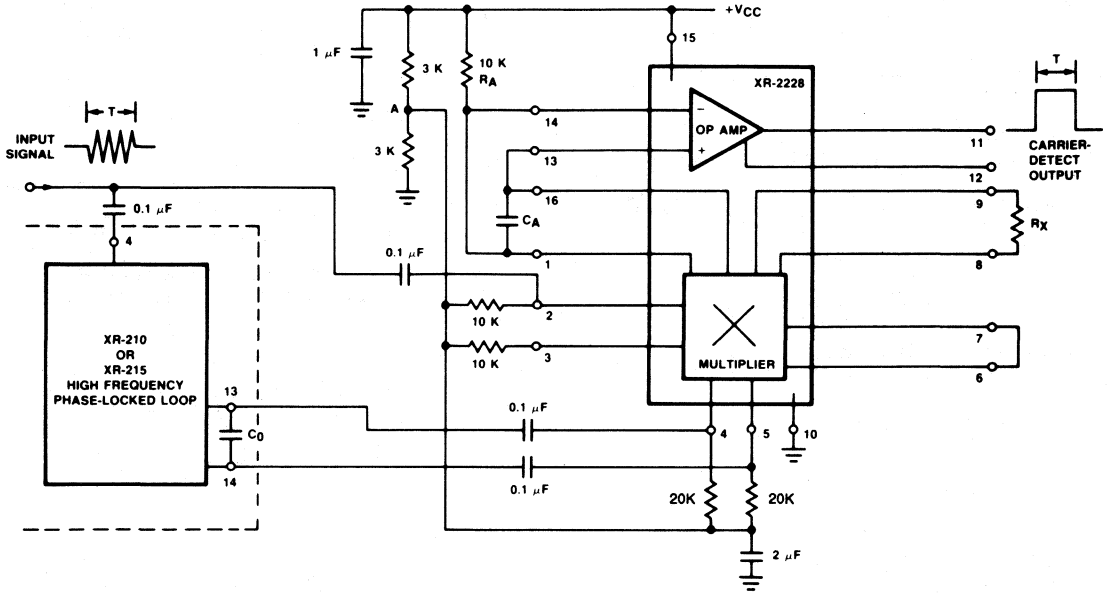


Figure 6. Recommended Circuit Connection of the XR-2228 with the XR-210 or the XR-215 High-Frequency Phase-Locked Loops for Tone- or Carrier-Detector Application.

at a "low" state when the PLL is not locked on a tone, and goes to a "high" state (near $+V_{CC}$) when the PLL circuit is locked on to an input tone. The output logic polarity can be reversed simply by reversing the op amp inputs.

The filter capacitor, C_A, connected across Pins 1 and 16 of the multiplier outputs, serves as the post-detection low-pass filter (Block 5 of Figure 1). The time constant of this filter is equal to (C_A R_B where R_B ($\approx$8 KΩ is the internal resistance of the IC at Pins 1 and 16. The value of C_A is chosen to provide a compromise between the response time and the spurious noise rejection characteristics of the circuit: increasing C_A improves the noise rejection characteristics of the circuit, but slows down the response time.

If chatter or oscillation is seen on the output of the XR-2228 op amp, a compensation capacitor of 200 pF from pin 12 to 11 should be added.

The detection threshold (minimum detectable input signal amplitude) varies inversely with the multiplier gain-setting resistor R_X. Figure 7 shows the typical detectable signal level, as a function of R_X, with the output offset resistor, R_A, equal to 10 KΩ. Note that the minimum detectable input signal, with R_X = 0, is approximately 100 mV, rms.

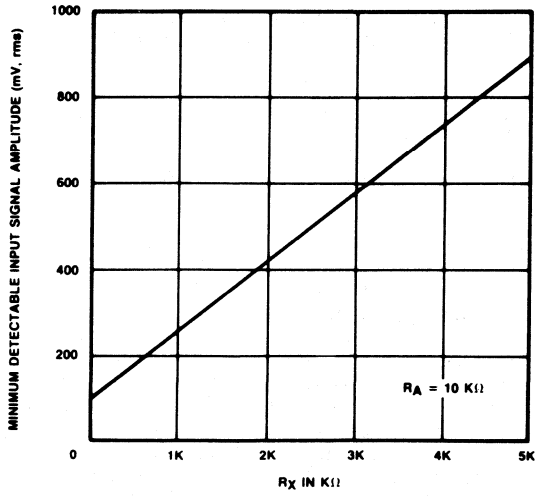


Figure 7. Minimum Detectable Input Carrier Level, as a Function of Multiplier Gain Setting Resistor, R_X.

Frequency-Selective AM Detection using Monolithic Phase-Locked Loops

INTRODUCTION

This application note describes the use of monolithic phase-locked loop (PLL) circuits in detection of amplitude-modulated (AM) signals. The detection capabilities of a PLL system, which is a frequency-selective FM demodulator, can be extended to cover AM signals simply by the addition of an analog multiplier (or mixer) and a low-pass filter to the basic phase-locked loop. This technique of AM demodulation, which is called synchronous AM detection, offers significant performance advantages over conventional peak-detector type AM demodulators, in terms of its dynamic range and noise characteristics.

This application note outlines some of the fundamental principles of synchronous AM detectors, and gives design examples using the XR-2228 multiplier/detector IC in conjunction with the XR-215 and the XR-2212 monolithic PLL circuits.

PRINCIPLES OF OPERATION

The phase-locked loop AM detector circuits operate on the so-called "coherent AM detection" principle, where the amplitude modulated input signal is mixed with an unmodulated "coherent" carrier signal, and then low-pass filtered to produce the desired demodulated output signal. Figure 1 gives a simplified block diagram of such a detector system.

The amplitude-modulated input signal can be described by an expression of the form:

$$\text{Input Signal} = V_m(t) \cos \omega_o t$$

where $V_m(t)$ is the modulated amplitude of the input signal and ω_o is the input signal frequency expressed in radians/seconds. If this signal is linearly multiplied with an *unmodulated* signal which has the *same* frequency and phase as the input signal, then the output of the multiplier, $V_0(t)$, is a composite signal of the form:

$$V_0(t) = K_0 V_m(t) [1 + \cos (2 \omega_o t)]$$

where K_0 is the gain of the multiplier circuit. If the above signal is then passed through a low-pass filter, to eliminate the double-frequency term, the resulting output signal is:

$$V_{out} = \text{Output Signal} = K_0 V_m(t)$$

which corresponds to the detected AM information.

The phase-locked loop AM detectors also operate on a similar principle: the PLL is made to "lock" on the carrier frequency of the input AM signal; then the VCO output of the PLL will regenerate the unmodulated coherent carrier signal necessary for detection. When this signal is mixed with the input AM signal and the resulting composite signal is passed through a low pass filter, one obtains the demodulated output. Figure 2 gives a block diagram of such an AM detector system. Compared to the basic synchronous AM detector system of Figure 1, the phase-locked loop AM detector of Figure 2 also has one added feature: the output of the PLL control voltage (i.e., output of the PLL low-pass filter) can be used as an FM detector or a frequency discriminator. Thus, such a system is capable of simultaneous AM and FM detection. In other words, the frequency and the amplitude modulation information present on the input signal can be *separately* and *simultaneously* demodulated. The particular design and application examples given in this application note fall into this category.

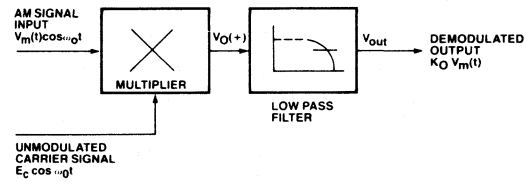


Figure 1 Block Diagram of a Synchronous AM Detector.

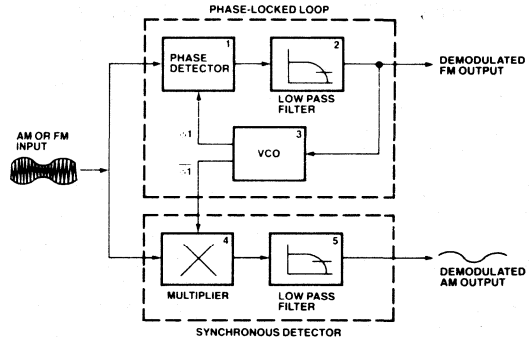


Figure 2. The Basic Phase-Locked Loop AM Detector.

XR-2212 AND XR-2228 MONOLITHIC CIRCUITS

The XR-2212 monolithic PLL is made up of an input preamplifier, a phase-detector, a high-gain differential amplifier and a stable voltage-controlled oscillator (VCO) as shown in Figure 3. The key feature of the XR-2212 PLL is the temperature stability and the frequency accuracy of its VCO section; it offers 20 ppm/°C typical temperature stability and a frequency accuracy of ± 1% for an external RC setting. The oscillator section of the XR-2212 contains a separate "quadrature output" terminal (Pin 15) which is particularly intended for interfacing with a synchronous AM detector such as the XR-2228.

The XR-2228 multiplier/detector IC is specifically intended as a basic building block for synchronous AM detection. It contains a four-quadrant analog multiplier and a high-gain op amp on the same chip, as shown in the functional block diagram of Figure 4.

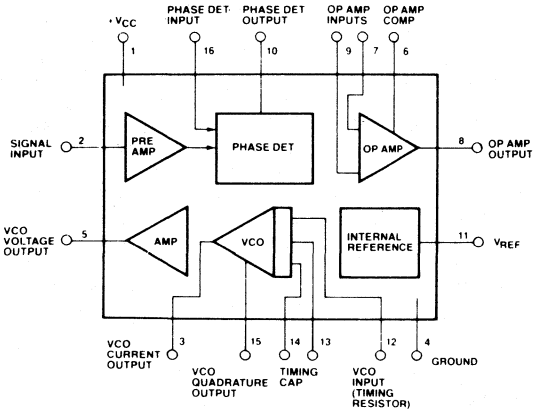


Figure 3. Functional Block Diagram of XR-2212 Precision Phase-Locked Loop.

XR-215 HIGH FREQUENCY PHASE-LOCKED LOOP

The XR-215 is a high frequency phase-locked loop circuit capable operating with input signal frequencies up to 35 MHz. It is comprised of a high frequency VCO, a phase-detector and an op amp section, as shown in the block diagram of Figure 5.

Unlike the XR-2212 PLL, the VCO section of the XR-215 does not have a separate quadrature output terminal. However, such a quadrature oscillator signal can be obtained by amplifying and "slicing" the triangle waveform available across the timing capacitor (Pins 13 and 14) of the XR-215 oscillator section. Figure 6 shows the relative phase relationship of these oscillator waveforms available from the circuit. The desired quadrature output signal (curve C of Figure 6) can be obtained by directly connecting one pair of the differential inputs of the XR-2228 directly across the timing capacitor terminals of the XR-215.

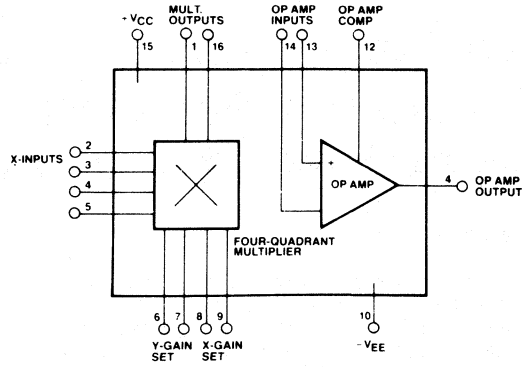


Figure 4. Functional Block Diagram of XR-2228 Multiplier/Detector IC.

AM/FM DETECTION USING THE XR-2212 PLL

Figure 7 shows a generalized circuit connection diagram for a two-chip AM and FM detection system, utilizing the XR-2212 PLL and the XR-2228 multiplier/detector. The XR-2212 section serves as the basic FM detector. The quadrature output of its VCO (Pin 15) is AC coupled to the Y input of the XR-2228.

The Y input of the XR-2228 is operated in its switching mode, with the Y gain terminals (Pins 6 and 7) shorted together. The AM and/or FM signal is simultaneously applied to both circuits through coupling capacitors; and all the mutliplier inputs are DC biased from the internal reference output of the XR-2212 (Pin 11). The output of the multiplier, at Pin 16, is AC coupled to the op amp section of the XR-2228, which serves as the post-detection amplifier for the demodulated AM signal.

The circuit configuration shown in Figure 7 can operate with a single power supply, over the supply voltage range, of 10V to 20V. Its operation or performance can be tailored for any particular AM and FM detection application by the choice external components shown in the figure, over a carrier frequency band of 1 kHz to

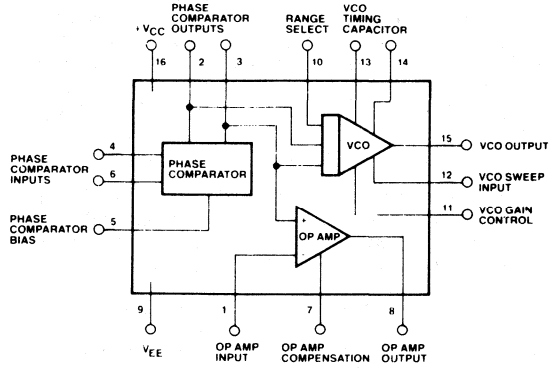


Figure 5. Functional Diagram of XR-215 High-Frequency Phase-Locked Loop.

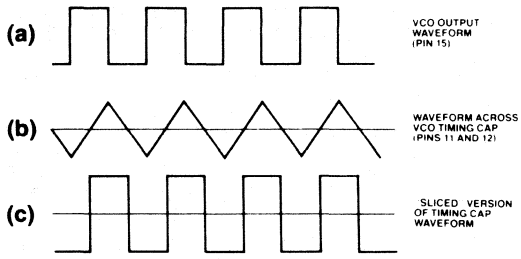


Figure 6. Timing Diagrams of VCO Output Waveforms from XR-215 Monolithic Phase-Locked Loop.

300 kHz. The functions of these external components are as follows:

a) R_0 and C_0 set the VCO center frequency for the XR-2212 PLL circuit. The center frequency, f_0, is given as:

$$f_0 = \frac{1}{R_0 C_0}$$

The VCO frequency f_0 is chosen to be equal to the carrier frequency of the input signal. R_0 is normally chosen to be in the range of 10 kΩ to 100 kΩ. This choice is arbitrary. For most applications $R_0 \approx 20$ kΩ is recommended. Once f_0 is given and R_0 is chosen, the C_0 can be calculated from the above equation.

b) R_1 determines the tracking bandwidth of the PLL. For a required tracking bandwidth, Δf (see Figure 9 of XR-2212 data sheet) and f_0, R_1 can be calculated as:

$$R_1 = R_0 \frac{f_0}{\Delta f}$$

This tracking bandwidth, Δf, is the band of frequencies in the vicinity of f_0, over which the PLL can maintain lock.

c) C_1 sets the loop-damping factor for the PLL. For most applications, C_1 is chosen to be equal to one-half of C_0.

d) R_2 and C_2 form a low-pass filter for the detected FM signal. The 3 dB frequencing, f_2, of this low-pass filter is:

$$f_2 = \frac{1}{2\pi R_2 C_2}$$

Normally, f_2 is chosen to be equal to the demodulated FM information bandwidth.

e) R_C and R_{F1} set the gain of the op amp section of the XR-2212 as:

$$A_V = 1 + \frac{R_{F1}}{R_C}$$

This op amp section serves as the post-detection amplifier for the demodulated FM signals.

f) R_X sets the multiplier gain for the X input and R_{F2} sets the gain of the op amp section of the XR-2228. Thus, the demodulated AM signal output swing, V_{out}, for a given input signal of peak amplitude of V_M and modulation index of m ($0 \leq m \leq 1$) can be approximated as:

$$V_{out} = \frac{(V_M)m}{4} \frac{R_{F2}}{R_X}$$

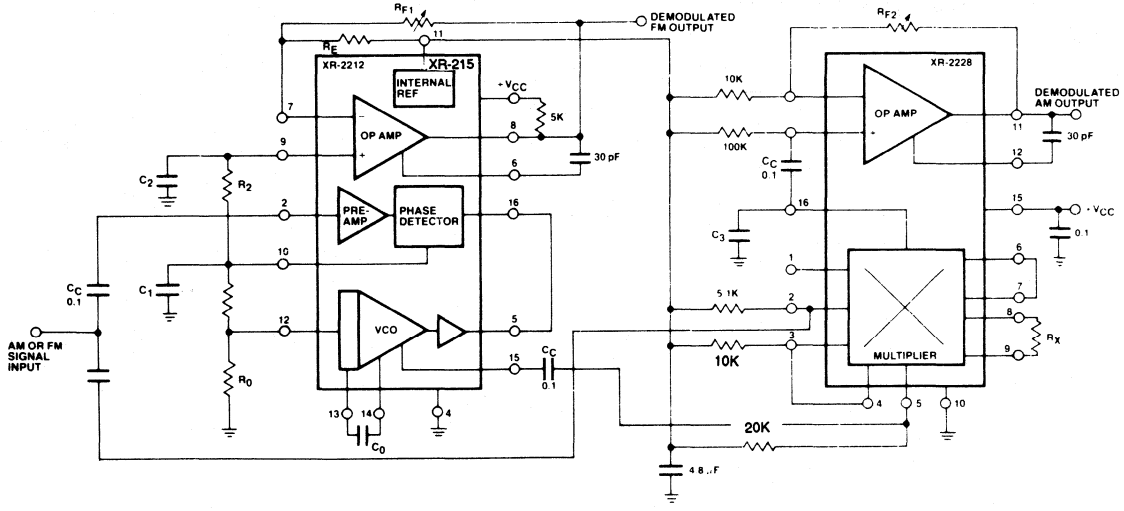


Figure 7. A Two-Chip AM/FM Detector System Using the XR-2212 Phase-Locked Loop and the XR-2228 Multiplier/Detector.

Thus, for example, a 100 mV peak input signal with 30% AM modulation (m = 0.3) will give a demodulated output of 150 mV peak, with R_{F2} = 100 kΩ and R_X = 5 kΩ, at Pin 11 of the XR-2228.

g) C_3, in conjunction with the 5 kΩ internal impedance of the multiplier output (Pin 16) serves as the low-pass post-detection filter for the demodulated AM signal.

For further explanation and description for the system design equations, the reader is referred to the XR-2212 and the XR-2228 data sheets.

Design Example

Design an AM demodulator for 100 kHz carrier frequency with a detection (tracking) bandwidth of ±4%. The demodulated information bandwidth is 3 kHz and an output level of one volt peak is required for a one volt peak input with 30% modulation.

Using the circuit of Figure 7, one proceeds as follows: Since FM detection is not required in this example, components R_2, C_2, R_C and R_{F1} are not essential to circuit operation. R_2 and R_C can be short-circuited, C_2 and R_{F1} can be left open-circuited. The rest of the component values are calculated as follows:

Step 1) Set f_0 = 100 kHz by choosing R_0 = 20 kΩ and calculating C_0 from paragraph (a) above.

$$C_0 = \frac{1}{R_0 f_0} = 500 \text{ pF}$$

Step 2) Determine R_1 to set tracking bandwidth to ± 4%, from paragraph (b): R_1 = 500 kΩ.

Step 3) Calculate C_1:$C_1 \approx C_0/2 \approx 250$ pF.

Step 4) From paragraph (f), calculate the value of R_X and R_{F2}. For a typical choice of R_X = 5 kΩ, and m = 0.3 (30% modulation) with one volt input carrier level, the value of R_{F2} to get one volt demodulated output is: R_{F2} = 67 kΩ.

Step 5) Calculate C_3 to get 3 kHz bandwidth for post-detection filter: $C_3 \approx 0.01$ μF.

AM DETECTION USING THE XR-215 PLL

Figure 8 shows the circuit connection diagram for a two-chip AM and FM detection system, using the XR-215 high-frequency PLL in conjunction with the XR-2228 multiplier/detector. Because of the high-frequency capability of the XR-215, the circuit of Figure 8 is useful as a phase-locked AM detector for carrier frequencies up to 20 MHz, and operates over a supply voltage range of 10V to 20V.

The VCO section of XR-215 does not have a separate quadrature output. However, this problem can be overcome by driving the XR-2228 multiplier directly from the timing capacitor terminals (Pins 13 and 14) of XR-215. The Y input of the XR-2228 is operated with maximum gain, since the Y gain control terminals (Pins 6 and 7) are shorted together. This causes the triangular waveform across C_0 to be converted to an effective quadrature drive as indicated by the timing diagram of Figure 6. The modulated input signal is simultaneously applied to both circuits through coupling capacitors. The phase-detector inputs of the XR-215, as well as the multiplier X inputs of the XR-2228, are biased at approximately one-half of V_{CC}, by means of an external resistive divider.

In Figure 8, C_0 sets the VCO frequency of the XR-215. In the case of FM demodulation, R_1 and C_1 serve as the post-detection filter for the detected FM signal and R_{F1} sets the gain of the FM post-detection amplifier.

The mode of operation of the XR-2228 is virtually the same as that described in connection with Figure 7: R_X sets the multiplier demodulation gain; C_3 serves as the low-pass post-detection filter. The values of R_X, R_{F2} and C_3 are calculated as given in paragraphs (f) and (g).

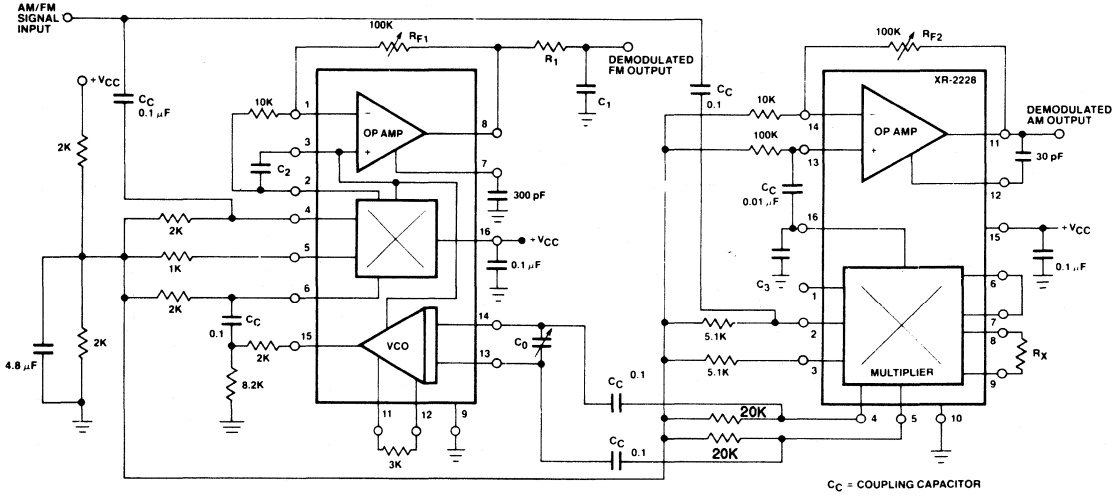


Figure 8. Circuit Connection for a High-Frequency AM and FM Detector Using the XR-215 and XR-2228.

High-Quality Function Generator System with the XR-2206

INTRODUCTION

Waveform or function generators capable of producing AM/FM modulated sine wave outputs find a wide range of applications in electrical measurement and laboratory instrumentation. This application note describes the design, construction and the performance of such a complete function generator system suitable for laboratory usage or hobbyist applications. The entire function generator is comprised of a single XR-2206 monolithic IC and a limited number of passive circuit components. It provides the engineer, student, or hobbyist with a highly versatile laboratory instrument for waveform generation at a very small fraction of the cost of conventional function generators available today.

GENERAL DESCRIPTION

The basic circuit configuration and the external components necessary for the high-quality function generator system is shown in Figure 1. The circuit shown in the figure is designed to operate with either a 12 V single power supply, or with ±6 V split supplies. For most applications, split-supply operation is preferred since it results in an output dc level which is nearly at ground potential.

The circuit configuration of Figure 1 provides three basic waveforms: since, triangle and square wave. There are four overlapping frequency ranges which give an overall frequency range of 1 Hz to 100 kHz. In each range, the frequency may be varied over a 100:1 tuning range.

The sine or triangle output can be varied from 0 to over 6 V (peak to peak) from a 600 ohm source at the output terminal.

A squarewave output is available at the sync output terminal for oscilloscope synchronizing or driving logic circuits.

TYPICAL PERFORMANCE CHARACTERISTICS

The performance characteristics listed below are not guaranteed or warranted by Exar. However, they represent the typical performance characteristics measured by Exar's application engineers during the laboratory evaluation of the function generator system shown in Figure 1. The typical performance specifications listed below apply only when all of the recommended assembly instructions and adjustment procedures are followed:

(a) Frequency Ranges: The function generator system is designed to operate over four overlapping frequency ranges:

1 Hz to 100 Hz
10 Hz to 1 kHz
100 Hz to 10 kHz
1 kHz to 100 kHz

The range selection is made by switching in different timing capacitors.

(b) Frequency Setting: At any range setting, frequency can be varied over a 100:1 tuning range with a potentiometer (see R_{13} of Figure 1).

(c) Frequency Accuracy: Frequency accuracy of the XR-2206 is set by the timing resistor R and the timing capacitor C, and is given as:

$$f = 1/RC$$

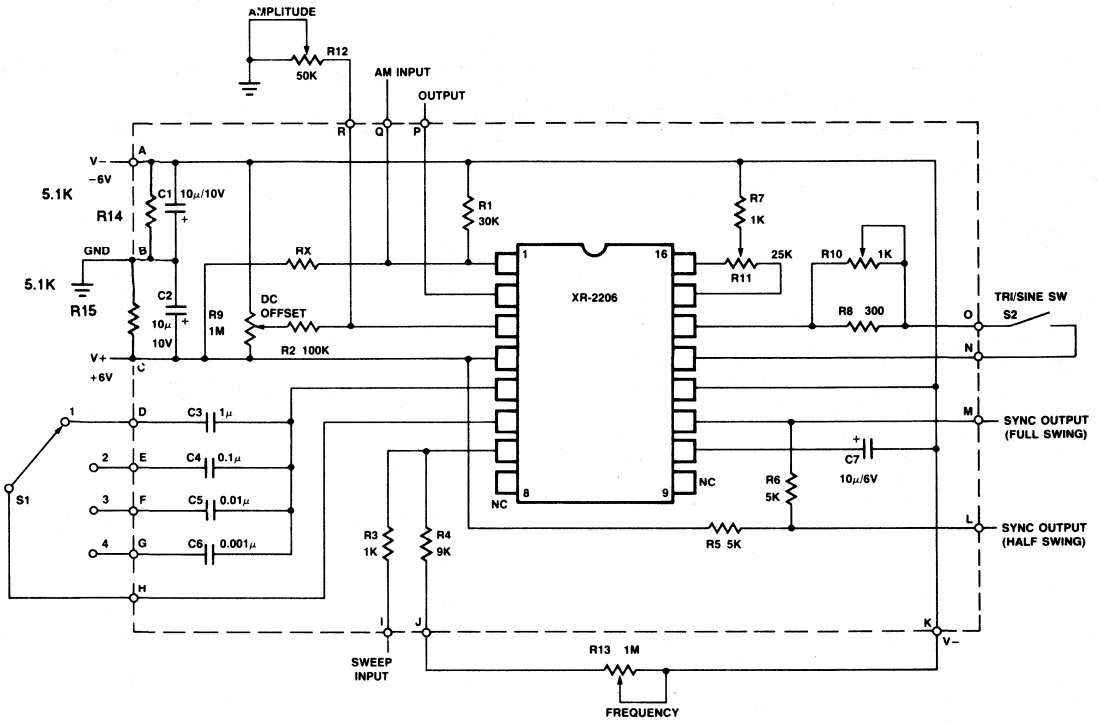
The above expression is accurate to within ±5% at any range setting. The timing resistor R is the series combination of resistors R_4 and R_{13} of Figure 1. The timing capacitor C is any one of the capacitors C_3 through C_6, shown in the figure.

(d) Sine and Triangle Output: The sine and triangle output amplitudes are variable from 0 V to 6 V_{pp}. The amplitude is set by an external potentiometer, R_{12} of Figure 1. At any given amplitude setting, the triangle output amplitude is approximately twice as high as the sinewave output. The internal impedance of the output is 600 Ω.

(e) Sinewave Distortion: The total harmonic distortion of sinewave is less than 1% from 10 Hz to 10 kHz and less than 3% over the entire frequency range. The selection of a waveform is made by the triangle/sine selector switch, S_2.

(f) Sync Output: The sync output provides a 50% duty cycle pulse output with either full swing or upper half swing of the supply voltage depending on the choice of sync output terminals on the printed circuit board (see Figure 1).

(g) Frequency Modulation (External Sweep): Frequency can be modulated or swept by applying an external control voltage to sweep terminal (Terminal I of Figure 1). When not used, this terminal should be left open-



NOTE:

1. For Single Supply Operation Lift GND Connection Keeping R12 Across Terminals R and B Intact, and Connect Terminal A to GND.

2. For Maximum Output, R_X may be open. R_X = 68 KΩ is Recommended for External Amplitude Modulation.

Figure 1. Circuit Connection Diagram for Function Generator. (See Note 1 for Single Supply Operation.)

circuited. The open circuit voltage at this terminal is approximately 3V above the negative supply voltage and its impedance is approximately 1000 ohms.

(h) Amplitude Modulation: The output amplitude varies linearly with modulation voltage applied to AM input (terminal Q of Figure 1). The output amplitude reaches its minimum as the AM control voltage approaches the half of the total power supply voltage. The phase of the output signal reverses as the amplitude goes through its minimum value. The total dynamic range is approximately 55 dB, with AM control voltage range of 4V referenced to the half of the total supply voltage. When not used, AM terminal should be left open-circuited.

(i) Power Source: Split supplies: ±6 V, or single supply: + 12V. Supply Current 15 mA (see Figure 2). For single supply operation bias resistors, R14 and R15 should be added, the GND point left floating and V⁻ tied to ground.

EXPLANATION OF CIRCUIT CONTROLS:

Switches

Range Select Switch, S1: Selects the frequency range of operation for the function generator. The frequency is inversely proportional to the timing capacitor connected across Pins 5 and 6 of the XR-2206 circuit. Nominal capacitance values and frequency ranges corresponding to switch positions of S1 are as follows:

Position	Nominal Range	Timing Capacitance
1	1 Hz to 100 Hz	1 μF
2	10 Hz to 1 kHz	0.1 μF
3	100 Hz to 10 kHz	0.01 μF
4	1 Hz to 100 kHz	0.001 μF

If additional frequency ranges are needed, they can be added by introducing additional switch positions.

Triangle/Sine Waveform Switch, S2: Selects the triangle or sine output waveform.

Trimmers and Potentiometers

Dc Offset Adjustment, R9: The potentiometer used for adjusting the dc offset level of the triangle or sine output waveform.

Sinewave Distortion Adjustment, R10: Adjusted to minimize the harmonic content of sinewave output.

Sinewave Symmetry Adjustment, R11: Adjusted to optimize the symmetry of the sinewave output.

Amplitude Control, R12: Sets the amplitude of the triangle or sinewave output.

Frequency Adjust, R13: Sets the oscillator frequency for any range setting of S1. Thus, R13 serves as a frequency dial on a conventional waveform generator and varies the frequency of the oscillator over an approximate 100 to 1 range.

Terminals

A. Negative Supply -6V
B. Ground
C. Positive Supply +6V
D. Range 1, timing capacitor terminal
E. Range 2, timing capacitor terminal
F. Range 3, timing capacitor terminal
G. Range 4, timing capacitor terminal
H. Timing capacitor common terminal
I. Sweep Input
J. Frequency adjust potentiometer terminal
K. Frequency adjust potentiometer negative supply terminal
L. Sync output (1/2 swing)
M. Sync output (full swing)
N. Triangle/sine waveform switch terminals
O. Triangle/sine waveform switch terminals
P. Triangle or sinewave output
Q. AM input
R. Amplitude control terminal

PARTS LIST

The following is a list of external circuit components necessary to provide the circuit interconnections shown in Figure 1.

Capacitors:

C1, C2, C7	Electrolytic, 10 μF, 10V
C3	Mylar, 1 μF, nonpolar, 10%
C4	Mylar, 0.1 μF, 10%
C5	Mylar, 0.01 μF, 10%
C6	Mylar, 1000 pF, 10%

Resistors:

R1	30 KΩ, 1/4 W, 10%
R2	100 KΩ, 1/4 W, 10%
R3, R7	1 KΩ, 1/4 W, 10%
R4	9 KΩ, 1/4 W, 10%
R5, R6	5 KΩ, 1/4 W, 10%
R8	300 KΩ, 1/4 W, 10%
RX	62 KΩ, 1/4 W, 10% (RX can be eliminated for maximum output)

The following two resistors are used in single supply applications:

R14, R15 5.1KΩ, 1/4 W 10%

Potentiometers:

R9	Trim, 1 MΩ, 1/4 W
R10	Trim, 1 KΩ, 1/4 W
R11	Trim, 25 KΩ, 1/4 W

The following additional items are recommended to convert the circuit of Figure 1 to a complete laboratory instrument:

Potentiometers:

R12	Amplitude control, linear, 50 KΩ
R13	Frequency control, audio taper, 1 MΩ

Switches:

S1	Rotary switch, 1-pole, 4 positions
S2	Toggle or slide, SPST

7" × 4" × 4" (approx.) Metal or Plastic
(See Figure 4(b).)

Power Supply:

Dual supplies ±6 V or single +12 V
Batteries or power supply unit
(See Figures 3(a) and 3(b).)

Miscellaneous:

Knobs, solder, wires, terminals, etc.

BOARD LAYOUT

Care should be given to the layout of the board, to prevent noise from the supplies from affecting the XR-2206 performance.

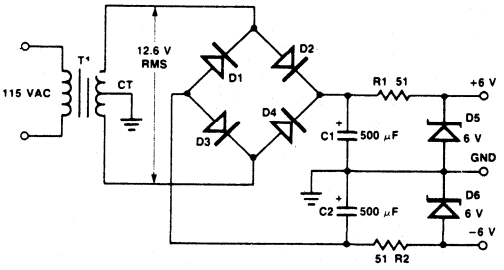
Any simple power supply having reasonable regulation may be used. Figure 2 gives some recommended power supply configurations.

Precaution: Keep the lead lengths small for the range selector switch. This will reduce stray capacitance.

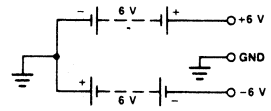
ADJUSTMENT PROCEDURE

When assembly is completed and you are ready to put the function generator into operation, make sure that the polarity of power supply and the orientation of the IC unit are correct. Then apply the dc power to the unit.

To adjust for minimum distortion, connect the scope probe to the triangle/sine output. Close S2 and adjust the amplitude control to give non-clipping maximum swing. Then adjust R10 and R11 alternately for minimum distortion by observing the sinusoidal waveform. If a distortion meter is available, you may use it as a final check on the setting of sine-shaping trimmers. The minimum distortion obtained in this manner is typically less than 1% from 1 Hz to 10 kHz and less than 3% over the entire frequency range.



(a) Zener Regulated Supply



(b) Battery Power Supply

T1: Filament Transformer
Primary 115V/Secondary 12.6 VCT, 0.5A
D1 — D4: IN4001 or Similar
D5, D6: IN4735 or similar
R1, R2: 51Ω, 1/2W, 10%

Figure 2. Recommended Power Supply Configurations.

An Electronic Music Synthesizer using the XR-2207 and the XR-2240

INTRODUCTION

This application note describes a simple, low-cost "music synthesizer" system made up of two monolithic IC's and a minimum number of external components. The electronic music synthesizer is comprised of the XR-2207 programmable tone generator IC which is driven by the pseudo-random binary pulse pattern generated by the XR-2240 monolithic counter/timer circuit.

PRINCIPLES OF OPERATION

All the active components necessary for the electronic music synthesizer system is contained in the two low-cost monolithic IC's, the XR-2207 variable frequency oscillator and the XR-2240 programmable counter/timer. Figure 1 shows the functional block diagram of the XR-2207 oscillator. This monolithic IC is comprised of four functional blocks: a variable-frequency oscillator which generates the basic periodic waveforms; four current switches actuated by binary keying inputs; and buffer amplifiers for both the triangle and squarewave outputs. The internal current switches transfer the oscillator current to any of four external timing resistors to produce four discrete frequencies which are selected according to the binary logic levels at the keying terminals (pins 8 and 9).

The XR-2240 programmable counter/timer is comprised of an internal time-base oscillator, a control flip-flop and a programmable 8-bit binary counter. Its functional block diagram is shown in Figure 2, in terms of the 16-pin IC package. The eight separate output terminals of the XR-2240 are "open-collector" type outputs which can either be used individually, or can be connected in a "wired-or" configuration.

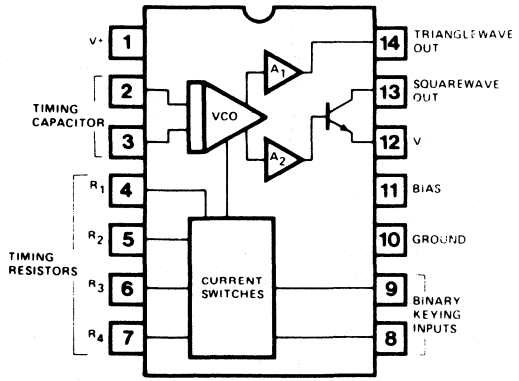


Figure 1. Functional Block Diagram of XR-2207 Oscillator Circuit.

Figure 3 shows the circuit connection for the electronic music or time synthesizer system using the XR-2207 and the XR-2240. The XR-2207 produces a sequence of tones by oscillating at a frequency set by the external capacitor C_1 and the resistors R_1 through R_6 connected to Pins 4 through 7. These resistors set the frequency or the "pitch" of the output tone sequence. The counter/timer IC generates the pseudo-random pulse patterns by selectively counting down the time-base frequency. The counter outputs of XR-2240 (Pins 1 through 8) then activate the timing resistors R_1 through R_6 of the oscillator IC, which converts the binary pulse patterns to tones. The time-base oscillator frequency of the counter/timer sets the "beat" or the tempo of the music. This setting is done through C_3 and R_0 of Figure 3.

The pulse sequence coming out of the counter/timer IC can be programmed by the choice of counter outputs (Pins 1 through 8 of XR-2240 connected to the programming pins (Pins 4 through 7) of the XR-2207 VCO. The connection of Figure 3 is recommended since it gives a particular melodic tone sequence at the output. T1 is an audio transformer with 10KΩ primary and a 4Ω - 16Ω secondary.

The pseudo-random pulse pattern out of the counter-timer repeats itself at 8-bit (or 256 count) intervals of the time-base period. Thus, the output tone sequence continues for about 1 to 2 minutes (depending on the "beat") and then repeats itself. The counter/timer resets to zero when the device is turned on; thus, the music, or the tone sequence, always starts from the same point when the synthesizer is turned on.

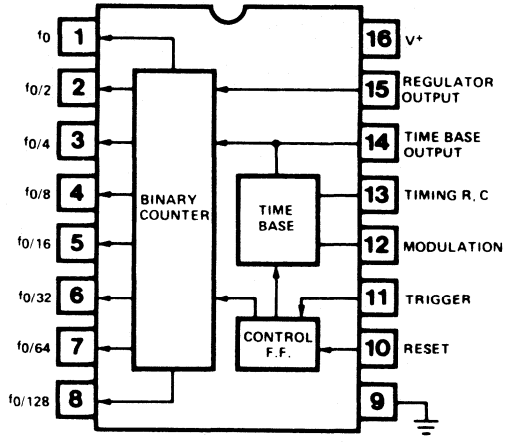


Figure 2. Functional Block Diagram of XR-2240 Counter/Timer.

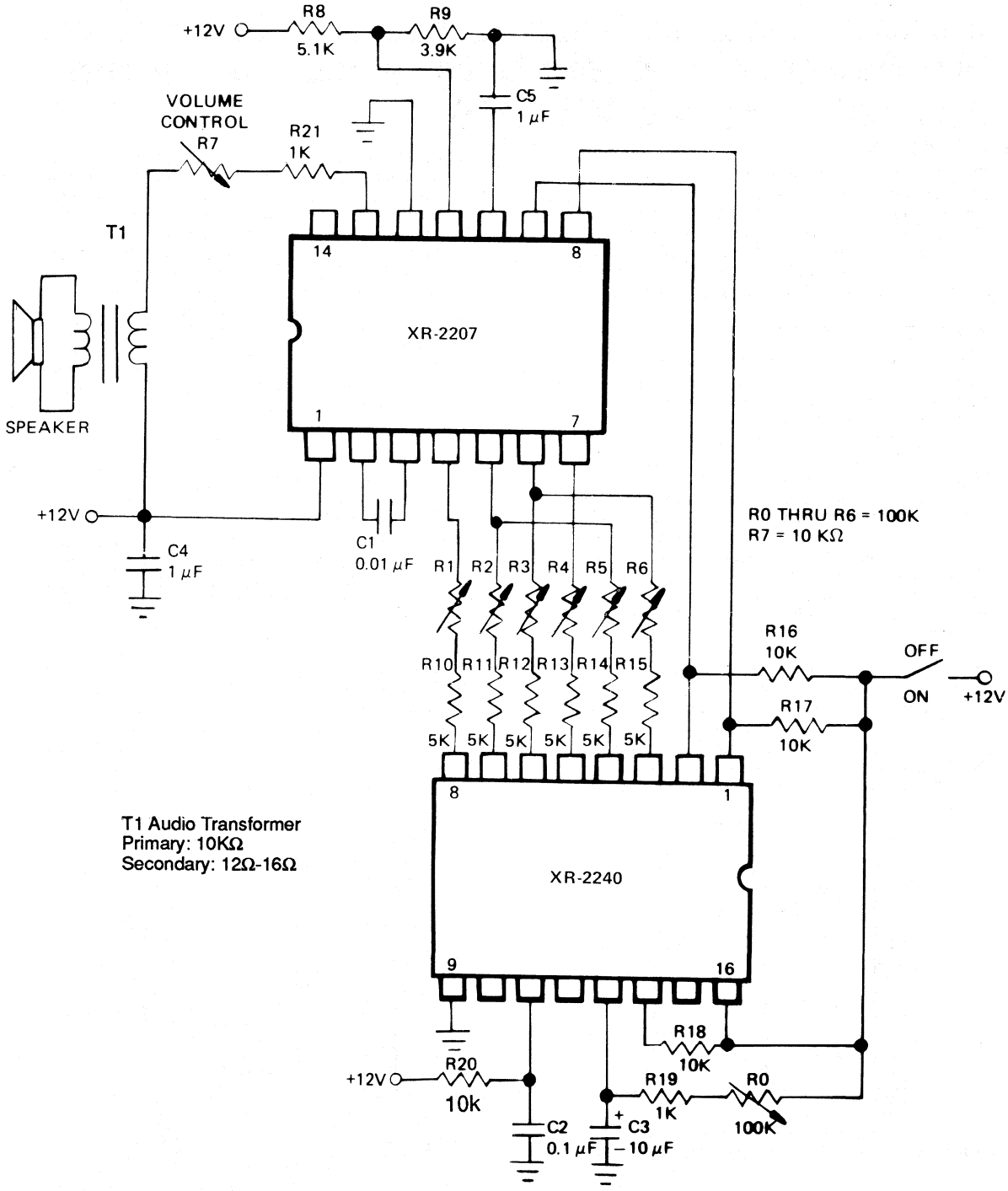


Figure 3. Circuit Connection Diagram for the Music Synthesizer.

Designing Wide-Tracking Phase-Locked Loop Systems

INTRODUCTION

Phase locked-loops with their excellent frequency tracking characteristics have found their way into many applications where synchronizing or synthesizing of signals is required. Although they do have the ability to track an incoming signal very well, the actual tracking range is quite limited by the nature of PLL's to less than 2:1. This range of less than 2:1 must be observed if harmonic locking, a plague to the designer, is to be avoided.

This application note describes the design of tracking PLL with a tracking range of greater than 100:1, with no harmonic locking problems. This design uses the XR-2212 Precision Phase-Locked Loop in conjunction with the XR-320 Monolithic Timer and an XR-084 Quad BiFet Operational Amplifier to form a wide range PLL with automatic tuning.

PRINCIPLES OF OPERATION

Figure 1 shows the block diagram of the tracking PLL. The circuit is comprised of three blocks: the PLL, the Frequency to Voltage Converter, and Precision Clamping Circuit. The blocks operate as follows. The PLL locks onto the incoming frequency and produces an output frequency identical to that of the input, but phase shifted. The center of the lock range is controlled by V_1. V_1 is derived from the F/V converter, which produces a voltage proportional to the incoming frequency. This voltage, V_1, thus provides an automatic PLL center frequency tuning signal. The swing of the phase detectors filtered voltage, V_2, controls the amount the VCO can be moved about its center frequency. The precision clamp fixes the swing on V_2 to a fixed percentage of V_1, keeping the tracking range of the PLL constant as its center frequency is varied.

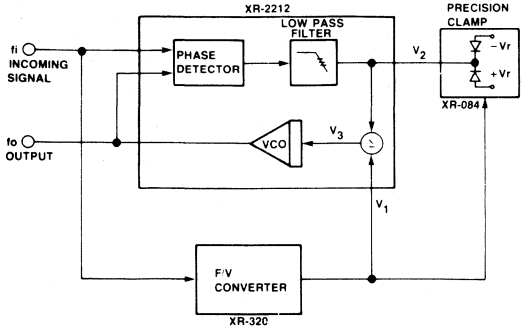


Figure 1. Tracking PLL Block Diagram.

The actual driving voltage for the VCO is now a voltage proportional to fi which can be varied a fixed percentage by the phase detector.

CIRCUIT DESIGN

The heart of the circuit is the XR-2212 Precision Phase-Locked Loop. Figure 2 shows the XR-2212's internal blocks and necessary external components. The VCO in the XR-2212 is actually a current controlled oscillator. Pin 12 is fixed at the reference voltage, $V_r \simeq \frac{V+}{2}$, and the current drawn from this terminal controls the frequency of oscillation of the VCO, f_0. With R_0 grounded, as shown, the VCO's free running or center frequency is:

$$f_0 = \frac{1}{R_0 C_0}$$

R_0 and C_0 are calculated using this relationship at f_0 maximum. With the PLL locked on its center frequency, the phase detector's dc output, Pin 10, is also at V_r and the current flowing in R_0 is proportional to f_0. If the bottom end of R_0 is now raised above ground, the current in R_0 will change linearily with the voltage, as will f_0 thus providing the voltage control input for the VCO. If R_0 is left at zero volts and fi is moved, the dc voltage at Pin 10 will inversely follow fi, increasing fi decreases the voltage at Pin 10, modulating the current from Pin 10 and thus f_0. The maximum swing of Pin 10 is $\simeq \pm V_r$, giving the following relationship:

$$\pm \frac{\Delta f}{f_0} = \frac{\frac{\pm V_r}{R_1}}{\frac{V_r}{R_0}} = \frac{R_0}{R_1} \pm \frac{(V_r R_0)}{V_r R_1} = \pm \frac{R_0}{R_1}$$

Δf being the PLL's tracking range.

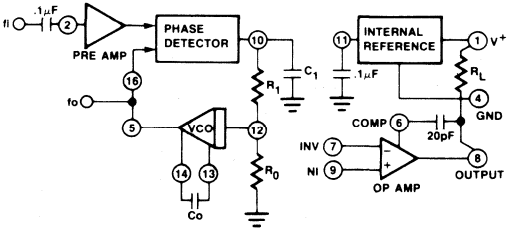


Figure 2. XR-2212 Internal Blocks with External Components.

In our application a constant $\frac{\Delta f}{f_0}$ is desired, so if the output of the phase detector, Pin 10, is clamped to $\sim V_{R0}$, the voltage across R_0, a constant tracking range will be maintained. C_1 serves as the loop, low pass filter, and is made to equal $\frac{C_0}{4}$ for a damping of ½.

The voltage driving R_0 comes from the F/V converter which is formed by the XR-320 Monolithic Timer. The internal blocks and external components of the XR-320 are shown in Figure 3. The input to the F/V is brought to the trigger input, Pin 6, which, when driven above the threshold, triggers the F/F and opens the internal switch transistor, S_1. The voltage on C_T will linearily rise, at a rate set by R_T until V_r is reached at which time the comparator resets the F/F and closes S_1, waiting now for the next rising edge on Pin 6. Once triggered the output, Pin 12, will go low for the timing period defined by the relationship:

$$T_{low} = 2R_TC_T$$

Since Pin 12 will now have a constant low time and a repetition rate equal to that of the incoming signal, fi, it can be filtered to provide a voltage proportional to fi.

Figure 4 shows the complete tracking PLL circuit. The precision clamp is formed by A_1-A_3 which samples the voltage across R_0 and clamps the XR-2212's phase detectors output to $\pm V_{R0}$. With the given values, the tracking range of the circuit is one kHz to 100 kHz, with the XR-2212's tracking range set at approximately ± 0.33 f_0. The input frequency voltage range is 10 mV RMS to 3 V RMS with the output producing a 10 V P-P square wave. Calibration is done by first applying 100 kHz to the input and adjusting P_1 for f_0 equal to fi in frequency but shifted in phase by approximately 90°, then with fi = 1 kHz P_2 is adjusted again for equal frequencies with 90° of phase shift.

WIDE RANGE SYNTHESIZER USING XR-2212 PLL

This same technique of automatic tuning can be used to form a wide range synthesizer as shown in the block diagram of Figure 5. Here a programmable frequency divider has been put into the loop between the VCO output and the phase detector input. Since the PLL will drive the VCO until its two inputs are at the same frequency, the VCO will be at:

$f_{VCO} = Nf_r$ where N in the binary number applied to the programmable divider ($N \geq 1$)

The F/V converter used in the previous application to drive R_0, or tune the PLL, is now replaced with a digital-to-analog converter, DAC. Its digital inputs come from the same lines which control N. The DAC's output voltage, which drives R_0, will now vary proportionally with N, or retuning the PLL with each new N. The same clamping network is used on the phase detectors output as discussed earlier.

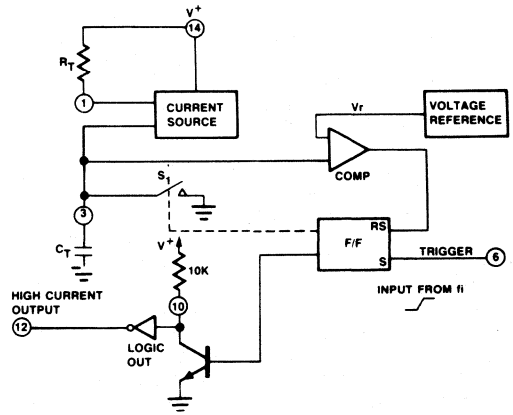


Figure 3. XR-320 Internal Blocks with External Components.

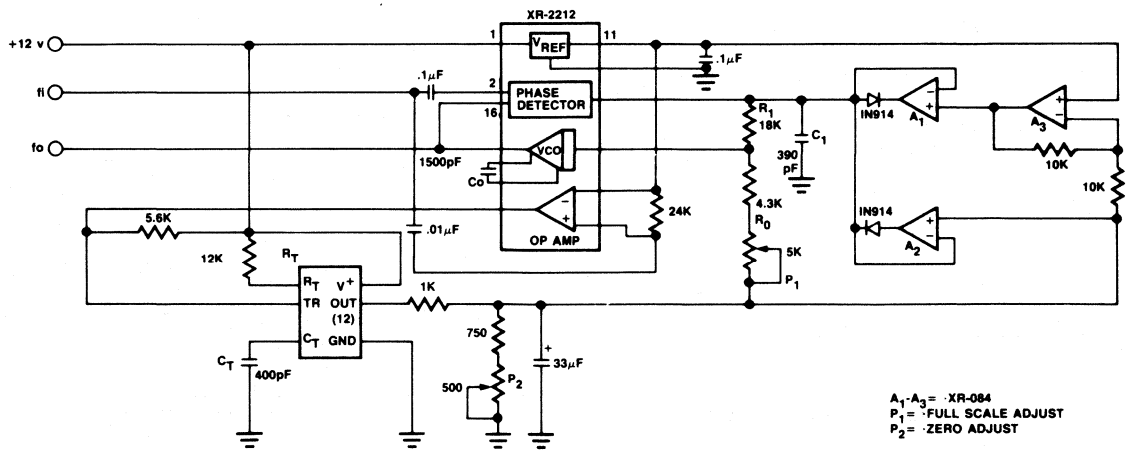


Figure 4. Wide Range Tracking PLL.

Figure 6 shows the complete wide range synthesizer circuit. The two 4-bit binary counters, 74161, and magnitude comparator, 8130, form the programmable divider. The output of the divider is a variable duty cycle pulse so that the flip-flop, 7474, was added so that phase detector was always presented with a square wave. Since the flip-flop also divides by two, the minimum value for the divider will be 2 or the actual N of the overall divider will be the binary input times two, 2N. The DAC uses the reference voltage of the XR-2212 as its reference with amplifier A_4 used to scale the voltage to R_0 correctly. C_1 provides loop compensation and its value will determine not only the response of the circuit but the short term frequency stability of f_0. A trade off must be made here as decreasing C_1 will provide for a faster responding loop but decrease the short term stability of f_0. It is probably most desirable to have a highly stable output frequency and slower responding loop, which the values in Figure 6 provide for.

With the values shown, f_o will be one kHz to 100 kHz with f_{ref} = 500 Hz and N = 1 to 100. The reference input voltage range is 10 mV RMS to 3 V RMS with the output providing a T^2L compatible square wave.

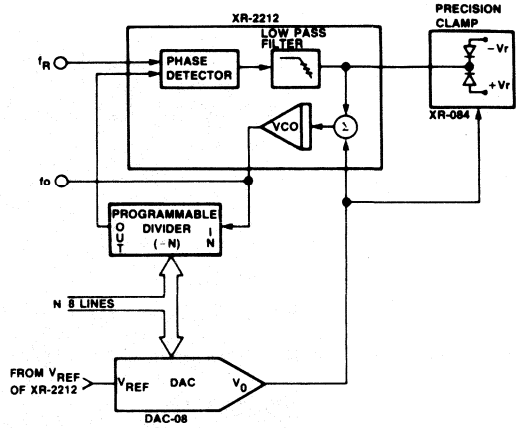


Figure 5. Wide Range Synthesizer Block Diagram.

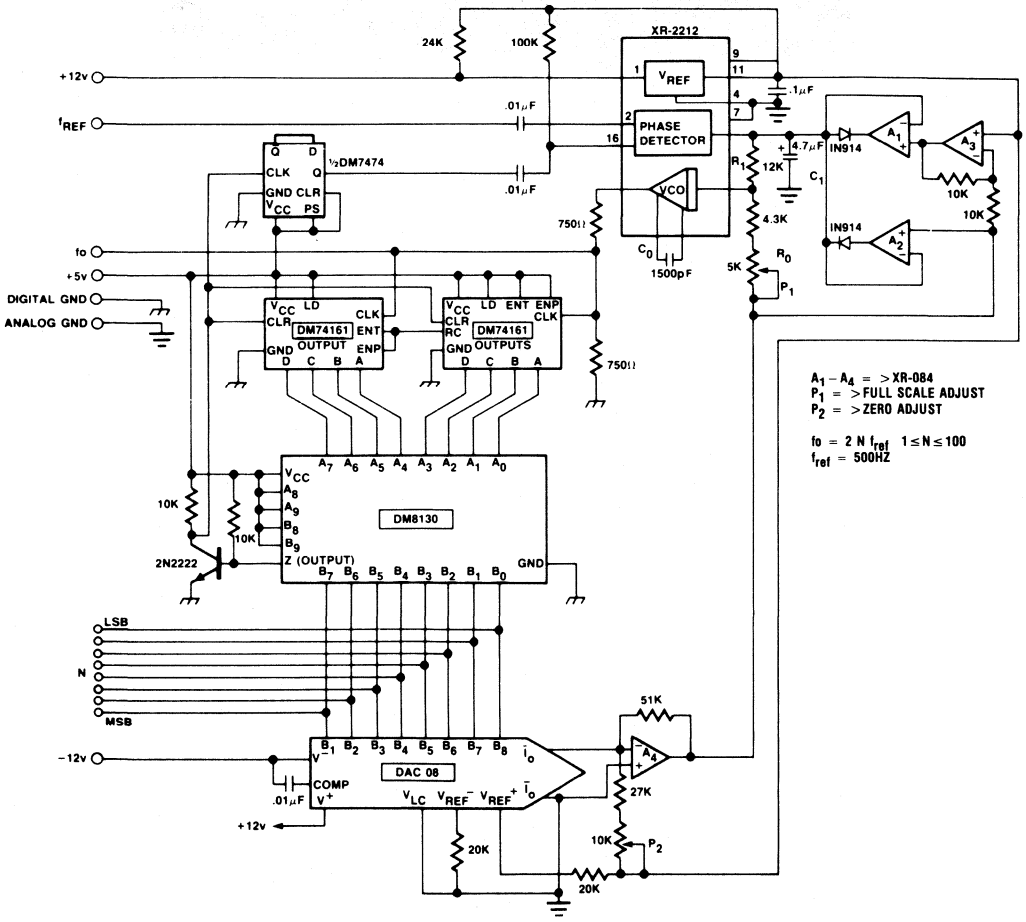


Figure 6. Wide Range Synthesizer.

Calibration is done by first adjusting P_1 for a 100 kHz output with N = 100 and then adjusting P_2 for a one kHz output with N = 1.

Typical input and output waveforms for r_{ref} = 500 Hz, top trace, and f_o, bottom trace, with N switching from 40 to 8 are shown in Figure 7.

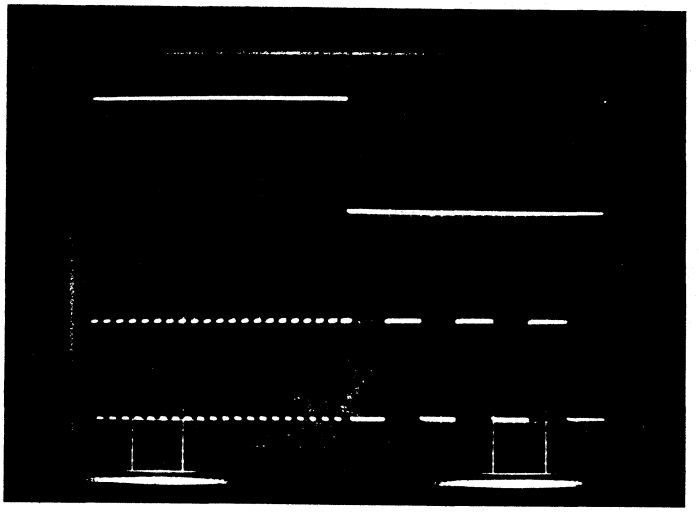


Figure 7. Typical Input and Output Waveform.

Clock Recovery System

INTRODUCTION

Recovering encoded serial data from floppy disk systems poses a major design problem since the synchronized clock used to encode the data is embedded within the data stream. The clock cannot be readily extracted using common phase-locked loop techniques since the clock may appear for only short periods of time in a common encoding format such as NRZI. This clock is necessary to decode the serial data and retrieve the original data.

This application note describes the design of a PLL (phase-locked loop) system which can be used to recover the clock from a serial data stream using NRZI protocol with very excellent stability. The design utilizes the XR-2212 Precision Phase-Locked Loop in conjunction with the XR-320 Monolithic Timer to form the heart of the system. The system also uses a 74123 Dual One-Shot and 398/13333 for timing and sample and hold purposes.

PRINCIPLES OF OPERATION

Figure 1 shows a data stream and clock using a typical NRZI protocol. In this protocol changes in signalling levels represent a binary zeros, while no transitions represent binary one. From the figure it can be seen that the data stream can have a maximum rate of change corresponding to a frequency equal to one half the clock frequency with the actual data being a string of zeros. This format guarantees that there will be no more than five ones in a row. The slowest rate of change will then be a frequency corresponding to one twelfth the clock.

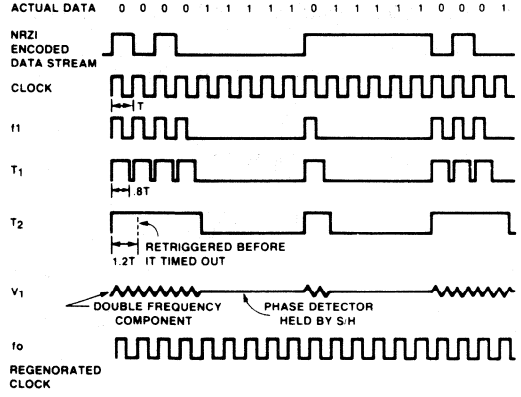


Figure 1. System Timing Diagram.

Figure 2 shows the block diagram of the clock recovery system. The XR-320 forms a bi-directional one-shot. It will produce a positive output pulse for both rising and falling edges on its input. The period of these output pulses is set equal to one half the total period of clock. This is used to provide a frequency component in the data stream equal to the clock even under worst case data conditions of five ones, zero, five ones, zero. (Seen in Figure 1.) This can also be seen to double the frequency of the data stream which is desirable as the PLL will now be able to lock to the original clock. The XR-2212 forms the PLL which, when the actual clock appears in the data stream, locks to and produces a frequency at its VCO output equal to and synchronized with the clock. The PLL's phase detector output is connected to the input of a sample and hold (S/H) as well as the S/H's output through a switch. This switch is held open by the 74123 as long as the clock appears in the data stream. Whenever a one is present the clock will not appear in the data stream and the 74123 places the sample and hold in the hold mode and closes the switch. This holds the voltage at the phase detector and keeps the proper driving voltage to the VCO, thus maintaining the frequency at the output of the VCO equal to and synchronized with the clock.

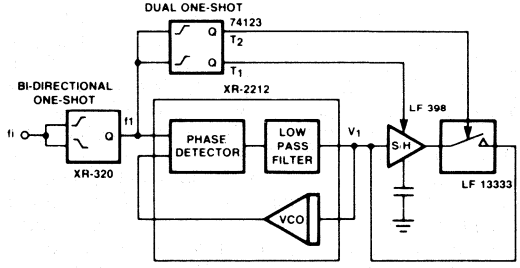


Figure 2. Clock Regenerator Block Diagram.

When the clock reappears in the data stream the 74121 drives the switch open and S/H to the sample mode with the PLL once again tracking the clock in the data stream. The length of T_1 is made equal to slightly less than the period of the clock so that the S/H is always ready in the event the clock is not in the data stream and any sample to hold glitches will not be transmitted to the phase detector's output. The length of T_2 is made slightly longer than the clock period which will cause the switch to close immediately after one clock pulse is missed. With a clock period T, these times, T_1 and T_2, are set equal to 0.8 T and 1.2 T, respectively.

CIRCUIT DESIGN

The heart of the circuit is the XR-2212 Precision Phase-Locked Loop. Figure 3 shows the XR-2212's internal blocks and necessary external components. The phase detector output is a high impedance current source output so it can be forced or held at a particular voltage easily, as by the S/H. The PLL's center frequency is equal to:

$$f_o = \frac{1}{R_0 C_0}$$

R_0 and C_0 are calculated using the data stream's clock **frequency set equal to f_o. The tracking range of the PLL is given by the following relationship:**

$$\Delta f = f_o \frac{R_0}{R_1} \quad \text{where } \Delta f = \text{tracking range}$$

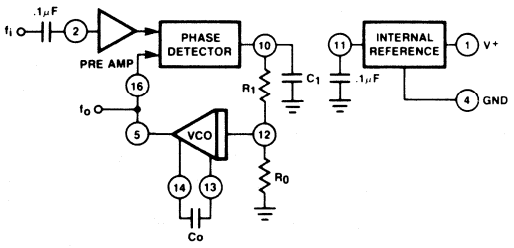


Figure 3. XR-2212 Internal Blocks with External Components.

The phase relationship between the incoming signal, f_i, and the output signal, f_o, will be 90° if f_i is equal to f_o and will vary up 90° or down 90° from this nominal if f_i is at either end of the tracking range. The voltage at the output of the phase detector will also vary linearly with these phase relationships. These relationships are shown in Figure 4. The tracking range is made very large since a constant phase relationship between the recovered clock is desirable. Therefore, any errors in the S/H or drops through the switch will not significantly alter this phase relationship. Δf is made equal to approximately 0.8 f_o, and R_1 is calculated accordingly. C_1 is used to remove the double frequency component from the phase detectors output and also in conjunction with C_0 controls the PLL transient response characteristics, according to the following relationship:

$$\xi = \frac{1}{4}\sqrt{\frac{C_0}{C_1}}$$

for a loop damping of ½, $C_1 = \frac{C_0}{4}$

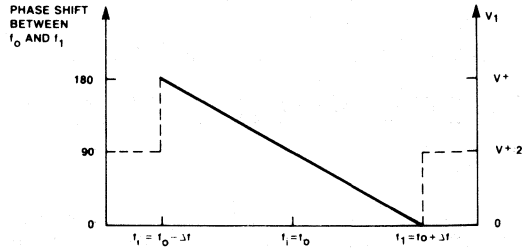


Figure 4. PLL In/Out Phase Relationships.

The XR-320 Monolithic Timer used for the bi-directional one-shot is shown in block form with its external components in Figure 5. The control flip-flop can be triggered by either positive or negative edges on its inputs, which are tied together for this application to provide bi-directional triggering. Once triggered, the output will provide a low level signal for a period defined by:

$$T_{LOW} = 2\, R_T C_T$$

These components are calculated with T_{LOW} set equal to one half the clock period.

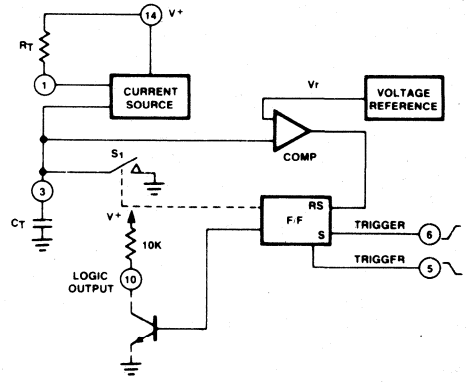
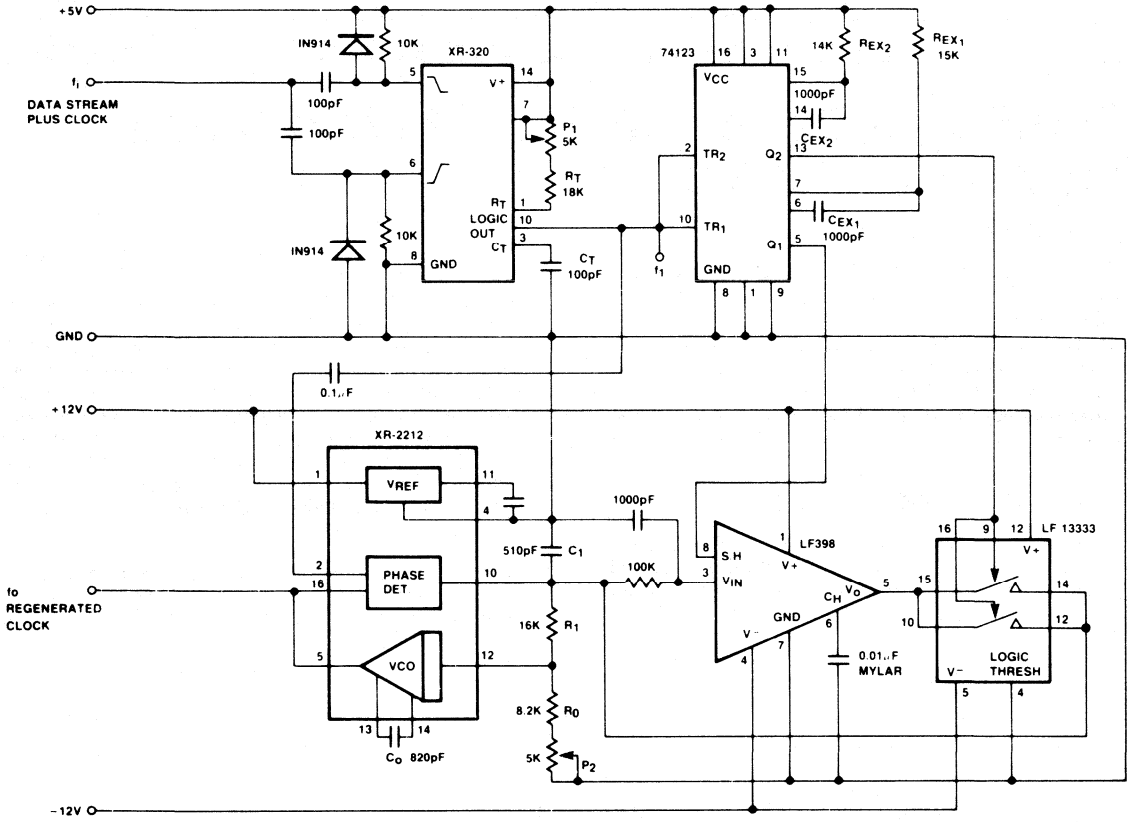


Figure 5. XR-320 Internal Blocks with External Components.

Table 1 summarizes the previously described formulas as well as those for the 74121 Dual One-Shot.

Table 1

FOR XR-2212	FOR XR-320	FOR 74123
(1) $R_0C_0 = \frac{1}{f_{CLK}}$	(4) $R_TC_T = \frac{1}{2\, f_{CLK}}$	(5) $R_{EX_1}C_{EX_1} = \frac{1}{0.8\, f_{CLK} \ln 2}$
(2) $R_1 = 1.2\, R_o$		(6) $R_{EX_2}C_{EX_2} = \frac{1}{1.2\, f_{CLK} \ln 2}$
(3) $C_1 = \frac{C_o}{4}$		



P_1 = > ADJUST SO POSITIVE PORTION OF fi IS EQUAL TO ½ OF THE CLOCK PERIOD
P_2 = > ADJUST FOR 90 PHASE SHIFT BETWEEN f1 and fo WITH $f_i = f_{CLK}$

Figure 6. Complete Clock Regenerator.

Figure 6 shows the complete clock recovery circuit with values designed for a clock of 122 kHZ. The input to the system will accept input low levels from 0 V to 0.5 V levels and high levels from 1.5 V to 5 V. The output provides a 10 V P-P square-wave. Calibration is accomplished by adjusting P_1 for the output of the XR-320 to equal exactly one half of the clock period and P_2 for a 90° phase shift between f_i and f_o with a constant string of zeros applied at f_i.

The oscilloscope photograph in Figure 7 shows the system waveforms with the input data stream on top and f_o on the bottom.

The same circuit can be used to regenerate or clean up a clock with occasional missing cycles by applying it to the point labeled f_i and eliminating the XR-320 from the circuit.

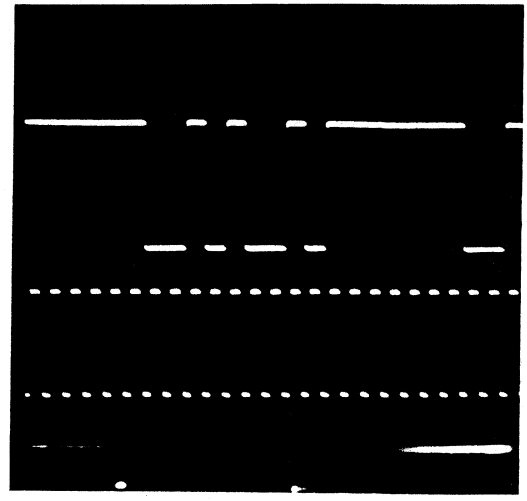


Figure 7. System Waveforms.

Building a Complete FSK Modem Using XR-2211 and XR-2206

INTRODUCTION

The application note describes the construction of a smple modem system using frequency shift keying, FSK, for serial data transmission. The system utilizes the XR-2206 as a modulator, the XR-2211 as a demodulator, and an XR-4136 amp as a bandpass filter. These three IC's make up a complete working 300 baud, full duplex, FSK modem.

GENERAL DESCRIPTION

Figure 1 shows the block diagram of an FSK system. The complete system is comprised of an answer and originate modem. The answer modem will convert input data to either 1070 Hz or 1270 Hz and send it to the phone line, while it will decode to "1's" and "0's" 2025 Hz and 2225 Hz received from the line. The originate modem simply reverses the frequencies for send and receive. The sinewave modulator will produce two discrete frequencies at its output corresponding to a "1" or a "0" at its data input. The line hybrid will steer these frequencies to the phone line while causing received frequencies to go to the bandpass filter and demodulator. This block will therefore provide isolation between modulator and demodulator at each end. The bandpass filter is used to remove unwanted signals and noise received from the phone line before they reach the demodulator.

The PLL demodulator will lock onto incoming frequencies at its input and produce "1's" or "0's" at its output. The carrier detect output will produce a low, "0" signal out when valid data is being received.

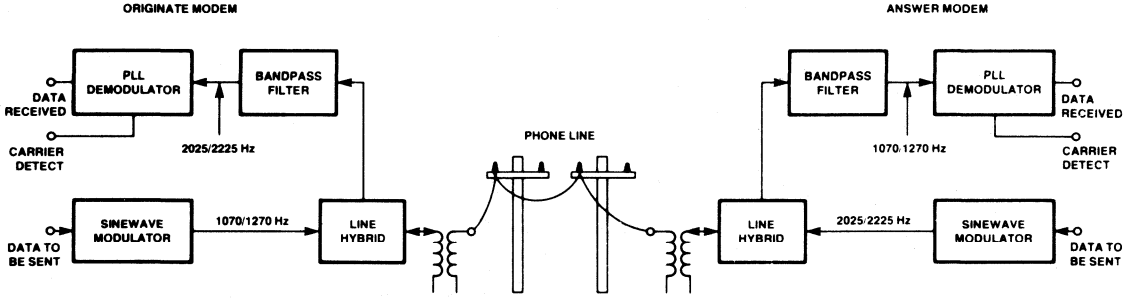


Figure 1. Block Diagram of FSK Modem System.

OPERATION AND CALIBRATION

The circuit has been designed for +12 volt operation. The data inputs accept TTL compatible signal levels, while the outputs provide 0V to +12V signal levels.

Calibration is done by first adjusting the modulator. With a low signal on its input, R_{21} is adjusted for 1270 Hz or 2225 Hz for originate and answer respectively. Then with a high signal in, R_{22} is adjusted for 1070 Hz or 2025.

The demodulator is adjusted by feeding an alternating 1070 Hz/1270 Hz or 2025 Hz/2225 Hz signal to the modem input. The modulating frequency should be 150 Hz, which is one-half the system baud rate of 300.

The answer modem can be used to drive the originate and vice-versa. R_{19} is then adjusted for a square-wave of 50% duty cycle on the data received output.

R_{20} is used to set the modulator output level. With the modulator output set at −6 dBm, the system will operate with an input signal range of +10 dBm to −48 dBm.

CIRCUIT CONSTRUCTION

Figures 2 and 3 show the circuit schematic and component layout. One PC board is used for answer or originate and should use the appropriate components as listed in Table 1.

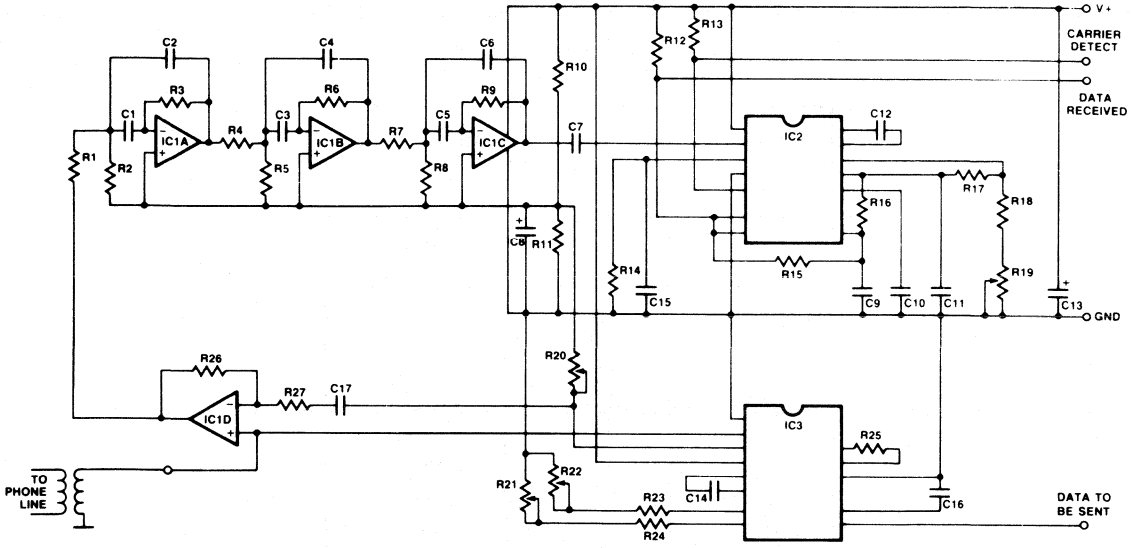


Figure 2. Complete FSK Modem Using XR-2211 and XR-2206.

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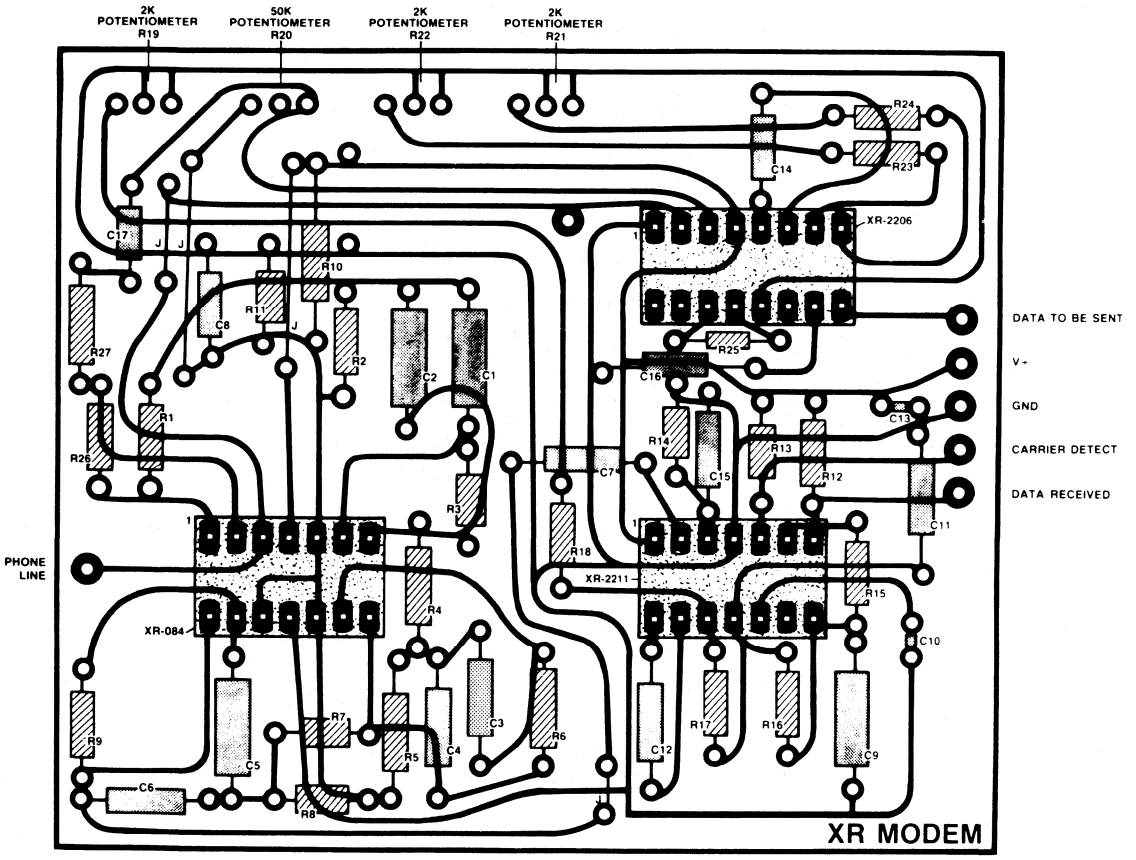


Figure 3. XR Modem Foil Side Shown (Not to Scale).

Table 1. Modem Parts List

IC1A-D	**XR-4136**	
IC2	XR-2211	
IC3	XR-2206	
	ANSWER	**ORIGINATE**
R_1*	40.2K	47.5K
R_2*	499	191
R_3*	270K	357K
R_4*	60.4K	39.4K
R_5*	680	160
R_6*	383K	270K
R_7*	24.9K	20K
R_8*	1.21K	360
R_9*	160K	160K
R_{10}	1K	1K
R_{11}	1K	1K
R_{12}	5.1K	5.1K
R_{13}	5.1K	5.1K
R_{14}	510K	510K
R_{15}	510K	510K
R_{16}	100K	100K
R_{17}	47K	100K
R_{18}	7.5K	9.1K
R_{19}	2K	2K
R_{20}	50K	50K
R_{21}	2K	2K
R_{22}	2K	2K
R_{23}	3.9K	8.2K
R_{24}	3.6K	6.8K
R_{25}	200	200
R_{26}	1M	1M
R_{27}	1M	1M
C_1-C_6*	0.01	0.01
C_7	0.1	0.1
C_8	22	22
C_9	0.01	0.01
C_{10}	0.1	0.1
C_{11}	0.022	0.01
C_{12}	0.1	0.047
C_{13}	1	1
C_{14}	0.1	0.1
C_{15}	0.1	0.1
C_{16}	1	1
C_{17}	1	1

All resistors are 1/4 watt −5% tolerance, except as marked with (*) which are 1% tolerance. Values given in (Ω).

All capacitors are 5% tolerance, except as marked with (*) which are 1% tolerance. Values given in μF.

Precision Narrow-Band Tone Detector

INTRODUCTION

The Phase-Locked Loop (PLL) is a very versatile building block with a wide range of applications in signal processing and communication systems. As a tone detector or tone discriminator, the PLL is accurate and stable enough for most applications not requiring very narrow bandwidths. The smallest, practical detection band is limited by the temperature stability of the PLL center frequency and accuracies of external components. For example, designing a tone detector using a single PLL to discriminate a 10 Hz tone out of 100 kHz can present great difficulty. A PLL with center frequency of 100 kHz can drift by 2 Hz/°C given a typical center frequency drift of 20 ppm/°C. A slight change in ambient temperature can cause the PLL to unlock. On the other hand, there are various applications involving pressure transducers and crystal oscillators that require a very stable system capable of detecting a small change in frequency over a wide frequency spectrum.

This application note describes the use of the XR-2213 PLL in conjunction with the XR-2208 analog multiplier as a frequency mixer. It is capable of detecting a 1 Hz tone out of a frequency spectrum greater than 1 MHz. It can accept almost any periodic waveform including sine, square, and triangular waves. Error due to temperature drift is typically 0.2 %/°C. The tone detector output changes to a high state when the input is within the detection band.

PRINCIPLES OF OPERATION

Figure 1 shows the block diagram of the narrow-band tone detector using the XR-2208 and XR-2213. The XR-2208 is being operated as a balanced modulator or frequency mixer. It "mixes" the input frequency, f_{IN}, with a stable frequency source, f_C, to produce the sum and difference frequencies of f_{IN} and f_C. The low pass filter removes the higher frequency component ($f_{IN} + f_C$) and passes the difference frequency to the XR-2213 PLL. The input signal is "mixed-down" in frequency in this manner, allowing the PLL center frequency, f_o, to be set at a much lower frequency than the input signal. With a lower f_o, the PLL drift (Hz/°C) becomes less, making the tone detector less susceptible to ambient temperature changes.

The input signal to the XR-2208 is a periodic waveform with frequency of:

$$f_{IN} \pm \Delta f_{IN}$$

where Δf_{IN} is the detection range. The range of frequencies for detection is between $f_{IN} - \Delta f_{IN}$ and $f_{IN} + \Delta f_{IN}$. It is necessary to band-limit the input frequency for proper operation of the tone detector. Since the XR-2208 takes the "absolute" difference in frequency between f_{IN} and f_C, it is possible to obtain the same output frequency with different values for f_{IN}, causing the tone detector to lock onto the "wrong" frequencies.

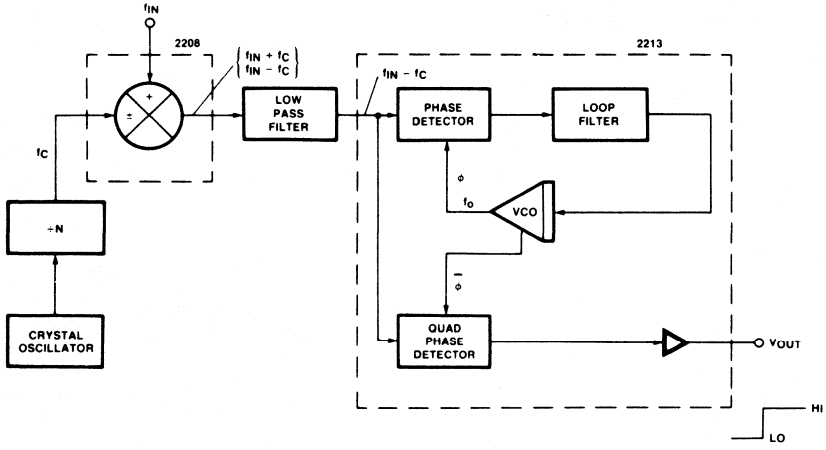


Figure 1. Functional Diagram of Narrow Band Tone Decoder.

In order to band-limit the input frequencies, a low pass filter with very sharp roll-off (6th order or higher) with the corner frequency around f_{IN} can be used. For high frequency applications (f_{IN} > 100 kHz), a bandpass crystal filter can be used. Crystal filters have stable frequency characteristics and very high Q's (Q > 1000) making very sharp bandpass filters. Crystal filters are commercially available through various manufacturers.

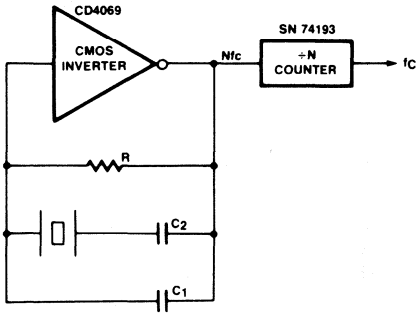
The control frequency, f_C, must come from a very stable and accurate source since any error in f_C will directly affect the tone decoder. A crystal oscillator with a "divide-by-N" counter as shown in Figure 2 can generate a very stable frequency, with temperature stability in the range of 1 ppm/°C.

The control frequency is given by:

$$f_C = f_{IN} + f_o$$

where f_o is the PLL center frequency in Hz. the Choice of f_o is arbitrary, however the larger f_o is, the more the PLL becomes susceptible to temperature variations but the better the acquisition time or "pull-in" time becomes. One the other hand, if f_o is small, then temperature variation has less effect but acquisition time becomes worse. Table 1 shows the relative performances of the tone decoder with respect to the ratio of $\Delta f_{IN}/f_o$.

The output of the low pass filter is fed into the pre-amp of the XR-2213 PLL. When this frequency falls within the detection band or the PLL ($f_o \pm \Delta f_C$), the voltage comparator goes to a high state and remains there until the input frequency falls outside the detection band; the output voltage then goes to a low state. when there is no input signal applied to the XR-2208, the PLL output remains low.



R = 5 MΩ ~ 10 MΩ

C_2 = 20 pF

C_1 = 1 pG ~ 30 pF

C_1 Pulls the crystal down (lower frequency)

C_2 Pulls the crystal up (higher frequency)

Figure 2. Crystal Oscillator.

Table 1. Tone Decoder Performance vs. $\Delta f_{IN}/f_o$

$\pm\Delta f_{IN}/f_o$	TYPICAL PLL f_o STABILITY (Hz/°C)	NORMALIZED RELATIVE ACQUISITION TIME	MAXIMUM f_{IN} ALLOWED (Hz)
0.1 %	0.02 × Δf_{IN}	0.1	$f_{IN} + \Delta f_{IN}(1999)$
0.5 %	0.004 × Δf_{IN}	0.5	$f_{IN} + \Delta f_{IN}(399)$
1.0 %	0.002 × Δf_{IN}	1.0	$f_{IN} + \Delta f_{IN}(199)$
5.0 %	0.0004 × Δf_{IN}	5.0	$f_{IN} + \Delta f_{IN}(39)$
10.0 %	0.0002 × Δf_{IN}	10.0	$f_{IN} + \Delta f_{IN}(19)$
20.0 %	0.0001 × Δf_{IN}	20.0	$f_{IN} + \Delta f_{IN}(9)$

f_{IN}, Δf_{IN} f_o in Hz. f_o = PLL center frequency

$f_{IN} \pm \Delta f_{IN}$ = input frequency range

DESIGN EQUATIONS (All R's in ohms; all C's in farads)

1. The XR-2208 control frequency, f_C, is given by:

$$f_C = f_{IN} + f_o$$

2. The maximum input frequency allowed is:

$$f_{IN}(max) \leq f_{IN} + 2f_o - \Delta f_C$$

Where $\pm\Delta f_C$ is the capture range of the PLL.

3. The capture range, $\pm\Delta f_C$, is set as:

$$\pm\Delta f_C = \pm\Delta f_{IN}$$

Where $\pm\Delta f_{IN}$ is the input frequency variation.

4. The lock range, $\pm\Delta f_L$, is set equal to $\pm\Delta f_C$:

$$\frac{\Delta f_C}{f_o} \quad \frac{R_0}{R_1} \qquad \text{(Hz)}$$

5. The loop damping factor, δ, is set to 0.63:

$$\delta = \frac{1}{4}\sqrt{\frac{C_0}{C_1}}$$

6. The PLL center frequency, f_o, is given by:

$$f_o = \frac{1}{R_0 C_0} \text{ (Hz)}$$

7. Loop detect filter capacitor, C_d, is given by:

$$C_d(\mu F) \geq 16/\Delta f_C \qquad \Delta f_C \text{ in Hz}$$

R_D is set to 470 kΩ.
Increasing C_d slows down the logic output response time.

8. The low pass filter time constants, C_F and R_F:

$$R_F C_F = \frac{1}{f_o} \qquad R_F \leq 20\ k\Omega$$

Where f_o is the PLL center frequency.

DESIGN EXAMPLE

Consider the design of a narrow-band tone detector with frequency detection range of 111.7 kHz ± 10 Hz ($f_{IN} \pm \Delta f_{IN}$).

1. Choose the PLL center frequency to be 100 Hz.

$$f_C = 111.8 \text{ kHz}$$

f_C can be produced by using a 3.58 MHz crystal (adjusted to 3.5776 MHz) and using a divide-by-32 counter in a crystal oscillator.

2. Maximum input frequency allowed is:

$$f_{IN}(max) = 111{,}890 \text{ Hz}$$

3. Capture range, $\pm \Delta f_C$ is:

$$\pm \Delta f_C = \pm 10 \text{ Hz}$$

4. PLL center frequency is 100 Hz (f_o):
Choose $R_o = 10$ KΩ (choice is arbitrarily set between 10 KΩ ≤ R_o ≤ 100 KΩ)

$$C_o = 1/f_o R_o = 1.0\ \mu F$$

5. $\pm \Delta f_C = \pm \Delta f_L = \pm 10$ Hz

$$R_1 = R_o f_o / \Delta f_C = 100 \text{ KΩ}$$

6. The damping factor is set to 0.63:

$$C_1 = C_o \left(\frac{1}{4\delta}\right)^2 = 0.16\ \mu F$$

7. Loop detect filter constants:

Choose $R_D = 75$ KΩ to prevent harmonic locking.

$$C_d = 16/20 \text{ Hz} = 0.8\ \mu F$$

8. Low pass filter time constants, C_F and R_F:

$$R_F = 20 \text{ KΩ}$$

$$C_F = 1/f_o R_o = 0.5\ \mu F$$

A circuit schematic for the above tone detector is shown in Figure 3.

Typical acquisition time for this circuit is less than 100 msec.

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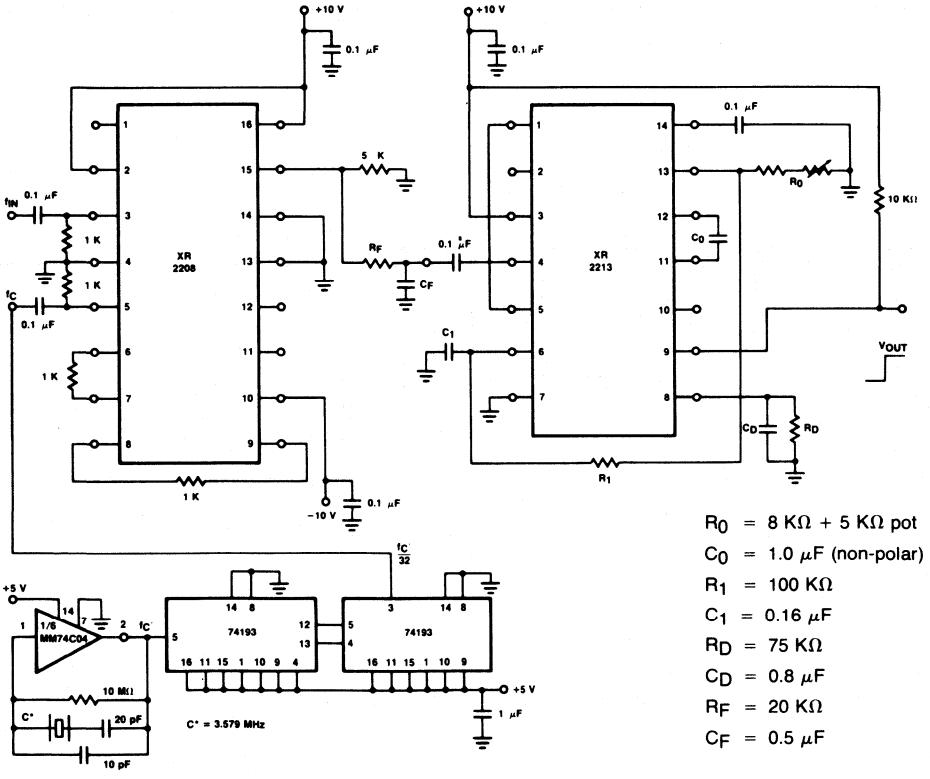


Figure 3. Circuit Schematic of Narrow Band Tone Decoder.

XR-210/XR-215/XR-S200 Phase-Locked Loops

INTRODUCTION

This Application Note discusses the various parameters and equations used in applying the XR-210, XR-215, and XR-S200 Phase Lock Loop (PLL) successfully. It describes the operation of the phase detector and the voltage controlled oscillator as well as a discussion on phase comparator gain, VCO gain, lock range, capture range and free running frequency. A section on low pass filters contains most common RC filters and a discussion on damping factor. Finally, a summary of PLL parameters and a design example are included.

XR-210

The functional diagram of the XR-210 Phase Locked Loop (PLL) is shown in Figure 1. The phase comparator produces a dc voltage which is directly proportional to the phase difference between the two input signals. This error voltage, V_{OUT}, is then filtered and applied to the voltage controlled oscillator (VCO), which in turn produces a periodic signal whose frequency is proportional to the error voltage. The VCO is actually a "current" controlled oscillator (ICO) in the sense that it is the current derived from V_{OUT} that actually controls the frequency of oscillation.

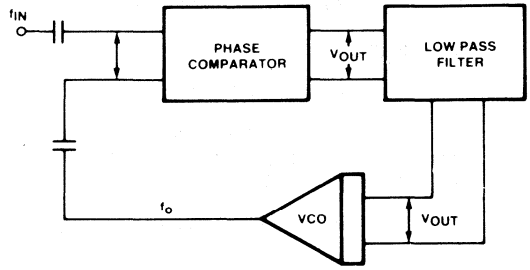


Figure 1. Phase Locked Loop Functional Diagram.

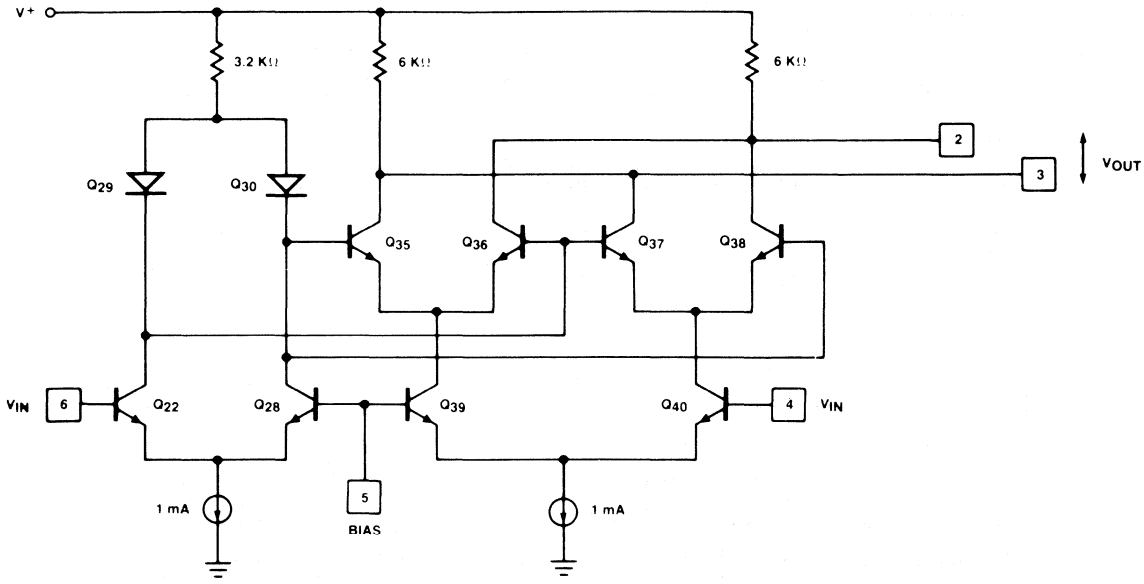


Figure 2. XR-210/XR-215 Phase Comparator.

PHASE COMPARATOR

The circuit diagram of the XR-210 phase comparator is shown in Figure 2. The input pins (4 and 6) and the bias pin (5) are externally biased to approximately ½ V^+ to insure proper operation. The input signals must be capacitively coupled to Pins 4 and 6.

The output voltage on Pins 2 and 3, V_{OUT}, depends on the relative phase, ϕ, of the iput signals. The change of V_{OUT} with respect to the change in ϕ is defined as the phase comparator conversion gain and is given by:

$$K\phi = \frac{\Delta V_{OUT}}{\Delta\phi} \frac{VOLTS}{RADIAN} \quad (1)$$

To examine how V_{OUT} changes with ϕ, consider the following three cases. It is assumed that the input voltage is large enough (> 50 mV_{RMS}) to cause limiting in the differential stage. All calculations are done at $V^+ = 12$ volts.

Case 1: Input voltages are equal to the bias voltage.

The operating current is shared equally between transistors Q_{22}, Q_{28}, Q_{39}, and Q_{40}. This causes approximately 0.5 mA to flow through the output resistor (6 KΩ) and hence $V_{OUT} = 0$ volts. The voltage on Pin 2 and Pin 3 is approximately equal to:

$$V^+ - (0.5\ mA)\ (6K\Omega) = 9\ volts.$$

Case 2: Input voltages are both greater than the bias.

Q_{22} and Q_{40} conduct 1 mA each, causing Q_{38} to conduct 1 mA. Therefore $V_2 \cong 6$ volts, $V_3 \cong 12$ volts and hence $V_{OUT} \cong -6$ volts.

The same output conditions are obtained if the input voltages were both less than the bias.

Case 3. Input voltages are out of phase and V_{IN} (Pin 6) is greater than the bias.

Q_{22} and Q_{39} conduct 1 mA each, causing Q_{35} to conduct 1 mA. Therefore, $V_3 \cong 6$ volts, $V_2 \cong 12$ volts and hence $V_{OUT} \cong +6$ volts.

The same output conditions are obtained if V_{IN} (Pin 4) were greater than the bias.

Figure 3 shows the output voltage wave form when the input signals are 90° and 45° out of phase.

Notice that the duty cycle of the output waveform changes as the phase difference of the input signals change. For illustration purposes, square waves are shown as input signals, however, other periodic waveforms would produce similar output waveforms.

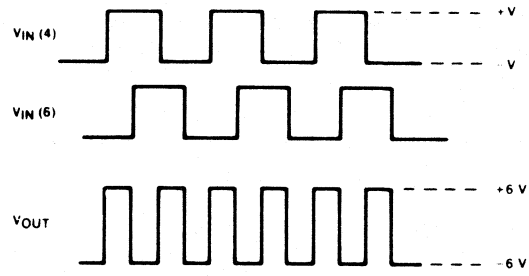


Figure 3a. 90° Out of Phase.

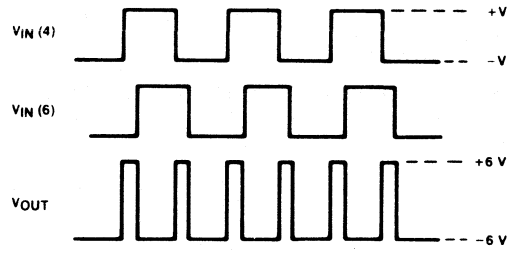


Figure 3b. 45° Out of Phase.

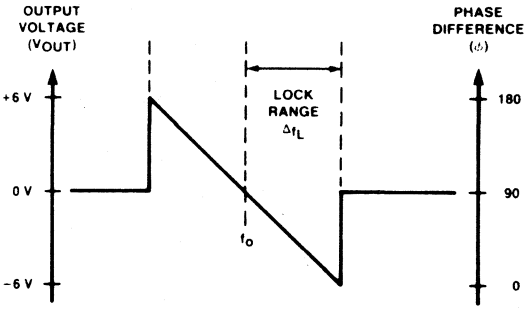


Figure 4a. Phase Detector With No Saturation.

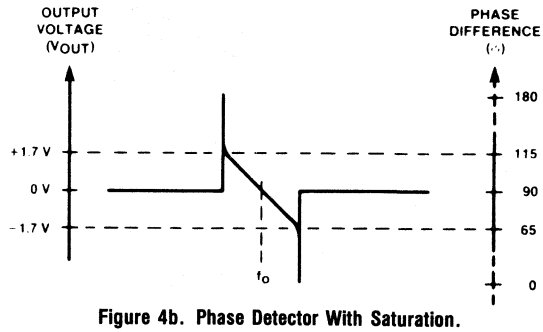


Figure 4b. Phase Detector With Saturation.

The output of the phase detector is connected to a low pass filter which converts the square wave output to an approximate dc voltage. The relationship of this dc voltage, V_{OUT}, with respect to the input phase difference, ϕ, is shown graphically in Figure 4a. Assuming no saturation occurs in the internal circuitry, a PLL can lock onto an input signal with maximum difference of 180° to 0° with respect to the VCO signal.

Due to internal saturation of the output, the maximum phase difference the XR-210 can track is approximately 50° or 90° ±25°. This is because the output transistors of the phase detector saturate at approximately 8.3 volts and the maximum output voltage, V_{OUT}, obtainable is about ±1.7 volts. Figure 4b shows the phase detector characteristic of the XR-210.

It is possible to obtain a tracking range close to 90° ± 90° by connecting an external resistor network to the phase detector output as shown in Figure 5. This circuitry limits the output swing to 10 ± 1 volt and prevents the internal circuitry from saturating at extreme phase conditions.

The phase comparator gain for the XR-210 is approximately given by:

$$K\phi \cong 4.0 \frac{\text{VOLTS}}{\text{RADIAN}} \quad (2)$$

With the external bias network, it is approximately:

$$K\phi \cong \mathbf{0.6} \frac{\text{VOLTS}}{\text{RADIAN}} \quad (3)$$

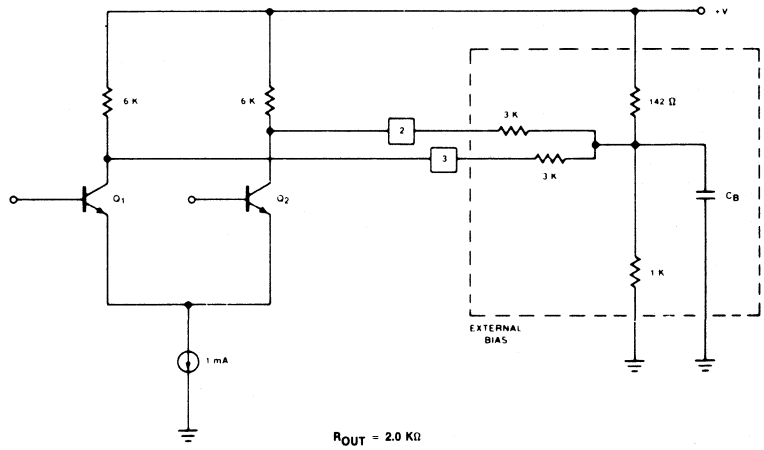


Figure 5. External Resistor Bias Network.

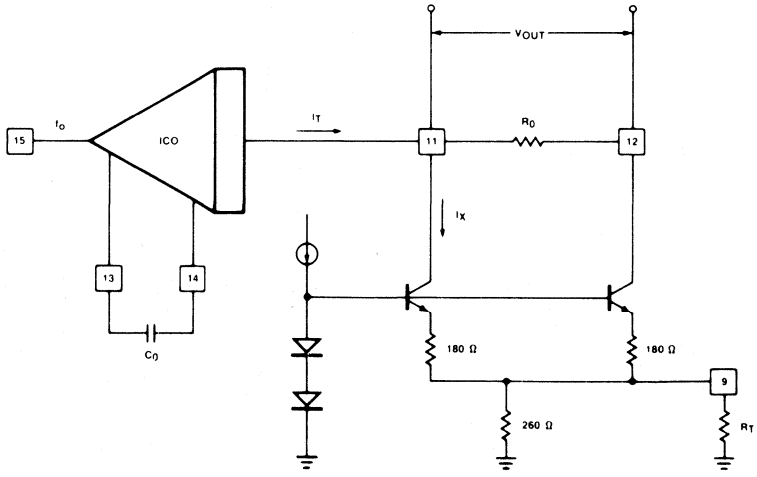


Figure 6. XR-210 Current Controlled Oscillator.

CURRENT CONTROLLED OSCILLATOR (ICO)

The functional diagram of the ICO is shown in Figure 6. The output frequency, f_o, is directly proportional to the total timing current, I_T, seen by the ICO.

$$f_o \propto I_T \tag{4}$$

Any change in output voltage of the phase comparator causes a change in f_o as follows:

$$\Delta f_o \propto \frac{\Delta V_{OUT}}{R_0} \tag{5}$$

where R_0 is the external resistor between Pins 11 and 12. It will be shown in the following section how R_0 sets the lock range of the PLL.

Combining equations 4 and 5 yields:

$$\frac{\Delta F}{\Delta V_{OUT}} = \frac{f_o}{R_O I_T} \tag{6}$$

where I_T is the total timing current with V_{OUT} = 0 volt. In this case, $I_T = I_X \cong 1$ mA. Substituting this into equation 6 yields the ICO conversion gain:

$$K_0 = \frac{\Delta\omega}{\Delta V_{OUT}} \cong \frac{2\pi f_o}{R_0} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \tag{7}$$

where R_0 is in KΩ.

The minimum value of R_0 should be approximately 1.7 KΩ. This is because the maximum current through R_0 must be limited to 1 mA and since V_{OUT} has a maximum range of approximately ±1.7 volts, R_0 must be limited to greater than 1.7 KΩ.

The free running frequency of the PLL is given by:

$$f_o \cong \frac{200}{C_0} \quad C_0 \text{ is in } \mu F. \tag{8}$$

Substituting this into ICO gain equation 7 yields:

$$K_0 \cong \frac{1256}{R_0 C_0} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \tag{9}$$

where R_0 is in KΩ and C_0 is in μF.

Experimental data yields:

$$K_0 \cong \frac{910}{R_0 C_0} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \tag{10}$$

The above equations were calculated without the ICO tuning resistor, R_T, connected to Pin 9. Adding R_T increases the timing current and hence increases the free running frequency. f_o:

The change in timing current with R_T is given by:

$$\Delta I_T \cong \frac{0.17}{R_T} \text{ mA} \tag{11}$$

The free running frequency can now be given by:

$$f_o \cong \frac{200}{C_0}\left(1 + \frac{0.17}{R_T} \text{ Hz}\right) \tag{12}$$

where R_T is in KΩ and C_0 is in μF.

The ICO gain is now:

$$K_0 = \frac{\Delta\omega}{\Delta V_{OUT}} = \frac{2\pi f_o}{R_0 I_T} \cong \frac{2\pi\left(\frac{200}{C_0} 1 + \frac{0.17}{R_T}\right)}{R_0 I_T} \tag{13}$$

However, the timing current is now:

$$I_T \cong \left(I_X + \frac{0.17}{R_T}\right) \text{mA} = \left(1 + \frac{0.17}{R_T}\right) \text{mA} \tag{14}$$

Substituting this into the ICO equation yields:

$$K_0 \cong \frac{200(2\pi)}{C_0 R_0} = \frac{1256}{R_0 C_0} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \tag{15}$$

and remains unchanged with the addition of R_T.

Note: The discrepancy between the calculated and measured K_0 can be attributed to tolerances of internal resistors and errors in approximating I_X.

LOCK RANGE

The lock range of a PLL, $\pm\Delta\omega_L$, is given by:

$$\pm\Delta\omega_L = (K\phi)(K_0)(\theta_E) \frac{\text{RADIANS}}{\text{SEC}} \tag{16}$$

where θ_E is the maximum phase difference at the detector inputs in radians. θ_E is approximately equal to 0.43 radians (25°).

Using measured values for $K\phi$ and K_0 yields:

$$\pm\Delta\omega_L \cong \frac{1565}{R_0 C_0} \frac{\text{RADIANS}}{\text{SEC}} \tag{17}$$

where R_0 is in KΩ and C_0 is in μF.

XR-215

The XR-215 PLL is basically the same as the XR-210. The major difference is in the ICO section which is described below.

PHASE COMPARATOR

The phase comparator conversion gain is given by:

$$K\phi \cong 3.6 \frac{\text{VOLTS}}{\text{RADIAN}} \quad (18)$$

Saturation of the internal circuitry occurs limiting the tracking range of the phase detector to about 90° ± 25°.

An external resistor network shown in Figure 5 can increase the range to about 90° ± 90°. The corresponding conversion gain becomes:

$$K\phi \cong 1.3 \frac{\text{VOLTS}}{\text{RADIAN}} \quad (19)$$

ICO

The current controlled oscillator of the XR-215 is shown in Figure 7. The ICO conversion gain is given by:

$$K_0 = \frac{2\pi f_o}{R_0 I_X} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \quad (20)$$

Since $I_X = 1.1$ mA and $f_o = \frac{220}{C_0}$,

$$K_0 \cong \frac{1256}{R_0 C_0} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \quad (21)$$

where R_0 is in KΩ and C_0 is in μF.

Experimental data yields:

$$K_0 \cong \frac{1140}{R_0 C_0} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \quad (22)$$

With the ICO tuning resistor, R_X, connected to Pin 10, the free running frequency is increased by a factor proportional to the change in timing current:

$$\Delta f \propto \Delta I_T \cong \frac{0.7}{R_X} \quad (23)$$

The ICO free running frequency is given by:

$$f_o \cong \frac{220}{C_0}\left(1 + \frac{0.7}{R_X}\right) \quad (24)$$

where R_X is in KΩ and C_0 is in μF.

$$K_0 \cong \frac{1140}{R_0 C_0} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \quad (25)$$

and remains unchanged with the addition of R_X.

LOCK RANGE

The lock range of the XR-215, $\pm\Delta\omega_L$, is given by:

$$\pm\Delta\omega_L = (K\phi)(K_0)(\theta_E) \quad (26)$$

where θ_E is approximately equal to 0.43 radians (25°). Using measured values for $K\phi$ and K_0 yields:

$$\pm\Delta\omega_L \cong \frac{1765}{R_0 C_0} \frac{\text{RADIANS}}{\text{SEC}} \quad (27)$$

where R_0 is in KΩ and C_0 is in μF.

Note: Using the external bias network (Figure 5) does not change K_0. To calculate the lock range with this network, θ_E should be set to approximately π/2 radians (90°).

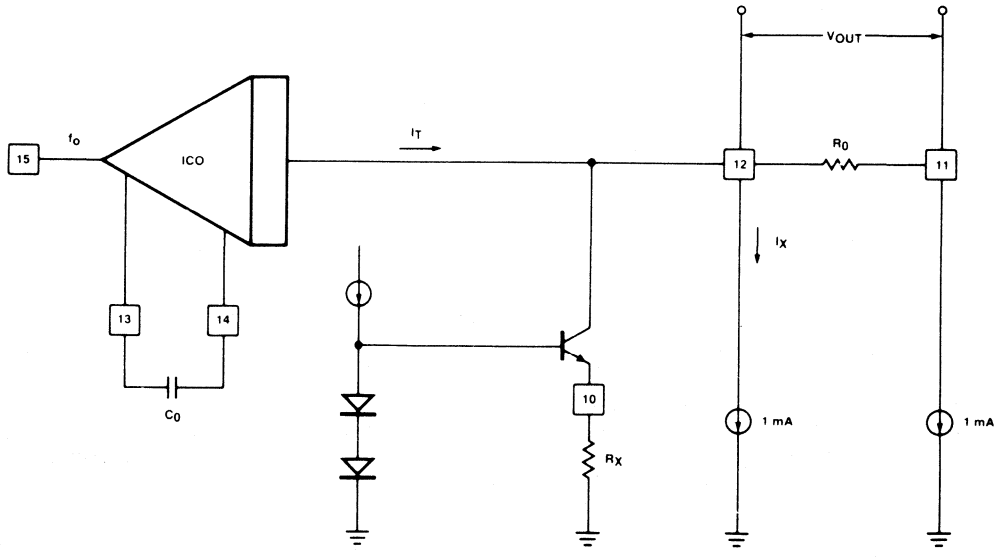


Figure 7. XR-215 ICO.

XR-S200

The XR-S200 PLL is basically the same as the XR-210 and 215 except that many of the interconnections are made external to the chip. These external connections can aid in the flexibility of the chip.

PHASE COMPARATOR

The phase comparator outputs are not tied internally to the ICO as the XR-210 and 215. The measured phase comparator gain is approximately:

$$K\phi \cong 4\,\frac{\text{VOLTS}}{\text{RADIAN}} \qquad (28)$$

Saturation of the internal circuitry occurs limiting the tracking range to about 90° ± 25°. This range can be increased by using the bias network shown in Figure 5.

ICO

The current controlled oscillator of the XR-S200 is shown in Figure 8. The ICO gain is given by:

$$K_0 = \frac{2\pi\, f_o}{R_0\, I_T}\,\frac{\text{RADIANS/SEC}}{\text{VOLT}} \qquad (29)$$

where I_T is the timing current when V_{OUT} = 0 volts.

The ICO free running frequency, f_o, can be modified by applying a digital pulse on Pins 15 and 16 through a diode and a 1 KΩ resistor. By changing the voltage states on these Pins, it is possible to obtain four discrete frequencies for f_o. By connecting a resistor from either Pin 15 or 16 to ground, it is also possible to modify the center frequency.

With Pins 15 and 16 open, f_o is given by:

$$f_o \cong \frac{200}{C_0}(I_X + I_1 + I_2) = \frac{500}{C_0}\ \text{Hz} \qquad (30)$$

since $I_X \cong 1$ mA, $I_1 \cong 0.5$ mA, $I_2 \cong 1$ mA.

With Pins 15 and 16 tied high, f_o is given by:

$$f_o \cong \frac{200}{C_0}(I_X) = \frac{200}{C_0}\ \text{Hz} \qquad (31)$$

where C_0 is in μF.

With Pins 15 and 16 open:

$$K_0 = \frac{2\pi\, f_o}{R_0\, I_T} \cong \frac{3142}{R_0\, C_0\, I_T} \qquad (32)$$

where $I_T = I_X + I_1 + I_2 \cong 2.5$ mA, thus

$$K_0 \cong \frac{1256}{R_0\, C_0}\,\frac{\text{RADIANS/SEC}}{\text{VOLT}} \qquad (33)$$

where R_0 is in KΩ and C_0 is in μF.

With Pins 15 and 16 tied high:

$$K_0 \cong \frac{1256}{R_0\, C_0\, I_T} \qquad (34)$$

where $I_T = I_X \cong 1$ mA. Thus

$$K_0 \cong \frac{1256}{R_0\, C_0}\,\frac{\text{RADIANS/SEC}}{\text{VOLT}} \qquad (35)$$

and remains unchanged.

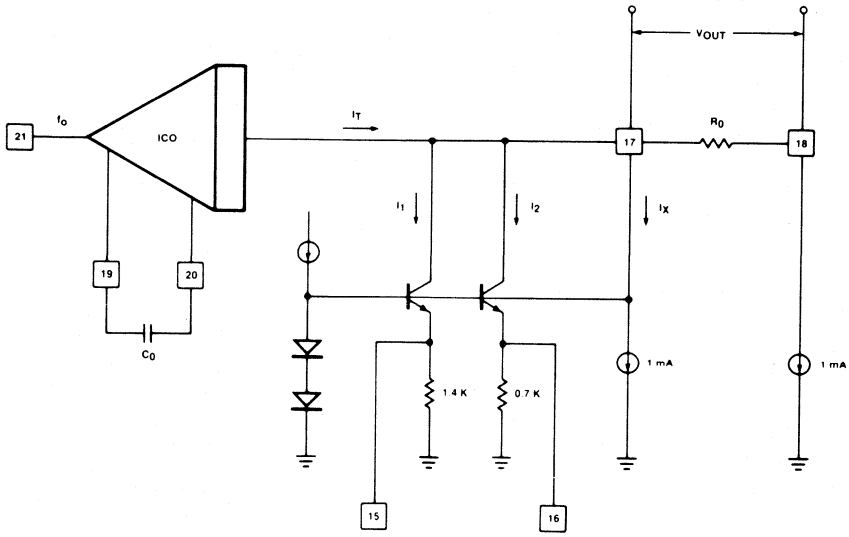


Figure 8. XR-S200 ICO.

LAG FILTER

$$F(S) = \frac{1}{1 + \tau_1 S}$$

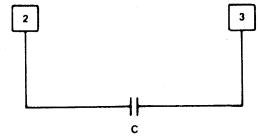
$\tau_1 = R_1 C \quad \tau_2 = R_1 C_2$

$$\omega_\eta = \sqrt{\frac{K_V}{\tau_1}}$$

$$\delta = \frac{1}{2\sqrt{K_V \tau_1}}$$

$KV = KOK\Phi$

LAG FILTER



$$F(S) = \frac{1}{1 + 2\tau_1 S}$$

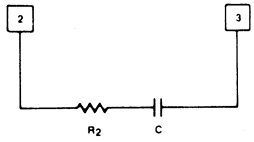
$\tau_1 = R_1 C$

$$\omega_\eta = \sqrt{\frac{K_V}{2\tau_1}}$$

$$\delta = \frac{1}{2\sqrt{2 K_V \tau_1}}$$

$KV = KOK\Phi$

LAG-LEAD FILTER



$$F(S) = \frac{1 + \tau_2 S}{1 + S(2\tau_1 + \tau_2)}$$

$\tau_1 = R_1 C; \tau_2 = R_2 C$

$$\omega_\eta = \sqrt{\frac{K_V}{(2\tau_1 + \tau_2)}}$$

$$\delta = \frac{1}{2}\sqrt{\frac{K_V}{2\tau_1 + \tau_2}}\left(\tau_2 + \frac{1}{K_V}\right)$$

FOR $\tau_1 \cdots \tau_2$

$$\delta = \frac{1}{2\sqrt{2K_V \tau_1}} \quad (1 + \tau_2 K_V)$$

$KV = KOK\Phi$

LAG-LEAD FILTER

$$F(S) = \frac{1 + \tau_2 S}{1 + S(\tau_1 + \tau_2)}$$

$\tau_1 = R_1 C; \tau_2 = R_2 C$

$$\omega_\eta = \sqrt{\frac{K_V}{\tau_1 + \tau_2}}$$

$$\delta = \frac{1}{2}\sqrt{\frac{K_V}{\tau_1 + \tau_2}}\left(\tau_2 + \frac{1}{K_V}\right)$$

FOR $\tau_1 \gg \tau_2$

$$\delta = \frac{1}{2\sqrt{K_V \tau_1}} \quad (1 + \tau_2 K_V)$$

$KV = KOK\Phi$

Figure 9. Low Pass Filters.

Measured value for K_0 is approximately:

$$K_0 \cong \frac{1262}{R_0 C_0} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \qquad (36)$$

LOCK RANGE

Using measured values for $K\phi$ and K_0 yields:

$$\pm\Delta\omega_L \cong \frac{2170}{R_0 C_0} \frac{\text{RADIANS}}{\text{SEC}} \qquad (37)$$

where R_0 is in KΩ, and C_0 is in μF.

LOW PASS FILTER

The low pass filter section for the XR-210/215/S200 is formed by connecting an external capacitor or RC network across the output of phase comparator section. Most common passive low pass filters are shown in Figure 9. R_1 is the internal resistor with nominal value of 6 KΩ. If an external bias network as shown in Figure 5 is used, R_1 = 2 KΩ. Pin numbers shown in Figure 9 apply to the XR-210 and XR-215.

The term K_V shown in the filters is the total forward gain of the PLL and is equal to the product of $K\phi$ and K_0.

CAPTURE RANGE

The capture or acquisition range of the PLL, $\pm\Delta\omega_C$, can be approximated as:

$$\pm\Delta\omega_C \cong \pm\Delta\omega_L |F(j\,\Delta\omega_C)| \qquad (38)$$

where $|F(j\,\Delta\omega_C)|$ is the magnitude of the low pass filter evaluated at $\omega = \Delta\omega_C$. Since $|F(j\,\Delta\omega_C)|$ is always less than unity, the capture range is always smaller than the lock range.

There is no explicit relationship for calculating $\Delta\omega_C$, however for a *simple lag* filter, it can be expressed as:

$$\pm\Delta\omega_C \cong \sqrt{\frac{K_V}{\tau_1}} \frac{\text{RADIANS}}{\text{SEC}} \qquad (39)$$

For lag-lead filters, capture range can be roughly estimated by ω_η. (See Figure 9.) Actual data indicates that capture range is larger than ω_η and approaches the lock range.

DAMPING FACTOR

The advantage of using a lag-lead filter is that generally speaking, it gives better stability due to the extra zero. The damping factor can be adjusted without necessarily changing the capture range. With a simple lag filter, however, by adjusting τ, the damping factor as well as the capture range is changed. These two parameters can be individually controlled in a lag-lead filter.

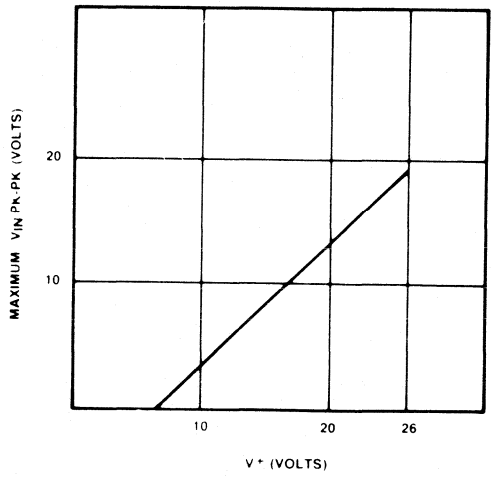


Figure 10. Maximum Input Voltage vs. Supply Voltage.

General systems and control theory indicates that for maximum stability the damping factor, δ, must be greater than 0.7. In many FSK demodulation circuits using Exar PLLs, it was found that with δ as low as 0.2, the circuit functions properly at high baud rates.

DESIGN EXAMPLE

Design an FSK demodulator using the XR-210 with the following specifications:

Mark frequency: 1070 Hz
Space frequency: 1270 Hz
V_{CC}: +12 volts

1. f_0 = 1170 Hz

   $$C_0 = \frac{200}{f_0} \cong 0.2\ \mu F$$

   Adjust R_T (Pin 9 to GND) for correct f_0.

2. $\Delta\omega_L = 2\pi(\Delta f_L) = 2\pi(200\text{ Hz}) = 1256$ RAD/SEC

   $$R_0 = \frac{1565}{\Delta\omega_L C_0} = 6.23\ K\Omega$$

3. Set capture range, $\Delta\omega_C$, equal to $\Delta\omega_L$. Using a lag-lead filter, $\Delta\omega_C$ can be approximated by:

$$\Delta\omega_C \cong \omega_\eta = \sqrt{\frac{K_V}{2\tau_1 + \tau_2}}$$

$$K_V = K_0 K\phi \cong 2921$$

Let $R_2 = 50\ \Omega$. Thus $\tau_1 \gg \tau_2$

$$C_1 = 0.15\ \mu F$$

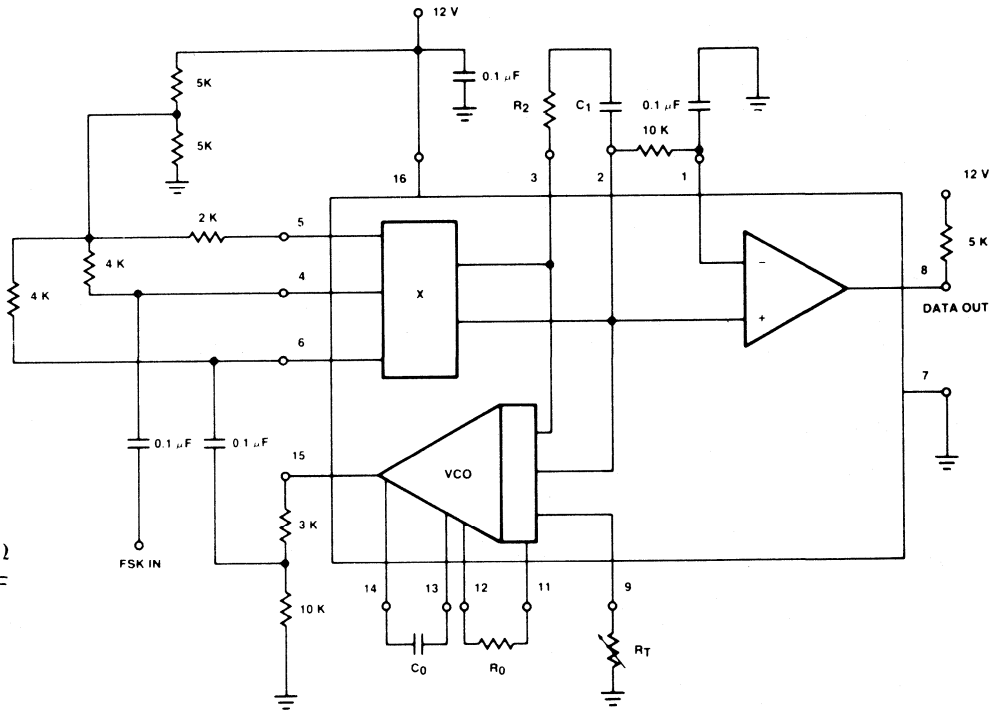
4. The damping factor is given by:

$$\delta = \frac{1}{2}\frac{1}{\sqrt{2\,K_V\,\tau_1}}\,(1 + \tau_2 K_V) \cong 0.22$$

Even with critical damping ($\delta < 1.0$), the XR-210 functions properly as an FSK demodulator with baud rate of 300 BPS.

5. For V+ of 12 volts, the input voltage should be limited to 5 volts PK-PK to avoid internal saturation (see Figure 10).

6. Schematic for the above example is shown in Figure 11.



$C_0 = 0.2\ \mu F$
$R_0 = 6.23\ K\Omega$
$C_1 = 0.15\ \mu F$
$R_2 = 50\ \Omega$
$R_T = 10\ K\Omega$

Figure 11. XR-210 FSK Demodulation.

Table 1. Summary of PLL Parameters (1) measured on a small sample of parts.

PARAMETER	XR-210	XR-215	XR-S200
Phase Comparator $K\phi$	$4.0\ \frac{\text{VOLTS}}{\text{RADIAN}}$	$3.6\ \frac{\text{VOLTS}}{\text{RADIAN}}$	$4.0\ \frac{\text{VOLTS}}{\text{RADIAN}}$
VCO K_0	$\frac{910}{R_0 C_0}\ \frac{\text{RAD/SEC}}{\text{VOLT}}$	$\frac{1140}{R_0 C_0}\ \frac{\text{RAD/SEC}}{\text{VOLT}}$	$\frac{1262}{R_0 C_0}\ \frac{\text{RAD/SEC}}{\text{VOLT}}$
Lock Range $\pm\Delta\omega_L$	$\frac{1565}{R_0 C_0}\ \frac{\text{RADIANS}}{\text{SEC}}$	$\frac{1765}{R_0 C_0}\ \frac{\text{RADIANS}}{\text{SEC}}$	$\frac{2170}{R_0 C_0}\ \frac{\text{RADIANS}}{\text{SEC}}$
Free Running Frequency f_o	$\frac{200}{C_0}\left(1 + \frac{0.17}{R_T}\right)$ Hz	$\frac{200}{C_0}\left(1 + \frac{0.7}{R_T}\right)$ Hz	$\frac{500}{C_0}$ Hz (2)
Capture Range $\pm\Delta\omega_C$ (Simple Lag) (3)	$\sqrt{\frac{K_0 K\phi}{\tau_1}}$	$\sqrt{\frac{K_0 K\phi}{\tau_1}}$	$\sqrt{\frac{K_0 K\phi}{\tau_1}}$
Damping Factor δ (Simple Lag)	$\frac{1}{2}\sqrt{\frac{1}{K_0 K\phi\ \tau_1}}$	$\frac{1}{2}\sqrt{\frac{1}{K_0 K\phi\ \tau_1}}$	$\frac{1}{2}\sqrt{\frac{1}{K_0 K\phi\ \tau_1}}$

(1) R_0, R_T, R_X in KΩ
C_0 in μF

(2) f_o shown for Pins 15 and 16 open

(3) For other filter configurations, refer to the filter section. $\tau_1 = R_1 C_1$.

5

High-Performance Frequency-To-Voltage Converter using the XR-2211

INTRODUCTION

A stable highly linear f/v converter can be easily designed using the XR-2211 phase locked loop. The f/v can be used for a dynamic range from ±1% to ±80% over a frequency range of .01 Hz to 1 MHz.

The block diagram of the f/v is shown in Figure 1. The circuit will perform f/v conversion according to the relationship

$$f_{IN} = -K_1 V_O + K_2$$

where K_1 and K_2 are set by the designer.

The transfer function relating V_O to f_{IN} is shown in Figure 2. The carrier detect output, Q, (Pin 6) which goes high over the tracking range is shown in Figure 3.

The basic circuit diagram is shown in Figure 4. The slope K_1 is determined by the relationship

$$K_1 = \frac{-1}{V_R C_0 R_1}$$

where $V_R = V_{CC}/2 - 650mV$
V_{BE} = 650 mV 1.3 V typically under absolute maximum conditions.
The x intercept or upper frequency, K_2 is determined by the relationship

$$K_2 = \frac{R_0 + R_1}{R_0 R_1 C_0} = f_{MAX}$$

DESIGN EXAMPLE

Design a f/v converter for the frequency range 100 Hz to 600 Hz.

The first step is to calculate the center frequency f_o, (Figure 2) in

$$f_o = \frac{f_L + f_H}{2} = \frac{100 + 600}{2} = 350 \text{ Hz}$$

Supply voltage is directly proportional to the degree of resolution obtainable.

In order to obtain a greater resolution a higher supply voltage is used. For this design an 18 V supply is used giving us a resolution of approximately

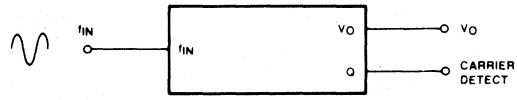


Figure 1. F/V Block Diagram.

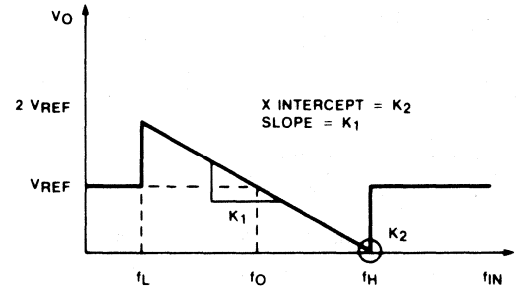


Figure 2. F/V Transfer Function.

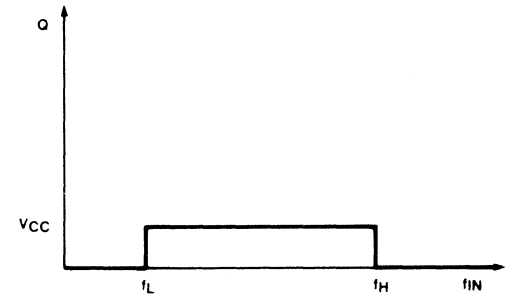


Figure 3. F/V Carrier Detect Output.

$$\text{resolution} \approx \frac{V_{CC} - V_{BE}}{f_H - f_L} = \frac{18 - 1.3}{600 - 100} = \frac{33.4 \text{ mV}}{\text{Hz}}$$

for V_{CC} = 18 V

We can now calculate V_{REF}

$$V_{REF} = V_{CC}/2 - V_{BE} = 9 \text{ V} - .65 \text{ V} = 8.35 \text{ V}$$

The center frequency is given by

$$f_o = \frac{1}{R_0 C_0}$$

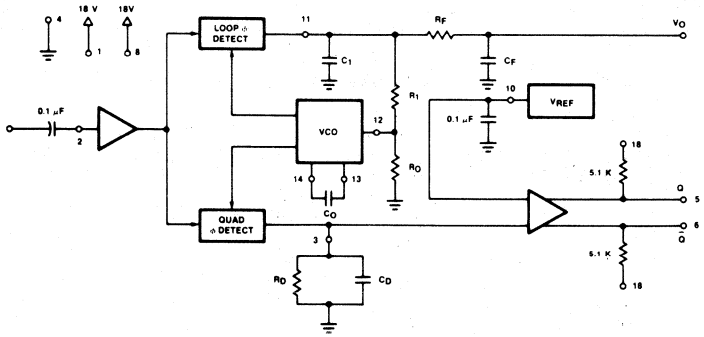


Figure 4. F/V Circuit Diagram.

choosing R_0 = 20 K and rearranging

$$C_0 = \frac{1}{R_0 F_0} = \frac{1}{(20\ K\Omega)\ (350\ Hz)}$$

$$= .143\ \mu F$$

Since $$\frac{R_0}{R_1} = \frac{(f_H - f_L)}{2\ f_o}$$

$$R_1 = \frac{2\ f_0\ R_0}{(f_H - f_L)} = \frac{2\ (350\ Hz)\ (20K)}{(600 - 100)\ Hz}$$

$$= 28\ K$$

The selection of C_1, the loop filter capacitor has a degree of flexibility in its value. For a damping coefficient of 1/2

$$C_1 \approx \frac{C_0}{4} = \frac{.143\ \mu F}{4} = .035\ \mu F$$

It should be noted that an increased value of C_1 will increase response time but reduce ripple, while a decreased value of C_1 will reduce response time, increase capture range, but increase ripple.

The slope K_1 can now be calculated

$$K_1 = \frac{1}{V_R C_0 R_1} = \frac{1}{(8.35)\ (.143\ \mu F)\ (28\ K)}$$

$$= 29.91\ \frac{Hz}{V}$$

and since $K_2 = f_{MAX} = 600$ Hz

The transfer function is then given by

$$f_{IN} = -29.91\ V_0 + 600$$

The filter $R_F C_F$ forms a one-pole post detection filter, with a time constant

$$\tau = R_F C_F$$

and a cut-off frequency

$$f_C = \frac{1}{2\mu R_F C_F}$$

Selecting R_F = 100K, C_F is then given by

$$C_F \approx \frac{3}{\Delta f/\Delta t}\ \mu F$$

where $\frac{\Delta f}{\Delta t}$ = maximum expected rate of change of input frequency

for $$\frac{\Delta f}{\Delta t} = 300\ cycles/sec$$

$$C_F = \frac{3}{300}\ \mu F = .01\ \mu F$$

giving τ = 1 μsecs F_C = 160 Hz

A carrier detect output is available at Pins 5 and 6 (Q and $\overline{Q}$). The components C_D and R_D comprise the lock-detect filter. For R_D = 470 K, and a capture range approaching the lock range, a minimum value of C_D is given by

$$C_D(\mu F) \geq \frac{16}{f_H - f_L} = \frac{16}{500} = .032\ \mu F$$

$$R_D = 470\ K$$

TEMPERATURE STABILITY

The XR-2211 is characterized by excellent temperature stability, in the order of 50 ppm/°C. The output voltage temperature coefficient can be calculated by

$$\frac{V}{°C} = \frac{1}{K_1} \times \frac{50\ ppm}{°C} \times (f_H - f_L)$$

substituting

$$= \frac{33.4\ mV}{Hz} \times 50\ ppm \times (600 - 100)\ Hz$$

$$= \frac{.8\ mV}{°C}$$

Digitally Programmable Phase-Locked Loop

INTRODUCTION

Most phase-locked loops require manual potentiometer adjustment if the center frequency of the circuit is critical. Also, once adjusted, if ambient temperature changes cause the PLL's VCO or center frequency to shift, the potentiometer would have to be readjusted if the accurate center frequency was to be maintained. Readjustments are, of course, an impractical solution.

This application note describes the design of a digitally programmable PLL. Being digitally controlled, a microprocessor or other digital circuitry could easily tune or retune the VCO when necessary. The design uses the XR-215 monolithic PLL together with the **BA-9201** D/A converter, which provides the tuning function.

PRINCIPLES OF OPERATION

Figure 1 shows the block diagram of the digitally programmable PLL. The circuit is comprised of two blocks: the PLL and the D/A converter. The PLL is used for FM demodulation, synchronizing signals, or frequency synthesis. It processes these signals, which are centered around its free-running frequency, f_o. This f_o is set by the internal voltage-controlled oscillator, VCO, in the PLL. The VCO within the XR-215 is really a current-controlled oscillator, ICO. This is, the frequency of oscillation of the ICO is directly proportional to the timing current, I_T. I_T is made up of two components: an internal fixed current and an externally programmable current, $I_{PIN\ 10}$. This $I_{PIN\ 10}$ control current is provided by a D/A converter with a current output. Since the D/A provides an output current that is directly set by an input digital code, this code will actually control the center frequency of the PLL's ICO, f_o.

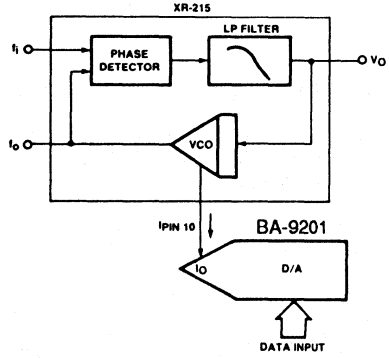


Figure 1. Programmable PLL Block Diagram.

CIRCUIT DESIGN

Figure 2 shows the XR-215 internal blocks and necessary external components. The VCO center frequency, f_o, is calculated by the formula:

$$f_o = \frac{200}{C_O}\left(1 + \frac{0.6}{R_X}\right) \begin{matrix} C_O \text{ in } \mu F \\ R_X \text{ in } K\Omega \end{matrix} \qquad (1)$$

In this application it is desirable to have a variable current drawn from Pin 10, and R_X omitted. Equation 1 is then modified to equation 2 is a current instead of a resistor is used at Pin 10.

$$f_o = \frac{200}{C_O}(1 + I_{PIN\ 10}) \begin{matrix} C_O \text{ in } \mu F \\ I_{PIN\ 10} \text{ in mA} \end{matrix} \qquad (2)$$

Equation 2 can now be used to determine $I_{PIN\ 10}$ for a given f_o adjustment range. Once the center frequency has been set, R_O can be calculated to adjust the tracking range using the relationship:

$$\pm\Delta W_L = 2\pi\Delta f_L \simeq \frac{1565}{R_O C_O} \begin{matrix} \text{rad} \\ \text{sec} \end{matrix} \begin{matrix} R_O \text{ in } K\Omega \\ C_O \text{ in } \mu F \end{matrix} \qquad (3)$$

or

$$R_O = \frac{1565}{2\pi\Delta f_L C_O} \quad R_O \text{ in } K\Omega,\ C_O \text{ in } \mu F \qquad (4)$$

Now with R_O calculated for Δf_L, the capture range, Δf_C is set using the loop time constant capacitors C_1:

$$\pm\Delta W_C = \sqrt{\frac{K_O K_\phi}{\tau_1}} = 2\pi\Delta F_C \qquad (5)$$

τ_1 = Loop Time Constant
K_O = VCO Conversion Gain
$K\phi$ = Phase Detector Conversion Gain

Substituting the values for $K_O K\phi$ and solving for F_C:

$$\Delta F_C = \frac{1}{2\pi}\sqrt{\frac{0.684}{R_O C_O C_1}} \qquad (6)$$

or

$$C_1 = \frac{0.017}{\Delta f_C^2 R_O C_O} \quad R_O \text{ in } K\Omega,\ C_O \text{ in } \mu F \qquad (7)$$

The resistors R_I and R_F are used to set the gain of the op amp when used for FM demodulation. C_C is op amp compensation and is in the range of 300 pF for unity gain to 50 pF for a gain of 10 and up. The resistors going to Pins 4, 5, and 6 are used to dc-bias the phase detector inputs at half supply, with their actual value not critical. The capacitors C_2 and C_1 are used for capacitive coupling.

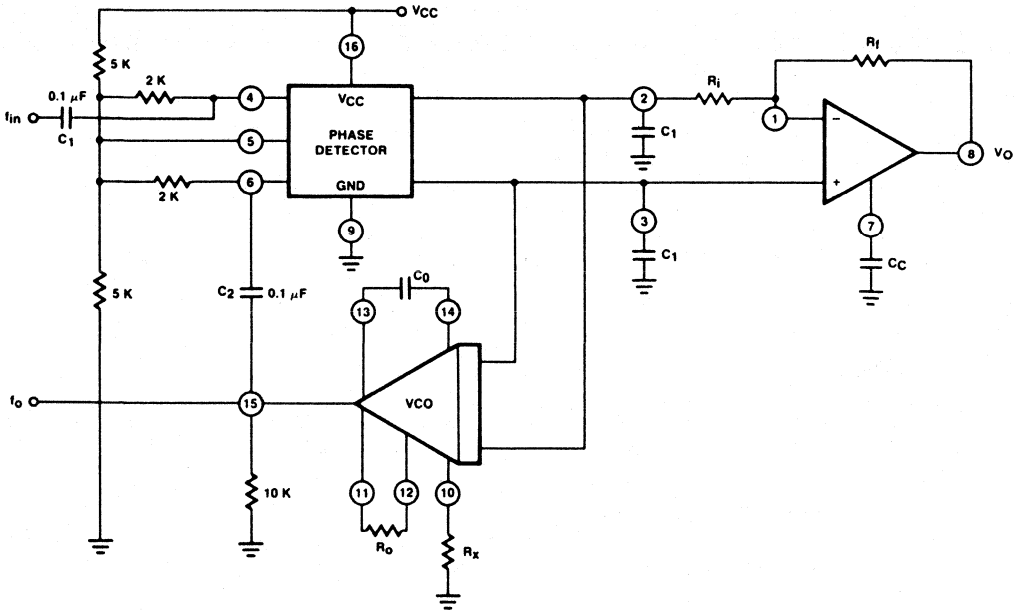


Figure 2. XR-215 with External Components.

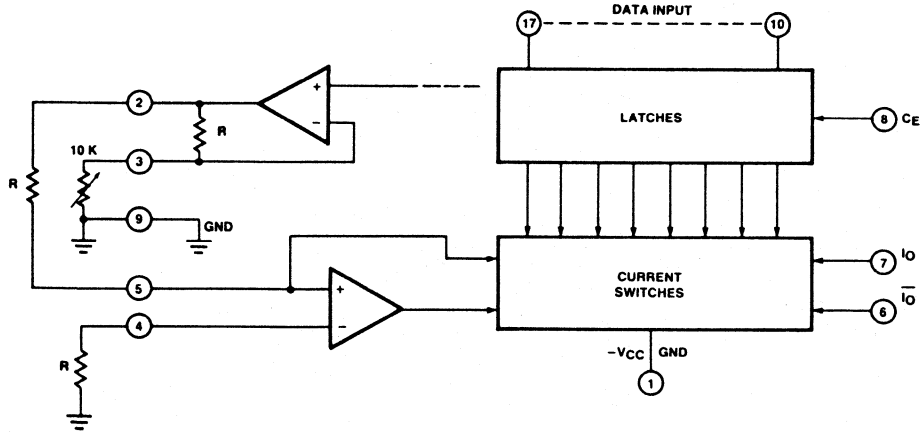


Figure 3. BA-9201 D/A with External Components (ROHM Corporation 714-855- 2131)

Figure 3 shows the D/A converter internal blocks with external circuitry. Data is fed into the input latches, which will allow data to flow through to the current switches when C_E is high and hold data when C_E is low. The output currents are related to the digital inputs by:

$$I_O = 2\, I_{REF}\left[\frac{B_7}{2}+\frac{B_6}{4}+\frac{B_5}{8}+\frac{B_4}{16}+\frac{B_3}{32}+\frac{B_2}{64}+\frac{B_1}{128}+\frac{B_0}{256}\right] \quad (8)$$

where B_N = 1 if bit N is high
B_N = 0 if bit N is low
B_7 = MSB
B_0 = LSB

Also: $I_O + \overline{I_O} = I_{FS}$ = Full-scale Current (9)

$$I_{FS} = 2\, I_{REF}\left(\frac{255}{256}\right) \quad (10)$$

The full-scale current is set using R by the relationship:

$$R = \frac{V_{REF}}{I_{REF}} \quad V_{REF} \simeq 2\ V \quad (11)$$

The 10 KΩ potentiometer from Pin 3 to ground is used to fine-adjust the internal reference to exactly 2.00 V.

DESIGN EXAMPLE

Design a digitally programmable PLL with a center frequency, f_o, equal to 20 kHz. Provide for a 10% digital tuning range. The circuit shall also have the following lock and capture ranges:

$$\pm\Delta f_L = 5 \text{ kHz}, \pm\Delta f_C = 4 \text{ kHz}$$

1. Using equation 2, first with $I_{PIN\ 10} = 0$ (digital inputs all zeros) C_O can be determined.

$$f_o = \frac{200}{C_O} \qquad C_O = 0.01\ \mu F$$

2. This same equation is used to determine the maximum value of $I_{PIN\ 10}$ for a 10% change in f_o. Rearranging equation 2 yields:

$$I_{PIN\ 10\ (max)} = \frac{f_o C_O}{200} - 1 = \frac{22\text{ K } (0.01)}{200} - 1 = 0.1 \text{ mA}$$

f_o = 20 K + 2 K Adjustment Range

3. R_O is now calculated from equation 4:

$$R_O = \frac{1565}{(2\pi)\ (5\text{ K})\ (0.01)} \simeq 5\ \text{K}\Omega$$

4. C_1 is determined by equation 7:

$$C_1 = \frac{0.017}{(4\text{ K})^2\ (5)\ (0.01)} \simeq 0.022\ \mu F$$

5. The D/A components can now by specified, first using equation 10 and the previously calculated $I_{PIN\ 10}$ maximum current:

$$I_{PIN\ 10\ max} = I_{FS}\ 2\ I_{REF}\left(\frac{255}{256}\right)$$

$$I_{REF} \simeq 50\ \mu A$$

6. The reference current setting resistor, R, is now determined using equation 11:

$$R = \frac{2.00}{50\ \mu A} = 40\ \text{K}\Omega$$

7. Calibration of the system is accomplished by adjusting potentiometer R_3 for V_{REF} on the **BA-9201** to exactly 2.00 V.

Figure 4 shows the completed design example.

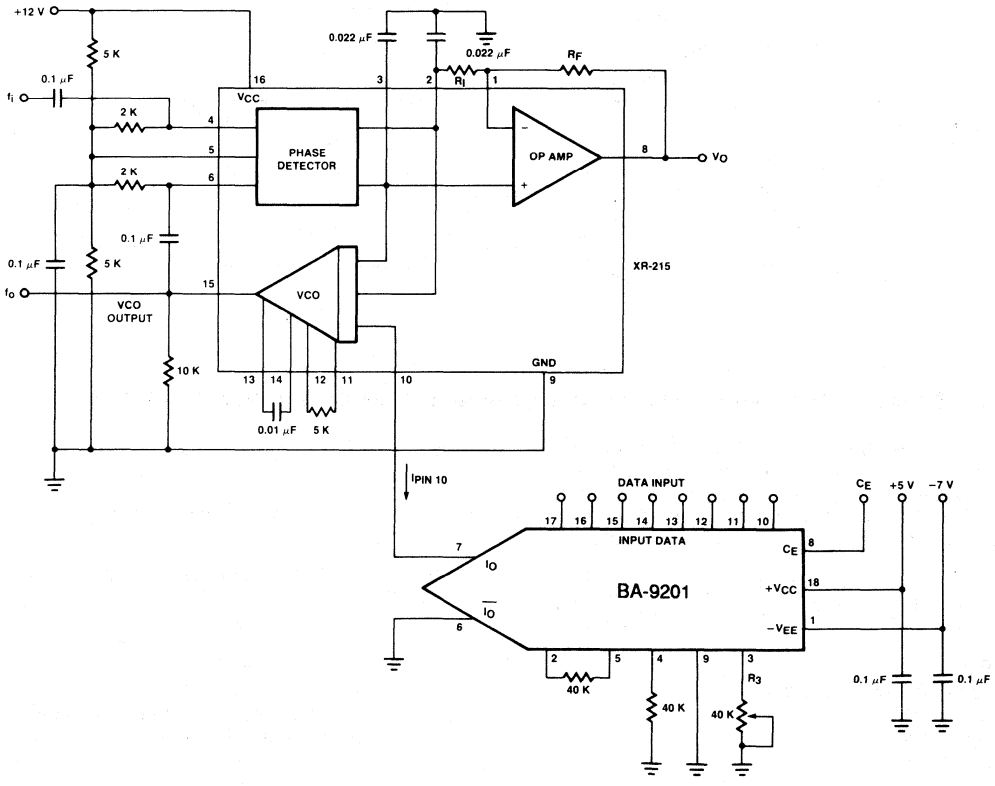


Figure 4. Digitally Programmable PLL

High-Speed FSK Modem Design

INTRODUCTION

As the need for transmitting data increases, some applications require data to be sent faster than the conventional telephone line modems. This application note describes the design and construction of a high speed full-duplex, FSK modem using XR-2206 as a modulator and XR-210 as the demodulator transmitting data at the rate of 100 Kilobaud.

PRINCIPLES OF OPERATION

The block diagram in Figure 1 describes the basic building block in any FSK modem system. The major difference is that in high speed applications, data is transmitted over a twisted pair wire or coaxial cable instead of the telephone line with its limited bandwidth. The complete system is comprised of an answer and originate modem. Simply stated, the modulator converts the input data to two discrete frequencies corresponding to its 1's and 0's and is then sent over a line or cable. The line hybrid steers these frequencies to the bandpass filter, where it will remove any unwanted signals that might have gotten through due to the line or cable before reaching the demodulator. The demodulator, which is a phase locked loop, will lock onto the incoming frequencies and produce 1's and 0's on its output. A detailed description on FSK techniques is given in AN-28.

DESIGN EQUATIONS — Refer to Figure 6

1. The frequency of oscillation of the XR-2206 when used as a modulator, with the FSK input (Pin 9) is high is:

$$\frac{1}{R7A + R7B\ C_3}$$

When the FSK input (Pin 9) is low the frequency equals

$$\frac{1}{R8A + R8B\ C_3}$$

2. The filter best suited for modem applications is the butterworth filter due to its linear phase response within the passband. Table 1 shows the normalized capacitor values for butterworth filters up to fifth order.

Table 1

ORDER NO.	C1	C2	C3
2	1.414	.7071	
3	3.546	1.392	.2024
4	1.082	.9241	
	2.613	.3825	
5	1.753	1.354	.4214
	3.235	.3090	

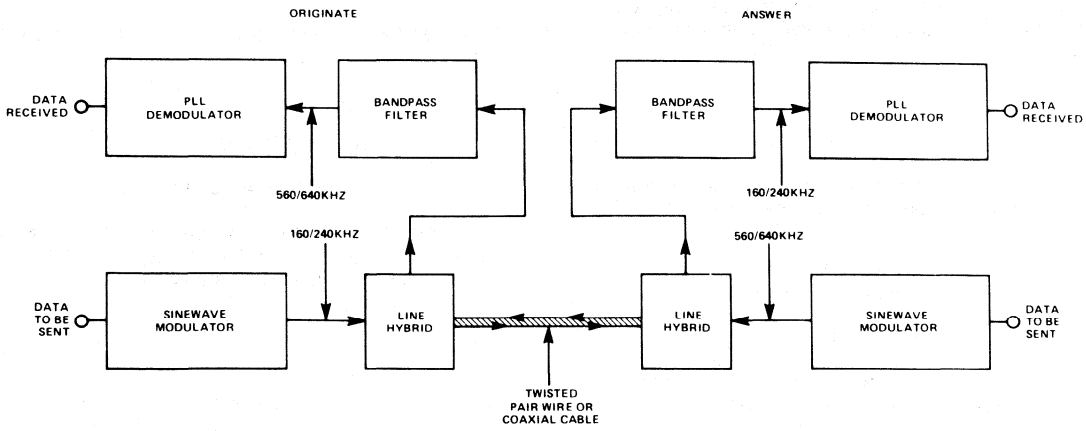


Figure 1. Block Diagram of High Speed FSK Modem System

Figure 3 shows a third order active high pass filter. To solve for the actual resistor values we use the formula:

$$R = \frac{1}{W_C\ CN\ C}$$

Where CN is the normalized capacitor and $W_C = 2\pi F_C$. In this equation, make all capacitors equal.

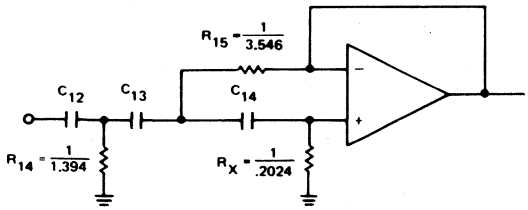


Figure 3.

After calculating R_X remember for single supply operation the op amp must be biased at 1/2 V_{CC}; therefore take twice the calculated value for R_X and configure as shown in Figure 4.

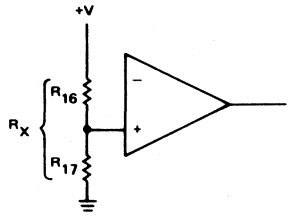


Figure 4.

Figure 5 shows a third order active butterworth low pass filter. To convert from the normalized capacitor values to the actual capacitor values, we use the formula:

$$C = \frac{CN}{W_C R}$$

Where CN is the normalized capacitor value and $W_C = 2\pi F_C$. In this equation, make all resistors equal.

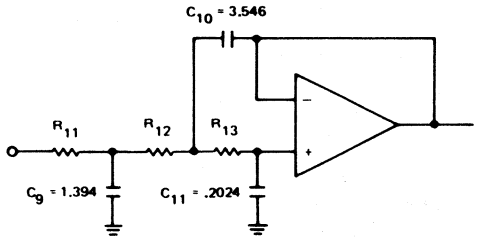


Figure 5.

The equations for using the XR-210 as an FSK demodulator are as follows:

$$\Delta F_L = (2)\Delta F$$

$$\Delta F = F_{mark} - F_{space}$$

$$\Delta F_L = 2(F_{mark} - F_{space})$$

$$F_0 = \frac{F_{mark} + F_{space}}{2}$$

$$F_0 = \frac{234}{C_0}\left(1 + \frac{.1}{R_T}\right) \quad \begin{matrix} C_0 \text{ is in } \mu f \\ R_T \text{ is in K}\Omega \end{matrix}$$

$$C_0 = \frac{234}{F_0}$$

$$\Delta W_C = \sqrt{\frac{\Delta WL}{6KC1}}$$

$$\Delta W_L = 2\pi\ \Delta F_L$$

$$C_1 = \frac{\Delta WL}{6K\Delta W_C{}^2}$$

$$R_0 = \frac{2(1565)}{\Delta WLC_0} \quad R_0 \text{ is in K}\Omega$$

$$C18 = \frac{10^{-4}}{2\pi\ (\text{Baud Rate})}$$

$$C19 = \frac{10^{-4}}{3\pi\ (\text{Baud Rate})}$$

DESIGN EXAMPLE

Design a FSK Demodulator with the following specification:

F_0 = 200 kHz

ΔF_L = 160 kHz

Baud Rate = 100 Kilobaud

In this example, we **must** know the mark and space frequencies. If F_{mark} = 160 kHz and F_{space} = 240 kHz, the free running frequency is equal to

$$\frac{F_{mark} + F_{space}}{2}$$

$$= 200 \text{ kHz}$$

In order to calculate the free running frequency, we use the formula:

$$F_0 = \frac{234}{C_0}$$

In this example we will use a variable resistor (R_T) in order to fine tune F_0 to exactly 200 kHz, therefore:

$$F_0 = \frac{234}{C_0}\left(1 + \frac{.1}{R_T}\right)$$

The lock range (ΔF_L) is equal to twice the difference of the mark and space frequencies, so

$$\Delta F_L = 2(F_{space} - F_{mark})$$

R_0, which sets the lock range equals:

$$R_0 = \frac{2(1565)}{\Delta WLC_0} \qquad \Delta WL = 2\pi F_L = 6.28\,(160\times10^3) = 1004800$$

$$= \frac{2(1565)}{1004800.0015}$$ Where C_0 is in μf and R_0 is in $K\Omega$

$$= 2.0\ K\Omega$$

The Capture Range (ΔF_C) is equal to:

$$\Delta W_C = \sqrt{\frac{\Delta WL}{6K\ C17}} \qquad \Delta W_C = 2\pi\Delta F_C \qquad \Delta W_L = 2\pi\Delta F_L$$

In order to solve for C17 we rearrange the equation to read.

$$C17 = \frac{\Delta WL}{(6K)\ W_C{}^2}$$

$$= \frac{1004800}{(6K)\ 753600^2} = 300\times10^{-12}$$

therefore:

$$\Delta W_C = \sqrt{\frac{1004800}{(6\times10^3)\ 300\times10^{-12}}}$$

$$= 118.97\ kHz$$

It is important to note C17 and 6K set the loop time constant. When used as an FSK Demodulator, the XR-210 has post detection filtering on the output of the phase detector. In order to calculate the values for C18 and C19 we use the relationships:

$$C18 = \frac{10^{-4}}{2\pi\ (Baud\ Rate)}$$

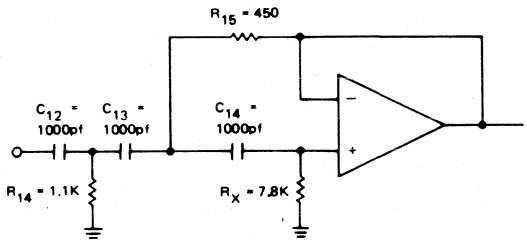
$$= \frac{10^{-4}}{6.28\ (100\times10^3)} = 160\times10^{-12}\ or\ 160\ pf$$

$$C19 = \frac{10^{-4}}{9.42\ (100\times10^3)} = 106\times10^{-12}\ or\ 106\ pf$$

For the filter, 18 dB of attenuation should be sufficient; therefore:

Design a third order high pass butterworth filter with f_c = 100 kHz.

1) In order to solve for actual resistor values use Table 1 and set all capacitors equal. The design example is shown below:



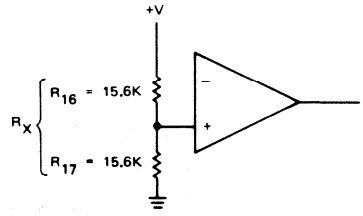
$$R = \frac{1}{W_C CN\ C}$$

$$R15 = \frac{1}{(6.28\times100\times10^3)3.546(1000\times10-12)} = 450\Omega$$

$$R14 = \frac{1}{(6.28\times100\times10^3)1.392(1000\times10-12)} = 1.1K\Omega$$

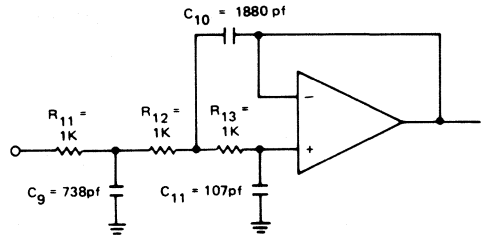
$$R_X = \frac{1}{(6.28\times100\times10^3).2024(1000\times10-12)} = 7.8K\Omega$$

After calculating R_X take twice the value and configure as shown below:



Design a third order lowpass butterworth filter with F_c = 300 kHz.

2) In order to solve the actual capacitances, use Table 1 and set all resistors equal. The design example is shown below:



$$C = \frac{CN}{W_C R} \qquad W_C = 2\pi F_C$$

$$C = \frac{3.546}{2\pi(300 \times 10^3)\ 1 \times 10^3} = 1880\ pf$$

$$C10 = \frac{3.546}{1884000000} = 1880\ pf$$

$$C9 = \frac{1.392}{1884000000} = 738\ pf$$

$$C11 = \frac{.2024}{1884000000} = 107\ pf$$

Design an FSK modulator with F_{mark} = 560 kHz and F_{space} = 640 kHz. The frequency of oscillation with the FSK input (Pin 9) is high is equal to:

$$F_{mark} = \frac{1}{R7A + R7B\ C3}$$

$$= \frac{1}{1\ K + 785\Omega .001\mu f} = 560 \times 10^3 \text{ or } 560\ kHz$$

When FSK input (Pin 9) is low the frequency is equal to:

$$F_{space} = \frac{1}{R8A + R8B\ C3}$$

$$= \frac{1}{1\ K + 562\Omega .001\mu f} = 640 \times 10^3 \text{ or } 640\ kHz$$

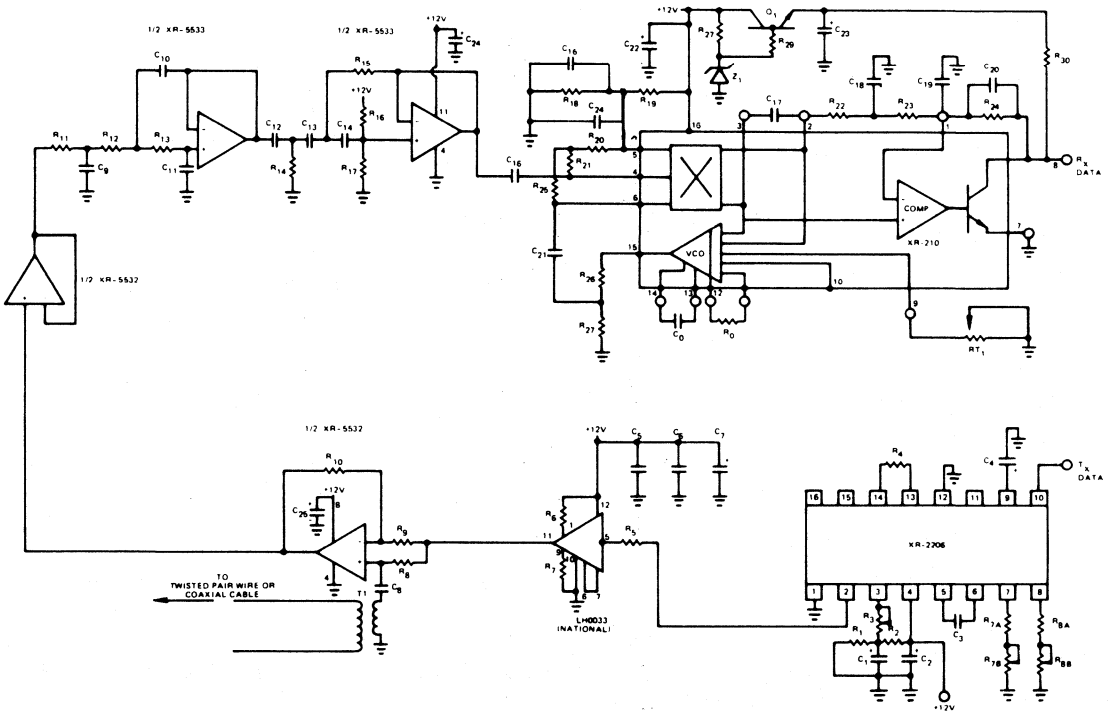


Figure 6. Complete Schematic for 100 Kilobaud FSK Modem

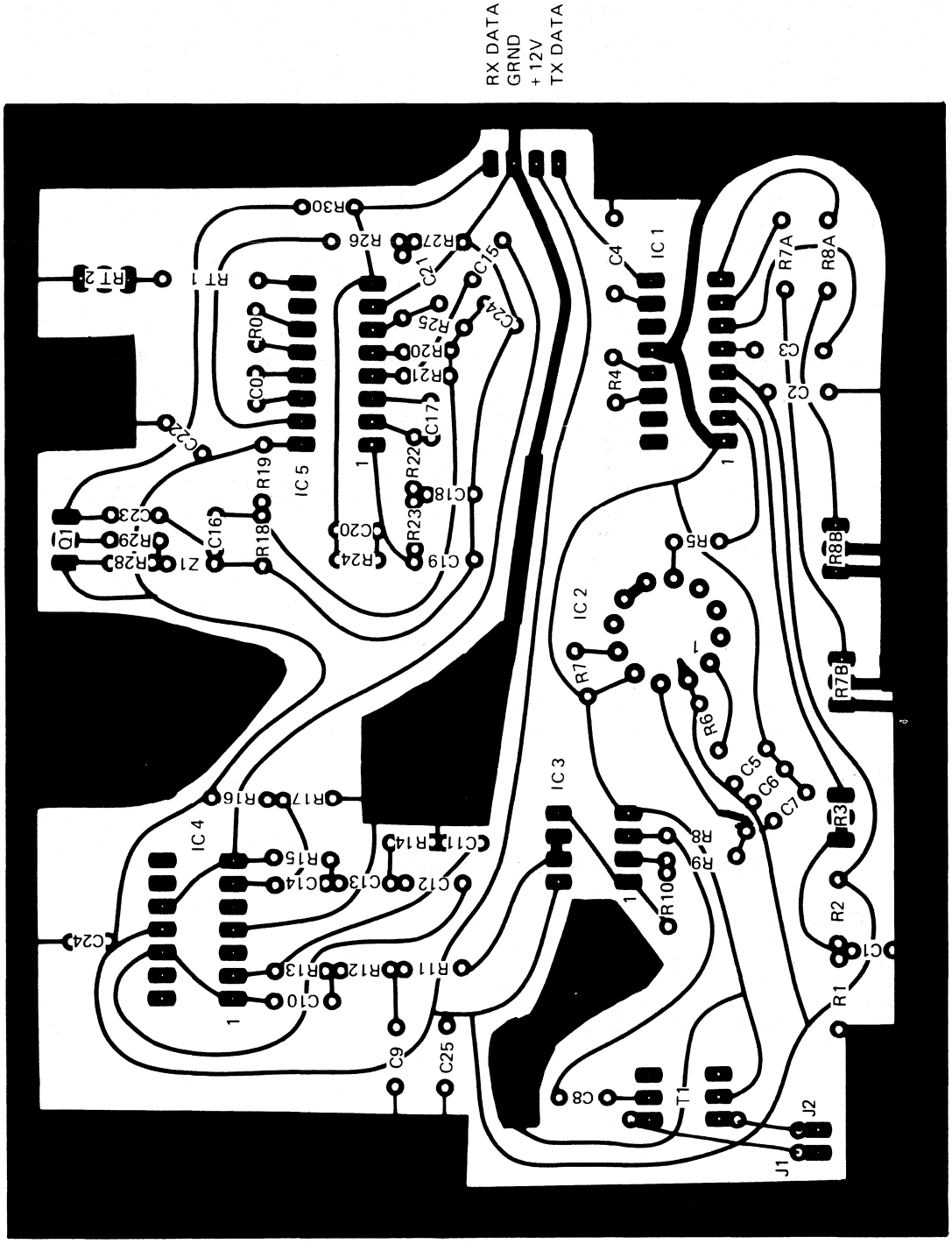


Figure 7. P.C. Board Layout for 100 Kilobaud FSK Modem–Component Side

PART NO	ANSWER	ORIGINATE	PART NO.	ANSWER	ORIGINATE
R1-R2	5.1K	5.1K	C1	47 μf	47 μf
R3	50KΩ Pot	50KΩ Pot	C2	4.7 μf	4.7 μf
R4	200Ω	200Ω	C3	.001 μf	.001 μf
R5	51Ω	51Ω	C4	4.7 μf	4.7 μf
R6-R7	100Ω	100Ω	C5-C6	.1 μf	.1 μf
*R8	**75Ω, 1W**	**75Ω, 1W**	C7	4.7 μf	4.7 μf
R9-R10	10 KΩ	10 KΩ	C8	1 μf	1 μf
R11-R13	1 KΩ	1 KΩ	C9	738 pf	317 pf
R14	1.1 KΩ	228Ω	C10	1800 pf	807 pf
R15	450Ω	90Ω	C11	107 pf	46 pf
R16-R17	16 KΩ	3 KΩ	C12-C14	1000 pf	1000 pf
R18-R19	5 KΩ	5 KΩ	C15	.22 μf	.22 μf
R20	2 KΩ	2 KΩ	C16	1 μf	1 μf
R21	4 KΩ	4 KΩ	C17	300 pf	300 pf
R22	10 KΩ	10 KΩ	C18	150 pf	150 pf
R23	5 KΩ	5 KΩ	C19	106 pf	106 pf
R24	249 KΩ	249 KΩ	C20	10 pf	10 pf
R25	4 KΩ	4 KΩ	C21	.1 μf	.1 μf
R26	3 KΩ	3 KΩ	C22-C25	4.7 μf	4.7 μf
R27	10 KΩ	10 KΩ	Q1	2N2222A	2N2222A
R28	5 KΩ	5 KΩ	T1	PE-576 **	PE-576 **
R29	562Ω	562Ω	Z1	1N5232	1N5232
R30	1.3 KΩ	1.3 KΩ	IC 1	XR-2206	XR-2206
RO	2.4 KΩ	7.4 KΩ	IC 2	LH0033†	LH0033†
RT2	1 KΩ Pot	1 KΩ Pot	IC 3	XR-5532	XR-5532
R7A	1.4 KΩ	562Ω	IC 4	XR-5533	XR-5533
R7B	1 KΩ Pot	1 KΩ Pot	IC 5	XR-210	XR-210
R8A	750Ω	3.3 KΩ			
R8B	1 KΩ Pot	1 KΩ Pot	J1-J2	JUMPER	JUMPER
RT1	50Ω	100Ω		WIRE	WIRE

* Coaxial Wire (75Ω)
** Pulse Engineering (619-268-2400)
‡National

Figure 8. Component List for 100 Kilobaud FSK Modem

Transformer Comments

The Pulse Engineering PE-5766 transformer provides a low inductance, for maximum power transfer and small physical size. Resistor R8, for 75Ω impedance coaxial cable should be 75Ω 1W. For twisted pair, the resistor should be 150Ω, 1W.

High-Frequency TTL Compatible Output from the XR-210 and XR-215 Monolithic PLL Circuits

INTRODUCTION

With digital circuitry as common as it is, it is necessary to be able to interface analog signals to digital systems. This can be done by using the XR-215, a monolithic PLL circuit, and an additional buffer circuit.

When an input signal is present within the capture range of the PLL system, the XR-215 will lock on the input signal and the VCO section of the PLL will synchronize with the input frequency. The VCO output can then be buffered in order to produce a TTL compatible output.

PRINCIPLES OF OPERATION

Figure 1 shows a functional block diagram of the XR-215 monolithic PLL system. The circuit contains a phase comparator, a voltage controlled oscillator (VCO), and an operational amplifier. A complete phase locked loop system can be made by simple ac coupling the VCO output to either of the phase comparator inputs, and by adding a low pass filter to the phase comparator outputs.

The VCO output can be buufered in order to produce a TTL compatible output at high frequencies by the simple common emitter circuit shown in figure 2. The amplitude of VCO degrades as frequency increases and at 21 MHz, the amplitude is reduced from approximately 2.5 Vpp to 50 mVpp. The dc outputlevel is 2 volts below V_{CC} so with V_{CC} equal to ±5 volts, the dc level is approximately 3 volts. The VCO output is ac coupled in order to block this dc level. The input signal causes Q_1 to be overdriven, where the amplitude is 400 mVpp offsetted at approximately 0.769 Vdc. When Q_1 is in the offstate, the collector voltage will be forced high and when this voltage exceeds 0.7 Vdc, Q_2 will turn on and the collector of Q_1 will be clamped at 0.7 Vdc. The output of the VCO at the TTL buffered output will be in phase.

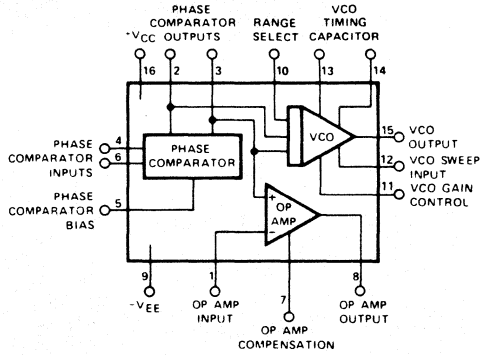


Figure 1. Functional Block Diagram of XR-215 Monolithic PLL Circuit.

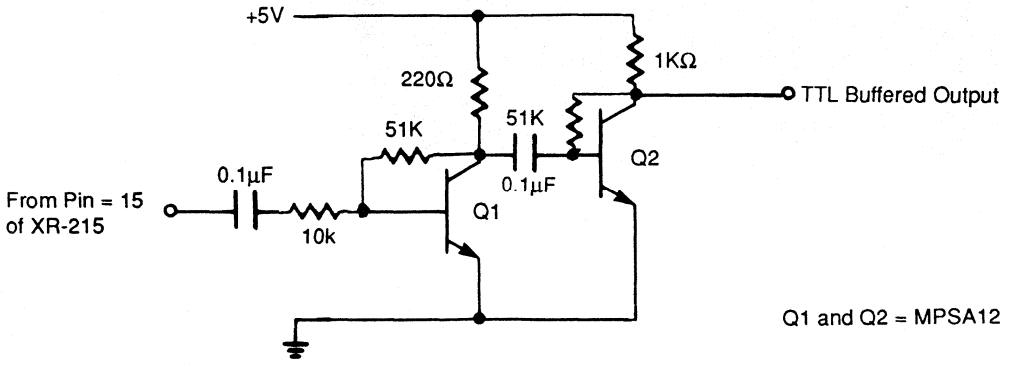
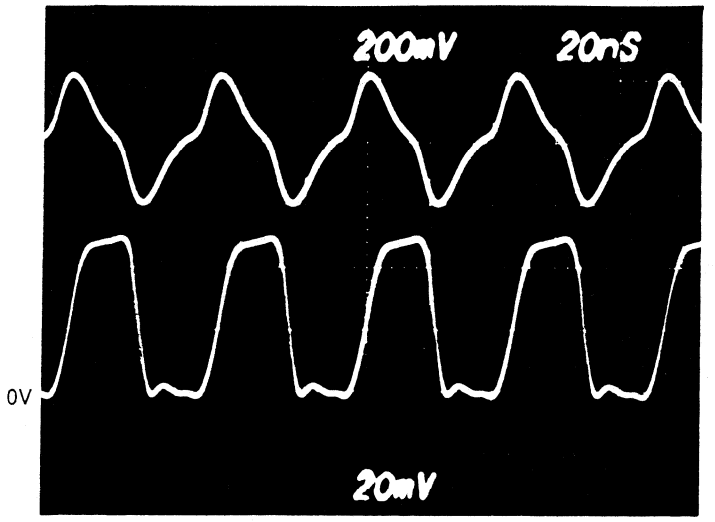
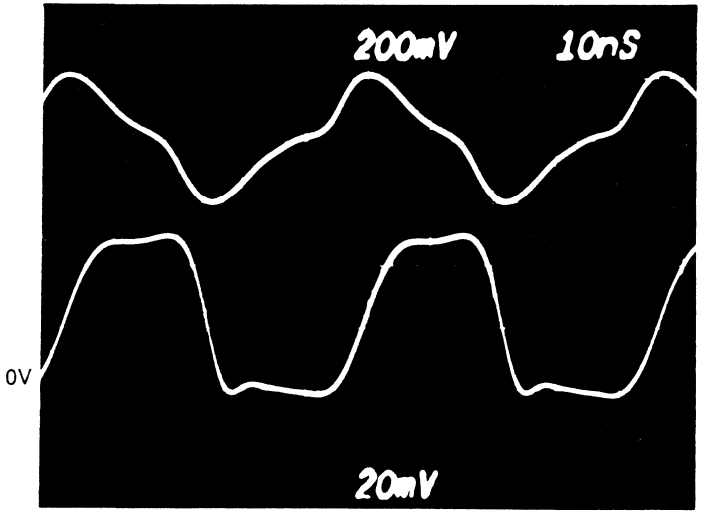


Figure 2. Common Emitter Buffer Circuit.



VCO Output (Pin 15)
of XR-215 (non-typical)

TTL Buffered Output
at 21 MHz measured
with X100 prode.



Propagation Delay is
approximately 5nS.

XR-212ACS Performance Testing

INTRODUCTION

The task of testing the performance of a modem is quite often at best a difficult one. To simulate in the laboratory, conditions that may exist on actual phone lines is not only difficult but requires special test equipment. However, to predict actual operating performance, this testing is necessary. This application note describes the test method and actual data on a 300 BPS/1200 BPS full duplex modem system.

The modem acts as the link between the digital, data side, and analog, line side, mediums as shown in Figure 1.

TEST INFORMATION

The performance or quality of the modem is measured by its' ability to send and receive data accurately. This is usually specified as its bit error rate (BER). The BER is specified as the number of errors for a given number of data bits received. For example, a BER of 1/10-5 states that one error may be seen for every 100,000 data bits received. The BER is usually given as a function of various impairments which may occur on the analog (phone) transmission medium.

The best reference for test conditions that occur on the GSTN is "1982/83 End Office Connection Study: Analog Voice and Voiceband Data Transmission performance Characterization of the Public Switched Network" by Carey, etal. AT&T Bell Laboratories Technical Journal Vol. 63 No.9, Novermber 1984.

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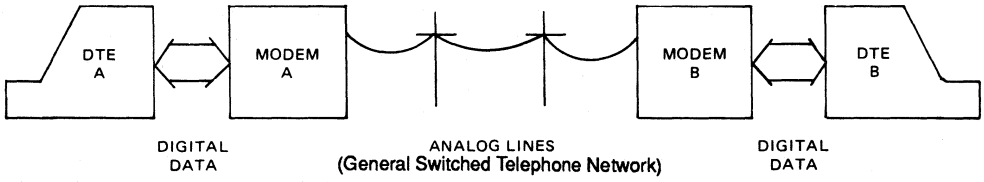


Figure 1. Modem Data Link

1. BER versus signal to noise ratio (S/N). This test is the specification which best describes a modem's actual performance in operating environments. The modem's transmitted carrier, $T_{X\ car}$, and received carrier $R_{X\ car}$, are set to fixed levels while noise is added to the $R_{X\ car}$. Figure 2 illustrates such a condition.

   The data error analyzers are used to both send a predictable data pattern as well as verifying if it is received properly. It will count errors for a given number of data bits.

2. BER vs. $R_{X\ car}$ level. The $T_{X\ car}$ is set to a fixed level and the $R_{X\ car}$ level is decreased while BER is measured at various levels.

3. BER vs. frequency offset. Frequency offset represents a shift in the frequency of the $R_{X\ car}$ due to the analog medium. For example, an $R_{X\ car}$ may be received with a frequency of 1203 Hz although it was originally transmitted at 1200 Hz.

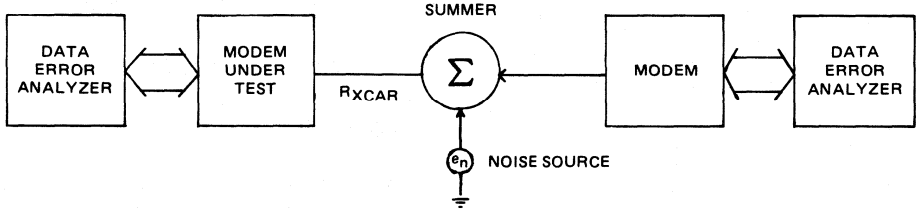


Figure 2. BER vs. S/N

The complete test set up is shown in Figure 3

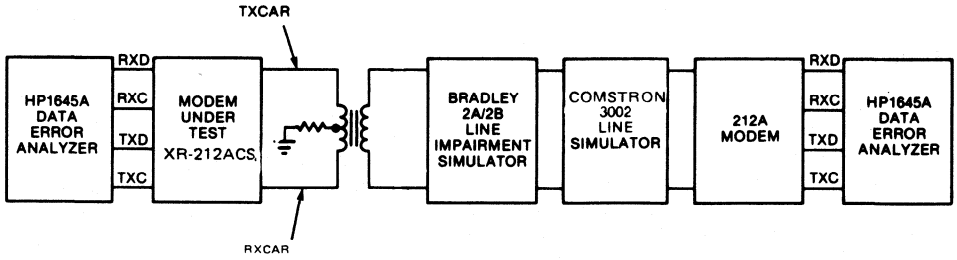


Figure 3. Complete Modem Test Set-Up

The HP 1645A testers are used to send and receive data and to measure BER. The modem under test is an Exar 212ACS type as described in application note AN-25. The Comstron unit is a fixed line simulator to give the characteristics of an actual phone line. Impairments to the line are generated by the Bradley 2A/2B. It is used to generate noise and frequency offset.

BER vs S/N is tested under the following conditions:

$R_{x\ car}$ = −30 dBM — Mode = Synchronous

$T_{x\ car}$ = −10 dBM — Speed = 1200 BPS

Frequency Offset = 0 Hz — Line Type = 3002 (worst case line)

The performance data is shown in Figure 4.

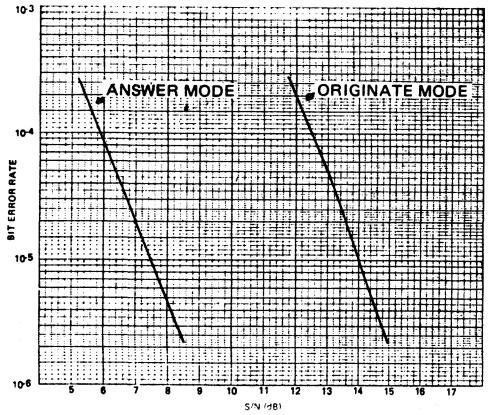


Figure 4. BER vs. S/N 1200 Baud Mode

Figure 5 illustrates BER vs. S/N for FSK (300 baud) operation. The test conditions are the same as those for PSK (1200 baud) operation.

The receiver sensitivity allows received carrier levels below -40 dBM without degrading BER performance. This sensitivity applies to both 1200 and 300 baud operation.

Frequency translation, or carrier frequency shift, is measured in the 1200 baud mode with carrier levels the same as with the BER testing. For both answer and originate a shift of up to plus or minus 4 Hz is possible before the error performance degrades.

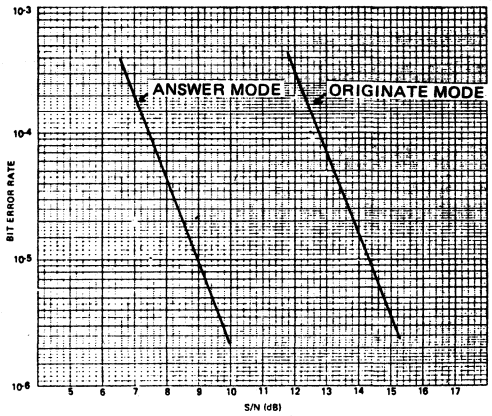


Figure 5. BER vs. S/N 300 Baud Mode

CONCLUSION

The three parameters measured in this application note are not the only characteristics used to specify a modem, however, they are key ones. They best describe operation as to that which may be seen on actual phone lines and are often used for comparison purposes.

A Square Wave to Sine Wave Converter Using the XR-1015

INTRODUCTION

In the world of microprocessors and digital logic control, there is still the need for a synchronized sinusoidal source. For many applications, this was done using a digital-to-analog converter and EPROM with the sine values sequentially selected. This required microprocessor time, as well as two relatively large components to be added to the system.

A synchronized sine wave can be obtained with an XR-1015 Seventh Order Elliptic Low Pass Filter and a single 74LS390 dual divide-by-10 counter. A single clock controls the frequency of the sine output, which can be controlled by the microprocessor using an on-chip timer, or with a digitally programmable counter accessed by the microprocessor data bus. The total harmonic distortion obtained in such a system is less than −60 db (0.1%) from 20 Hz to 20 kHz, excluding the sampling clock frequency.

PRINCIPLES OF OPERATION

The XR-1015 is a seven pole, six-zero elliptic low pass switched capacitor filter. With its greater than 70 dB of stop band rejection, the XR-1015 has the capability of reducing the amplitude of all out-of-band harmonics by a substantial amount.

The 74LS390 is a dual divide-by-10 counter. With the intermediate divide-by-5 and divide-by-2 points made available on the device, it can be wired to perform the divide-by-50 function needed for the dividie-by-2 output of the XR 1015, to create the square wave at the frequency of interest.

Figure 1 shows the basic circuit with its single clock input from the microprocessor applied to the XR-1015. The divide-by-2 output of the XR-1015 is then clamped to −0.7 V to +5 V and applied to the input of the 74LS390. This divider provides the divide-by-50 clock that is applied to the filter input of the XR-1015.

The clock-to-corner ratio of the XR-1015 is set at 100:1 which allows the corner frequency of the low pass filter to track the square wave input signal. The seven pole, six-zero elliptic low pass filter response of the XR-1015 reduces any harmonics from the applied signal providing a low distortion audio range sine wave at the output.

Figure 2 shows the harmonic content of the sine output at the XR-1015 when clocked at 2 kHz (sine output at 20 Hz). The total harmonic distortion is −53 dB. The lower side band created by the sampled system is −40 dB below the fundamental, and should not be a factor in most applications. If needed, an inprecise RC continous-time active filter could be added to the output with the corner controlled by switching in different resistor values.

Figure 3 shows the harmonic content of the sine output with the XR-1015 clocked at 2 MHz (sine output at 20 kHz). The total harmonic distortion is near −60 dB. This low distortion signal allows the sine output to be used for microprocessor controlled test equipment for the evaluation of distortion on tape recorders or telephone lines.

When single supply +5 VDC operation is desired, Figure 5 should be used. This circuit still performs the square wave to sine wave conversion. The harmonics in this case are attenuated by −50 dB (0.3%) allowing the circuit to be used for tone generation for the evaluation of telephone lines.

CONCLUSION

The phase relationship, which can be important in many applications (network analysis) is shown in Figure 4. The phase shift from the input of the XR-1015 to the output is a constant −50 degrees, as would be expected, since the corner frequency of the filter moves with the input frequency of the filter. Because of this, the system can be used for phase measurements for test instrumentation. With this circuit, a simplified synchronized sine wave can be provided where before a complicated digital-to-analog converter and EPROM was needed.

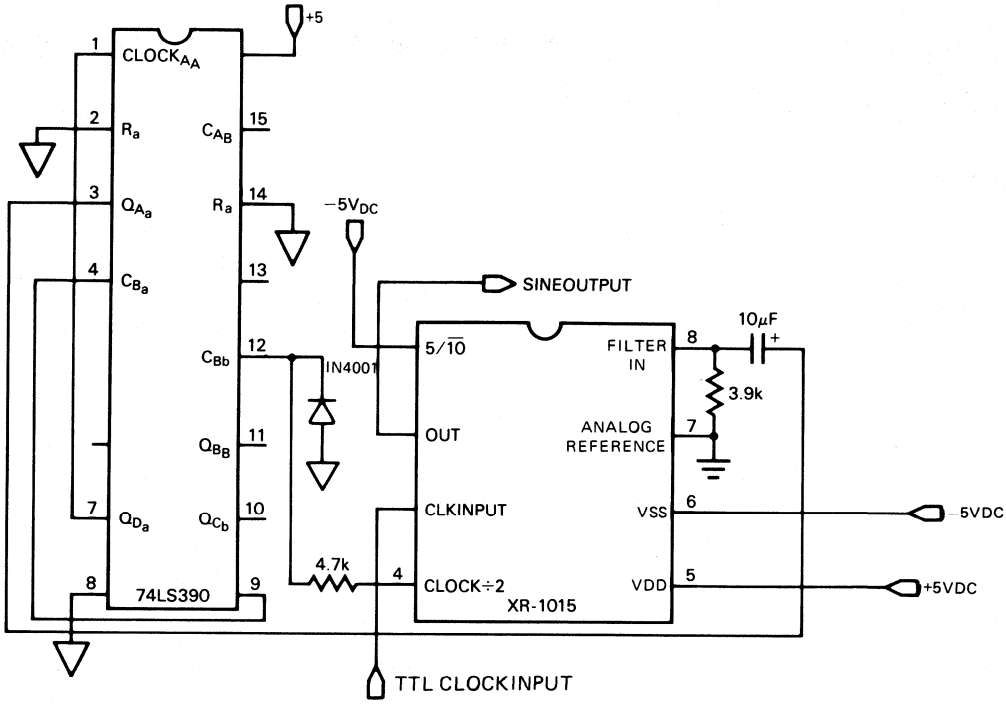


Figure 1. Basic Circuit - Single Clock Input

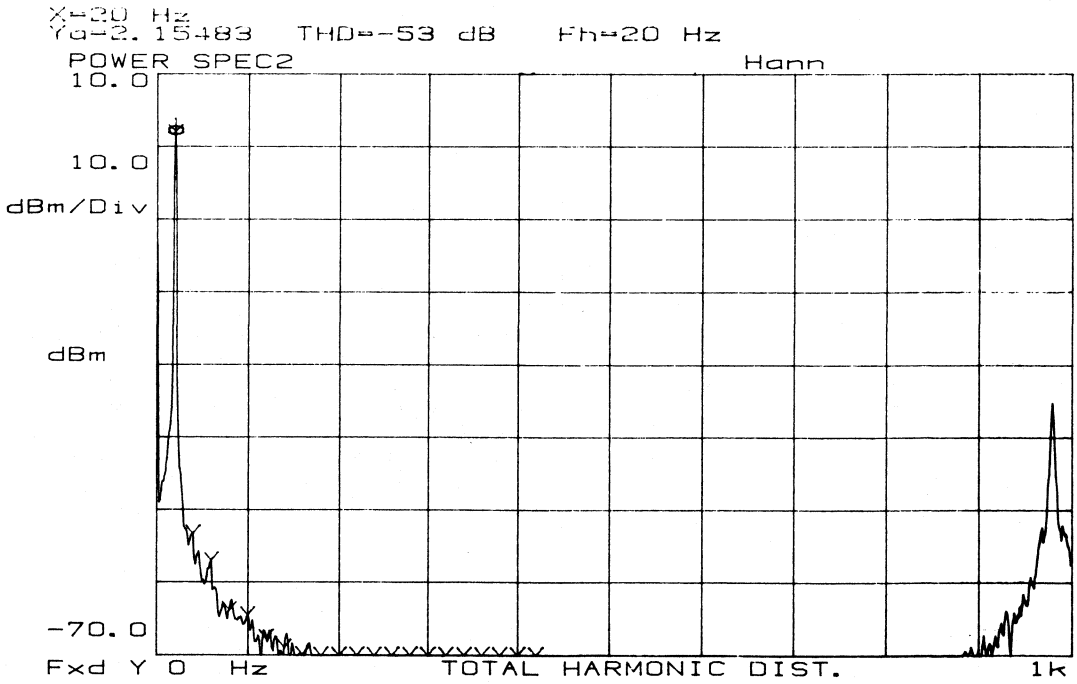


Figure 2. Harmonic Content of Sine Output

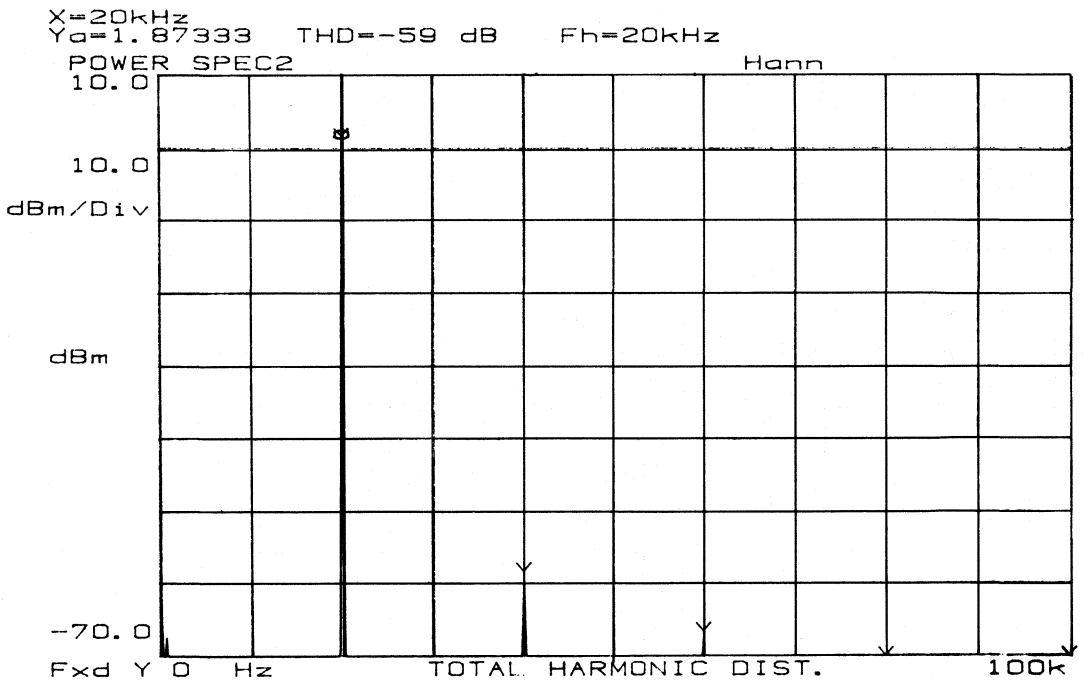


Figure 3. Harmonic Content of Sine Output

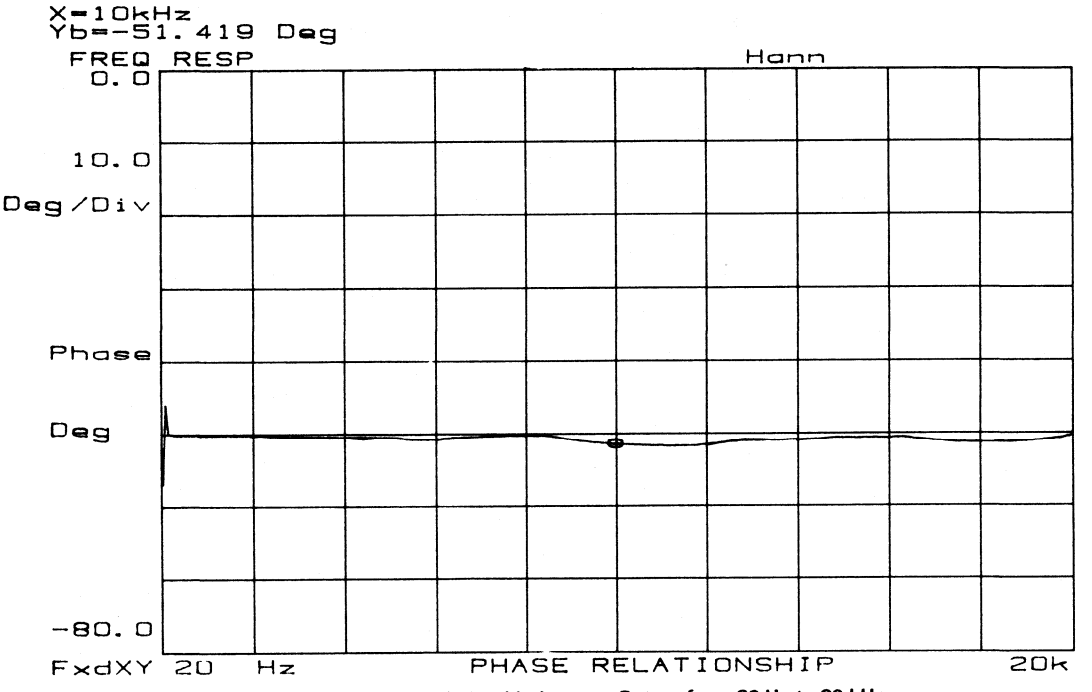


Figure 4. Phase Relationship Input to Output from 20 Hz to 20 kHz

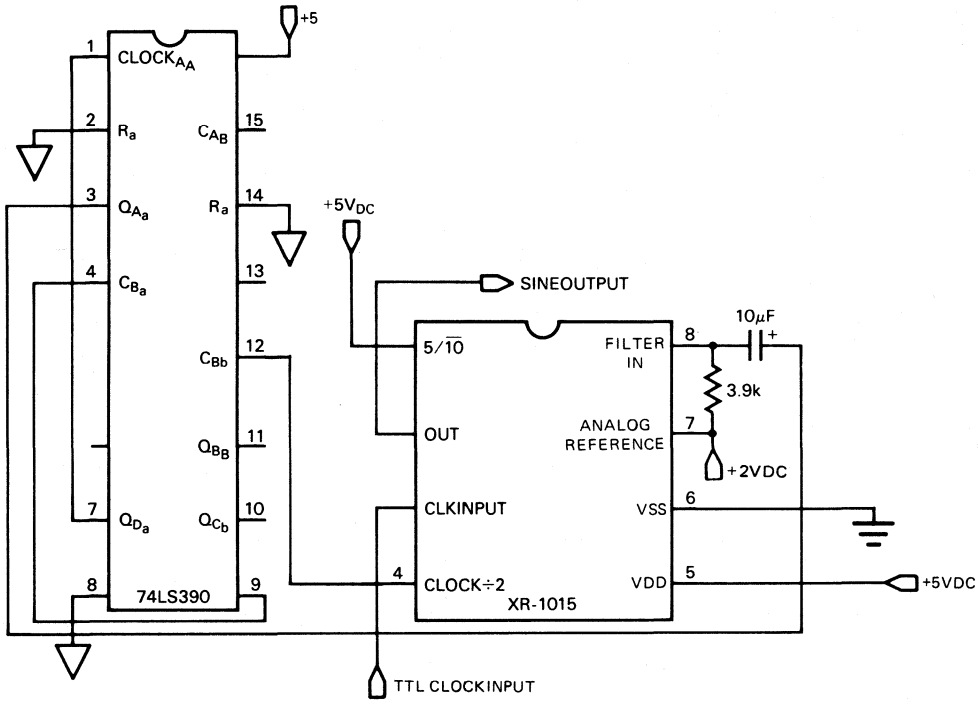


Figure 5. Basic Circuit - Single Clock Input, Single Supply

Introduction to Phase-Locked Loops

INTRODUCTION

The phase locked loop provides frequency selective tuning and filtering without the need for coils or inductors. As shown in Figure 1, the PLL in its most basic form is a feedback system comprised of three basic functional blocks: a phase comparator, low-pass filter and voltage controlled oscillator (VCO).

The basic principle of operation of a PLL can briefly be explained as foolows: With no input signal applied to the system, the error voltage $V_e(t)$ equal to zero. the VCO operates at a set frequency, f_o, which is known as the free-running frequency. If an input signal is applied to the system, the phase comparator compares the phase and frequency of the input signal with the VCO frequency and generates an error voltage, $V_e(t)$, that is related to the phase and frequency difference between the two signals. This error voltage is then filtered and applied to the control terminal of the VCO. If the input frequency, f_s, is sufficiently close to f_o, the feedback nature of the PLL causes the VCO to sychronize, or lock, with the incoming signal. Once in lock, the VCO frequency is identical to the input signal, except for a finite phase difference.

Two key parameters of a PLL system are its lock and capture ranges. They can be defined as follows:

Lock range: The range of frequencies in the vicinity of f_o, over which the PLL can maintain lock with an input signal. It is also known as the tracking or holding range. Lock range increases as the over all gain of the PLL is increased.

Capture range: The band of frequencies in the vicinity of f_o where the PLL can establish or acquire lock with an input signal. It is also known as the acquisition range. It is always smaller than the lock range and is related to the low-pass filter bandwidth. It decreases as the filter bandwidth is reduced.

The lock and the capture ranges of a PLL can be illustrated with reference to Figure 2, which shows the typical frequency-to-voltage characteristics of a PLL. In the figure, the input is assumed to be swept slowly over a broad frequency range. The vertical scale corresponds to the loop error voltage.

In the upper part of Figure 2, the loop frequency is being gradually increased. The loop does not respond to the signal until it reaches a frequency f_1, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input, causing a negative jump of the loop error voltage. Next, V_d varies with frequency with a slope equal to the reciprocal of the VCO voltage-to-frequency conversion gain, and goes through zero as $f_S = f_o$. The loop tracks the input until the input frequency reaches f_2, corresponding to the upper edge of the lock range. The PLL then loses lock, and the error voltage drops to zero.

If the input frequency is now swept slowly back, the cycle repeats itself as shown in the lower part of Figure 2. The loop recaptures the signal at f_3 and traces it down to f_4. The frequency spread between (f_1, f_3) and (f_2, f_4) corresponds to the total capture and lock ranges of the system; that is, $f_3 - f_1$ = capture range and $f_2 - f_4$ = lock range. The PLL responds only to those input signals sufficiently close to the VCO frequency, f_o, to fall within the "lock" or "capture" range of the system. Its performance characteristics, therefore, offer a high degree of frequency selectivity, with the selectivity characteristics centered about f_o.

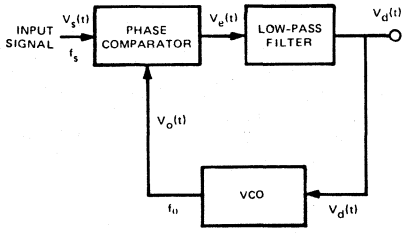


Figure 1. The basic phase locked loop consists of three functional blocks: a phase comparator, a low pass filter and a voltage-controlled oscillator.

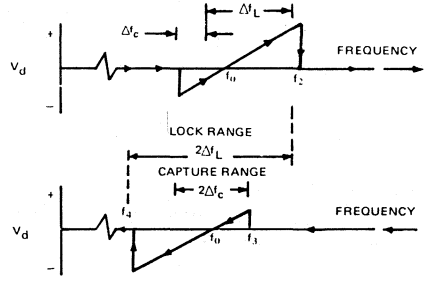


Figure 2. Typical PLL frequency-to-voltage transfer characteristics are shown for increasing (upper diagram) and decreasing (lower diagram) input frequency.

EXAMPLES OF APPLICATIONS

As a versatile building block, the PLL covers a wide range of applications. Some of the more important are the following:

FM demodulation: In this application, the PLL is locked on the input FM signal, and the loop-error voltage, $V_d(t)$ in Figure 1 (see Box), which keeps the VCO in lock with the input signal, represents the demodulated output. Since the system responds only to input signals within the capture range of the PLL, it also provides a high degree of frequency selectivity. In most applications the quality of the demodulated output (i.e., its linearity and signal/noise ratio) obtained from a PLL is superior to that of a conventional discriminator.

FSK demodulation: Frequency-shift keyed (FSK) signals are commonly used to transmit digital information over telephone lines. In this type of modulation, the carrier signal is shifted between two discrete frequencies to encode the binary data. When the PLL is locked on the input signal, tracking the shifts in the input frequency, the error voltage in the loop, $V_d(t)$, converts the frequency shifts back to binary logic pulses.

Signal conditioning: When the PLL is locked on a noisy input signal, the VCO output duplicates the frequency of the desired input but greatly attenuates the noise, undesired sidebands and interference present at the input. It is also a tracking filter since it can track a slowly varying input frequency.

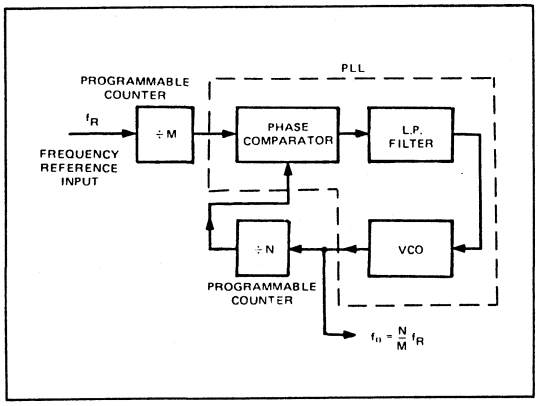


Figure 3. A frequency multiplier/divider can be constructed using a phase locked loop.

Frequency synthesis: The PLL can be used to generate new frequencies from a stable reference source by either frequency multiplication and division, or by frequency translation. Figure 3 shows a typical frequency multiplication and division circuit, using a PLL and two programmable counters. In this application, one of the counters is inserted between the VCO and phase comparator and effectively divides the VCO frequency by

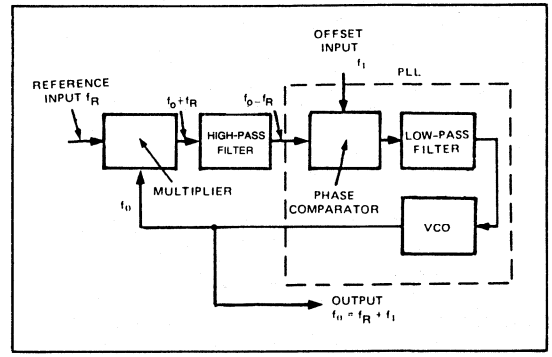


Figure 4. Frequency translation can be accomplished with a phase locked loop by adding a multiplier and an additional low-pass filter to the basic PLL.

the counter's modulus N. When the system is in lock, the VCO output is related to the reference frequency, f_R, by the counter moduli M and N as:

$$f_O = \left(\frac{N}{M}\right) f_R$$

By adding a multiplier and an additional low-pass filter to a PLL (Figure 4), one can form a frequency translation loop. In this application, the VCO output is shifted from the reference frequency, f_R, by an amount equal to the offset frequency, f_1, i.e., $f_O = (f_R + f_1)$.

Data synchronization: The PLL can be used to extract synchronization from a composite signal, or can be used to synchronize two data streams or system clocks to the same frequency reference. Such applications are useful in PCM data transmission, regenerative repeaters, CRT scanning and or drum memory read-write synchronization.

At the onset of his design, the user of monolithic PLL products is faced with the key question of choosing the phase-locked loop IC best suited to his application. The broad line of PLL products offered by Exar cover a wide range of applications. It is often difficult to determine a a glance the best circuit for a given application. The purpose of this section is to review some of the key performance requirements, from an applications point of view, and help answer the question, "What is the best PLL product for the job?"

Table 2 gives a brief listing of some of the major classes of PLL applications, and lists the recommended circuits for each. A further discussion of the key performance parameters associated with each application is listed below.

FM demodulation: Essentially all the PLL circuits listed in Table 1 can be used for FM demodulation. However, it is often possible to narrow the choice down to 2 or 3 circuits, based on the particular performance criteria. In general, there are three key performance parameters which should be examined:

- ☐ Quality of demodulated output: This is normally measured in terms of the output level, distortion, and signal/noise ratio for a given FM deviation.
- ☐ VCO frequency range and frequency stability: For reliable operation, VCO upper frequency limit (see Table 1) should be at least 20% above the FM carrier frequency. VCO frequency stability is important, especially if a narrow-band filter is used in front of the PLL, or multiple input channels are present. If the VCO exhibits excessive drift, the PLL can drift out of the input signal band as the ambient temperature varies.
- ☐ Detection threshold: This parameter determines minimum signal level necessary for the PLL to lock and demodulate an FM signal of given deviation.

In most FM demodulation applications, it is also desirable to control the amplitude of the demodulated output. This feature is provided in some of the PLL circuits (such as the XR-215 and the XR-2212) by means of a variable-gain amplifier contained on the chip.

For low-frequency FM detection (below 300 kHz carrier frequency) the XR-2212 is recommended because of its versatility and temperature stability. For FM demodulation at frequencies above 300 kHz, the XR-215 offers the best performance because of its high frequency capability.

FSK decoding: Frequency-shift keying used in digital communications is very similar to analog FM modulation. Therefore, any PLL IC can be used for FSK decoding, provided that its input sensitivity and the tracking range are sufficient for a given FSK signal deviation. Some of the basic requirements and desirable features for a PLL used in FSK decoding are:

- ☐ Center frequency stability.
- ☐ Logic compatible output.
- ☐ Control of VCO conversion gain.

Center frequency stability is essential to insure that the VCO frequency range stays within the signal band over the operating temperature range. A logic compatible output is desirable to avoid the need for an external voltage comparator (slicer) to square the output pulses. It is particularly convenient if the output conforms to RS-232C standard, thereby eliminating the need for a separate line-driver circuit. Control of the VCO's conversion gain allows the circuit to be used for both large deviation FSK signals (such as 1200 baud operation) as well as for small deviation (75 baud) FSK signals.

For FSK decoding at low frequencies (i.e., below 300 kHz) the XR-2211 is by far the optimum circuit to use because of its frequency stability and carrier-detect capability. For FSK detection at higher frequencies (up to 10 MHz) the XR-210 is the recommended circuit.

Frequency synthesis: This application requires a PLL circuit with the loop opened between the VCO output and the phase comparator input, so that an external frequency divider can be inserted into the feedback loop of the PLL. This requirement is satisfied by XR-S200, XR-210, XR-215 and the XR-2212 PLL circuits.

For frequency synthesis at low frequencies (i.e., with maximum output frequency less than 300 kHz) the XR-2212 is by far the best suited circuit since it has the best VCO stability and interfaces easily with all logic families. For operation above 300 kHz, either the XR-210 or the XR-215 PLL IC's can be used for frequency synthesis; however the XR-215 offers the highest frequency capability.

Signal conditioning: Most signal conditioning applications require very narrow-band operation of the PLL. This in turn may require the use of active filters within the loop (between the phase detector and the VCO). The PLL circuits which allow active filers to be inserted into the loop are the XR-S200 and the XR-2212. Both of these circuits already contain an op. amp. on the chip for active filtering. For low frequencies (i.e. below 300 kHz) the XR-2212 is the best suited circuit because of its adjustable tracking bandwidth and excellent frequency stability. For higher frequencies the XR-S200 is the recommended circuit.

Tone decoding: The PLL circuits especially designed for this application are the XR-567, the XR-L567, the XR-2567 and the XR-2211. The XR-2211 offers the highest frequency stability among the three circuits and independent control of system bandwidth and response time. The XR-567 has a relatively high input threshold (≈ 20 mV, rms) and may require input preamplification; however it requires fewer external components than the XR-2211. The XR-2567, which contains two independent 567-type tone decoders on the same chip may be more economical to use in multiple-tone detection systems.

AM detection: The PLL can be converted to a synchronous AM detector with the addition of a non-critical phase-shift network, an analog multiplier and a low-pass filter. The system block diagram for this application is shown in Figure 5.

In this application, as the PLL tracks the carrier of the input signal, the VCO regenerates the unmodulated carrier and feeds it to the reference input of the multiplier section. In this manner, the system functions as a synchronous demodulator with the filtered output of the multiplier representing the demodulated audio information.

Tone detection: In this application, the PLL is again connected as shown in Figure 5. When a signal tone is present at the input, within a frequency band corresponding to the capture range of the PLL, the output dc voltage is shifted from its tone-absent level. This shift is easily converted to a logic signal by adding a threshold detector with logic-compatible output levels.

Motor speed control: Many electromechanical systems, such as magnetic tape drives and disc or drum head drivers, require precise speed control. This can be achieved using a PLL system, as shown in Figure 6. The VCO section of the monolithic PLL is separated from the phase-comparator and used to generate a voltage controlled reference frequency, f_R. The motor shaft and the tachometer output provide the second signal, frequency f_M, which is compared to the reference frequency. The controller is a power amplifier which drives the speed-control windings of the motor. Thus, the motor and tachometer combination essentially functions as a VCO which is phase locked to the voltage controlled reference frequency, f_R.

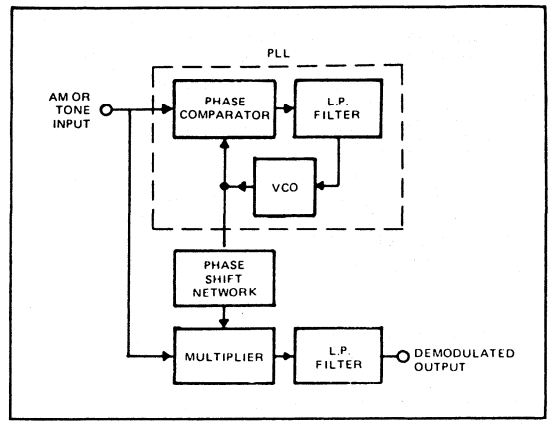


Figure 5. AM and tone detection are possible by adding three functional blocks to the basic phase locked loop.

Stereo decoding: In commercial FM broadcasting, suppressed carrier AM modulation is used to superimpose the stereo information on the FM signal. To demodulate the complex stereo signal, low-level pilot tone is transmitted at 19 kHz (1/2 of actual carrier frequency). The PLL can be used to lock onto this pilot tone, and regenerate a coherent 38 kHz carrier which is then used to demodulate the complete stereo signal. A number of highly specialized monolithic circuits have been developed for this application. A typical example of monolithic stereo decoder circuits using the PLL principle is the XR-1310 stereo demodulator IC.

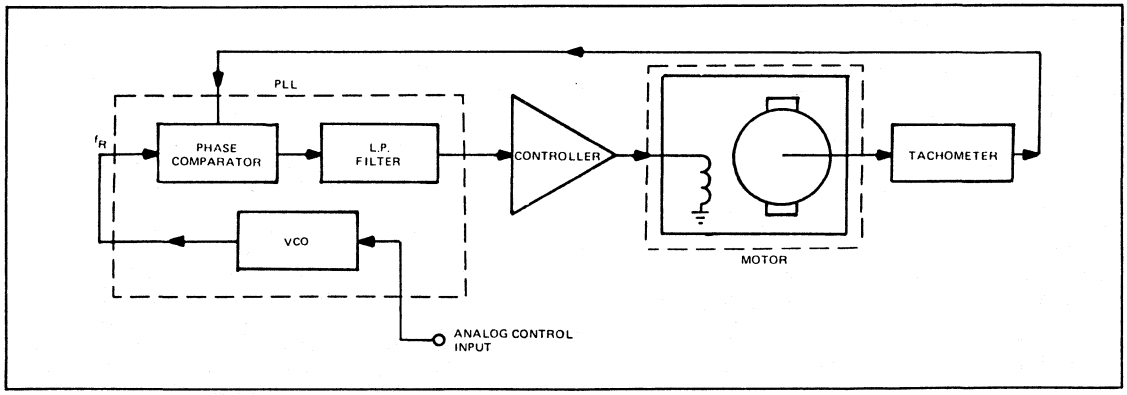


Figure 6. Very precise motor speed control is possible with a phase locked loop system of this type.

Table 1.
Major Applications for Exar's PLL Circuits

Major Application	Part Number							
	XR-S200	XR-210	XR-215	XR-2211	XR-2212	XR-567	XR-L567	XR-2567
FM Demodulation	√	√	√					
High Frequency			√		√			
Low Frequency			√		√			
Frequency Synthesis								
High Frequency	√	√	√					
Low Frequency		√	√		√			
FSK Demodulation		√		√				
Signal Conditioning	√				√			
Tone Detection				√		√	√	√
Motor Speed Control	√				√			
Data Synchronization			√		√			
Low Power Operation							√	

5

Table 2. A Summary of Exar's PLL Circuits

Product Designation	Package	Operating Supply Range	High Frequency Limit	VCO Stability		Primary Applications
				Power Supply	Temp. (ppm/°C)	
XR-S200	24 Pin DIP	6V to 30V ±3V to ±15V	30 mHz	0.08 (typ) 0.5 (max)	300 (typ) 650 (max)	Multi-function building block for FM/FSK detection, frequency systhesis
XR-210	16 Pin DIP	5V to 26V	20 mHz	0.05 (typ) 0.5 (max)	200 (typ) 550 (max)	FSK modem, frequency synthesis, data synchronization
XR-215	16 Pin DIP	5V to 26V	35 mHz	0.1 (typ) 0.5 (max)	250 (typ) 600 (max)	General purpose PLL. FM detection, tracking filter, frequency synthesis
XR-2211	16 Pin DIP	4.5V to 20V	300kHz	0.05 (typ) 0.5 (max)	±20 (typ) ±50 (max)	FSK demodulatio. tone decoding, carrier detection
XR-2212	16 Pin DIP	4.5V to 20V	300kHz	0.05 (typ) 0.5 (max)	±20 (typ) ±50 (max)	Frequency synthesis, FM detection, data synchronization, tracking filter
XR-567	8 Pin DIP	4.75V to 9V	500kHz	0.5 (typ) 1 (max)	±140 (typ)	Tone detection
XR-L567	8 Pin DIP	4.75V to 9V	50kHz	0.5 (typ) 2 (max)	-150 ppm (typ)	Tone detection low-power equivalent of XR-567
XR-2567	16 Pin DIP	4.75V to 15V	600kHz	0.05 (typ) 0.2 (max)	±100 (typ	Dual tone decoder (Dual tone equivalent

Fundamentals of Monolithic Waveform Generation and Shaping

INTRODUCTION

Waveform or function generators find a wide range of applications in communications and telemetry equipment, as well as for testing and calibration in the laboratory. In most of these applications, commercially-available monolithic IC oscillators and function generators provide the system designer with a low-cost alternative to conventional, non-integrated units costing several hundred dollars or more.

The fundamental techniques of waveform generation and shaping are well suited to monolithic IC technology. In fact, monolithic integrated circuits offer some inherent advantages to the circuit designer, such as the availability of a large number of active devices and close matching and thermal tracking of component values. By making efficient use of the capabilities of integrated components and the batch-processing advantages of monolithic circuits, it is now possible to design integrated waveform generator circuits that can provide a performance comparable to that of complex discrete generators, at a very small fraction of the cost. This article provides a brief review of the fundamental principles of monolithic waveform generation and wave-shaping methods.

Basics of IC Waveform Generation

Essentially a waveform generator is a stable oscillator circuit that outputs well-defined waveforms; and, these can be externally modulated or swept over a frequency range. A waveform generator usually consists of four sections: (1) an oscillator to generate the basic periodic waveform; (2) a wave-shaper; (3) an optional modulator section to provide AM capability, and (4) an output buffer amplifier to provide the necessary load drive.

Figure 1 shows a simplified generator using the four functional blocks. Each block can be built readily in monolithic form with established linear IC technology. Hence fabrication of all four blocks on a single monolithic chip has evolved as a natural extension of earlier circuits.

The oscillator, usually a relaxation type, can generate linear, triangle or ramp waveforms. The usual technique involves constant-current charging and discharging of an external timing capacitor. Figure 2 shows a typical, though simplified, example: an emitter-coupled multivibrator circuit, which can generate a square wave as well as a triangle or a linear ramp output.

The circuit's operation is as follows: At any given time, either Q_1 and D_1 or Q_2 and D_2 are conducting such that capacitor C_O is alternately charged and discharged by constant-current I_1. The output across D_1 and D_2 corresponds to a symmetrical square wave, having a pk-pk amplitude of $2V_{BE}$, or twice the transistor base-emitter voltage drop. Output V_A, constant when Q_1 is on, becomes a linear ramp with a slope equal to $-I_1/C_O$ goes off. Except for a half cycle delay, output $V_B(t)$ is the same as $V_A(t)$.

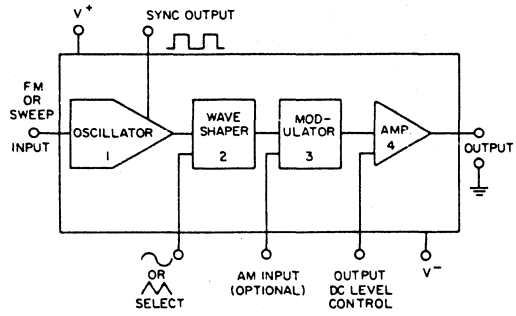


Figure 1. Basically, a waveform generator consists of four sections. Each section can be built readily in monolithic form with established IC technology.

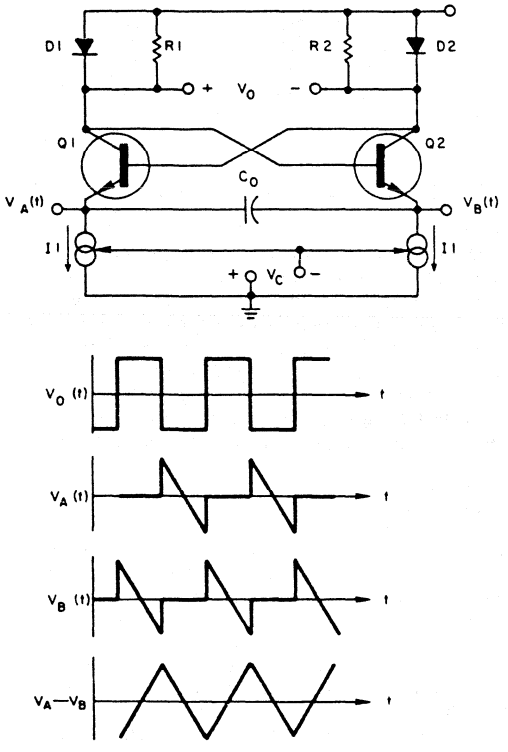


Figure 2. A simple oscillator circuit can be used to generate square, ramp and triangle waveforms.

Both linear ramp waveforms have pk-pk amplitudes of $2V_{BE}$. Their frequency of oscillation, f_O, can be determined from the formula

$$f_O = \frac{I_1}{4V_{BE}C_O}.$$

And f_O can be controlled by variation of charging-current I_1 via control voltage V_C. A subtraction of one output ramp voltage from the other, by use of a simple differential amplifier, obtains the linear triangular waveform.

Symmetry of triangle and square-wave outputs may be adjusted by replacement of one of the two current sources in Figure 2 by I_2, where $I_2 \neq I_1$. Then the duty cycle of the output waveforms becomes the following:

$$\text{Duty Cycle} = 50\frac{I_1}{I_2}\%.$$

The duty cycle of the output may be varied over a wide range by varying the ratio of the currents I_1 and I_2.

Wave-Shaping Techniques

The most useful waveform in signal processing applications is the sine wave. In the design of function generators, sinusoidal output is normally obtained by passing a triangular wave through a wave shaping circuit. In most discrete-component generators, wave-shaping involves a diode-resistor or a transistor-resistor ladder network. Introduction of a finite number of "break points" on the triangle wave changes it to a lower distortion sine wave.

Although this method can also be adapted to monolithic circuits, it is not as practical because it requires extremely tight control of resistor values and diode characteristics. A simpler, and more practical, sine shaper for monolithic circuits employs the "gradual cutoff" characteristics of a basic differential gain stage, as in Figure 3.

Reduction of the emitter = degeneration resistance, R_E, allows either transistor Q_3 or Q_4 to be brought near their cutoff point when the input triangle waveform reaches its peaks. For the proper choice of the input amplitude and bias-current levels, the transfer characteristics at the peaks of the input triangle waveform become logarithmic rather than linear. Thus, the peaks of the triangle become rounded, and the output appears as a low distortion sine wave.

Use of this technique permits output harmonics to be reduced to less than 0.5% with only a single adjustment. The low distortion is possible because the technique relies on component matching rather than their absolute values. Since monolithic ICs can be designed readily for close matching, this wave-shaping is ideally suited to monolithic design.

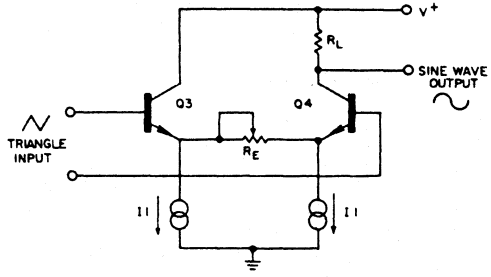


Figure 3. Conversion of triangle to sine wave employs a differential gain stage, which avoids dependence on absolute values of components.

Phase-Locked Loop Design

The current-controlled or voltage-controlled oscillator (VCO) is one of the essential components of a phase-locked loop (PLL) system. The key requirement for this application is that the oscillator should have a high degree of frequency stability and linear voltage or current-to-frequency conversion characteristics. Sinusoidal output, although often useful, is generally not required in this application.

Although all of Exar's IC oscillators can be used as a VCO in designing PLL systems, the XR-2207 or its low-cost and simplified version, the XR-2209, are often the best suited devices for this application. For additional information refer to Application Note AN-06, entitled "Precision PLL System Using the XR-2207 and the XR-2208" included in this Data Book.

Sweep Oscillator

A sweep oscillator is required to have a large linear sweep range. Among Exar's function generators, the XR-2207 and the XR-2206 have the widest linear sweep range (over 1000:1), and are best suited for such an application.

By using a linear ramp output from the XR-2207 to sweep the frequency of the XR-2206, one can build a two-chip sweep oscillator system which has a 2000:1 sweep range and sinusoidal output.

Low-Cost General Purpose Oscillator

In many digital design applications, one needs a stable, low-cost oscillator IC to serve as the system clock. For such applications, the XR-2209 precision oscillator is a logical design choice since it is a simple, low-cost oscillator circuit and offers 20 ppm/°C frequency stability.

The monolithic timer circuits, such as 555 types or the micropower version, the XR-L555, can also be used as low-cost, general purpose oscillators by operating them in their free-running, i.e., self-triggering mode.

Ultra-Low Frequency Oscillator

In certain applications such as interval-timing or sequencing, stable, ultra-low frequency oscillators which can operate at frequencies of 0.01 Hz or lower are required. Among Exar's oscillator circuits, the IC most suited to such an application is the XR-8038 since it can operate with a polarized electrolytic capacitor as its timing component. All other oscillator circuits described in this book require non-polar timing capacitors, and therefore are not pratical for ultra-low frequency operation.

An alternate approach to obtaining stable ultra-low frequency oscillators is to use the XR-2242 counter/timer as an oscillator in its free-running mode. Such a circuit generates a square wave output with a frequency of 1/256 RC where R and C are the external timing component value.

CHOOSING THE RIGHT IC OSCILLATOR

At the onset of his/her design, the user of monolithic oscillator products is faced with the key question of choosing the oscillator or the function generator best suited to his application. The broad line of function generator products offered by Exar covers a wide range of applications. It is often difficult to determine at a glance the best circuit for a given application. The purpose of this section is to review some of the key performance requirements, from an applications point of view, and help answer the question. "What is the best IC oscillator for the job?

Sine Wave Generation

In evaluating the output characteristics of sinusoidal IC oscillators, total harmonic distortion (THD) of the output waveform is usually the key performance criteria. In a number of voice-grade telecommunication or laboratory applications, sine wave distortion of 2% to 3% may be tolerable. However, for audio-quality signals, distortion level of 1% or less is required. Furthermore, it is desirable that the output distortion should be relatively independent of the output amplitude, frequency or temperature changes; and that the distortion level be minimized with a minimum amount of external adjustments.

Exar manufactures three separate families of IC oscillators which provide sinusoidal output waveforms. These are the XR-205, XR-2206 and the XR-8038. All of these circuits require external trimming to minimize the output distortion. In the case of XR-205, the untrimmed distortion is about 5%; in the case of the XR-2206 and the XR-8038, untrimmed distortion is typically less than 2%, and can be reduced to 0.5% with additional trimming.

For low frequency sine wave generation (below 100 kHz), the XR-2206 and the XR-8038 are the recommended circuits. The XR-8038 has a fixed output level, whereas the XR-2206 offers separate output dc level and amplitude adjustment capability.

AM Generation

Linear modulation of output amplitude by means of an analog control signal is a desirable feature for telemetry and data transmission applications. In monolithic IC

oscillators, this capability is normally obtained by including a four-quadrant transconductance multiplier on the IC chip. Both the XR-205 and the XR-2206 circuits have such a feature included on the chip and can be used for generating sinusoidal AM signals. They can operate both in suppressed-carrier or conventional double-sideband AM generator mode. For operation with frequencies below 100 kHz, the XR-2206 has superior performance characteristics over the XR-205.

FM Generation

Essentially all of Exar's IC oscillator circuits can be used for generating frequency-modulated waveforms. For small frequency deviations (i.e., ±5% or less) about the center frequency, all of these oscillators have FM nonlinearity of 0.1% or less. However, if wider FM deviations are required the XR-2209, XR-2207 and the XR-2206 offer the best FM linearity.

FSK Generation

Frequency-shift keying (FSK) is widely used in data communications, particularly in data-interface or MODEM systems. In monolithic IC oscillators, FSK capability is obtained by using a current-controlled oscillator and keying its control current between two or more programmed levels which are set by external resistors. This results in output waveforms which are phase-continuous during the frequency transitions between the "mark" and "space" frequencies.

The XR-2207 can produce four discrete frequencies, set by one external capacitor and four setting resistors. Frequency keying between these four frequencies is achieved by a two-bit binary logic input. The circuit produces both triangle and square wave outputs. The XR-2206 produces two discrete frequencies, f_1 and f_2, and has a one-bit keying logic input. The key advantage of XR-2206 over the XR-2207 in FSK MODEM design is the availability of a sinusoidal output waveform.

Exar has compiled a comprehensive application note describing the use of both of these IC products in the design of FSK MODEM systems. This application note (AN-01) entitled "Stable FSK MODEMs Featuring the XR-2207, XR-2206 and the XR-2211" is also included in this Data Book.

Laboratory Function Generator

One of the main applications for oscillators is for laboratory or test instrumentation or calibration where a variety of different output waveforms are required. Such applications require both AM./FM modulation capability, linear frequency sweep and sinusoidal output. The circuit fitting this application the best is the XR-2206. It has all the fundamental features of a complete function generator system.

A comprehensive description of building a self-contained laboratory-quality function generator system using the XR-2206, Application Note AN-14, is included in this Data Book.

Fundamentals of Operational Amplifiers

The "ideal" operational amplifier can be defined as a voltage-controlled voltage amplifier circuit which offers infinite voltage gains with an infinite input impedance, zero output impedance, and infinite bandwidth. The advantage of such an idealized block of gain is that one can perform a large number of mathematical "operations", or generate a number of circuit functions by applying passive feedback around the amplifier.

The key features of operational amplifier application can be illustrated using the simple feedback circuit of Figure 1, and assuming that the operational amplifier has infinite gain and infinite input impedance. Then, the following two conditions have to be satisfied:

a) Since the voltage gain is infinite, the net voltage across the input terminals of the operational amplifier must be zero, if the operational amplifier output voltage is to be finite. In the circuit of Figure 1, this causes the inverting input terminal of the operational amplifier to behave as a "virtual ground".

b) Since the input impedance of the ideal operational amplifier is infinite, no input current is drawn by the operational amplifier, the total current going into the circuit node connected to the inverting input of the operational amplifier (node Q in Figure 1) must be equal to the total current coming out, i.e.:

$$I_S = -I_F \text{ and } \frac{V_{IN}}{R_S} = -\frac{V_O}{R_F} \qquad (1)$$

Solving for the overall voltage gain, one obtains:

$$A_V = \frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_S} \qquad (2)$$

Because of this property, the noninverting input of an operational amplifier is often referred to as its "summing input".

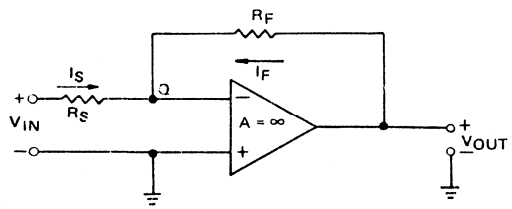


Figure 1. The "Ideal" Operational Amplifier as a Feedback Amplifier

In the case of actual operational amplifiers, both the voltage gain and the input impedance are quite high, but still finite. Figure 2 shows the same basic feedback circuit assuming that the amplifier now has a finite input resistance, R_{IN}, and a finite voltage gain A. For simplicity, the output impedance of the operational amplifier is assumed to be negligible. The overall voltage gain of the circuit can now be expressed as:

$$A_V = V_{OUT}/V_{IN} = -\frac{R_F}{R_S}\left[\frac{1}{1+\frac{1}{A}(1+R_F/R_S+R_F/R_{IN})}\right] \qquad (3)$$

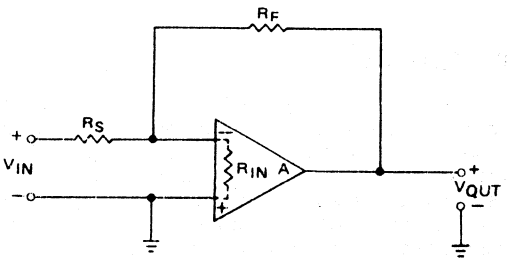


Figure 2. Basic Feedback Configuration Using an Operational Amplifier With Finite Input Impedance and Gain

It should be noted that, for large values of R_{IN}, as the voltage gain increases (i.e. $A \rightarrow \infty$), this expression rapidly converges to that given in equation 2; and the circuit performance becomes solely determined by the external components.

In addition to having finite gain and input impedance, an actual operational amplifier circuit also has finite input bias currents as well as input offset voltage and currents. A more complete model of a practical operational amplifier is shown in Figure 3 where I_B indicates the finite input bias currents; V_{io} and I_{io} represent the voltage and current offsets associated with the circuit and R_O is the output resistance. Due to non-zero values of V_{io} and I_{io} in a practical operational amplifier circuit, $V_{OUT} \neq 0$ for $V_{IN} = 0$.

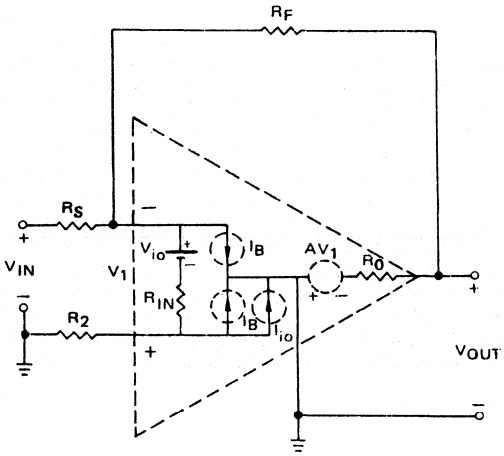


Figure 3. Equivalent Circuit of a Practical Operational Amplifier Showing the Effects of Finite Input Impedance, Current and Voltage Offsets

DEFINITIONS OF OP-AMP PARAMETERS

Since the operational amplifier has become a universal building block for circuit and system design, a number of widely accepted design terms have evolved which describe the comparative merits of various operational amplifiers. Some of these terms are defined below:

Input Offset Voltage: The input voltage which must be applied across the input terminals to obtain zero output voltage.

Input Offset Current: The difference of the currents into the two input terminals with the output at zero volts.

Input Bias Current: The average of the two input currents.

Input Common-Mode Range: Maximum range of input voltage that can be simultaneously applied to both inputs without causing cutoff or saturation of amplifier gain stages.

Common-Mode Rejection Ratio: Ratio of the differential open-loop gain to the common-mode open-loop gain.

Supply Voltage Rejection Ratio: Input offset voltage change per volt of supply voltage change.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output at zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Full-Power Bandwidth: Maximum frequency over which the full output voltage swing can be obtained.

Unity-Gain Bandwidth: Frequency at which the open loop voltage gain is equal to unity.

Slew Rate: The maximum time rate of change of the output voltage, for a voltage step applied to the input. It is normally measured at the zero crossing point of the output voltage swing with the amplifier frequency compensated for unity gain.

Overload Recovery Time: Time required for the output stage to return to active region, when driven into hard saturation.

Gain Margin: The amount by which the voltage gain is below the unity (0 dB) level, at the frequency where the *excess* phase shift across the amplifier is exactly 180°. It is measured in decibels, and must be positive for unconditional stability.

Phase Margin: 180° minus the excess phase shift at the Frequency where the magnitude of the open loop voltage gain is equal to unity. It is measured in degrees and must be positive for unconditional stability.

APPLICATIONS OF OP-AMPS

The general usefulness of the operational amplifier stems from the fact that when used in a feedback loop, its overall performance and transfer characteristics are determined almost totally by the choice of feedback components. To be universally useful in such an application, the "ideal" operational amplifier should exhibit infinite gain, infinite input impedance and infinite bandwidth. Although these are all idealized characteristics, the practical monolithic operational amplifiers closely approximate these features, particularly for low frequency applications.

The availability and the low-cost of the integrated operational amplifier makes it an extremely versatile building block for analog system or equipment design. Therefore, it is mandatory that the circuit designer be familiar with the fundamental applications of operational amplifiers. This section is intended to familiarize the designer with some of the simple but fundamental circuit configuration using IC operational amplifiers. The discussion is slanted toward the practical applications of operational amplifiers, as controlled by the external feedback circuitry. The particular operational amplifier parameters will be discussed as they effect the circuit performance and accuray.

The integrated operational amplifiers shown in the figures are for the most part internally compensated, so frequency stabilization components are not shown: however, other amplifiers using external compensation may be utilized to achieve greater operating speed in many circuits.

The Inverting Amplifier

The basic operational amplifier circuit is shown in Figure 1. This circuit gives closed-loop gain of R_2/R_1 when this ratio is small compared with the amplifier open-loop gain and, as the name implies, is an inverting circuit. The input impedance is equal to R_1. The closed-loop bandwidth is equal to the unity-gain frequency divided by one plus the closed-loop gain.

The only cautions to be observed are that R_3 should be chosen to be equal to the parallel combination of R_1 and R_2 to minimize the offset voltage error due to bias current; and that there will be a DC offset voltage error due to bias current; and that there will be a DC offset voltage at the amplifier output equal to closed-loop gain times the offset voltage at the amplifier input.

Offset voltage at the input of an operational amplifier is comprised of two components, these components are identified in specifying the amplifier as input offset voltage and input bias current. The input offset voltage is fixed for a particular amplifier; however, the contribution due to input bias current is dependent on the circuit configuration used. For minimum offset voltage at the amplifier input without circuit adjustment, the source resistance for both inputs should be equal. In this case, the maximum offset voltage would be the algebraic sum of amplifier offset voltage and the voltage drop across the source resistance due to offset current. Amplifier offset voltage is the predominant error term for low source resistances, and offset current causes the main error for high source resistances.

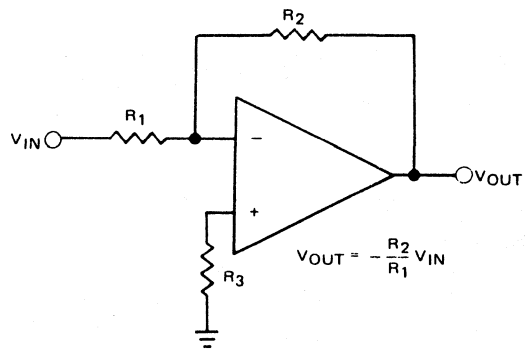


Figure 1. inverting Amplifier

In high source resistance applications, offset voltage at the amplifier output may be adjusted by adjusting the value of R_3 and using the variation in voltage drop across it as an input offset voltage trim.

Offset voltage at the amplifier output is not as important in AC coupled applications. Here the only consideration is that any offset voltage at the output reduces the peak-to-peak linear output swing of the amplifier.

The gain-frequency characteristic of the amplifier and its feedback network must be such that oscillation does not occur. To meet this condition, the phase shift through amplifier and feedback network must never ex-

ceed 180° for any frequency where the combined gain of the amplifier and its feedback network is greater than unity. In practical applications, the phase shift should not approach 180° since this is the situation of conditional stability. Obviously, the most critical case occurs when the attenuation of the feedback network is zero.

Amplifiers which are not internally compensated may be used to achieve increased performance in circuits where feedback network attenuation is high, i.e., the amount of feedback around the amplifier is low. The compensation trade-off for a particular connection is stability versus bandwidth. Larger values of compensation capacitor yield greater stability and lower bandwidth and vice versa.

The Non-Inverting Amplifier

Figure 2 shows a high input impedance non-inverting circuit. This circuit gives a closed-loop gain equal to the ratio of (R_1 + R_2) to R_1. Its closed-loop 3-dB bandwidth is equal to the amplifier unity-gain frequency divided by the closed-loop gain.

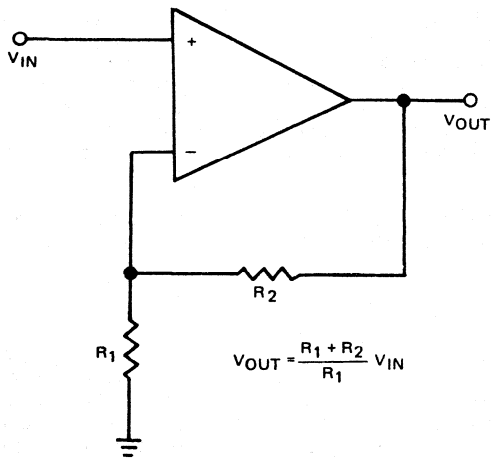


Figure 2. Non-Inverting Amplifier

The primary differences between this connection and the inverting circuit are that the output is not inverted and that the input impedance is very high and is equal to the differential input impedance multiplied by loop gain (open-loop gain/closed-loop gain). In DC coupled applications, input impedance is not as important as input current and its voltage drop across the source resistance. To minimize the output error due to the input bias current of the operational amplifier, (R_1 + R_2) should be chosen equal to the source impedance of the input signal. Applications cautions are the same for this amplifier as for the inverting amplifier with one exception: the amplifier output will go into saturation if the input is allowed to float. This may be important if the amplifier must be switched from source to source. The compensation trade off discussed for the inverting amplifier is also valid for this connection.

The Unity-Gain Buffer

The unity-gain buffer is shown in Figure 3. The circuit gives the highest input impedance of any operational amplifier circuit. Input impedance is equal to the differential input impedance multiplied by the open-loop gain, in parallel with common mode input impedance. The gain error of this circuit is equal to the reciprocal of the amplifier open-loop gain or to the common-mode rejection, whichever is less. Input impedance is a misleading concept in a DC coupled unity-gain buffer. Bias current for the amplifier will be supplied by the source resistance and will cause an error at the amplifier input due to its voltage drop across the source resistance.

The cautions to be observed in applying this circuit are as follows: the amplifier must be compensated for unity-gain operation, and the output swing of the amplifier may be limited by the amplifier common-mode range. The input signal swing should not exceed the input common-mode range, since this may cause a latch-up condition.

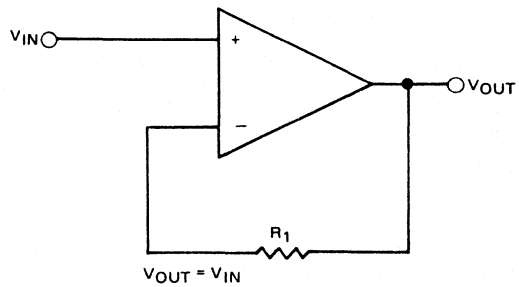


Figure 3. Unity-Gain Buffer

Summing Amplifier

The summing amplifier, a special case of the inverting amplifier, is shown in Figure 4. The circuit gives an inverted output which is equal to the weighted algebraic sum of all three inputs. The gain of any input of this circuit is equal to the inverse ratio of the appropriate input resistor to the feedback resistor, R_4. Amplifier bandwidth may be calculated as in the inverting amplifier shown in Figure 1 by assuming the input resistor to be the parallel combination of R_1, R_2, and R_3. Application cautions are the same as those for the inverting amplifier. If an uncompensated amplifier is used, compensation is calculated on the basis of this bandwidth as is discussed in the section describing the simple inverting amplifier.

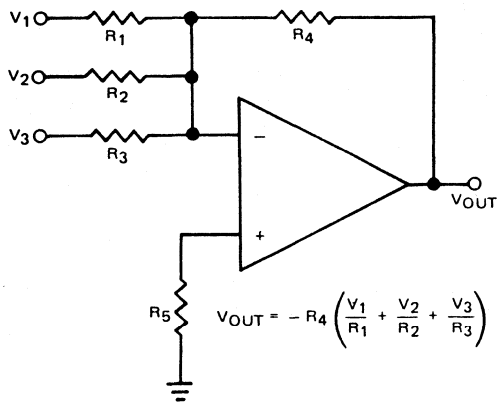


Figure 4. Summing Amplifier

The advantage of this circuit is that there is no interaction between inputs, therefore, operations such as summing and weighted-averaging are implemented very easily.

The Difference Amplifier

The difference amplifier is the complement of the summing amplifier and allows the subtraction of two voltages or, as a special case, the cancellation of a single common to the two inputs. This circuit is shown in Figure 5 and is useful as a computational amplifier, in making a differential to single-ended conversion, or in rejecting an unwanted common-mode signal.

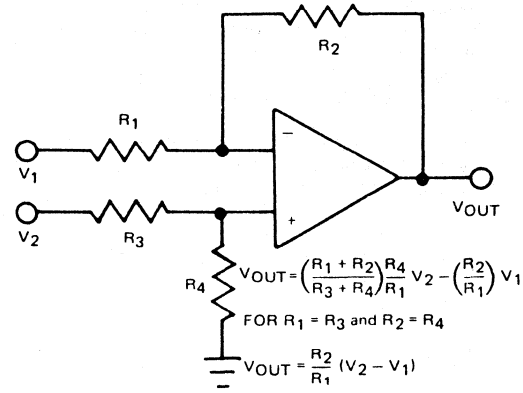


Figure 5. Difference Amplifier

Circuit bandwidth may be calculated in the same manner as for the inverting amplifier, but input impedance is somewhat more complicated. Input impedance for the two inputs is not necessarily equal: inverting input impedance is the same as for the inverting amplifier of Figure 1 and the noninverting input impedance is the sum of R_3 and R_4. Gain for either input is the ratio of R_1 to R_2 for the special case of a differential input single-ended output where $R_1 = R_3$ and $R_2 = R_4$. The general expression for gain is given in the figure. Compensation should be chosen on the basis of amplifier bandwidth.

Care must be exercised in applying this circuit since input impedances are not equal for minimum bias current error.

Differentiator Circuit

The basic principle of a differentiator circuit is shown in the simplified connection diagram of Figure 6. However, although mathematically accurate, this particular connection is not directly useful in practice because it is extremely susceptible to high frequency noise since AC gain increases at the rate of 6 dB per octave. In addition, the feedback network of the differentiator made up of the resistor R_3 and the capacitor C_3 is an RC low pass filter which contributes 90° phase shift to the loop and may cause stability problems even with an amplifier which is compensated for unity-gain.

A practical differentiator which corrects the high frequency noise problem is shown in Figure 7. Here both the stability and noise problems are corrected by addition of two additional components, R_1 and C_2. R_2 and C_2 form a 6 dB per octave high frequency roll-off in the feedback network, and R_1C_1 form a 6 dB per octave roll-off network in the input network for a total high frequency roll-off of 12 dB per octave, to reduce the effect of high frequency input and amplifier noise. In addition R_1C_1 and R_2C_2 form lead networks in the feedback loop which, if placed below the amplifier unity-gain frequency, provide 90° phase lead to compensate the 90° phase lag of R_2C_1 and prevent loop instability.

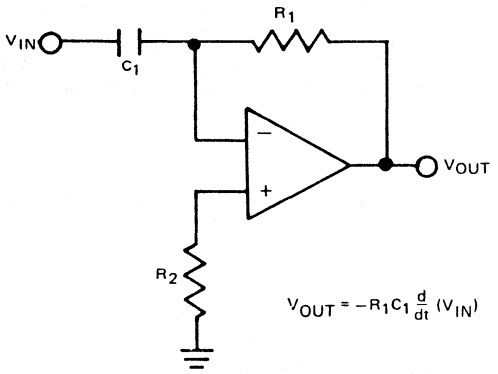


Figure 6. Basic Differentiator Connection

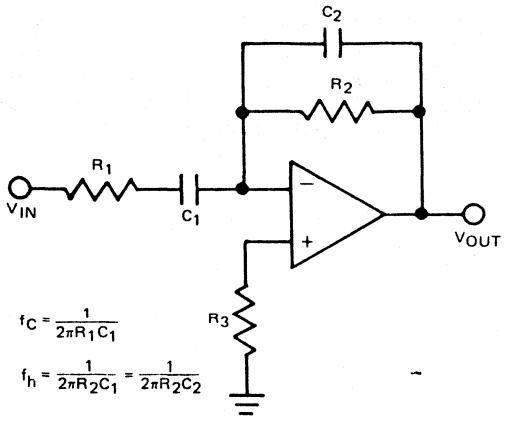


Figure 7. Practical Differentiator Circuit

Integrator Circuit

Figure 8 shows the basic circuit connection for performing the mathematical operation of integration. This circuit is essentially a low-pass filter with a constant frequency roll-off of −6 dB per octave.

The circuit must be provided with an external method of establishing initial conditions. This is shown in the figure as the double-pole, single-throw switch S_1. When S_1 is in position 1, the amplifier is connected in unity-gain configuration, and capacitor C_1 is discharged, setting an initial condition of zero volts. When S_1 is in position 2, the amplifier is connected as an integrator, and its output will be the time-integral of the input voltage.

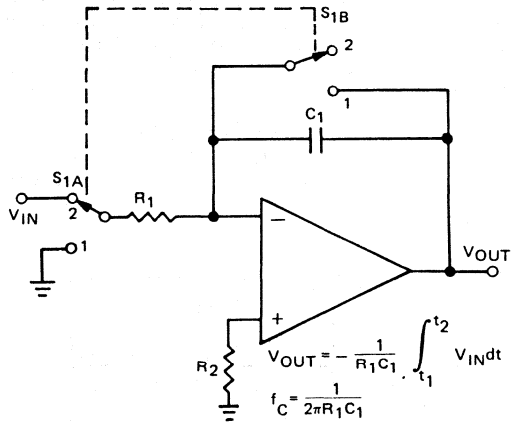


Figure 8. The Integrator Circuit

The cautions to be observed with this circuit are two: the amplifier used should generally be stabilized for unity-gain operation and R_2 must equal R_1 for minimum error due to bias current.

Simple Low-Pass Filter

The simple low-pass filter is shown in Figure 9. This circuit has a 6 dB per octave roll-off after a closed-loop 3-dB point defined by f_C. Gain below this corner frequency is defined by the ratio of R_3 to R_1. The circuit may be considered as an AC integrator at frequencies well above f_C; however, the time domain response is that of a single RC rather than an integral.

A gain vs. frequency plot of circuit response is shown in Figure 10 to illustrate the difference between this circuit and the true integrator. Note that the frequency response is flat for frequencies below f_C

$$\text{where } f_C = \frac{1}{2\pi R_3 C_1}$$

Current-to-Voltage Converter

Current may be measured in two ways with an operational amplifier: the current may be converted into a voltage with a resistor and then amplified or it may be injected directly into a summing node. Converting into voltage is undesirable for two reasons: first, an impedance is inserted into the measuring line causing an error; second, amplifier offset voltage is also amplified with a subsequent loss of accuracy. The use of a current-to-voltage converter avoids both of these problems.

The current-to-voltage converter is shown in Figure 11. The input current is fed directly into the summing note, and the amplifier output voltage changes to extract the same current from the summing node through R_1. The

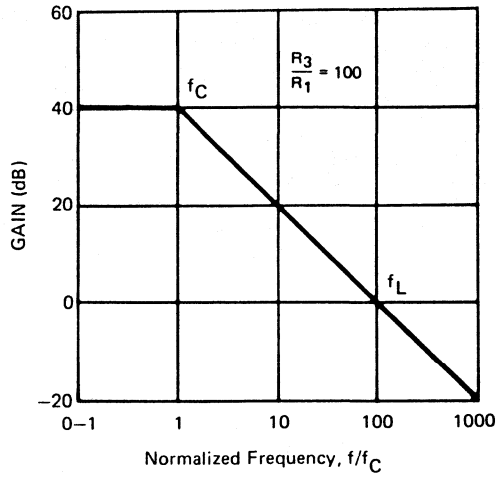


Figure 10. Frequency Response of the Simple Low-Pass Filter

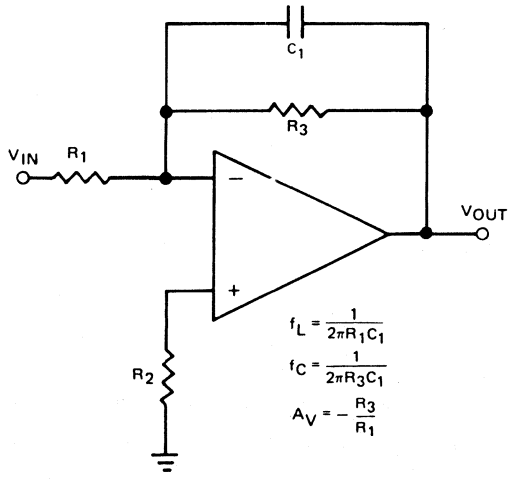


Figure 9. A Simple Low-Pass Filter Circuit

scale factor of this circuit is R_1 volts per ampere of current. The only conversion error in this circuit is the bias current of the operational amplifier input which is summed algebraically with the input current, I_{IN}. The main design constraints are that scale factors must be chosen to minimize errors due to bias current and since voltage gain and source impedance are often indeterminate (as with photocells) the amplifier must be compensated for unity-gain operation.

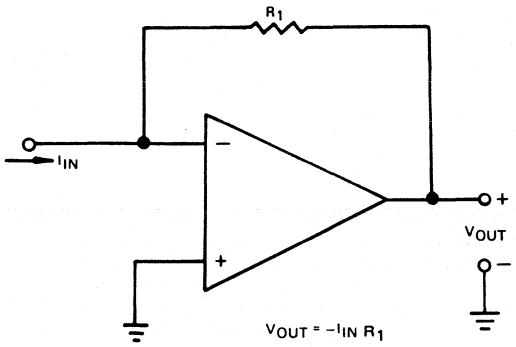


Figure 11. Operational Amplifier as a Current-to-Voltage Converter

Voltage Controlled Current-Source

Figures 12, 13, and 14 show three simple circuit configurations for voltage-controlled constant-current stages. The circuit of Figure 12 is a basic current-sink circuit which uses a pair of Darlington connected NPN transistors external to the operational amplifier. Assuming that the base current of T_1 is negligible compared to the controlled current I_0, the current of the output transistors is equal to V_{IN}/R_1.

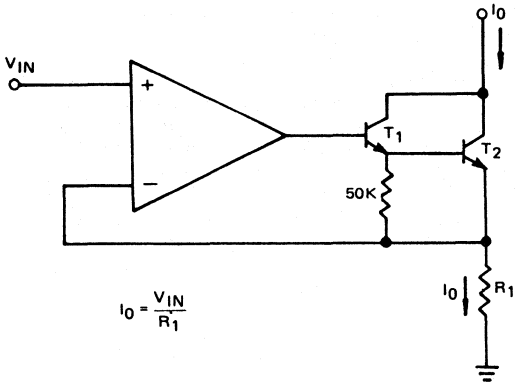


Figure 12. Voltage-Controlled Current-Sink Circuit

Figure 13 shows a current-source circuit which uses a composite connection of external PNP and NPN transistors and produces a constant output current which is proportional to the net voltage drop across the sensing resistor, R_1.

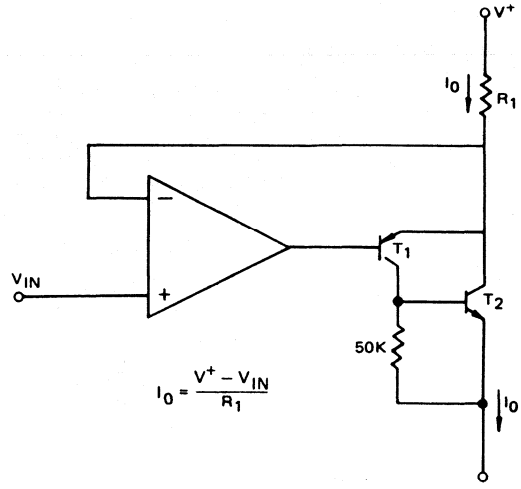


Figure 13. Voltage-Controlled Current-Source Circuit

Figure 14 shows an alternate approach to obtaining a voltage-controlled current source which does not require additional active devices. The circuit provides an output current proportional to the input voltage V_{IN}. If the resistors R_1 through R_4 are chosen to be equal and much larger than R_5, then the output current is:

$$I_{OUT} = V_{IN}/R_5$$

The above expression assumes that the current through R_3 is much smaller than I_0.

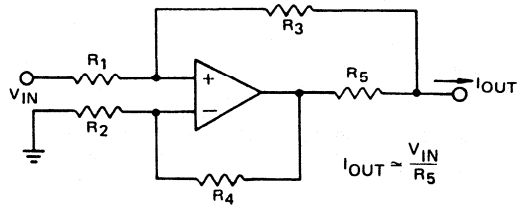


Figure 14. A Voltage-Controlled Current Source Circuit Which Does Not Require External Active Devices

This circuit can supply an output current of either polarity, up to the maximum positive or negative output current available from the operational amplifier. The maximum voltage compliance of the output is limited by the output swing of the operational amplifier minus the voltage drop across the sensing resistor, R_5.

Triangle Wave Oscillator

A constant amplitude triangular wave generator is shown in Figure 15. This circuit provides a variable frequency triangular wave whose amplitude is independent of frequency. This entire circuit can be built inexpensively, using a dual operational amplifier IC, such as the XR-5532.

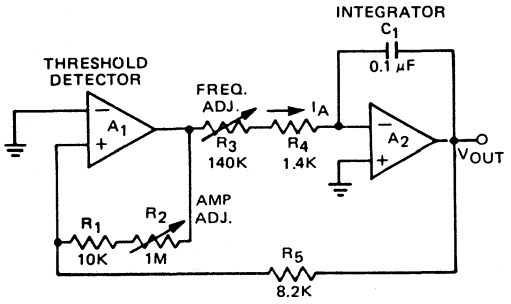


Figure 15. A Simple Triangle Wave Oscillator

The generator embodies an integrator as a ramp generator and a threshold detector with hysteresis as a reset circuit. The integrator has been described in a previous section and requires no further explanation. The threshold detector is similar to a Schmitt trigger in that it is a latch circuit with a large dead zone. This function is implemented by using positive feedback around an operational amplifier. When the amplifier output is in either the positive or negative saturated state, the positive feedback network provides a voltage at the noninverting input which is determined by the attenuation of the feedback loop and the saturation voltage of the amplifier. To cause the amplifier to change states, the voltage at the input of the amplifier must be caused to change polarity by an amount in excess of the amplifier input offset voltage. When this is done, the amplifier saturates in the opposite direction and remains in that state until the voltage at its input again reverses. The complete circuit operation may be understood by examining the operation with the output of the threshold detector in the positive state. The detector positive saturation voltage is applied to the integrator summing junction through the combination R_3 and R_4 causing the current I_A to flow.

The integrator then generates a negative-going ramp with a rate of I_A/C_1 volts per second until its output equals the negative trip point of the threshold detector. The threshold detector then changes to the negative output state, and supplies a negative current, I_B, at the integrator summing point. The integrator now generates a positive-going ramp with a rate of I_B/C_1 volts per second until its output equals the positive trip point of the threshold detector, where the detector again changes output state and the cycle repeats.

Triangular wave frequency is determined by R_3, R_4 and C_1 and the positive and negative saturation voltages of the amplifier A_1. Amplitude is determined by the ratio of R_5 to the combination of R_1 and R_2 and the threshold detector saturation voltages. Positive and negative ramp rates are equal and positive and negative peaks are equal if the detector has equal positive and negative saturation voltages. The output waveform may be offset with respect to ground if the inverting input of the threshold detector, A_1, is offset with respect to ground.

The generator may be made independent of temperature and supply voltage if the detector is clamped with matched zener diodes.

The integrator section should be compensated for unity-gain. The detector section may require compensation if power supply impedance causes oscillation during its transition time. The current into the integrator should be large with respect to the input bias current for maximum symmetry; and offset voltage should be small with respect to peak output voltage swing.

OP-AMP FAMILIES

General Purpose Op-Amps

A wide variety of op-amp applications such as low-frequency amplifiers, active filters, voltage-to-current converters and voltage regulators are most economically accomplished using the low-cost general purpose IC op-amps. These op-amps are almost all variations of the basic 741-type op-amp, and offer significant cost savings over any special-purpose op-amps. They are commercially available in single, dual or quad versions. The dual and quad op-amps are particularly cost-effective for applications such as active filters which require a multiplicity of op-amps. The cost per op-amp is usually lower if one can use multiple op-amp IC's rather than single op-amps.

The single and dual general purpose op-amps are available in both internally compensated and uncompensated versions. The quad op-amps are almost invariably internally compensated, to reduce the IC package pin count. Most general purpose IC op-amps have comparable electrical characteristics, namely open loop gain of $\geq$ 20 mV/V, small-signal unity gain bandwidth of 1 to 2 MHz and a slew rate of $\approx$ 1V/μsec.

Ground Sensing Op-Amps

These types of op-amps have an input stage common-mode range which extends all the way to the negative supply rail. This is obtained by using Darlington-connected PNP transistors at the input stage of the op-amp. The key advantage of this class of op-amps is that they can be operated with a single positive supply, and still be able to detect or sense small signals near ground potential. The particular circuit recommended for this application is Exar's XR-3403 quad operational amplifier.

Programmable Op-Amps

Programmable op-amps allow the user to "program" or set the operating current levels within the IC op-amp by means of an external setting resistor, and thus be able to trade-off power dissipation for slew-rate or signal bandwidth. These circuits are normally available in quad form, where the power levels of all or some of the op-amps in the package can be programmed by one or two external setting resistors. The key areas of applications for programmable op-amps are active filters and telecommunication channel filters where the user is normally concerned with power dissipation. These op-amps can also be programmed to operate at micro-power levels, by the choice of external setting resistors.

The programmable quad operational amplifiers are available with either one or two separate setting controls. Those with a single setting control have all four of the operational amplifiers programmed from same current setting control. Those with two setting controls have the four op-amps on the chip programmed either in groups of two, or in groups of one and three op-amps. The advantage of partitioned programming is that some of the op-amps in the IC package can be operated at a different power or bandwidth level than the rest of the op-amps in the same chip. For example, in an active filter application, the three op-amps performing the filtering can be operated at a low-power level, yet the fourth op-amp which may be serving as an output buffer can be operated at a higher power level to provide load-drive capability. The XR-146/246/346 amps family is an example of this line of op amps.

FET-Input Op-Amps

Finite input impedance or input bias currents associated with conventional bipolar op-amps can be a problem in specific applications such as sample-hold circuits or signal sensing applications from high-impedance signal source such as transducer systems. For such applications, op-amps with junction-FET input stages offer significant performance advantages since they offer input resistances of the order of 10^{12} ohms, and input bias currents in the low pico-ampere range. Another unique feature of FET-input op-amps is their high slew-rate and wide bandwidth. For example, most FET-input op-amps offer slew-rates in excess of 10 V/μsec and unity gain bandwidth of 3 MHz.

The FET-input op-amps offer somewhat higher offset voltages and input noise than all-bipolar op-amps. The XR-062 is an example of such op-amps.

Low Noise Op-Amps

These op-amps are particularly suited for audio amplifier and mixer applications, where low noise is of prime importance. The noise characteristics of an op-amp are determined by the noise generated at the input stage, since the noise generated at this point is amplified by the full open-loop gain of the amplifier. In most cases, input noise voltages of 10 $nV/\sqrt{Hz}$ or less is required to be suitable for high quality or professional audio signal processing applications. Such low noise characteristics are normally obtained by careful device design and manufacturing processing of the IC chips. In general, all-bipolar operational amplifiers tend to have better low noise characteristics than the FET-input op-amps. Exar manufactures a number of low noise op-amp circuits uniquely suited to audio applications. Among Exar's family of low noise op-amps, the XR-5534 operational amplifier, and its dual version, the XR-5532, offer the best noise performance.

Low Distortion Op-Amps

In addition to low noise characteristics, another key performance requirement for audio applications is low distortion. The distortion characteristics of op-amps are normally determined by the design of the output stage as well as the amplifier bandwidth characteristics. The total harmonic distortion (THD) is made up of three components: (a) intermodulation distortion; (b) cross-over distortion which depends on output stage design, and (c) slew-induced distortion which occurs when the output of the op-amp is forced to slew faster than its slew-rate.

The cross-over distortion can be avoided by using op-amps which have class-AB, rather than class-B type output stages. All of Exar's op-amps fall into this category.

To avoid slew-induced distortion, one should ensure that the slew rate of the amplifier is never exceeded during the excursions of the input signal. The high-speed operational amplifiers such as Exar's XR-34072, XR-34074 and XR-5534 op-amps which have slew rates in excess of 10 V/μsec with a power bandwidth of 200 kHz, can easily cover the entire audio frequency range without introducing slew-induced distortion.

Fundamentals of IC Timers

INTRODUCTION

Monolithic timing circuits or *timers* find a wide variety of applications in both linear and digital signal processing. In a large number of industrial control or test sequencing applications, these circuits provide direct and economical replacement for mechanical or electromechanical timing devices.

Monolithic timers generate precise timing pulses, or time delays whose length or repetition rate is determined by an external timing resistor, R, and a timing capacitor, C. The timing interval is proportional to the external (RC) product, and can be varied from microseconds to minutes, days or months, by the choice of the external R and C. Integrated circuit timers can be classified into two categories, based on their principle of operation:

1. **One-Shot or Single-Cycle Timers:** These timer IC's operate by charging an external capacitor with a current set by an external resistor. Upon triggering, the charging cycle happens only *once* during the timing interval. The total timing interval, T, is the time duration necessary for the voltage across the capacitor to reach a threshold value.

2. **Multiple-Cycle or Timer/Counters:** These timer circuits charge and discharge the external timing capacitor, not once, but a *multiple number of times* during the timing interval. The number of times the capacitor is charged and discharged is set by means of a pre-set count, N, stored in a binary counter included on the chip. Thus, the resulting time interval is proportional to N times the external (RC) product.

Both the one-shot and the timer/counter type IC's can be operated in either their monostable or free-running (i.e., self-triggering) mode. They can also be used for sequential timing, clock generation, as well as for pulse-position or pulse-width modulation, as outlined in Table I.

Precision Timing
Time-Delay Generation
Sequential Timing
Pulse Generation/Shaping
Pulse-Position Modulation
Pulse-Width Modulation
Missing-Pulse Detection
Sweep Generation
Pulse Counting
Clock Generation

Table 1. Typical Applications of Monolithic Timers

5

ONE-SHOT OR SINGLE-CYCLE TIMERS

One-shot or single-cycle timers operate by charging a timing capacitor through an external resistor or a current source. The simplest form of the one-shot type timer is the "exponential-ramp generator" circuit shown in Figure 1. Normally all the components except the R and the C shown in the Figure are internal to the IC, and the switch S_1 is a grounded-emitter NPN transistor included in the IC chip.

The operation of the circuit can be briefly explained as follows: In the rest, or reset condition, the switch S_1 is closed; and the voltage across the capacitor is clamped to ground. The timing cycle is initiated by applying an external trigger pulse to "set" the flip-flop and to open the switch S_1 across the timing capacitor. The voltage across the capacitor rises exponentially toward the supply voltage, V_{CC}, with a time-constant of RC. When this voltage level reaches an internally set threshold voltage, V_{REF}, the voltage comparator changes state, resets the flip-flops, closes the switch S_1, and end the timing cycle. The output is taken from either the Q or $\overline{Q}$ terminal of the flip-flop and corresponds to a timing pulse of duration T, where:

$$T = RC \ln \left[\frac{V_{CC}}{V_{CC} - V_{REF}} \right] \qquad (1)$$

Normally, the internal threshold voltage, V_{REF}, is generated from the supply voltage by means of a resistor divider as shown in Figure 1. Then, V_{REF} is equal to a fraction of the supply voltage:

$$V_{REF} = V_{CC}\left[\frac{R_2}{R_1 + R_2}\right] \quad (2)$$

and the basic timing equation becomes independent of the supply voltage:

$$T = RC \ln\left[1 + \frac{R_2}{R_1}\right] \quad (3)$$

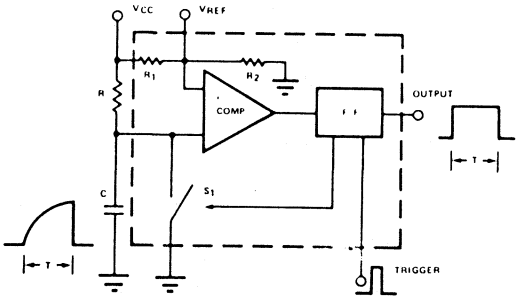


Figure 1. Exponential-Ramp Type Timing Circuit

Since the resistors R_1 and R_2 are inside the IC, their ratio is set by the design of the IC, and is normally accurate to within ±1%. Thus, virtually all the accuracy of the timing interval is determined by the external R and C.

In most timer/counter designs, it is convenient to set the ratio of resistors R_1 and R_2 such that:

$$\frac{(R_1 + R_2)}{R_1} = e = 2.718 \ldots \quad (7)$$

where "e" is the base of the natural logorithm. This makes the period of the time-base oscillator directly equal to 1.0 RC and simplifies the selection of external R or C values for a given timer setting.

An alternate approach to the design of one-shot timers is the "linear-ramp generator" circuit, shown in Figure 2. This circuit operates on a principle similar to that of the basic exponential timer, except the timing capacitor C is now charged *linearly* with a constant current, I, and generates a linear-ramp waveform with a constant slope of (I/C). The constant-current is in turn controlled by an external control voltage, V_C, applied to the current source. The total timing interval, T, is the time necessary for the voltage across C to rise from ground to V_{REF}, at a constant slope of (I/C), or:

$$T = (V_{REF})(C/I) \quad (4)$$

Normally, V_{REF} and V_C (and consequently I) would be derived from V_{CC} by means of resistor-dividers; therefore, they would be both proportional to V_{CC}. Thus, the effects of supply voltage variations cancel, and the basic timing equation for the linear-ramp type timer circuit of Figure 2 becomes

$$T = \alpha RC$$

where α is a constant of proportionality set by the internal resistor-dividers within the IC, and R and C are the external timing components.

The exponential-ramp type timing circuit of Figure 1 is inherently simpler and more accurate than the linear-ramp type circuit. However, the latter has the advantage of providing a linear voltage across the capacitor which is proportional to the *elapsed-time* during the timing cycle and can be used as a "linear sweep" or time-base signal for oscilloscope or X-Y recorder displays.

Normally, the internal threshold reference, V_{REF}, of one-shot IC's is available as a package terminal and can be modulated by an external input signal. This permits the user to modulate or vary the timing interval by means of an external control signal. This feature can also be used for generating pulse-width modulated

V_{CC} with a time constant set by the external R and C. When the voltage across it reaches the upper threshold, V_A, comparator #1 changes state and sets the flip-flop again, and discharges C back to the lower threshold level. V_B. In this manner, the circuit continues to oscillate, with the voltage level across C exponentially rising to V_A, then rapidly decaying to V_B, and then repeating its cycle. The output of the circuit is a sequence of narrow pulses, with a repetition rate T, given as:

$$T = RC \ln \left[1 + \frac{R_2}{R_1}\right] \quad (6)$$

where R_1 and R_2 are the internal bias resistors setting up the threshold levels V_A and V_B. The train of output pulses coming out of the time-base oscillator are counted by the binary counter; and when a given count, N, is reached, the control flip-flop is latched in its reset condition until the next trigger input to the circuit.

UNIQUE FEATURES OF TIMER/COUNTERS

The combination of a stable time-base oscillator and a programmable binary counter on the same IC chip offer some unique application and performance features. Some of these are outlined below:

Generating Long Delays with Small Capacitors: For a given time delay setting, the timer/counter would require a timing capacitor, C, that is N times smaller than that needed for the "one-shot" type timer, where N is the count programmed into the binary counter. Since large-value, low-leakage capacitors are quite expensive, this technique may provide substantial cost savings for generating long time delays in excess of several minutes.

Generating Ultra-Long Delays by Cascading: When a cascading two timer/counters, one cascades the counter stages of both timers. Since the second timer/counter further divides down the counter output of the first timer, the total available count is increased *geometrically*, rather than arithmetically. For example, if one timer/counter gives a time delay of NRC, two such timer/counters cascaded will produce a time delay of N^2 RC where N is the count setting of the binary counter. Thus, a cascade of two timer/counter IC's, each with an 8-bit binary counter, can produce a time delay in excess of 32,000 RC.

Generating Multiple Delays From Same RC Setting: By using a programmable binary counter, whose total count can be programmed between a minimum count of 1, to a maximum count of N, one can obtain N different time intervals from the same external RC setting.

Easy to Set or Calibrate: Although timer/counters are normally used for generating long time delays or intervals, their accuracy characteristics are only determined by the characteristics of the time-base oscillator. The counter section does not affect the over-all timing accuracy. Thus, time setting or calibration for long interval timing can be done quickly, without waiting for the entire timing cycle, by setting the accuracy of the time-base oscillator.

CHOOSING THE RIGHT IC TIMER

Because of its versatility, the monolithic IC timer offers a very wide range of applications in circuit or system design. However, during the design phase, once the "paper design" is accomplished, the user is faced with the key question: which IC timer is the best choice for a given application? If the performance characteristics and the limitations of the timer IC is not carefully considered, the total system performance may be degraded; similarly, if the timing function is overspecified with an excessive amount of "overkill", particularly with regards to its stability and accuracy requirements, then the system cost will increase unnecessarily.

The key selection criteria in choosing the right timer for the job is finding the monolithic IC which will result in the lowest system cost (including the external components) for a given performance requirement.

A very large majority of applications for IC timers can be classified into one of the four categories listed below:

- Interval or Event Timing
- Pulse Generation and Shaping
- Oscillation or Clock-Generation
- Ramp Generation

These categories of applications are discussed in more detail in the following sections, with the particular emphasis on "choosing the right IC timer" for the particular application.

INTERVAL OR EVENT TIMING

In such an application one uses the IC timer either to control the *time interval* between events, or the *duration* of an event. A typical example of such application would be to control the opening or closing of an electromechanical relay or sequencing of indicator lights.

General Purpose Timing: Most timing applications fall within the time interval range of a few microseconds to several minutes. For such applications the basic one-shot **timer, such as the 555 type is often the best choice, based on its low cost and versatility.**

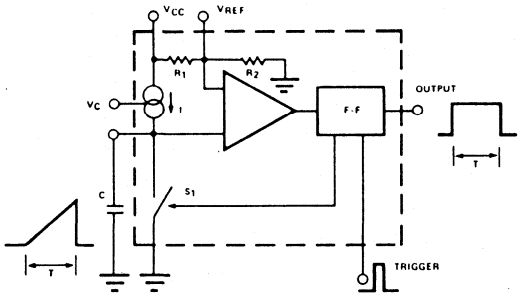


Figure 2. Block Diagram of a Linear-Ramp Type Timer Circuit

(PWM), or pulse-position modulated (PPM) signals, or allows the timer circuit to be used as a voltage-controlled oscillator.

PRACTICAL LIMITATIONS OF ONE-SHOT TIMERS

The accurate timing intervals which can be obtained from commercially available one-shot type timer IC's are limited to the range of several micro-seconds to several minutes. For generating very short timing pulses (in the few micro-second range) the internal time delays associated with the switching speeds of the comparator, the flip-flop and the discharge transistor (i.e., the switch S_1) may contribute additional timing errors. Similarly, for long time delays (in the several minute range) which require large values of R and C, the input bias current of the comparator, and the leakage currents associated with the timing capacitor, or the internal discharge transistor, may limit the timing accuracy of the circuit.

In general, for timing applications requiring time delays in excess of several minutes, the multiple-cycle or timer/counter type timer circuits provide a more economical and practical solution than the one-shot type IC timers.

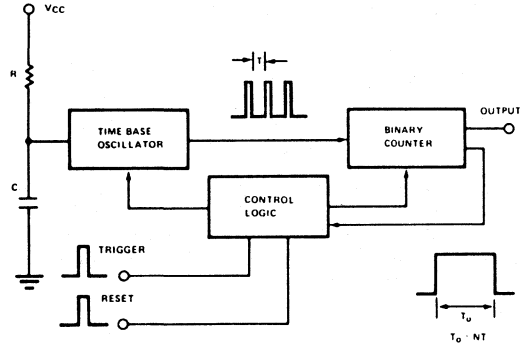


Figure 3. Simplified Block Diagram of a Timer/Counter

TIMER/COUNTER CIRCUITS

The timer/counter, or multiple-cycle timing circuits use the combination of a time-base oscillator and a binary counter to generate the desired time delay. Figure 3 shows a simplified block diagram of a timer/counter IC, which is made up of three basic blocks: (1) a time-base oscillator; (2) a binary counter; and (3) a control flip-flop.

With reference to the simplified block diagram of Figure 3, the principle of operation of a timer/counter can be explained as follows: when the circuit is at rest, or reset condition, the time-base oscillator is disabled, and the counter is reset to zero. Once the circuit is triggered, the time-base oscillator is activated and produces a series of timing pulses whose repetition rate is proportional to external timing resistor R, and the capacitor

C. These timing pulses are then counted by the binary counter; and when a pre-programmed count is reached, the binary-counter resets the control flip-flops, stops the time-base oscillator and ends the timing cycle. The total timing interval, T_0, is then proportional to N times the (RC) product, where N is the pre-programmed count.

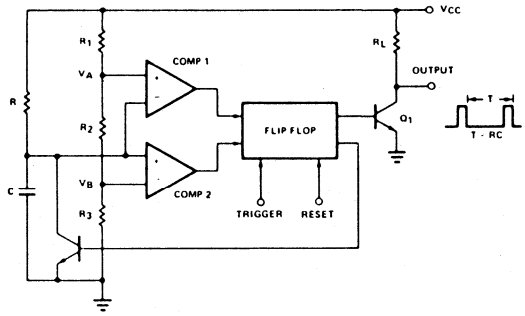


Figure 4. Simplified Schematic of a Time-Base Oscillator Circuit

Time-Base Oscillator: The time-base oscillator used in most of the timer/counter IC's is derived from the simple exponential-ramp type timer circuit. Figure 4 shows the simplified circuit diagram of such an oscillator. The timing components, R and C, are external to the chip. The operation of such an oscillator can be described as follows: when the circuit is at rest the flip-flop is latched in its reset state, and the transistor Q_1 is "off", the external capacitor C is fully charged to a voltage approximately equal to V_{CC}. When the circuit is triggered, the flip-flop is unlatched and set, which causes the discharge transistor Q_1 to turn "on" and discharge C rapidly. When the voltage across C discharges to the voltage level V_B, the comparator #2 changes state, resets the flip-flop and turns Q_1 "off". Then, C charges toward

Low-Power Timing: Many timing applications involving battery-operated or portable equipment, require a low-power timer which can perform the general purpose timing functions with a minimum amount of power dissipation. The XR-L555 Micropower Timer IC, which operates with less than 1 mW of power dissipation and with supply voltages as low as 2.7 volts, is especially designed for such applications.

Long Interval Timing: For timing applications requiring interval timing in the minutes, hours, or days range, the timer/counter IC's present the most economical approach, since they can produce long time delays using a small value capacitor. For such an application of the low-cost XR-2242 Long Range Timer, which operates on the timer/counter principle, is the most cost-effective circuit.

Sequential Timing: Many timing applications require *sequencing* of timing functions, i.e., one timer completes its operation and initiates the next timer, and so on. Since these applications require a multiplicity of timer circuits, they are best served by a dual-timer IC, such as the XR-L556.

Delayed Timing: Certain timing applications require that the start of the timing pulse be delayed by a specific time from the occurrence of the trigger. This can be easily accomplished by using a dual-timer, such as the XR-L556, where one section of the dual-timer can be used to set the initial "delay" subsequent to the trigger; and the second section can be used to generate the actual timing pulse.

Event Counting: In such an application, one needs to keep an accurate count of "events" which are normally a series of incoming pulses. This function can be easily performed with a programmable timer/counter IC, such as the XR-2240, where the binary counter section can be programmed to count a given number of input pulses and stop the count, and/or reset the circuit when the programmed count is reached. In the case of the XR-2240, the existing count in the counters is displayed in a 8-bit parallel binary-format.

Digitally-Programmed Timing: Some timing applications may require that the timing interval be digitally programmable, without switching additional precision resistors and capacitors into the circuit. Such a function can be easily achieved by using a programmable timer/counter, such as the XR-2240, where output duration can be programmed from 1.0 RC to 255 RC, in 1 RC increments, where R and C are the external timing components.

PULSE GENERATION AND SHAPING

A popular class of applications for the one-shot type timers is pulse shaping or stretching. Some specific examples of such applications and the recommended types of IC timers for each are given below.

Pulse Stretching: In such an application the IC timer is operated in its monostable mode and is triggered by an input series of pulses, whose repetition period is *longer* than that timing period of the IC. The output from the timer will then have the same repetition rate as the input pulse train, except that each output pulse will now have a uniform duration or length, as set by the RC time constant of the timer. The two IC's best suited to this application are the XR-L555 and the XR-320. The XR-L555 has the advantage of low unit price, whereas the XR-320 has the advantage of being able to trigger on *either* positive- or negative-going edge of the input pulses.

Delayed-Pulse Generation: In this application it is necessary to convert the input pulse train to a different pulse sequence which has the *same* repetition rate but a *different* duration and a *different* phase. This function can be accomplished with a dual-timer circuit, such as the XR-L556, where the first timer which is triggered by the input signal, sets the phase difference or "delay" between the input and the output pulse sequence; and the second timer which is triggered at the trailing-edge of the first one, sets the output pulse-width.

Pulse Blanking: In this application it is necessary to selectively "interrupt" or "blank-out" a pulse train. Such an application can be performed using a dual-timer IC, such as the XR-L556, where one section of the timer can be operated as a "pulse-stretcher" triggered by the input pulse train; and the second timer section can be triggered by a separate timing signal and serve as an enable/disable control for the first timer, thus interrupting or "blanking" its output during its timing interval.

Pulse-Width Modulation: In certain timing applications it is necessary to modulate the pulse-width of an output pulse sequence, without affecting its repetition rate. Such a requirement can be met by a one-shot timer, such as the XR-L555 operating in its monostable mode and being triggered by a fixed-frequency input pulse-train. The width of the output pulses from the timer IC can be modified without affecting the repetition rate, by simply applying a control-voltage to the modulation terminal of XR-L555.

Pulse-Position Modulation: This application requires the generation of a pulse sequence whose pulse-width is constant (and usually very narrow) and, whose repetition rate is modulated. Such a function can be easily implemented using a dual-timer IC, such as the XR-556, where the second timer generates the narrow output pulses when triggered by the output of the first timer. The first timer section is then operated in its free-running (i.e., astable) mode and its frequency is then externally modulated by applying a control-voltage to its modulation terminal.

OSCILLATION OR CLOCK-GENERATION

IC Timers can be operated in their free-running or "self-triggering" mode, to generate periodic timing pulses. Since the output pulse-width or the frequency can be controlled by the choice of external resistors and capacitors. These circuits make excellent low-cost clock oscillators, for a number of digital systems. Some of these applications are outlined below.

Clock Generator: In such applications, the IC is used to generate a fixed-frequency output waveform with nearly 50% duty cycle. The **XR-L555** timer, whose output duty-cycle can be controlled by the choice of two external resistors, is ideally suited for such an application, for clock frequencies up to 300 kHz.

High-Current Oscillator: Certain oscillator applications require that the circuit output should be able to source or sink high load currents ($\geq$ 100 mA) in order to drive electromechanical relays or capacitive loads. The XR-555 Timer IC, which can provide up to 200 mA of current drive, is well suited for such applications.

Micropower Oscillator: Battery operated or remote-controlled instruments often require a low-power clock oscillator. The **XR-L555** Micropower Timer, which operates with less than 1 mW of power drain, is the recommended choice for such applications, since it dissipates 1/15th the power of the conventional 555-type timer.

Voltage-Controlled Oscillator: Voltage-controlled oscillator (VCO) circuits find a wide range of applications in phase-locked loop systems. The XR-L555, which has a separate modulation terminal (Pin 5), can be used as a VCO by applying the proper control voltage to its modulation terminal and operating the IC in its self-triggering mode.

Low-Voltage Oscillator: Low threshold CMOS logic circuits normally require stable clock oscillators which can operate with a single 3 volt supply. The XR-L555 Micropower Timer which can operate with supply voltages as low as 2.7 volts is particularly suited for such applications.

Ultra-Low Frequency Oscillator: Certain battery operated or remote-controlled equipment require a stable ultra-low frequency clock oscillator, whose frequency can be as low as one cycle per day. The XR-2242 Long-Range Timer circuit which produces a square-wave output with a period of 256 RC, when operating in its free-running mode, is a very cost-effective replacement for such an oscillator.

Digitally-Programmed Oscillator: In certain applications it may be necessary to program the frequency of an oscillator by means of a binary control signal, without switching additional resistors or capacitors into the circuit. The XR-2240 Programmable Timer/Counter, when operating in its delayed-trigger mode (see Exar Application Note AN-07) can be used in such an application to generate an output frequency whose period is equal to (N + 1)RC, where N is the binary count which can be digitally programmed by an external 8-bit binary signal, to be any integer between 1 and 255.

Binary Pattern Generator: In certain test instrumentation design, it is necessary to generate a pseudorandom binary data pattern, which would then repeat itself periodically. The XR-2240 Programmable Timer/Counter which provides eight separate "open-collector" outputs, can perform such a function by selective shorting of one or more of its outputs to a common pull-up resistor.

Tone-Burst Generator: Some instrumentation applications require the generation of a certain tone or frequency signal, at periodic intervals. This function can be accomplished using a dual-timer IC, such as the XR-L556 where one of the timer sections would operate as a keyed oscillator which is turned "on" and "off" by the other section. The output of the first timer section. The output of the first timer section will then be a "tone-burst", which will be present only during the timing cycle of the second timer.

RAMP GENERATION

In a number of timing applications, it is necessary to generate an analog voltage which is proportional to the time elapsed during the timing cycle. This function is particularly useful for generating linear sweep voltage for oscilloscope or X-Y recorder display applications and it can be accomplished either *linearly* or *digitally*, as described below.

Linear Ramp Generator: A linear ramp can be obtained by charging a timing capacitor with a constant-current source. Since the XR-320 Timer IC operates on such a principle, it is ideally suited for this application. Upon triggering, the XR-320 produces a positive-going ramp at its current-source output (Pin 3). This ramp starts

from the ground level and rises up to a voltage level approximately equal to 80% of the supply voltage, during the timing interval. Since the current-source output at Pin 3 is a high impedance terminal, the sweep or linear ramp signal at this point should be buffered by a high impedance op amp connected as a voltage follower. amp connected as a voltage follower.

Digital Ramp Generator: In certain applications, a digitally generated "staircase" voltage is preferred over a linear ramp signal. Such a digital ramp signal can be generated using the XR-2240 Programmable Timer/Counter, along with an external resistor ladder and a current-summing op amp. The digital ramp signal is particularly useful for analog-to-digital conversion or digital sample-and-hold applications.
tions.

Fundamentals of Switching Regulators

In the design of modern electronic equipment and systems, supply voltage regulation is one of the critical circuit functions required for optimum system performance. The function of a voltage regulator is to provide a constant output voltage, under changing line or load conditions.

The advent of monolithic IC regulators has greatly simplified power supply design by reducing design complexity, improving reliability and ease of maintenance. Until recently, the field of IC regulators was dominated by linear or "series-pass" type regulators which are easy to use and require a minimum number of external components. However, under changing load and line voltage conditions, series regulators have relatively poor efficiency in power handling: a significant amount of the input power is dissipated, or wasted, in the regulator, particularly under large line input variations.

In many regulator applications, or in power supply designs, the limitations of series regulators can be overcome by using "switching regulator" systems for voltage and power flow control. Although switching regulators require somewhat more complex circuitry external to the chip, they can provide significant improvement in efficiency and versatility over conventional series regulators. Within recent years, power supplies using switching regulators have proliferated greatly, because of improvements in circuit components specifically made for them. Some of these are the inexpensive high-speed switching power transistors, low-loss ferrite cores for inductors and the complex LSI circuits which contain all the critical control circuitry. As a result, the cost and complexity of switching regulator systems have been reduced greatly, making them economically feasible for a wide range of applications.

This data book is intended as a design and applications aid for the circuit designer involved in voltage regulator or power supply design. It covers the basic principles of operation of switching regulator systems, and the monolithic LSI circuits which can be used in designing them.

CLASSES OF IC REGULATORS

The function of a voltage regulator is to provide a well-specified and constant output voltage level from a poorly specified and sometimes fluctuating input voltage. The output of the voltage regulator would then be used as a supply voltage for the other circuits in the system. In this manner, the fluctuations and random variations of a supply voltage under changing load conditions are essentially eliminated.

Since the regulation and control of supply voltage is one of the most fundamental and critical requirements of any electronic system design, the monolithic voltage regulator or power control circuits have become one of the essential building blocks of any analog or digital system. As a result, the monolithic voltage regulators, similar to the case of monolithic op amps, have gained wide acceptance and have greatly simplified the tedious task of designing power supply circuits.

Today, there are two very distinctly different types of IC voltage regulators which have gained wide acceptance and popularity. There are the so-called "series regulators" and "switching regulators". The series regulators control the output voltage by controlling the voltage drop across a power transistor which is connected in series with the load. The power transistor is operated in its linear region and conducts current continuously. The switching regulators, on the other hand, control the flow of power to the load by turning on-and-off one or more of the power switches connected in parallel or series with the load, and make use of inductive and capacitive energy storage elements to convert the switched current pulses into a continuous and regulated load current.

SERIES-PASS REGULATORS

The series or series-pass type voltage regulator is connected in series between the load and unregulated supply line. It is a feedback circuit comprised of three main sections, shown in Figure 1. These are the reference voltage element, the error amplifier and the series-pass element. In most cases, a fourth section, called "overload protection circuitry, is also included in the system to prevent against burn-out under accidental overload conditions.

With reference to the simplified block diagram of Figure 1, the principle of operation of a series regulator can be briefly described as follows: The internal voltage reference generator generates a reference voltage level, V_R, which is independent of the unregulated supply voltage or the temperature changes. The error amplifier compares V_R with the sampled and scaled output voltage, V_S, and generates a corrective error signal to regulate the voltage drop across the pass element such that the $V_R = V_S$ condition is fulfilled. The scaled voltage, V_S, is derived from the actual

output voltage by means of the so-called sampling resistors, R_1 and R_2. If the error amplifier gain is very high, one can show by a simple feedback system analysis that the output voltage is, to a first order, proportional to the reference voltage V_R and independent of the input voltage:

$$V_{out} = V_R\left(\frac{R_1 + R_2}{R_2}\right) \qquad (2.1)$$

The pass element is normally a high-current transistor, or a Darlington connection of two transistors. Depending on the current and power handling requriements, the pass transistor may be left external to the monolithic IC chip. For proper operation of the pass transistor, it must be biased in its linear region. Therefore, the total voltage drop, V_{in}-V_{out}, across the pass element must not exceed the breakdown voltage of the pass transistor, and must be greater than a minimum amount, called the drop-out voltage, necessary to keep the pass transistor in its linear or active region.

SWITCHING REGULATORS

The switching regulators, which are also called switch-mode regulators, find a wide range of applications in power supply design where high-power and high-efficiency are important. The principle of operation of a switching regulator differs significantly from that of a conventional series regulator circuit. In the case of series regulators, the pass transistor is operated in its linear region to provide a controlled voltage drop across it with a steady dc current flow. In the case of switching regulators, the pass transistor is used in a controlled switch and is operated at either the **cut-off** or the **saturated** state. In this manner, the power is transmitted across the pass device in discrete current pulses, rather than a steady current flow.

The most important advantage of switching regulators over the conventional series regulators is greater efficiency, since the pass device is operated as a low impedance switch. When the pass device is at cut-off, there is no current through it, thus, it dissipates no power. When the pass device is in saturation, it is nearly a short circuit with negligible voltage drop across it; thus, it dissipates only a small amount of average power provided that it can handle the peak current loads. In either case, very little power is wasted in the regulator and pass devices, and almost all the power is transferred to the load. In this manner, a very high degree of regulator efficiency is achieved, typically in the range of 70% to 90%, relatively independent of the input/output voltage differentials. The efficiency of switching regulators is particularly apparent when there is a large input/output voltage difference across the regulator. For example, if one considers the case of a regulator operating with a 28-volt input and delivering a 5-volt output at 1A current, a conventional series regulator would require a drop of 23 volts across the series pass transistor. Thus, a total of 23 watts of power is wasted in the regulator, resulting in an overall regulator efficiency of approximately 18%. As will be described in later sections, a switching regulator can be readily designed to perform the same function with greater than 75% efficiency under similar operating conditions.

Another important advantage of the switching regulator circuits is their versatility; they can provide output voltages which can be less than, greater than, or of opposite polarity to the input voltage, as determined by the mode of operation of the circuit. In this manner, one can step-up, step-down, or invert the polarity of an input voltage to generate any arbitrary set of dc voltages within the power distribution system.

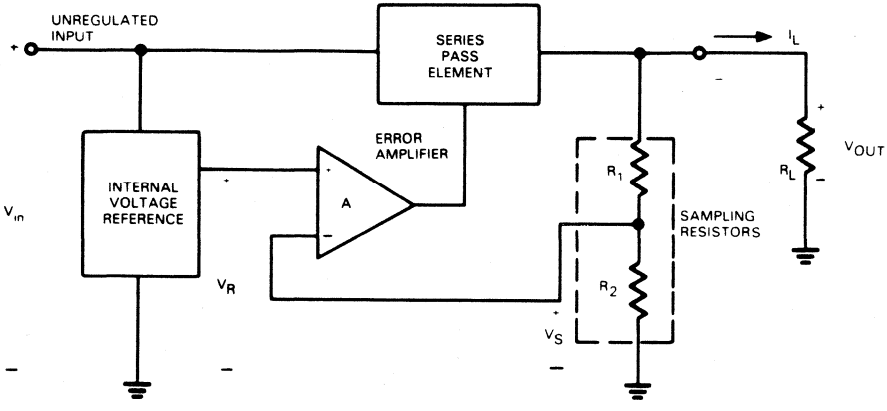


Figure 1. Simplified Block Diagram of a Series Regulator

Switching regulators also have some drawbacks. They are more complex, and require external components such as inductors or transformers. They generate more noise and output ripple than conventional series regulators, and are slower responding to transient load changes. One area of caution, when using switching regulators, is the generation of electromagnetic and radio frequency interference (RFI). This interference problem is usually solved by the use of feedthrough low-pass filters isolating the power lines into the regulator, and by using ground-shields around the regulator to suppress the interference. However, even with these precautions, switching regulator circuits are not recommended for powering very low level signal processing circuitry, where noise characteristics are very critical.

Figure 2 shows the simplified block diagram of a switching regulator power supply system, which comprises several basic blocks. With reference to the figure, the principle of operation of the switching regulator system can be described as follows: The control element is essentially a power switch, which is either "on" (i.e., a virtual short circuit) or "off" (i.e., an open circuit). The duty cycle of the control element is determined by the control logic circuitry, which is driven by an internal oscillator, and puts out periodic control pulses which activate the control pulses (i.e., the on and off duration of the switch over a given period of time is controlled by the output of the error amplifier).

The control element, or switch, delivers pulses of energy into the load circuit which is normally made up of inductive and capacitive components, and diodes. The function of the load circuit is to convert these power pulses to a steady stream of current flow into an external load resistor, R_L. The voltage level across R_L is sensed by means of a sampling resistor network, and is connected to the input of the error amplifier. The error amplifier compares the sampled output level with that of a reference voltage, and causes the pulse width of the control logic section to vary in such a manner to keep the output voltage level across R_L constant.

The power switch which forms the control element portion of the switching regulator is normally a power transistor which is switched between cutoff and saturation. One advantage of the switching regulator over the conventional linear regulator is greater efficiency, since the cutoff and saturation modes are the two most efficient modes of operation. In the cutoff mode, there is a large voltage across the transistor but little current through it; in the saturation mode, the transistor has little voltage across it but a large amount of current. In either case, little power is wasted, and most of the input power is transferred to the output; therefore, the efficiency is high. Regulation is achieved by varying the duty cycle that controls the average current transferred to the load. As long as this average current is equal to the current required by the load, regulation is maintained.

In addition to high efficiency operation, one added advantage of the switching regulator is the the flexibility of the choice of output voltages available. Depending on the particular load circuit configuration used, the output can be greater than or less than the input voltage, or be of opposite polarity to the input. These features will be explained further in the following sections.

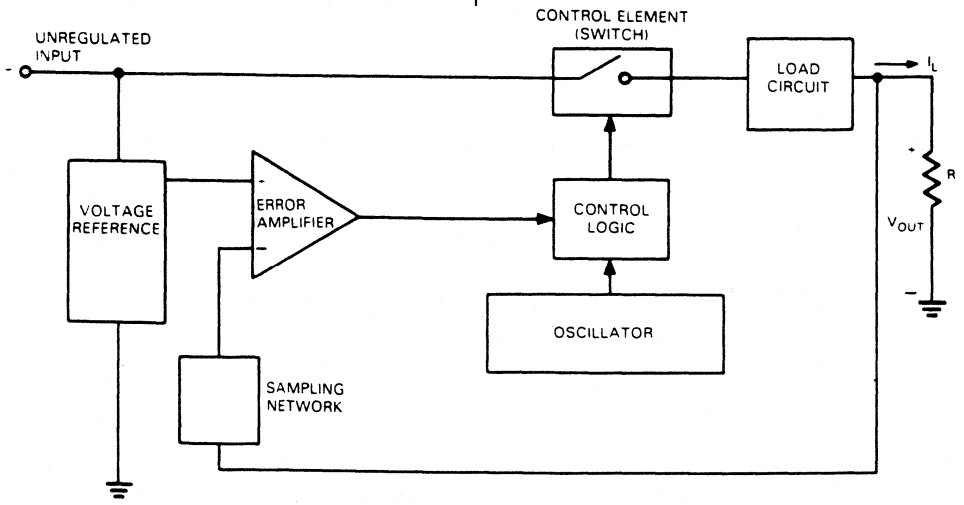


Figure 2. Simplified Block Diagram of a Switching Regulator System

PRINCIPLES OF OPERATIONS

The functional block diagram of a switching regulator circuit is shown in Figure 2. The basic principle of operation of the entire regulator system was qualitatively described in the previous section. Although the switching regulator system contains a large number of subsystems, it can be divided into two major sections:

a) Control Circuitry
b) Output Load Circuitry

Control circuitry is comprised of the voltage reference, sampling network, error amplifier, oscillator and the control logic sections shown in Figure 2. The purpose of this circuitry is to control the rate of power flow to the load circuit, and ultimately into the output load, R_L. The control of power flow is achieved by generating control pulses which determine the on/off period of the control element. The control circuitry normally operates at very low power levels.

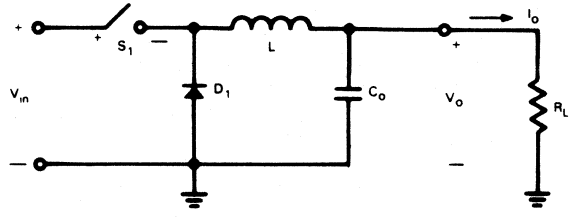
The output load circuitry is made up of the control element and the load circuit. The control element functions as a power switch, and delivers discrete packets of power, in the form of current pulses into the load current. The load circuit converts these into a steady current flow through the external load.

Depending on the type of output load circuitry used, switching regulator power supplies can be classified into three categories. These are:

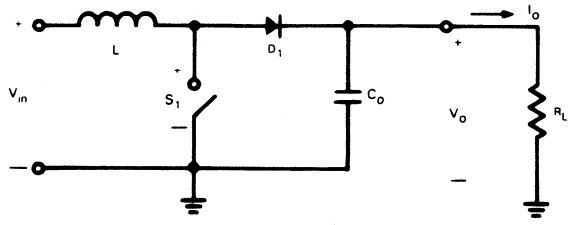
1. Single-ended inductor circuits.
2. Diode/Capacitor circuits.
3. Transformer coupled circuits.

Figure 3 shows the three basic configurations for the output circuitry of single-ended inductor type switching regulators. These are among the most frequently used output circuit configurations since they are by far the easiest to design and control for medium and high-current applications.

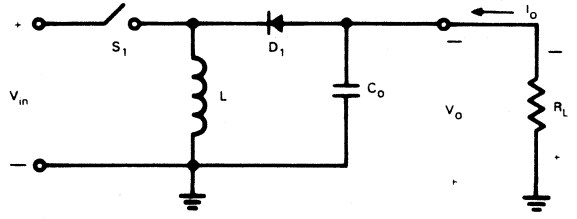
Figure 4 shows the switching regulator configurations using diode/capacitor circuits. These circuits are typically used for very low current applications, and primarily as voltage multipliers, to increase the voltage level available from a low voltage battery. Examples of such applications are the generation of voltage drive for LCD displays in watch circuits from a 1.5-volt or 3-volt battery, and in low voltage hearing aid amplifiers.



(a) STEP-DOWN CONFIGURATION ($V_{in} > V_o$)



(b) STEP-UP CONFIGURATION ($V_o > V_{in}$)



(c) INVERTING CONFIGURATION

Figure 3. Single-Ended Inductive Load Circuits

Figure 5 shows the two basic configurations of transformer coupled output circuits. The circuit of Figure 5(a) is the so-called push-pull circuit used in conventional dc-to-dc converters, with each switch controlled for 0 to 45% duty cycle modulation. The configuration of Figure 5(b) is the so-called single-ended flyback converter, which is useful at low-to-medium current loads.

The design of power supply systems using discrete circuits and the various types of output circuitry shown in Figures 3 through 5 are well covered in the literature. In the following discussions, we will primarily focus on switching regulator circuits using the single-ended inductor type output circuit shown in Figure 3, since these represent by far the most common category of application.

The control circuitry section of a switching regulator system, which controls the on/off duty cycle of the switch transistors, can be readily integrated in a monolithic IC form. In many cases, the switching transistors up to 1A current rating can also be incorporated into the monolithic chip. If higher power levels are required, the switch transistor on the chip is used as a drive for an external high current switch.

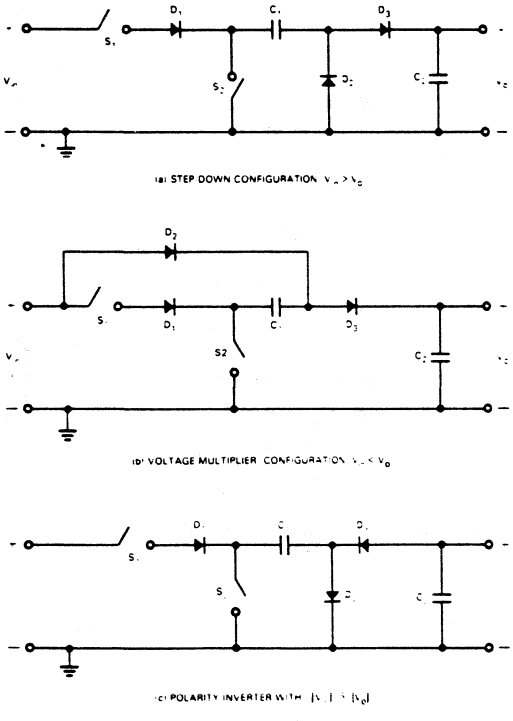


Figure 4. Diode/Capacitor Type Load Circuits

Figure 6 shows a simplified block diagram of a typical switching regulator IC used in conjunction with the single-ended inductor configuration of Figure 3(a). The circuit generates a stream of pulses which turn switch S_1 "on" and "off". The output dc level is sensed through the sampling resistors, R_1 and R_2, and compared against an internal voltage reference, V_{ref}, with the on/off time on the duty cycle of the switch, S_1, varied accordingly to keep the output voltage constant under changing load conditions.

Neglecting the current in the sampling resistors, the average or dc value of the output current, I_o, delivered to the load is proportional to the duty cycle of the power switch, S_1, as illustrated in Figure 7. If the sampled output voltage is lower than V_{ref}, the polarity of the comparator output signal causes the control logic to increase the duty cycle of S_1 and, thus, causes the output voltage level to increase until the equilibrium is reached such that the output voltage, scaled down by the sampling resistors, is equal to the internal reference voltage. Similarly, if the output load current, I_o, is decreased, this would cause the output voltage to increase which in turn would be sensed by the control circuitry and would reduce the duty cycle of the switch accordingly.

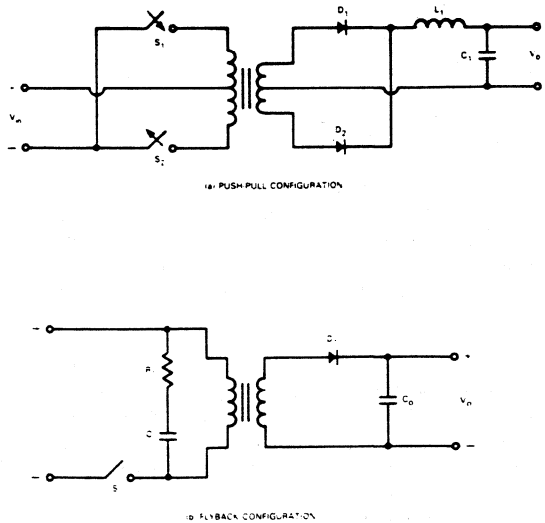


Figure 5. Transformer Coupled Load Circuits

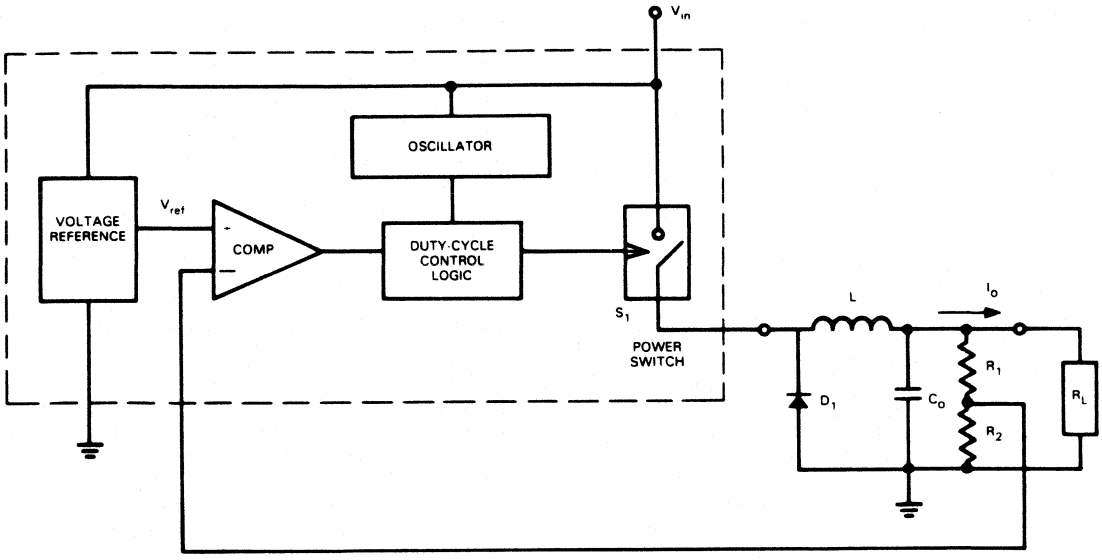


Figure 6. Simplified Block Diagram of a Switching Regulator IC in "Step-Down" Configuration

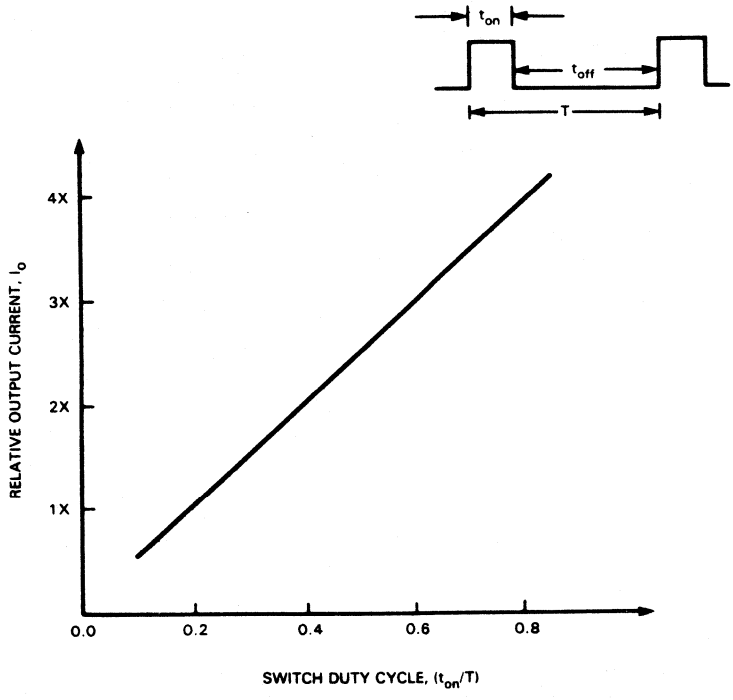


Figure 7. Output Load Current, I_o, as a Function of Switch Duty Cycle

METHODS OF DUTY CYCLE CONTROL

The switch duty cycle, (t_{on}/T), can be controlled by pulse width modulation at a fixed frequency, or by fixing the "on" or "off" time, and varying the frequency. The relative merits and disadvantages of these techniques are briefly examined below.

(a) Fixed Frequency, Variable Duty Cycle Operation:

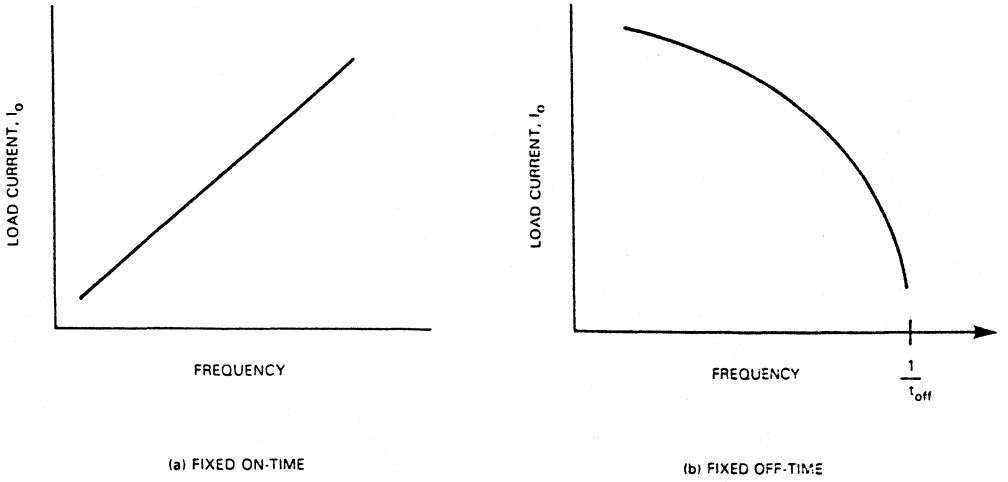
In this type of a switching regulator, the operating frequency is fixed and the duty cycle of the pulse train is varied to change the average power. This method is often referred to as pulse width modulation (PWM). The fixed frequency concept is particularly advantageous for systems employing transformer coupled output stages. The fixed frequency aspect enables the efficient design of the associated magnetics. In addition, filtering or shielding the surroundings from the radio frequency or electromagnetic interference generated by the regulator is somewhat simplified because of the fixed frequency of switching. Because of these features, the majority of the switching regulator control IC's utilize a fixed frequency, variable duty cycle control method.

(b) Fixed On-Time, Variable Frequency:

In this method, the switch has a fixed or predetermined "on" time, and the duty cycle is varied by varying the frequency or repetition rate of the control pulses. This methods provides ease of design in voltage conversion applications using the single-ended inductive output circuit configurations of Figure 3, and simplifies design calculations for the inductor value. The fixed on-time method is also advantageous for inductive output circuitry, since a consistent amount of charge is developed in the inductor during the fixed on-time. This eases the design or the selection of the inductor by defining the operating area to which the inductor is subjected under transient load conditions. Figure 8(a) shows the typical frequency vs. load current characteristics of a fixed on-time, variable frequency regulator, where the frequency increases linearly with increasing load.

(c) Fixed Off-Time, Variable Frequency:

In this type of a voltage regulator, the dc voltage at the output is varied by changing the on-time, t_{on}, of the switch, while maintaining a fixed off-time, t_{off}. As shown in Figure 8(b), the fixed off-time switching regulator behaves in an opposite manner to the fixed on-time system; as the load current increases, the on-time becomes longer, thus decreasing the frequency. This approach is advantageous for the design of a switching regulator which will operate at a well-defined minimum frequency and low ripple current under full load conditions. One basic drawback of the fixed off-time system is that the maximum current in the inductor, under transient load conditions, is not well-defined. Thus, additional care is required to ensure that the saturation characteristics of the inductor are not exceeded.



(a) FIXED ON-TIME

(b) FIXED OFF-TIME

Figure 8. Typical Load Current vs Frequency Characteristics of (a) Fixed On-Time and (b) Fixed Off-Time Variable Frequency Switching Regulators

MODES OF OPERATION WITH INDUCTIVE OUTPUT CIRCUITS

Two of the most important advantages of switched regulators are their high efficiency and their ability to step-up step-down, or change polarity of an input voltage. These basic features can be best understood by examining the voltage and current waveforms at the output of the regulator. In this section, some of the waveforms and key design equations associated with the inductive output circuits of Figure 3 will be examined for various modes of operation under steady-state load conditions. For the sake of brevity, rigorous derivations will be omitted and only their conclusions will be presented.

STEP-DOWN OPERATION

In the step-down operation, the switching regulator produces an output dc voltage, V_O, which is lower than the input voltage, V_{in}. Figure 9 shows the basic voltage and current waveforms associated with the circuit under steady-state operation. The switch, S_1, is assumed to have a voltage drop of V_{sat} in its "on" condition, and the diode, D_1, has a forward drop of V_D when it is conducting.

When S_1 is closed, or on, D_1 is off, and the current in the inductor, I_{PK}, rises linearly from zero to its peak value, I_L, with the slope:

$$\frac{dI_L}{dt} = \frac{V_L}{L} = \frac{V_{in} - V_{sat} - V_O}{L} \qquad (4.1)$$

At the end of the switch on-time, t_{on}, this current reaches its maximum value, I_{PK}. When S_1 is off, the inductor generates the necessary voltage to forward bias D_1, and keep I_L from changing instantaneously. During this portion of the cycle, I_L linearly decays to zero at the end of the off-time t_{off}.

At steady-state, average or dc current through C_O is zero, therefore, the output dc current, I_o, is equal to the average value of I_L, or:

$$I_o = (I_L)_{aug} = \frac{I_{pk}}{2} \qquad (4.2)$$

From the waveforms shown in Figure 9, the switch "on" and "off" times can be related to the voltage levels at the input and output of the circuit, as:

$$\frac{t_{on}}{T_{off}} = \frac{V_O + V_D}{V_{in} - V_{sat} - V_O} \qquad (4.3)$$

or, V_O, can be to the rest of the voltages as:

$$V_O = \left(\frac{t_{on}}{T}\right)(V_{in} - V_{sat}) - \left(\frac{t_{off}}{T}\right) V_D \qquad (4.4)$$

assuming an ideal case where both the saturation and diode voltages are zero or negligible, this reduces to:

$$(V_O)_{ideal} = \left(\frac{t_{on}}{T}\right) V_{in} \qquad (4.5)$$

Equation (4.5) implies that, ideally, the switching regulator in its step-down mode provides a down scaling of the input voltage by a scale factor equal to the duty cycle of the switch transistor.

Another important parameter of the step-down regulator is the peak-to-peak output ripple voltage, $(\Delta V_O)_{pp}$. Assuming that C_O is sufficiently large so that the ripple voltage is much lower than the average or dc value of the output, $(\Delta V_O)_{pp}$ can be expressed as:

$$(\Delta V_O)_{pp} = \frac{I_{pk}}{8C_O}(t_{on} + t_{off}) = \frac{I_{pk}}{8C_O f} \qquad (4.6)$$

where $f = 1/T$ is the frequency or the repetition rate at which the switch opens and closes.

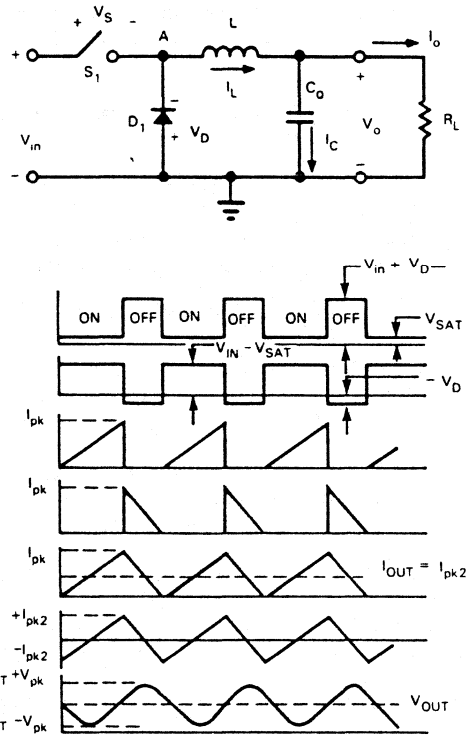


Figure 9. Switching Regulator Voltage and Current Waveforms in Step-Down Mode

STEP-UP OPERATION

In the step-up mode the switching regulator produces an output dc voltage V_O, which is higher than V_{in}. The circuit configuration for this mode of operation, along with the associated voltage and current waveforms, is shown in Figure 10 under steady-state operation.

With reference to Figure 10, the operation of the circuit can be summarized as follows: Assuming that S_1 is open and closes at the moment $I_L = 0$, the current in the inductor rises linearly from zero to a peak value, I_{PK}, during t_{on}. At the end of on-time, S_1 is opened. Since I_L cannot change instantaneously, the inductor generates the necessary voltage at node A to forward-bias D_1, and keep the current continuous. During the off-time, I_L decays linearly, and reachs zero at t_{off}. Then, S_1 closes again, and the cycle repeats itself. While D_1 is conducting, it supplies current to both the hold and the loading capacitor, C_O; when D_1 is nonconducting, the output current is drawn from C_O. Note that at steady-state, the average or dc current through D_1 is equal to the output or load current, I_L, and the net charge supplied to C_O, per cycle of operation, is zero.

The peak current, I_{PK}, is related to the steady-state output current as:

$$I_{pk} = 2\, I_o \left(\frac{V_D + V_o - V_{sat}}{V_{in} - V_{sat}}\right) \qquad (4.7)$$

and the on/off times of the switch, necessary for I_L to ramp from zero to I_{PK} and back to zero, are related as:

$$\frac{t_{on}}{T_{off}} = \frac{V_D + V_o - V_{sat}}{V_{in} - V_{sat}} \qquad (4.8)$$

Solving Eq. (4.8) for V_O, one obtains:

$$V_o = V_{in}\left(\frac{T}{t_{off}}\right) - V_{sat}\left(\frac{t_{on}}{t_{off}}\right) - V_D \qquad (4.9)$$

where $T (= t_{on} + T_{off})$ is the period of one full cycle of operation. In the idealized case, where the diode drop and V_{sat} of the switch are negligible, Eq. (4.9) reduces to:

$$(V_o)_{ideal} = V_{in}\left(\frac{T}{t_{off}}\right) \qquad (4.10)$$

or, in other words, the step-up mode of operation results in up-scaling the input voltage by the ratio (T/t_{off}).

The peak-to-peak output ripple voltage can be expressed as:

$$(\Delta V_o)_{pp} = \frac{(I_{pk} - I_o)2}{2\, I_{pk}}\,(t_{off} / C_O) \qquad (4.11)$$

with the assumption that $(\Delta V_O) \ll V_O$.

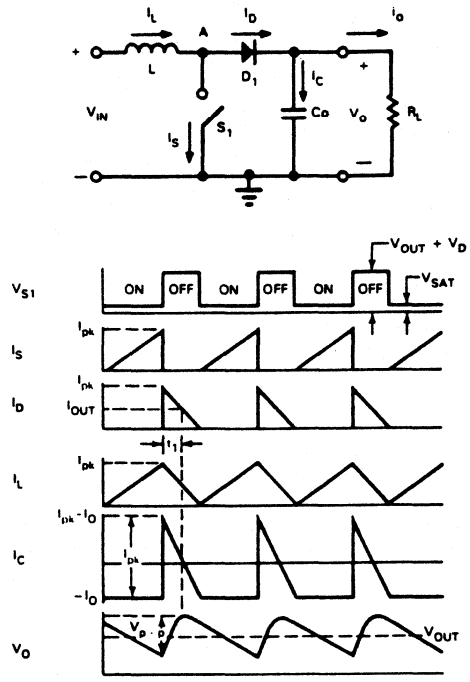


Figure 10. Voltage and Current Waveforms in Step-Up Mode

POLARITY-INVERTING OPERATION

In the polarity-inverting mode of operation, the switching regulator produces an output voltage across the load which is the opposite polarity to the input. Figure 11 shows the basic circuit configuration for this mode of operation. The polarity inversion is achieved by making the inductor force a current in the opposite direction through the load.

The operation of the circuit can be briefly described as follows: The current, I_L, through the inductor ramps up from zero to I_{PK} during t_{on}, and ramps down to zero during t_{off}, similar to the other two modes of operation described earlier. During t_{off}, with S_1 open, the inductor generates a negative voltage at node A to forward bias D_1 and keep I_L continuous. As in the case of step-up circuits, the average value of the diode current, I_D, is the steady state load current I_o, since C_O cannot pass any dc current Thus, from the waveforms and timing relations of Figure 11, one can express the peak current, I_{PK}, as:

$$I_{pk} = 2\, I_o \left(\frac{V_{in} + V_D - V_o - V_{sat}}{V_{in} - V_{sat}}\right) \qquad (4.12)$$

and the on/off times of the switch, necessary for I_L to ramp up from zero to I_{PK} and back to zero, are:

$$\frac{t_{on}}{t_{off}} = \left(\frac{V_D - V_o}{V_{in} - V_{sat}}\right) \quad (4.13)$$

Solving the above equation for V_o, one gets:

$$V_o = -\left[(t_{on}/t_{off}) (V_{in} - V_{sat}) - V_D \right] \quad (4.14)$$

In the idealized case, where V_D and V_{sat} are neglected, Eq. (4.14) will reduce to:

$$(V_o)_{ideal} = -\left(\frac{t_{on}}{t_{off}}\right) V_{in} \quad (4.15)$$

or in other words, the polarity-inverting mode of operation results in the reversal of polarity of the output voltage as well as its being scaled by the (t_{on}/t_{off}) ratio.

The peak-to-peak output ripple, $(\Delta V_o)_{pp}$, associated with the inverting operation can be expressed as:

$$(\Delta V_o)_{pp} = \frac{(I_{pk} - I_o)^2}{2 I_{pk}} \left(\frac{t_{off}}{C_O}\right) \quad (14.16)$$

which is identical to the case of step-up operation (see Eq. 4.16).

One word of caution is in order when using the polarity inverting configuration: Since the output polarity is reversed, the feedback polarity from the sampling resistors to the voltage comparator in the control circuitry (see Figure 6) must be reversed. Normally, this is done by reversing the reference and feedback inputs into the voltage comparator.

EFFICIENCY CONSIDERATIONS

The efficiency of a voltage regulator is defined as the ratio of the output power to the input power, i.e.:

$$\text{Regulator Efficiency} = \eta = \frac{P_O}{P_{in}} \quad (5.1)$$

where P_O is the power delivered to the load, and P_{in} is the power drawn from the power lines.

The efficiency advantage of switching regulator circuits can be illustrated best by comparing their efficiency with that of a series-pass type regulator.

Efficiency of a Series Regulator

In calculating the efficiency of a series regulator, similar to that shown in Figure 1, one can use a simple equivalent model of power dissipation within the regulator, as shown in Figure 12.

In this model, the current source, I_B, represents the total bias and operating current consumed in the regulator circuitry, and V_B represents the voltage drop across the pass transistor. For proper operation of the circuit, V_B is restricted to be greater than the drop-out voltage.

From the simple model of Figure 12, the input and output power levels can be written as:

$$P_{in} = V_{in} (I_B + I_L) \quad (5.2)$$

and

$$P_O = V_O I_L \quad (5.3)$$

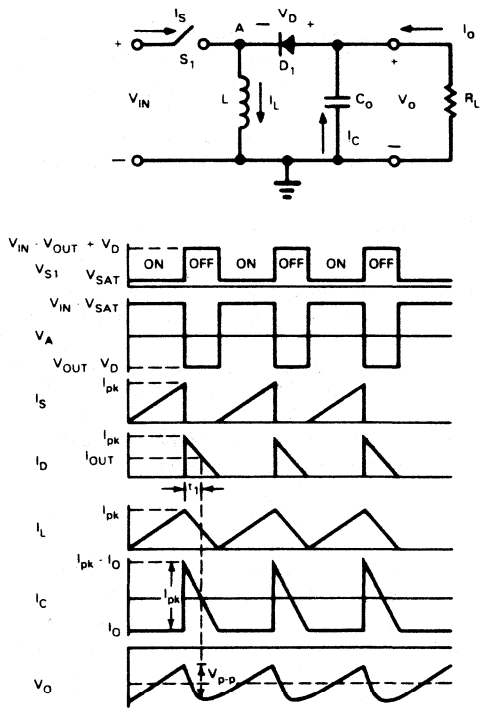


Figure 11. Voltage and Current Waveforms in Polarity-Inverting Mode

Then, the efficiency, η, can be expressed as:

$$\eta = \frac{P_o}{P_{in}} = \frac{1}{(1 + V_B/V_o)(1 + I_B/I_L)} \quad (5.4)$$

As given by Eq. (5.3), regulator efficiency depends directly on the ratio of load voltage and load current to the bias voltage and bias current. Since the bias current, I_B, is more or less fixed by the regulator design, the maximum rated efficiency, η, is obtained when the regulator is delivering its maximum rated current with the minimum input/output voltage differential. If the input contains large ac components, or large minimum/maximum fluctuations, the maximum efficiency is reduced since the average level of the input voltage would have to be increased to ensure that the instantaneous value of V_B is greater than the drop-out voltage.

Efficiency of Switching Regulators

Starting with the basic definition of efficiency given in Eq. (5.1), one can obtain the expressions for switching regulator efficiency under various operating modes.

For the case of the step-down regulator circuit, one can derive, from Eq. (4.2) through (4.4), an experession for efficiency as:

$$(\eta)_{\text{step-down}} = \left(\frac{V_o}{V_o + V_D}\right)\left(\frac{V_{in} + V_D - V_{sat}}{V_{in}}\right) \quad (5.5)$$

In a similar manner, the efficiency expression for step-up operation can be derived from Eq. (4.7) through (4.9) as:

$$(\eta)_{\text{step up}} = \left(\frac{V_o}{V_o + V_D - V_{sat}}\right)\left(\frac{V_{in} - V_{sat}}{V_{in}}\right) \quad (5.6)$$

The efficiency expression for inverted polarity operation can be derived from Eq. (4.12) through (4.14) as:

$$(\eta)_{\text{inverter}} = \left(\frac{|V_o|}{V_D + |V_o|}\right)\left(\frac{V_{in} - V_{sat}}{V_{in}}\right) \quad (5.7)$$

The efficiency expressions given above do not take into account the quiescent power dissipation in the control circuitry, which can cause the efficiency to decrease at very low current levels, when the average input current is of the same order of magnitude as the quiescent current. The switching transient losses in the switch transistor and diode, as well as the parasitic resistances associated with the inductor, are also not included in the above expressions. In practical regulator systems, these latter losses will cause small but finite reduction in the observed efficiency as compared to the theoretical results given in Eq. (5.5) through 5.7). The exact nature of this reduction in efficiency depends on the specific transistor, diode and inductor characteristics used, as well as on the selection of operating frequency.

There are two additional observations which can be made regarding the efficiency expressions:

1. In the ideal case, where both V_{sat} and V_D go to zero, all three regulator configurations provide an ideal efficiency of 100%.
2. The efficiency expressions of Eq. (5.5) through (5.7) are not sensitive to input/output voltage differential across the regulator. This is very different than the case of a conventional series regulator where efficiency varies inversely with the input/output voltage differential (see Eq. 5.4).

As an illustration, it is worthwhile comparing the efficiency of a power supply system with a 20-volt input and a 5-volt output with a conventional series regulator, to that with a step-down switching regulator. For simplicity, quiescent power dissipation associated with the control circuitry will be neglected.

In the case of a conventional series regulator, the efficiency is:

$$(\eta)_{\text{series}} \approx \frac{5}{20} = 25\% \quad (5.8)$$

For the case of a step-down regulator, assuming typical values of V_D = 1 volt, and V_{sat} = 1.5 volts, one gets from Eq. (5.5):

$$(\eta)_{\text{switching}} = (5/6)\left(\frac{19.5}{20}\right) = 81.25\% \quad (5.9)$$

which illustrates one of the most important features of switching regulators namely efficient transfer of power.

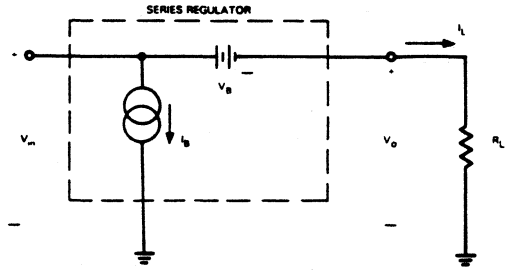


Figure 12. A Simplified Model for Calculating Efficiency of a Series Regulator

STABILITY CONSIDERATIONS

Similar to the case of conventional regulators, switched-mode power supplies are operated as closed-loop feedback systems; the output voltage level is constantly sensed, and a corrective signal is generated via a negative feedback path to keep it very nearly constant under varying load conditions. Since the overall regulator is a feedback system, it must be designed to meet certain stability criteria in order to assure its proper operation.

As in all feedback systems, the switching regulator circuits must also meet the so-called "Nyquist Criteria" for stability; namely the total phase shift around the regulator feedback loop must be less than -180 degrees when the total loop gain is unity (i.e., 0 dB). Stated in another way, this criteria also states that the loop gain must be less than zero dB when the phase shift reaches -180 degrees.

A convenient parameter to measure the margin of stability in a switching regulator is the so-called phase margin, which is defined as the amount of margin left in degrees before the phase reaches -180 degrees, at the frequency-where the gain is equal to zero dB. For example, if the total phase shift around the feedback-loop is -130 degrees when the gain reaches unity, this corresponds to a phase margin of 50 degrees.

The higher the phase margin, the higher is the margin of stability. However, if the phase margin is too high, the system response tends to be too slow and sluggish. As a general rule, a phase margin of approximately 45 degrees is desireable for maximum stability.

In order to investigate the stability in a switching regulator, it is usually necessary to examine the gain and phase shift characteristics of each of the functional blocks that make up the system. Then a gain and phase vs. frequency plot is constructed for each block and combined to generate a composite frequency response of the total system. The gain of each block can be added algebraically (in dB) to obtain the overall loop gain. Then, the combined gain and phase characteristics can be examined to calculate the overall phase margin. If the overall phase margin is less than 45 degrees, it is usually necessary to modify the system to enhance its stability.

The functional blocks which contribute most of the loop gain and phase shift are the error amplifier and the output LC filter. However, the sampling network and pulse width modulator must also be considered.

Gain and phase shift of the LC network is of most importance since it contributes most of the phase shift in the loop. Figure 13 shows a plot of phase shift vs. frequency for an LC filter. Note that with high values of $(R/\sqrt{LC})$, the phase shift approaches -180 degrees. Figure 14 shows a plot of gain vs. frequency for the same filter. For high values of $(R/\sqrt{LC})$, the resonant peak becomes dominant.

Gain and phase plot of the error amplifier are usually provided in the manufacturer's data sheet. By tailoring the feedback network around the amplifier, it is possible to alter the closed loop frequency response for improved stability. There are various compensation and feedback techniques, such as lead, lag, and integrating networks, that will produce different gain and phase responses.

The sampling network in most switched mode power supplies is usually a resistive network to level shift the output voltage to a suitable range for the error amplifier. This contributes some voltage attenuation but no phase shift.

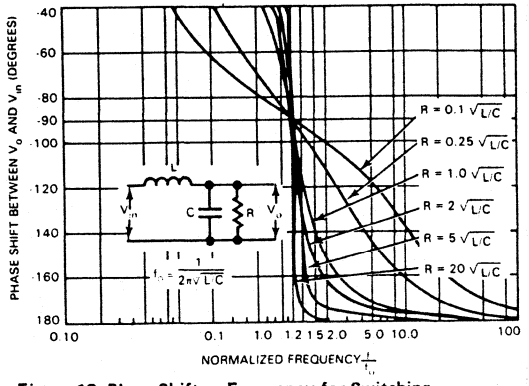


Figure 13. Phase Shift vs Frequency for Switching Regulator LC Filter

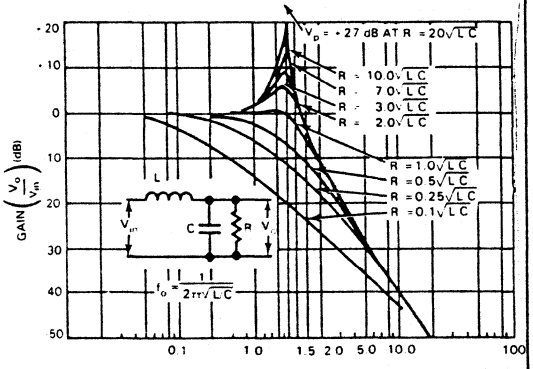


Figure 14. Gain vs Frequency for Switching Regulator LC Filter

SELECTION OF EXTERNAL COMPONENTS

Switching regulator systems require the use of external inductors, capacitors, switching transistors, and diodes, in addition to the basic controller IC chip. In this section, some of the requirements of design and selection criteria for these external components shall be reviewed.

Selecting the Inductors

In the selection of the inductor, one important criteria is the choice of the core material. The core must provide the desired inductance without saturating magnetically at the maximum peak current. In this respect, each core has a specific energy storage capability, LI^2_{sat}, where I_{sat} is the magnetic saturation current of the inductor.

The window area for the core winding must permit the number of turns necessary to obtain the required inductance with a wire size that has acceptable dc losses in the winding at maximum peak current. Each core has a specific dissipation capability, LI^2, that will result in a specific power loss or temperature rise. This temperature rise, plus the ambient temperature, must not exceed the Curie temperature of the core.

The value of the inductance, L, can be related to the basic core parameters and the total number of turns, N, in the wound core as:

$$L = N^2 \times 0.4\,\pi\,\mu\,A_e\,l_e \times 10^{-5} \qquad (7.1)$$

where:

- μ = effective permeability of core
- ee = effective magnetic path length (cm)
- Ae = effective magnetic cross section (cm^2)

Another useful inductor parameter is the inductor index, A_L, which is defined as:

$$A_L = 0.4\,\pi\,\mu\,A_e\,l_e \times 10 \text{ (mH/1000 turns)} \qquad (7.2)$$

From these equations, the magnetic energy, (LI^2), stored in the core at a given current level can be written as:

$$LI^2 = (NI)^2\,(A_L \times 10^{-6}) \text{ (millijoules)} \qquad (7.3)$$

The maximum ampere turn capability, (NI), of a given inductor is limited by the magnetic saturation of the core material. If the inductor index, A_L, and the saturation current, I_{sat}, are given for a particular inductance value, the maximum ampere turns can be calculated from Eq. (7.3).

If the saturation flux density, B_{sat}, is given, then the maximum energy which can be stored in the inductor can be expressed as:

$$LI^2 = \frac{(B_{SAT})^2\,(A_e^2 \times 10^{-4})}{A_L} \text{ (millijoules)} \qquad (7.4)$$

The core selected for an application must have an LI^2_{sat} value greater than calculated, to insure that the core does not saturate under maximum peak current conditions.

In switching regulator applications, power dissipation in the inductor is almost entirely due to dc losses in the winding. The dc resistance of the winding, R_W, can be calculated as:

$$R_W = P(l_W/A_W))\,N \qquad (7.5)$$

where:

- P = resistivity of wire (Ω/cm)
- w = length of turn (cm)
- A_W = effective area of wire (cm^2)

Core geometry provides a certain window area, A_C, for the winding. The effective area, A'_C, is 0.5 A_C for toroids and 0.65 A_C for pot cores. Equation (7.6) relates the number of turns, area of wire, and effective window area of a fully wound core:

$$A_W = A'_C/N \ (cm^2) \qquad (7.6)$$

From Eq. (7.5) and (7.6), the power dissipation, P_W, in the inductor winding can be calculated as:

$$P_W = I^2R_W = I^2P\frac{l_W}{A'_C}N^2 \qquad (7.7)$$

Substituting for N and rearranging:

$$LI^2 = P_W\,\frac{A_LA_C}{Pl_W} \times 10^{-6} \text{ (millijoules)} \qquad (7.8)$$

Equation (7.8) shows that the LI^2 capability is directly related to and limited by the maximum permissible power dissipation. One procedure for designing the inductor is as follows:

1. Calculate the inductance, L, and the peak current, I_{PK}, for the application. The required energy storage capability of the inductor, LI^2_{PK}, can now be defined (7.4) or (7.8),
2. Next, from Eq. (0.0) or (0.0), calculate the maximum LI^2_{sat} capability of the selected core, where:

$$LI^2_{sat} > LI^2_{PK}$$

3. From Eq. (7.1), calculate the number of turns, N, required for the specified inductance, L, and finally, from Eq. (7.5), the power dissipation, P_W. P_W should be less than the maximum permissible power dissipation of the core.
4. If the power losses are unacceptable, a larger core or one with a higher permeability is required, and steps 1 through 3 will have to be repeated.

Several design cycles are usually required to optimize the inductor design. With a little experience, educated guesses as to core material and size come close to requirements.

Selection of Switching Components

The designer should be fully aware of the capabilities and limitations of power transistors used in switching applications. Transistors in linear applications operate around a quiescent point, whereas in switching applications, operation is fully on or fully off. Transistors must be selected and tested to withstand the unique stress caused by this mode of operation. Parameters such as current and voltage ratings secondary breakdown ratings, power dissipation, saturation voltage and switching times, critically affect transistor performance in switching applications. Similar parameters are important in diode selection, including voltage, current, and power limitations, as well as forward voltage drop and switching speed.

Initial selection can begin with the voltage and current requirements. Voltage ratings of the switching transistor and diode must be greater than the maximum input voltage including any transient voltages that may appear at the input of the switching regulator. Transistor saturation voltage, $V_{CE(sat)}$, and diode forward voltage, V_D, at full load output current should be as low as possible to maintain high operating efficiency. The transistor and diode should be selected to handle the required maximum peak current and power dissipation.

Good efficiency requires fast switching diodes and transistors. Transistor switching losses become significant when the combined rise, t_r, plus fall time, t_f, exceeds:

$$0.05\ (t_{on} + t_{off})$$

For 20 kHz operation, $t_r + t_f$ should be less than 2.5 μs for maximum efficiency. While transistor delay and storage times do not affect efficiency, delays in turn-on and turn-off can result in increased output voltage ripple. For optimal operation, combined delay time, t_d, plus storage time, t_s, should be less than:

$$0.05\ (t_{on} + t_{off})$$

Selection of Filter Capacitors

In general, output capacitors used in switching regulators are large (> 100 μF), must operate at high-frequencies (> 20 kHz), and require low ESR and ESL. An excellent trade-off between cost and performance is the solid tantalum capacitor, constructed of sintered tantalum power particles packed around a tantalum anode, which makes a rigid assembly or slug. Compared to aluminum electrolytic capacitors, solid tantalum capacitors have higher CV product-per-unit volume, are more stable, and have hermetic seals to eliminate the effects of humidity.

Reducing Electromagnetic Interference (EMI)

Due to the wiring inductance in a circuit, rapid changes in current generate voltage transients. These voltage spikes are proportional to both the wiring inductance and the rate at which the current changes:

$$V = -L \frac{di}{dt}$$

The energy of the voltage spike is proportional to the wiring inductance and the square of the current:

$$E = 1/2\ LI^2$$

Interference and voltage spiking are easier to filter, if the energy in the spikes is low and the components predominantly high-frequency.

To minimize the EMI problem, the following precautions are recommended:

- Keep loop inductance to a minimum by utilizing appropriate layout and interconnect geometry.
- Keep loop area and lead lengths as small as possible and, in step-down mode, return the input capacitor directly to the diode to reduce EMI and ground-loop noise.
- Select an external diode that can hold peak recovery current as low as possible. This reduces the energy content of the voltage spikes.

5

EXAR ...the analog plus™ company

PRODUCT ORDERING INFORMATION

Part Identification

XX	XXXXX	X	X	883C
Manufacturer's Prefix	Basic Type	Case Outline	Lead Finish	Screening

XR = Exar Corporation

Case Outline (See MIL-M-38510H, Figure C-I)

P = 8 Lead Ceramic DIP
E = 16 Lead Ceramic DIP
C = 14 Lead Ceramic DIP
Q = 40 Lead Ceramic DIP
L = 24 Lead Ceramic DIP
Y = 28 Lead Ceramic DIP
X = 44 Lead Ceramic Leadless Chip Carrier
Z = 32 Lead Ceramic Leadless Chip Carrier

Lead Finish (See MIL-M-38510H, Paragraph 3.6.2.7)

A = Hot Solder DIP
C = Gold Plate (used for LCC packages only)

Screening

883C = MIL-STD-883C, Class B, Revision C. The device is processed with 883, Revision C, Class B Screening. This includes electrical test at -55°C to + 125°C.

Example: XR146EA883C

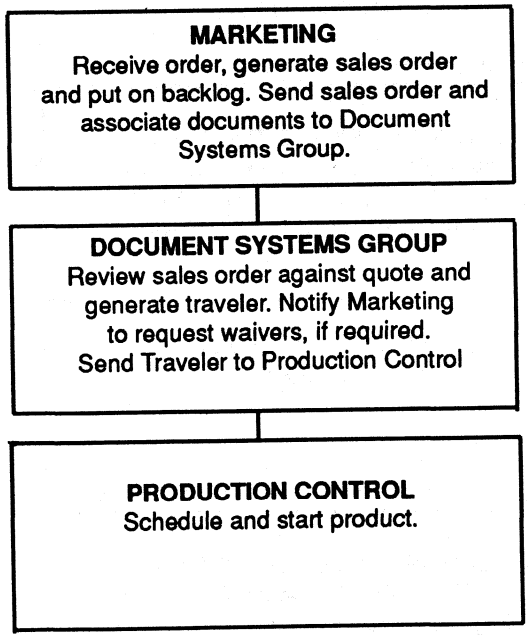
XR	146	E	A	883C
Manufacturer's Prefix	Basic Type	Case Outline	Lead Finish	Screening

DOCUMENTATION SYSTEMS

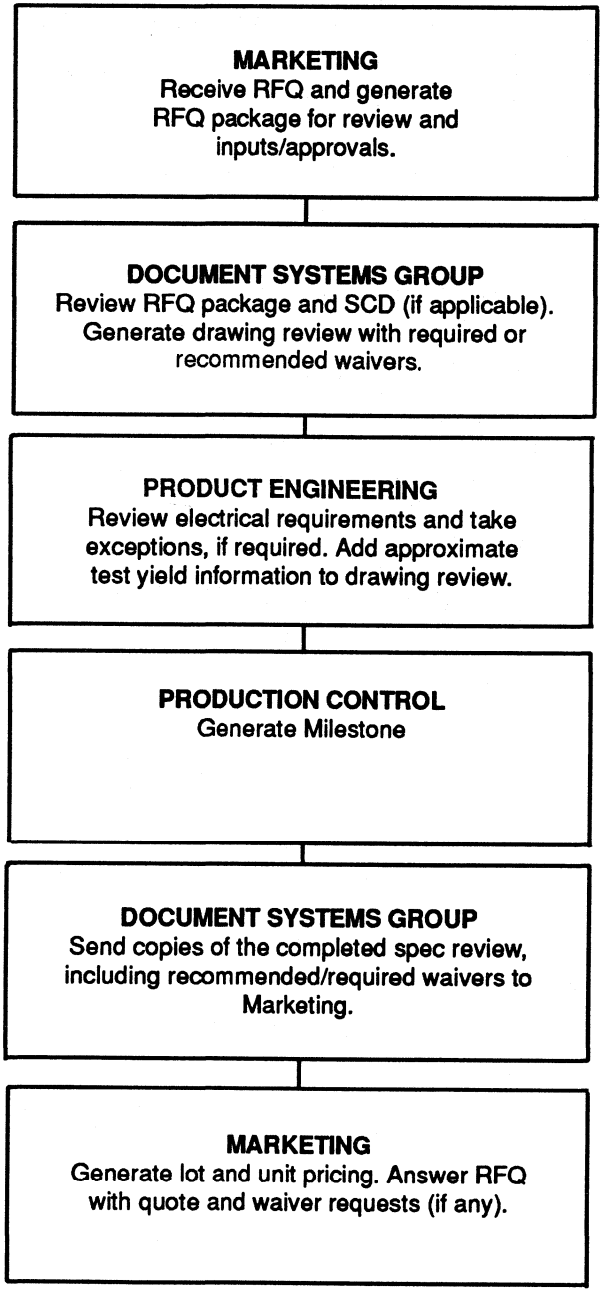
Documentation Systems maintains a program to ensure that the revision level of documents is correct for the design, manufacture and test of product. This program includes change control notification and the maintenance of historical records for documents.

Documentation Systems also reviews customer specifications and purchase orders and generates customized internal travelers to assure compliance to customer requirements.

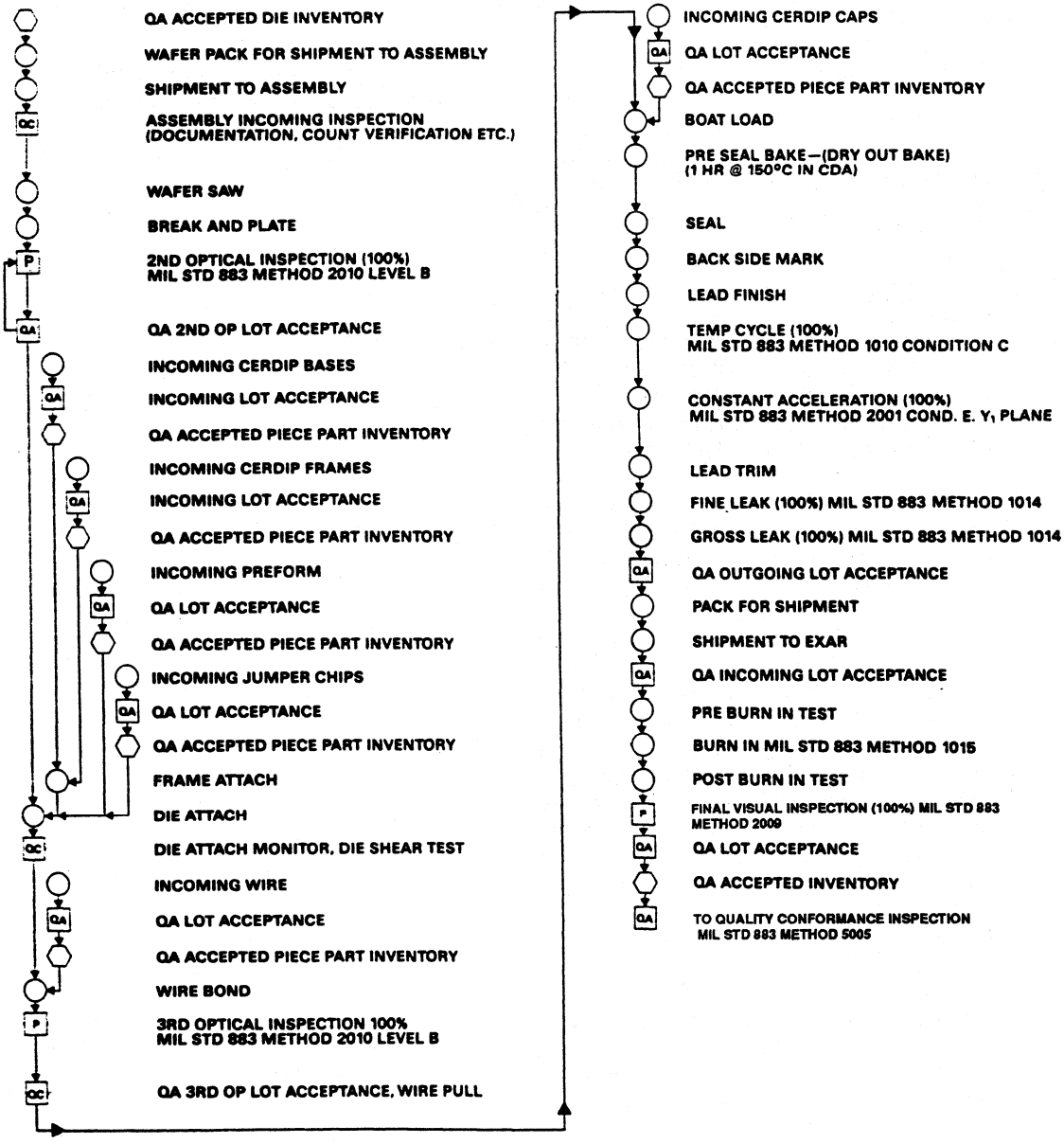
MILITARY ORDER ENTRY



RFQ FLOW FOR MILITARY PRODUCT



MILITARY STANDARD 883C SCREENING FLOW



LEGEND

ACCEPTED MATERIAL PROCESS QA INSPECTION

P = PRODUCTION QA = QUALITY ASSURANCE QC = QUALITY CONTROL

6

QUALITY CONFORMANCE INSPECTION MIL-STD-883 REV. C, METHOD 5005, GROUPS A, B, C AND D

EXAR will be performing Method 5005 Q.C.I. in accordance with paragraph 4.5 of MIL-M-38510. Group A consists of sample electrical testing and is performed on each lot. Group B consists of assembly related construction testing and is also performed on each lot. Group C is primarily a test of die reliability. Group C is performed on one lot of each microcircuit group for each twelve months of wafer fabrication. Group D is performed on one lot of each package type for each twelve months of production. The twelve month time period for Group D is based on date of seal. The date of seal also determines the date code for the lot.

EXAR will maintain Group A and Group B test data for each lot of 883C devices. EXAR will also have generic test data for Group C and Group D for each lot of 883C devices. Group C and Group D generic test data may not be from the same lot as the production (shippable) parts. However, Group C generic test data will be from a device lot in the same microcircuit group as the production lot. The data will fall within the 12 month time frame. Similarly Group D generic test data will be from a lot with the same package type as the production lot. The data will fall within the 12 month time frame.

Group A and B test data as well as Group C and D generic test data will be available at a nominal charge for all EXAR 883C standard product. Customers requiring group test data from their particular production lot will be charged full price. In any case, customer requirements for QCI test data are best negotiated at the time of RFQ. Please consult your EXAR distributor, sales representative or the factory for details of price and availability of QCI test data.

SOURCE INSPECTION

Source inspection is the surveillance by a customer's quality representative at the manufacturer's plant of devices being screened by the manufacturer. There are several points in the screening process where customers may request source inspection. The most popular is a final source inspection which typically includes a review of all the documentation for the lot and witnessing electrical test on a sample basis. Other points for source inspection, can be pre-cap visual inspection, post-cap visual inspection, burn-in and environmental testing.

It is Exar policy to charge for all source inspections per source point and per lot. It is advisable to request source inspection at the time a purchase order is placed or before. Customers requesting to witness 100% of final electrical test will be charged in addition to the normal charge for witnessing on a sample basis. Also, the majority of Exar's assembly work is being done offshore. This makes pre-cap visual inspection impractical. Customers may either request post-cap visual inspection on an LTPD basis or onshore assembly at an extra cost. Please consult the factory for details.

DATA CAPABILITY

With each shipment of Exar 883C product the customer will receive a Certificate of Conformance. An example of this Certificate is shown here. Also upon request, Method 5005 Group A and B attributes data is available at no charge. Attributes data indicates the total number of devices subjected to and passing or failing the various screening steps. Generic attributes data is available for Method 5005, Group C and D upon request at a nominal charge. Customers may also request assembly lot travelers and screening lot travelers.

Variables data, commonly known as read and record data, gives actual parametirc values measured for each device. Variables data is not available unless specifically requested prior to placing an order. There is an extra charge for variables data.

For devices built to a customer's source control drawing Group A and B attributes data is available upon request at no charge. However if Group C and D attributes data is required upon a customer's specific lot and generic data is not sufficient then an extra charge will be assessed. Again, customers are asked to clarify all data requirements prior to placing an order. Please consult the factory for further details.

GROUP A ELECTRICAL TEST[1]

Subgroups Quantity/accept no. = 116/0
Subgroup 1 Static tests at 25°C
Subgroup 2 Static tests at maximum rated operating temperature
Subgroup 3 Static test at minimum rated operating temperature
Subgroup 4 Dynamic tests at 25°C
Subgroup 5 Dynamic test at maximum rated operating temperature
Subgroup 6 Dynamic tests at minimum rated operating temperature
Subgroup 7 Functional tests at 25°C
Subgroup 8A Functional tests at maximum rated operating temperature
Subgroup 8B Functional tests at minimum rated operating temperature
Subgroup 9 Switching test at 25°C
Subgroup 10 Switching tests at maximum rated operating temperature
Subgroup 11 Switching tests at minimum rated operating temperature

[1] The specific parameters to be included for tests in each subgroup shall be as specified in the applicable procurement document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

GROUP B TEST FOR CLASS B[1]

Test	MIL-STD-883		Quantity/(accept no.) or LTPD
	Method	Condition	
Subgroup 2 (a) Resistance to solvents	2015		4(0)
Subgroup 3 (a) Solderability[4]	2022 or 2003	Soldering temperature of 245 ± 5°C	10
Subgroup 5 (a) Bond strength[5] (1) Thermocompression (2) Ultrasonic or wedge (3) Flip-chip (4) Beam lead	2011	 (1) Test condition C or D (2) Test condition D or D (3) Test condition F (4) Test condition H	15

[1] Post burn in electrical reject from the same inspection lot may be used for all subgroups when end-point measurements are not required.

[4] All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin fusing after burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.

[5] Test samples for bond strength may, at all manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection, prior to sealing provided all other specifications requirements are satisfied (e.g. bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the LTPD sample size for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds).

GROUP C (DIE-RELATED TEST) (FOR CLASS B ONLY)

Test	MIL-STD-883		Quantity/(accept no.) or LTPD
	Method	Condition	
Subgroup 1 (a) Steady state life test	1005	Test condition to be specified (1,000 hours at 125°C)	5
(b) End-point electrical		As specified in the applicable device specification	

GROUP D (PACKAGE RELATED TEST) (FOR ALL CLASSES)

Test[1]	MIL-STD-883		Quantity/(accept no.) or LTPD
	Method	Condition	
Subgroup 1[2] (a) Physical dimensions	2016		15
Subgroup 2[2] (a) Lead integrity[3] (b) Seal[4] (1) Fine (2) Gross	2004 1014	Test condition B_2 (lead fatigue) As applicable	15
Subgroup 3[5] (a) Thermal shock (b) Temperature cycling (c) Moisture resistance[6] (d) Seal (1) Fine (2) Gross (e) Visual examination (f) End-point electrical parameters[7]	1011 1010 1004 1014	Test condition B as a minimum, 15 cycles minimum. Test condition C, 100 cycles minimum. As applicable Per visual criteria of method 1004 and 1010 As specified in the applicable device specification	15
Subgroup 4[5] (a) Mechanical shock (b) Vibration, variable frequency (c) Constant acceleration (d) (e) Visual examination (f) End-point electrical parameters	2002 2007 2001 8	Test condition B minimum Test condition A minimum Test condition E minimum (see 3), Y_1 orientation only As specified in the applicable device specification	15
Subgroup 5[2] (a) Salt atmosphere[6] (b) Seal (1) Fine (2) Gross (c) Visual examination	1009 1014	Test condition A minimum As applicable Per visual criteria of method 1009	15(0)
Subgroup 6[2] (a) Internal water-vapor content	1018	5,000 ppm maximum water content at 100°C	3(0) or 5(1)[9]

See footnotes on following page.

GROUP D (PACKAGE RELATED TESTS) (FOR ALL CLASSES) (Continued)

Test	MIL-STD-883		Quantity/(accept no.) or LTPD
	Method	Condition	
Subgroup 7[2] (a) Adhesion of lead finish 10,11	2025		15(0)
Subgroup 8 (a) Lid torque[2,12]	2024		5(0)

1. In-line monitor data may be substituted for subgroups D1, D2, D6, D7, and D8 upon approval by the qualifying activity. The monitors shall be performed by package type and to the specified subgroup test method(s). The monitors sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. This in-line monitor data shall be traceable to the specific inspection lot (s) represented (accepted or rejected) by the data.
2. Electrical reject devices from that same inspection lot may be used for samples.
3. For leadless chip carrier packages only, use test condition D. For leaded chip carrier packages, use condition B1. For pin grid array leads and rigid leads use method 2028.
4. Seal test (subgroup 2b) need be performed only on packages having leads exiting through a glass seal.
5. Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".
6. Lead bend stress initial conditioning is not required for leadless chip carrier packages.
7. At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.
8. Visual examination shall be in accordance with method 1010 or 1011.
9. Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e., 3 or 5 devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with 5 additional devices. from the same lot.
10. The adhesion of lead finish test shall not apply for leadless chip carrier packages.
11. LTPD based on number of leads.
12. Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (i.e., whenever frit seal establishes hermeticity or package integrity).

EXAR
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TWX 910 339 9233

QUALITY CONTROL
DELIVERABLE DOCUMENTATION CHECKLIST
AND
CERTIFICATE OF CONFORMANCE

PART NO. AND REV.	SALES ORDER NO:	QUANTITY SHIPPED:
CUSTOMER NAME:	PURCHASE ORDER NO:	PRODUCT I.D. CODE:
ADDRESS:		
CUSTOMER DETAIL DWG. NO. AND REV.	CUSTOMER PART NO:	DATE CODE:
CUSTOMER GENERAL DWG. NO. AND REV.	LOT NUMBER/WAFER RUN NO:	TRAVELOG NO:
PRODUCT ASSURANCE LEVEL:		

DOCUMENTATION ITEM	Req'd	N/A	See Remark	DOCUMENTATION ITEM	Req'd	N/A	See Remark
CUSTOMER WAIVER(S)				SEM PHOTOS AND REPORT			
CUSTOMER SOURCE INSPECTION (CSI)				X-RAY PHOTOS AND REPORT			
GOVERNMENT SOURCE INSPECTION (GSI)				DESTRUCT UNIT SAMPLES			
TEST DATA				ADDITIONAL SAMPLES			
GENERIC DATA				SPECIAL PACKAGING			
QUALITY CONFORMANCE TESTS (GRP A, B, C & D)				SPECIAL MARKING ON PARTS			
FAILURE ANALYSIS REPORT				SPECIAL LABELING ON CONTAINER			
FORM DD 250 & 1149							

REMARKS:

CERTIFICATE OF CONFORMANCE

We certify that the articles and/or services listed and shipped herewith under your purchase order mentioned above have been inspected and are in full requirements of said purchase order and the drawings and specifications applicable to that order. We certify that inspection evidence, including test data, necessary to substantiate this certification is available from our files.

EXAR Corporation

QUALITY CONTROL _____ STAMP _____ SHIPPING DATE _____

200336

MICROCIRCUIT GROUP ASSIGNMENTS
PER 38510 APPENDIX E

Microcircuit Group 49 - 146 (bipolar op amps)

Microcircuit Group 54 - 2240 (timers)

Microcircuit Group 52 - 1524, 1543 (regulators)

Microcircuit Group - Tone Decoders-567, 567A, L567, 2567

Microcircuit Group - Function Generator - 2206, 2207, 2209, 8038

Microcircuit Group - Phase Locked Loops - 210, 2211, 2212, 2208

Microcircuit Group - UARTs - 68C681, 88C681, 82C684

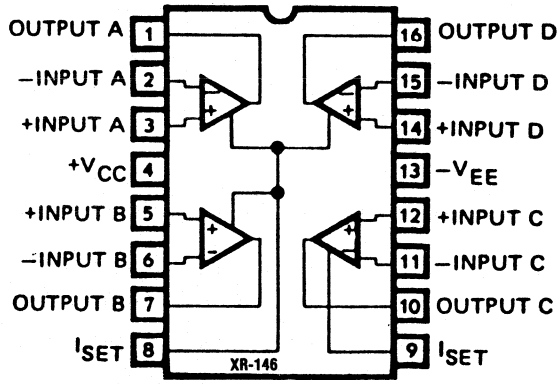
Programmable Quad Operational Amplifiers

GENERAL DESCRIPTION

The XR-146 family of quad operational amplifiers contain four independent high-gain, low-power, programmable op-amps on a monolithic chip. The use of external bias setting resistors permit the user to program gain-bandwidth product, supply current, input bias current, input offset current, input noise and the slew rate.

The basic XR-146 family of circuits offer partitioned programming of the internal op-amps where one setting resistor is used to set the bias levels in the three op-amps, and a second bias setting is used for the remaining op-amp.

FUNCTIONAL BLOCK DIAGRAMS



FEATURES

Programmable
Micropower operation
Low noise
Wide power supply range
Class AB output
Ideal pin out for biquad active filters
Overload protection for input and output
Internal frequency compensation

APPLICATIONS

Total Supply Current = 1.4 mA (I_{SET}/10 μA)
Gain Bandwidth Product = 1 MHz (I_{SET}/10μA)
Slew Rate = 0.4V/μs (I_{SET}/10 μA)
Input Bias Current ≅50 nA (I_{SET}/10 μA)

I_{SET} = Current into pin 8, pin 9 (see schematic)

$$I_{SET} = \frac{V+ - V- - 0.6V}{R_{SET}}$$

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
XR-146	±22V
Differential Input Voltage	
XR-146	±30V
Common Mode Input Voltage	
XR-146	±15V
Power Dissipation	
XR-146	900 mW
Output Short Circuit Duration	
XR-146	Indefinite
Maximum Junction Temperature	
XR146	150°C
Storage Temperature Range	
XR-146	−65°C to +150°C

Rev-A

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-146

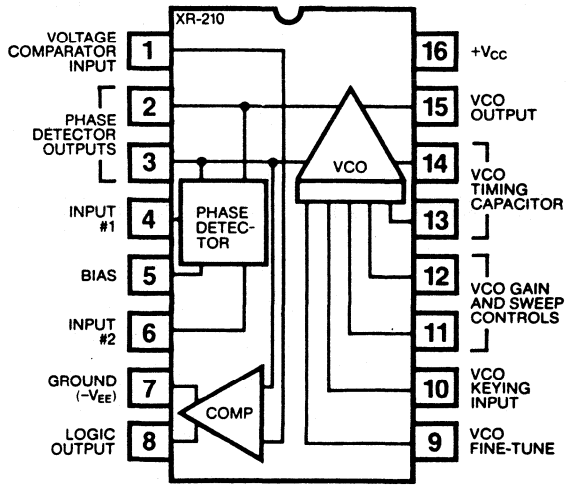
TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current	Icc	Vs = ±15V ISET = 10μA	T_A = +25°C -55°C≤T_A≤+125°C		2.00 2.00	mA mA	1 2, 3
Supply Current	Icc	Vs = ±22V ISET = 10μA	T_A = +25°C		4.00	mA	1
Input Offset Voltage	Vos	Vs = ±15V, Rs = 50Ω ISET = 10μA	T_A = +25°C -55°C≤T_A≤+125°C		5.00 6.00	mV mV	1 2, 3
Input Bias Current	Ib	Vs = ±15V, Rs = 10KΩ ISET = 10μA	T_A = +25°C -55°C≤T_A≤+125°C		100 100	nA nA	1 2, 3
Input Offset Current	Ios	Vs = ±15V, Rs = 100KΩ ISET = 10μA	T_A = +25°C -55°C≤T_A≤+125°C		20 25	nA nA	1 2, 3
Power Supply Rejection Ratio	PSRR	Rs = 10KΩ ±10V≤Vs≤±15V	T_A = +25°C -55°C≤T_A≤+125°C	 76	100	uV/V dB	1 2, 3
Common Mode Rejection Ratio	CMRR	VCM = ±13.5V Vs = ±15V, RL = 10KΩ	T_A = +25°C -55°C≤T_A≤+125°C	80 70		dB dB	1 2, 3
Large Signal Voltage Gain	AVO	Vo = ±10V, Rs = 50Ω Vs = ±15V, RL = 10KΩ	T_A = +25°C	100		V/mV	4
		Vo = ±10V Vs = ±15V, RL = 10KΩ	-55°C≤T_A≤+125°C	50		V/mV	5, 6
Output Voltage Swing	Vo	RL = 10KΩ Vs = ±15V, Rs = 125Ω	T_A = +25°C	±12		V	4
		Vs = ±15V, RL = 10KΩ	-55°C≤T_A≤+125°C	±12		V	5, 6
Short Circuit Current	Isc	Vs = ±15V, Rs = 50Ω	T_A = +25°C	5	30	mA	1
Supply Current	Icc	Vs = ±15V, ISET = 1μA	T_A = +25°C		250	μA	1
Input Offset Voltage	Vos	Rs = 50Ω, Vs = ±15V ISET = 1μA	T_A = +25°C		5.00	mV	1
Input Bias Current	Ib	Rs = 10KΩ, Vs = ±15V ISET = 1μA	T_A = +25°C		20	nA	1
Input Offset Voltage	Vos	Rs = 50Ω, Vs = ±1.5V ISET = 10μA	T_A = +25°C		5.00	mV	1
Common Mode Rejection Ratio	CMRR	Rs = 50Ω, Vs = 1.5V VCM = ±0.7V	T_A = +25°C	60		dB	1
Output Voltage Swing	Vo	RL = 10KΩ, Rs = 50Ω Vs = ±1.5V, ISET = 10μA	T_A = +25°C	±0.6		V	4

FSK Modulator/Demodulator

GENERAL DESCRIPTION

The XR-210 is a highly versatile monolithic phase-locked loop system, especially designed for data communications. It is particularly well suited for FSK modulation/demodulation (MODEM) applications, frequency synthesis, tracking filters, and tone decoding. The XR-210 operates over a power supply range of 5V to 26V, and over a frequency band of 0.5 Hz to 20 MHz. The circuit can accommodate analog signals between 300 μV and 3V, and can interface with conventional DTL, TTL, and ECL logic families.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Wide Frequency Range	0.5 Hz to 20 MHz
Wide Supply Voltage Range	5V to 26V
Digital Programming Capability	
RS-232C Compatible Demodulator Output	
DTL, TTL and ECL Logic Compatibility	
Wide Dynamic Range	300 μV to 3V
ON-OFF Keying & Sweep Capability	
Wide Tracking Range	±1% to ±50%
Good Temperature Stability	200 ppm/°C
High-Current Logic Output	50 mA
Independent "Mark" and "Space" Frequency Adjustment	
VCO Duty Cycle Control	

APPLICATIONS

Data Synchronization
Signal Conditioning
FSK Generation
Tone Decoding
Frequency Synthesis
FSK Demodulation
Tracking Filter
FM Detection
FM and Sweep Generation
Wideband Discrimination

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 Volts
Power Dissipation	750 mW
Derate Above +25°C	6.0 mW/°C
Storage Temperature	−65°C to +150°C

Rev-C

SYSTEM DESCRIPTION

The XR-210 is made up of a stable wide-range voltage-controlled oscillator (VCO), exclusive OR gate type phase detector, and an analog voltage comparator. The VCO, which produces a square wave as an output, is either used in conjunction with the phase detector to form a phase-locked loop (PLL) for FSK demodulation and tone detection or as a generator in FSK modulation schemes. The phase detector when used in the PLL configuration produces a differentional output voltage with a 6 KΩ output impedance, which when capacitively loaded forms a single pole loop filter. The voltage comparator is used to sense the phase detector output and produces the output in the FSK demodulation connection.

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-210

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current	Icc	Vcc = ±6V	T_A = +25°C	5.0	16.0	mA	1
			-55°C≤T_A≤+125°C	5.0	**20.0**	mA	**2, 3**
Supply Current	Icc	Vcc = ±13V	T_A = +25°C		26.0	mA	1
			-55°C≤T_A≤+125°C		26.0	mA	**2, 3**
VCO Power Supply Stability	PSR	**±6V≤V_{CC}≤±12V**	T_A = 25°C		0.5	%/V	**9**
			-55°C≤T_A≤+125°C		1.0	%/V	**10, 11**
VCO Sweep Range	FSW		T_A = 25°C	5:1			**9**
			-55°C≤T_A≤+125°C	**3:1**			**10, 11**
VCO Duty Cycle Asymmetry	DC		T_A = +25°C		±3	%	**9**
			-55°C≤T_A≤+125°C		**±10**	%	**10, 11**
Phase Detector Output Offset Voltage		Measured Across Pin 1 and Pin 3, VIN = 0	T_A = +25°C		±150	mV	1
			-55°C≤T_A≤+125°C		±150	mV	**2, 3**
Logic Output Leakage Current	I_{OH}	**V_{CC} = ±12V**	T_A = +25°C		10.0	μA	1
		V_{CC} = ± 6V	-55°C≤T_A≤+125°C		100.0	μA	**2, 3**
Logic Output Low Voltage	V_{OL}	I_L = 10 mA	T_A = +25°C		0.4	V	1
			-55°C≤T_A≤+125°C		0.7	V	**2, 3**
Logic Output Sink Current	I_{SINK}	Vo≤1V	T_A = +25°C	30		mA	1
			-55°C≤T_A≤+125°C	25		mA	**2,3**

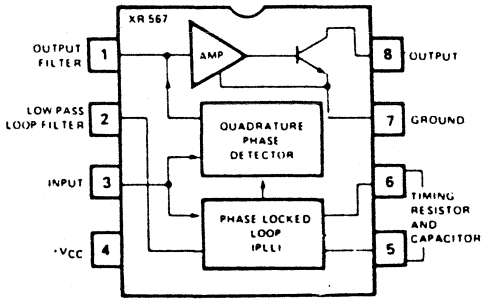
Monolithic Tone Decoder

GENERAL DESCRIPTION

The XR-567 is a monolithic phase-locked loop system designed for general purpose tone and frequency decoding. The circuit operates over a wide frequency band of 0.01 Hz to 500 kHz and contains a logic compatible output which can sink up to 100 milliamps of load current. The bandwidth, center frequency, and output delay are independently determined by the selection of four external components.

The circuit consists of a phase detector, low-pass filter, and current-controlled oscillator which comprise the basic phase-locked loop; plus an additional low-pass filter and quadrature detector that enables the system to distinguish between the presence or absence of an input signal at the center frequency.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Bandwidth adjustable from 0 to 14%.
Logic compatible output with 100 mA current sinking capability
High stable center frequency.
Center frequency adjustable from 0.01 Hz to 500 kHz
Inherent immunity to false signals
High rejection of out-of-band signals and noise
Frequency range adjustable over 20:1 range by external resistor.

APPLICATIONS

Touch-Tone® Decoding
Sequential Tone Decoding
Communications Paging
Ultrasonic Remote-Control
Telemetry Decoding

ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Derate Above +25°C	2.5 mW/°C
Temperature	
Storage	−65°C to +150°C

Rev-B

SYSTEM DESCRIPTION

The XR-567 monolithic tone decoder consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection on in-band signals. The device has a normally high open collector output capable of sinking 100 mA.

The input signal is applied to Pin 3 (20 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6 and can typically reach 500 kHz. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; bandwidth and skew are also dependent upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 4 is $+V_{CC}$ (4.75 to 9V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is open collector output, pulling low when an in-band signal triggers the device.

In applications requiring two or more 567-type devices, consider the XR-2567 dual tone decoder. Where center frequency accuracy and drift are critical, compare the XR-567A. Investigate employing the XR-L567 in low power circuits.

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-567

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current Quiescent	Icc	Vcc = +5V	T_A = +25°C		8.00	mA	1
			-55°C≤T_A≤+125°C		**9.80**	mA	**2, 3**
Supply Current Quiescent	Icc	Vcc = +9V	T_A = +25°C		20.00	mA	1
			-55°C≤T_A≤+125°C		18.00	mA	**2, 3**
Highest Center Frequency	Fc	Vcc = +9V Vin = 300 mVrms	T_A = +25°C	100		KHz	**9**
			-55°C≤T_A≤+125°C	100		KHz	**10, 11**
Center Frequency Drift with Supply	DRFT	4.75V≤Vcc≤6.75V	T_A = +25°C		1.00	%/V	**9**
			-55°C≤T_A≤+125°C		6.00	%/V	**10, 11**
Output Saturation Voltage	VSAT	Ic = 30 mA Vin = 30 mVrms	T_A = +25°C		0.4	V	1
			-55°C≤T_A≤+125°C		0.4	V	**2, 3**
Output Saturation Voltage	VSAT	Ic = 100 mA Vin = 30 mVrms	T_A = +25°C		1.0	V	1
			-55°C≤T_A≤+125°C		**1.2**	V	**2, 3**
Output Leakage Current	I_{OL}	Vin = 7.5 mVrms	T_A = +25°C		25	µA	1
			-55°C≤T_A≤+125°C		**50**	µA	**2, 3**
Largest No Output Input Voltage	V_{IL}		T_A= +25°C	10		mVrms	7
			-55°C≤T_A≤+125°C	**5**		mVrms	**8**
Smallest Detectable Input Voltage	V_{IS}		T_A = +25°C		25	mVrms	7
			-55°C≤T_A≤+125°C		50	mVrms	**8**
Largest Detection Bandwidth	LDBW		T_A = +25°C	12.0	16.0	%	4
			-55°C≤T_A≤+125°C	**7.0**	**19.0**	%	**5, 6**
Largest Detection Bandwidth Skew	SKEW		T_A = +25°C		2.0	%	4
			-55°C≤T_A≤+125°C		**4.0**	%	**5, 6**
Supply Current Activated	Icc	Vcc = +5V	T_A = +25°C		13.0	mA	1
			-55°C≤T_A≤+125°C		**14.5**	mA	**2, 3**

Precision Tone Decoder

GENERAL DESCRIPTION

The XR-567A provides all the necessary circuitry for constructing a variety of tone detectors and frequency decoders. Phase-locked loop circuit techniques are used to provide operation from 0.01 Hz tp 500 kHz. The circuit also features an input preamp, a high-current logic output, and programmable output delay.

The XR-567A, available in an 8-Pin DIL package, is designed to offer improved frequency accuracy and drift characteristics over the standard industry 567. These changes offer improved overall circuit performance, while reducing initial circuit adjustments.

FEATURES

Programmable Detection Bandwidth	0% to 14%
Logic Output	100 mA
Wide Center Frequency Range	0.01 Hz to 500 kHz
High Rejection of Out-of-Band Signals and Noise	
Direct Replacement for standard 567	
Inherent immunity to out-of-band signals & noise	

APPLICATIONS

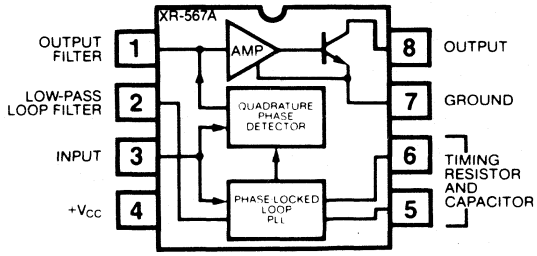
Tone Detection
Touch-Tone® Decoding
Communications Paging
Ultrasonic Remote Control
Precision Oscillator
Wireless Intercom
Carrier-Tone Transceiver
FSK Demodulation
Dual Time Constant Tone Detector

ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation	
Ceramic Package	385 mW
Derate above 25°C	2.5 mW/°C
Storage Temperature Range	−65°C to +150°C

REV-B

FUNCTIONAL BLOCK DIAGRAM



6

SYSTEM DESCRIPTION

The XR-567A is an improved version of the popular 567 tone decoder. Center frequency accuracy is guaranteed by design modifications and testing to 5%, and is typically better than 2%. Temperature drift of the center frequency is also improved. Thus, in most applications, no trimming is required.

The XR-567A monolithic tone decoder consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. The device has a normally high open collector output capable of sinking 100 mA.

The input signal is applied to Pin 3 (20 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6 and can typically reach 500 kHz. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; bandwidth and skew are also dependant upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 4 is $+V_{CC}$ (4.75 to 9V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is open collector output, pulling low when an in band signal triggers the device.

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-567A

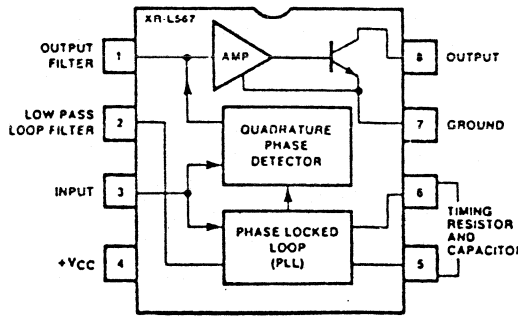
TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current Quiescent	Icc	Vcc = +5V	T_A = +25°C		8.00	mA	1
			-55°C≤T_A≤+125°C		**9.80**	mA	2, 3
Supply Current Quiescent	Icc	Vcc = +9V	T_A = +25°C		20.00	mA	1
			-55°C≤T_A≤+125°C		18.00	mA	2, 3
Supply Current Activated	Icc	Vcc = +5V VIN = 300 mVrms	T_A = +25°C		13.00	mA	1
			-55°C≤T_A≤+125°C		**14.50**	mA	2, 3
Highest Center Frequency	Fc	Vcc = +5V	T_A = +25°C	100		KHz	9
			-55°C≤T_A≤+125°C	100		KHz	10, 11
Center Frequency Drift with Supply	DRFT	4.75V≤Vcc≤6.75V	T_A = +25°C		1.00	%/V	9
			-55°C≤T_A≤+125°C		6.00	%/V	10, 11
Output Saturation Voltage	VSAT	Ic = 30 mA Vin = 30 mVrms	T_A = +25°C		0.4	V	1
			-55°C≤T_A≤+125°C		0.4	V	2, 3
Output Saturation Voltage	VSAT	Ic = 100 mA Vin = 30 mVrms	T_A = +25°C		1.0	V	1
			-55°C≤T_A≤+125°C		**1.20**	V	2, 3
Output Leakage Current	I_{OL}	Vin = 7.5 mVrms	T_A = +25°C		25	µA	1
			-55°C≤T_A≤+125°C		**50**	µA	2, 3
Largest No Output Input Voltage	V_{IL}		T_A= +25°C	10		mVrms	7
			-55°C≤T_A≤+125°C	**5**		mVrms	8
Smallest Detectable Input Voltage	V_{IS}		T_A = +25°C		25	mVrms	7
			-55°C≤T_A≤+125°C		50	mVrms	8
Largest Detection Bandwidth	LDBW		T_A = +25°C	12.0	16.0	%	4
			-55°C≤T_A≤+125°C	**7.0**	**19.0**	%	5, 6
Largest Detection Bandwidth Skew	SKEW		T_A = +25°C		2.0	%	4
			-55°C≤T_A≤+125°C		**4.0**	%	5, 6

Micropower Tone Decoder

GENERAL DESCRIPTION

The XR-L567 is a micropower phase-locked loop (PLL) circuit designed for general purpose tone and frequency decoding. In applications requiring very low power dissipation, the XR-L567 can replace the popular 567-type decoder with only minor component value changes. The XR-L567 offers approximately 1/10th the power dissipation of the conventional 567-type tone decoder, without sacrificing its key features such as the oscillator stability, frequency selectivity, and detection threshold. Typical quiescent power dissipation is less than 4 mW at 5 volts. It operates over a wide frequency band of 0.01 Hz to 60 kHz and contains a logic compatible output which can sink up to 10 milliamps of load current. The bandwidth, center frequency, and output delay are independently determined by the selection of four external components.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Very Low Power Dissipation (≈4 mW at 5V).
Bandwidth Adjustable from 0 to 14%.
Logic Compatible Output with 10 mA Current Sinking Capability.
Highly Stable Center Frequency.
Center Frequency Adjustable from 0.01 Hz to 60 kHz.
Inherent Immunity to False Signals.
High Rejection of Out-of-Band Signals and Noise.
Frequency Range Adjustable Over 20:1 Range by External Resistor.

APPLICATIONS

Battery-Operated Tone Detection
Touch-Tone® Decoding
Sequential Tone Decoding
Communications Paging
Ultrasonic Remote-Control
Telemetry Decoding

ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Storage Temperature	−65°C to +150°C

Rev-A

SYSTEM DESCRIPTION

The XR-L567 monolithic circuit consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. The device has a normally high open collector output.

The input signal is applied to Pin 3 (100 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; band-width and skew are also dependant upon the circuitry here. Pin 4 is $+V_{CC}$ (4.75 to 8V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is the open collector output, pulling low when an in-band signal triggers the device.

The XR-L567 is pin-for-pin compatible with the standard XR-567-type decoder. Internal resistors have been scaled up by a factor of ten, thereby reducing power dissipation and allowing use of smaller capacitors for the same applications compared to the standard part. This scaling also lowers maximum device center frequency and load current sinking capabilities.

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-L567

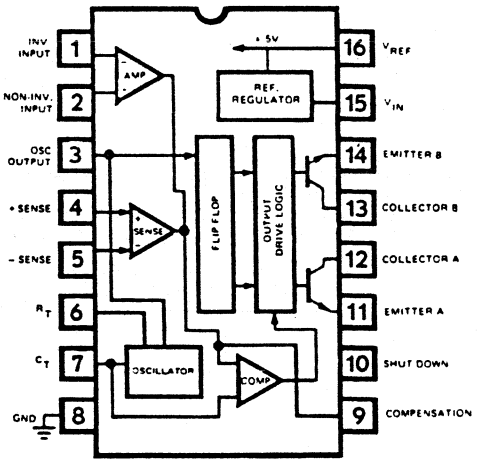
TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current Quiescent	Icc	Vcc = +5V	T_A = +25°C		1000	µA	1
			-55°C≤T_A≤+125°C		1000	µA	2, 3
Supply Current Quiescent	Icc	Vcc = +8V	T_A = +25°C		2000	µA	1
Supply Current Activated	Icc	Vcc = +5V	T_A = +25°C		1400	µA	1
			-55°C≤T_A≤+125°C		2000	µA	2, 3
Highest Center Frequency	Fc		T_A = +25°C	10		KHz	9
			-55°C≤T_A≤+125°C	10		KHz	10, 11
Center Frequency Drift with Supply	DRFT	4.75V≤Vcc≤8V	T_A = +25°C		2.0	%/V	9
			-55°C≤T_A≤+125°C		3.0	%/V	10, 11
Output Saturation Voltage	VSAT	Ic = 2 mA Vin = 25 mVrms Vcc = +5V	T_A = +25°C		0.4	V	1
			-55°C≤T_A≤+125°C		0.4	V	2, 3
Output Saturation Voltage	VSAT	Ic = 10 mA Vin = 25 mVrms Vcc = +5V	T_A = +25°C		0.6	V	1
			-55°C≤T_A≤+125°C		0.6	V	2, 3
Output Leakage Current	I_{OL}	Vin = 7.5 mVrms Vcc = 15V	T_A = +25°C		25	µA	1
			-55°C≤T_A≤+125°C		25	µA	2, 3
Largest No Output Input Voltage	V_{IL}	Vcc = +5V	T_A= +25°C	10		mVrms	4
			-55°C≤T_A≤+125°C	10		mVrms	5, 6
Smallest Detectable Input Voltage	V_{IS}		T_A = +25°C		25	mVrms	4
			-55°C≤T_A≤+125°C		25	mVrms	5, 6
Largest Detection Bandwidth	LDBW		T_A = +25°C	10	18	%	4
			-55°C≤T_A≤+125°C	10	20	%	5, 6
Largest Detection Bandwidth Skew	SKEW		T_A = +25°C		3.0	%	4
			-55°C≤T_A≤+125°C		3.0	%	5, 6

Pulse-Width Modulating Regulator

GENERAL DESCRIPTION

The XR-1524 family of monolithic integrated circuits contain all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The XR-1524 is specified for operation over the full military temperature range of -55°C to +125°C

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Pin-for-Pin Replacement for SG-1524/2524/3524
Complete PWM power control circuitry
Single ended or push-pull outputs
Line and load regulation of 0.2%
Total supply current less than 10 mA
Operation beyond 100 kHz

APPLICATIONS

Switching Regulators
Pulse-width Modulated Power Control Systems

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Output Current (each output)	100 mA
Reference Output Current	50 mA
Oscillator Charging Current	5 mA
Power Dissipation	
Ceramic Package	1000 mW
Derate above +25°C	8 mW/°C
Operating Temperature Range	
XR-1524	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

SYSTEM DESCRIPTION

The XR-1524 pulse width modulating regulator is a complete monolithic switching regulator. An internal 5V reference, capable of supplying up to 50 mA to external loads, provides an onboard operating standard. The oscillator frequency and duty cycle are adjusted by an external RC network. Regulation is controlled by an error amplifier which, combined with the sense amplifier, also allows current limiting and remote shutdown functions. The outputs of the XR-1524 are two identical NPN transistors with both emitters and collectors uncommitted. Each output transistor has antisaturation circuitry for fast response and local current limiting set at 100 mA.

XR-1524 ELECTRICAL PERFORMANCE CHARATERISTICS

TEST	SYMBOL	CONDITIONS		LIMITS		UNIT	GROUP A SUBGROUP
		CONDTIONS	TEMPERATURE	MIN	MAX		
REFERENCE SECTION							
Output Voltage	V_{REF}	V_{IN} = 20V	TA = 25°C -55°C≤TA≤+125°C	4.8 4.8	5.2 5.2	V V	1 2, 3
Line Regulation	V_{RLINE}	8V≤V_{IN}≤40V	TA = 25°C -55°C≤TA≤+125°C		20 20	mV mV	1 2, 3
Load Regulation	V_{RLOAD}	0mA≤I_L≤20mA	TA = 25°C -55°C≤TA≤+125°C		50 50	mV mV	1 2, 3
Short Circuit Current Limit	I_{OS}	V_{REF} = 0	TA = 25°C -55°C≤TA≤+125°C		150 150	mA mA	1 2, 3
OSCILLATOR SECTION							
Voltage Stability	Δf_{OSC}	8V≤V_{IN}≤40V	TA = 25°C -55°C≤TA≤+125°C		1 1	% %	1 2, 3
ERROR AMPLIFIER SECTION							
Input Offset Voltage	V_{IO}		TA = 25°C -55°C≤TA≤+125°C		5 5	mV mV	1 2, 3
Input Bias Current	I_{IB}		TA = 25°C -55°C≤TA≤+125°C		10 10	µA µA	1 2, 3
Open Loop Gain	A_{VS}		TA = 25°C -55°C≤TA≤+125°C	72 72		db db	4 5, 6
Common Mode Rejection Ratio	CMRR	1.8≤V_{CM}≤3.4V	TA = 25°C -55°C≤TA≤+125°C	46 46		db db	4 5, 6
Output High Level	V_{HI}		TA = 25°C -55°C≤TA≤+125°C	3.8 3.8		V V	1 2, 3
Output Low Level	V_{LO}		TA =25°C -55°C≤TA≤125°C		0.5 0.5	V	1 2, 3
CURRENT LIMITING SECTION							
Sense Voltage	V_{SEN}		TA =25°C	190	210	mV	1
OUTPUT SECTION							
Emitter Output Voltage	V_{EO}	V_{IN} = 20V	TA =25°C -55°C≤TA≤125°C	17 17		V V	1 2, 3
Saturation Voltage	$V_{CE(SAT)}$	I_C = 50mA	TA =25°C -55°C≤TA≤125°C		2 2	V V	1 2, 3
Collector Leakage Current	I_{CEX}	V_{CE} = 40V	TA =25°C -55°C≤TA≤125°C		50 50	µA µA	1 2, 3
Standby Current	I_{IN}	V_{IN} = 40V	TA =25°C -55°C≤TA≤125°C		10 10	mA mA	1 2, 3

Power Supply Output Supervisory Circuit

GENERAL DESCRIPTION

The XR-1543 is a monolithic integrated circuit that contains all the functions necessary to monitor and control the output of a power supply system. Included in the 16-pin dual-in-line package is a voltage reference, an operational amplifier, voltage comparators, and a high-current SCR trigger circuit. The functions performed by this device include over-voltage sensing, under-voltage sensing and current limiting, with provisions for triggering an external SCR "crow-bar".

The internal voltage reference on the XR-1543 is guaranteed for an accuracy of ±1% to eliminate the need for external potentiometers. The entire circuit may be powered from either the output that is being monitored or from a separate bias voltage.

FEATURES

Over-Voltage Sensing Capability	
Under-Voltage Sensing Capability	
Current Limiting Capability	
Reference Voltage Trimmed	±1%
SCR "Crowbar" Drive	300 mA
Programmable Time Delays	
Open Collector Outputs and Remote Activation Capability	
Total Standby current	Less than 10 mA

APPLICATIONS

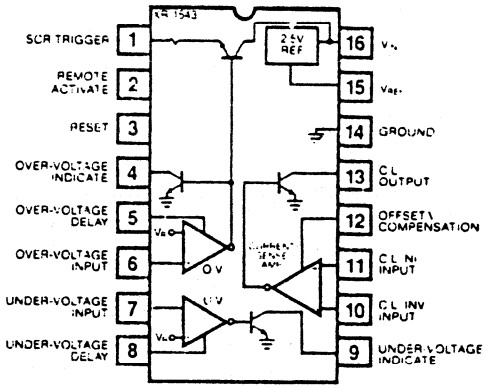
DC/DC Converters
Switch Mode Power Supplies
Power Line Monitors
Linear Power Supplies

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{IN}	40V
Sense Inputs	V_{IN}
SCR Trigger Current (Note 1)	300 mA
Indicator Output Voltage	40V
Indicator Output Sink Current	50 mA
Power Dissipation (Ceramic)	1000 mW
Derate Above T_A = +25°C	8 mW/°C
Operating Junction Temperature (T_J)	+150°C
Storage Temperature Range	−65°C to +150°C

Note 1: At higher input voltages, a dissipation limiting resistor, R_G, is required.

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

An output supervisory circuit, such as the XR-1543, is used to control and monitor the performance of a power supply. In many systems, it is crucial that the supply voltage is always within some minimum and maximum level, to guarantee proper performance, and to prevent damage to the system. If the supply voltage is out of tolerance, it is often desirable to shut down the system or to have some form of indication to the operator or system controller. As well as protecting the system, the power supply sometimes needs to be protected under short circuit and current overload situations. By providing an SCR "crowbar" on the output of a power supply, it can be shut off under certain fault conditions as well.

The over-voltage sensing circuit (O.V.) can be used to monitor the output of a power supply and provide triggering of an SCR, when the output goes above the prescribed voltage level. The under-voltage sensing circuit (U.V.) can be used to monitor either the output of a power supply or the input line voltage.

XR-1543 ELECTRICAL PERFORMANCE CHARATERISTICS

TEST	SYMBOL	CONDITIONS		LIMITS		UNIT	GROUP A SUBGROUP
		CONDITIONS	TEMPERATURE	MIN	MAX		
Supply Current		V_{IN} = 40V	TA = 25°C -55°C≤TA≤125°C		10 10	mA mA	1 2, 3
Reference Section							
Output Voltage		V_{IN} = 10V	TA = 25°C -55°C≤TA≤125°C	2.48 2.45	2.52 2.55	V V	1 2, 3
Line Regulation		V_{IN} = 5Vto30V	TA = 25°C -55°C≤TA≤125°C		5 5	mV mV	1 2, 3
Load Regulation		i_{REF} = 0 to 10mA	TA = 25°C -55°C≤TA≤125°C		10 10	mV mV	1 2, 3
Short Circuit Current		V_{REF} = 0V	TA = 25°C -55°C≤TA≤125°C	12 12	40 40	mA mA	1 2, 3
SCR Trigger Section							
Peak Output Current		Tested Go-No Go	TA = 25°C -55°C≤TA≤125°C		400 400	mA mA	1 2, 3
Peak Output Voltage		V_{IN} = 5V Io = 100mA	TA = 25°C -55°C≤TA≤125°C	12 12		V V	1 2, 3
Output Off Voltage		V_{IN} = 40V	TA = 25°C -55°C≤TA≤125°C		0.1 0.1	V V	1 2, 3
Remote Activate Current			TA = 25°C -55°C≤TA≤125°C		800 800	µA µA	1 2, 3
Remote Activate Voltage			TA = 25°C -55°C≤TA≤125°C		6.0 6.0	V V	1 2, 3
Reset Current			TA = 25°C -55°C≤TA≤125°C		800 800	µA µA	1 2, 3
Reset Voltage			TA = 25°C -55°C≤TA≤125°C		6.0 6.0	V V	1 2, 3
COMPARATOR SECTIONS							
Input Threshold		Tested Go-No Go Only	TA = 25°C -55°C≤TA≤125°C	2.45 2.40	2.55 2.60	V V	1 2, 3
Input Bias Current			TA = 25°C -55°C≤TA≤125°C		1.0 1.0	µA µA	1 2, 3
Delay Saturation			TA = 25°C -55°C≤TA≤125°C		0.5 0.5	V V	1 2, 3
Delay High Level			TA = 25°C -55°C≤TA≤125°C	5.0 5.0	8.0 8.0	V V	1 2, 3
Delay Charging Current			TA = 25°C -55°C≤TA≤125°C	200 200	300 300	µA µA	1 2, 3
Indicate Saturation Voltage		I_L = 10mA	TA = 25°C -55°C≤TA≤125°C		0.5 0.5	V V	1 2, 3

CURRENT LIMIT AMPLIFIER SECTION							
Input Voltage Range		V_{IN} = 10V	TA = 25°C -55°C≤TA≤125°C		V_{IN} -3V	V	1 2, 3
Input Bias Current			TA = 25°C -55°C≤TA≤125°C		1.0 1.0	µA µA	1 2, 3
Input Offset Voltage			TA = 25°C -55°C≤TA≤125°C		10 10	mV mV	1 2, 3
Input Offset Voltage		P_{IN}12 = 10K to GND	TA = 25°C -55°C≤TA≤125°C	80 80	120 120	mV mV	1 2, 3
CMRR			TA = 25°C -55°C≤TA≤125°C	60 60		dB dB	1 2, 3
Open Loop Gain			TA = 25°C -55°C≤TA≤125°C	72 72		dB dB	1 2, 3
Output Saturation Voltage		I_L = 10mA	TA = 25°C -55°C≤TA≤125°C		0.5 0.5	V V	1 2, 3
Output Leakage Current		V_{OUT} =40V	TA = 25°C -55°C≤TA≤125°C		1.0 1.0	µA µA	1 2, 3
Indicate Leakage Current		V_{OUT} =40V	TA = 25°C -55°C≤TA≤125°C		1.0 1.0	µA µA	1 2, 3

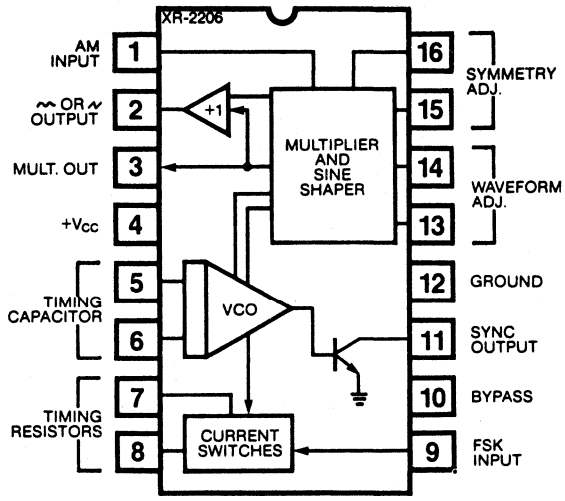
Monolithic Function Generator

GENERAL DESCRIPTION

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01 Hz to more than 1 MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range, with an external control voltage, having a very small affect on distortion.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Low-Sine Wave Distortion	0.5%, Typical
Excellent Temperature Stability	20 ppm/°C, Typical
Wide Sweep Range	2000:1, Typical
Low-Supply Sensitivity	0.01%V, Typical
Linear Amplitude Modulation	
TTL Compatible FSK Controls	
Wide Supply Range	10V to 26V
Adjustable Duty Cycle	1% to 99%

APPLICATIONS

Waveform Generation
Sweep Generation
AM/FM Generation
V/F Conversion
FSK Generation
Phase-Locked Loops (VCO)

ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation	750 mW
Derate Above 25°C	5 mW/°C
Total Timing Current	6 mA
Storage Temperature	−65°C to +150°C

Rev-A

SYSTEM DESCRIPTION

The XR-2206 is comprised of four functional blocks; a voltage-controlled oscillator (VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches.

The VCO actually produces an output frequency proportional to an input current, which is produced by a resistor from the timing terminals to ground. The current switches route one of the timing pins current to the VCO controlled by an FSK input pin, to produce an output frequency. With two timing pins, two discrete output frequencies can be independently produced for FSK Generation Applications.

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-2206

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current	Icc1	Vcc = 12V	T_A = +25°C		17.0	mA	1
			-55°C≤T_A≤+125°C		17.0	mA	2, 3
Supply Current	Icc2	Vcc = 26V	T_A = +25°C		25.0	mA	1
			-55°C≤T_A≤+125°C		25.0	mA	2, 3
Squarewave Leakage Current	I_L	V_{11} = 26V	T_A = +25°C		20	µA	1
			-55°C≤T_A≤+125°C		20	µA	2, 3
Squarewave Saturation Voltage	V_{SAT}	I_L = 2mA	T_A = +25°C		0.4	V	1
			-55°C≤T_A≤+125°C		0.6	V	2, 3
Reference Bypass Voltage	V_{REF}	A_T Pin 10	T_A = +25°C	2.9	3.3	V	1
			-55°C≤T_A≤+125°C	2.5	3.5	V	2, 3
FSK Input Threshold	V_{IN}KEY	Vcc = 12V	T_A = +25°C	0.8	2.4	V	1
			-55°C≤T_A≤+125°C	0.8	2.4	V	2, 3
Max. Frequency	F_{MAX}	RT = 1Kohm	T_A = +25°C	500		KHz	9
		CT = 1000PF	-55°C≤T_A≤+125°C	500		KHz	10, 11
Frequency Accuracy	Fo	Vcc = 12V	T_A = +25°C	.96	1.04	KHz	9
		CT = 0.01µF	-55°C≤T_A≤+125°C	.96	1.04	KHz	10, 11
		RT = 100Kohm					
Frequency Accuracy	Fo	Vcc = 12V	T_A = +25°C	9.0	11.0	KHz	9
		CT = 0.01µF	-55°C≤T_A≤+125°C	9.0	11.0	KHz	10, 11
		RT = 10Kohm					
Frequency Accuracy Low Voltage		Vcc = 10V	T_A = +25°C	4.0	6.0	KHz	9
		RT = 20Kohm	-55°C≤T_A≤+125°C	4.0	6.0	KHz	10, 11
		CT = .01µF					
		V_{IN}KEY = 2.4V					
Frequency Accuracy Low Voltage		Vcc = 10V	T_A = +25°C	4.0	6.0	KHz	9
		RT = 20Kohm	-55°C≤T_A≤+125°C	4.0	6.0	KHz	10, 11
		CT = .01µF					
		V_{IN}KEY = 0.8V					
Frequency Accuracy High Voltage		Vcc = 26V	T_A = +25°C	4.0	6.0	KHz	9
		RT = 20Kohm	-55°C≤T_A≤+125°C	4.0	6.0	KHz	10, 11
		CT = .01µF					
		V_{IN}KEY = 2.4V					
Frequency Accuracy High Voltage		Vcc = 26V	T_A = +25°C	4.0	6.0	KHz	9
		RT = 20Kohm	-55°C≤T_A≤+125°C	4.0	6.0	KHz	10, 11
		CT = .01µF					
		V_{IN}KEY = 0.8V					
Supply Sensitivity	PSRR	Vcc = 10 to 20V	T_A = +25°C		0.1	%/V	9
		RT = 20Kohm	-55°C≤T_A≤+125°C		0.1	%/V	10, 11
		CT = 0.01µF					
		V_{IN}KEY = 2.4V					

Supply Sensitivity	PSRR	V_{CC} = 10 to 20V RT = 20Kohm CT = 0.01μF V_{IN}KEY = 0.8V	T_A = +25°C -55°C≤T_A≤+125°C		0.1 0.1	%/V %/V	**9** **10, 11**
Low Timing Resistor	F_{MAX}	RT = 1KΩ CT = 1000pF	T_A = +25°C -55°C≤T_A≤+125°C	500 500		KHz KHz	**9** **10, 11**
High Timing Resistor	F_{MIN}	RT = 2MΩ CT = 1000pF	T_A = +25°C -55°C≤T_A≤+125°C	400 400	600 600	Hz Hz	**9** **10, 11**
Sweep Range		F_{MAX}/F_{MIN}	T_A = +25°C -55°C≤T_A≤+125°C	1000 1000			**9** **10, 11**
Sine Wave Amplitude		RT = 100KΩ CT = .01μF	T_A = +25°C -55°C≤T_A≤+125°C	40 20	80 120	mV/ Kohm mV/ Kohm	**4** **5, 6**
AM Sine Wave Amplitude		RT = 100KΩ VAM = 3V CT = .01μF	T_A = +25°C -55°C≤T_A≤+125°C	30 10	60 100	mV/ Kohm mV/ Kohm	**4** **5, 6**
AM Sine Wave Amplitude		RT = 100KΩ VAM = 9V CT =..01μF	T_A = +25°C -55°C≤T_A≤+125°C	30 10	60 100	mV/ Kohm mV/ Kohm	**4** **5, 6**
AM Sine Wave Amplitude Symmetry			T_A = +25°C -55°C≤T_A≤+125°		10 **10**	mV **mV**	**4** **5, 6**
Symmetry Adjust Resistor	R15	Pin 15	T_A = +25°C -55°C≤T_A≤+125°C	1.7 1.5	2.6 3.0	Kohm Kohm	**4** **5, 6**
Symmetry Adjust Resistor	R16	Pin 16	T_A = +25°C -55°C≤T_A≤+125°C	1.7 1.5	2.6 3.0	Kohm Kohm	**4** **5, 6**
Symmetry Adjust Balance		R16-R15	T_A = +25°C -55°C≤T_A≤+125°C	-0.1 -0.2	0.1 0.2	Kohm Kohm	**4** **5, 6**

Voltage-Controlled Oscillator

GENERAL DESCRIPTION

The XR-2207 is a monolithic voltage-controlled oscillator (VCO) integrated circuit featuring excellent frequency stability and a wide tuning range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01 Hz to 1 MHz. It is ideally suited for FM, FSK, and sweep or tone generation, as well as for phase-locked loop applications.

The XR-2207 has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 1000:1 range with an external control voltage; and the duty cycle of both the triangle and the squarewave outputs can be varied from 0.1% to 99.9% to generate stable pulse and sawtooth waveforms.

FEATURES

Excellent Temperature Stability (20 ppm/°C)
Linear Frequency Sweep
Adjustable Duty Cycle (0.1% to 99.9%)
Two or Four Level FSK Capability
Wide Sweep Range (3000:1 Typical)
Logic Compatible Input and Output Levels
Wide Supply Voltage Range (±4V to ±13V)
Low Supply Sensitivity (0.1%/V)
Wide Frequency Range (0.01 Hz to 1 MHz)
Simultaneous Triangle and Squarewave Outputs

APPLICATIONS

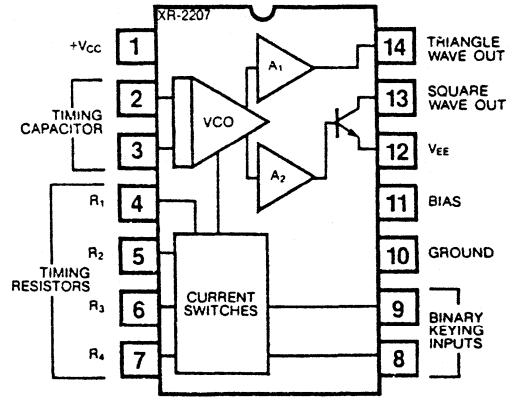
FSK Generation
Voltage and Current-to-Frequency Conversion
Stable Phase-Locked Loop
Waveform Generation
  Triangle, Sawtooth, Pulse, Squarewave
FM and Sweep Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation (package limitation)	
Ceramic package	750 mW
Derate above +25°C	6.0 mW/°C
Storage Temperature Range	-65°C to +150°C

Rev-B

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-2207 utilizes four main functional blocks for frequency generation. These are a voltage controlled oscillator (VCO), four current switches which are activated by binary keying inputs, and two buffer amplifiers for triangle and squarewave outputs. The VCO is actually a current controlled oscillator which gets its input from the current switches. As the output frequency is proportional to the input current, the VCO produces four discrete output frequencies. Two binary input pins determine which timing currents are channelled to the VCO. These currents are set by resistors to ground from each of the four timing terminals.

The triangle output buffer provides a low impedance output (10Ω TYP) while the squarewave is an open-collector type. A programmable reference point allows the XR-2207 to be used in either single or slip supply configurations.

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-2207

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	
Supply Current	I_{CC1}	Positive, V_{CC} = ±6V	T_A = +25°C -55°C≤T_A≤+125°C		7.0 12.0	mA mA	1 2, 3
Supply Current	I_{EE1}	Negative, V_{CC} = ±6V	T_A = +25°C -55°C≤T_A≤+125°C	-6.0 -11.0		mA mA	1 2, 3
Supply Current	I_{CC2}	Positive, V_{CC} = ±13V	T_A = +25°C -55°C≤T_A≤+125°C		19.0 20.0	mA mA	1 2, 3
Supply Current	I_{EE2}	Negative, V_{CC} = ±13V	T_A = +25°C -55°C≤T_A≤+125°C	-19.0 -20.0		mA mA	1 2, 3
Squarewave Output Leakage Current	I_L	V_{CC} = ±13V **V_{CC} = ±10V**	T_A = +25°C -55°C≤T_A≤+125°C		100 200	µA µA	1 2, 3
Sqarewave Output Low Voltage	V_{OL}	Referenced to V_{EE} V_{CC} = ±6V	T_A = +25°C -55°C≤T_A≤+125°C		0.40 1.00	V V	1 2, 3
Squarewave Output Amplitude	V_O	V_{CC} = ±6V	T_A = +25°C -55°C≤T_A≤+125°C	11.0 11.0		V V	4 5, 6
Frequency Accuracy	f_{STD}	CT = 5000pF RT = 20 Kohm	T_A = +25°C -55°C≤T_A≤+125°C	9.70 9.50	10.30 10.50	KHz KHz	9 10, 11
Power Supply Stability		±6V≤V_{CC}≤±13V	T_A = +25°C -55°C≤T_A≤+125°C		10.0 11.0	% %	9 10, 11
Frequency Matching	f_{XX}	VKEYA = 1.4V VKEYB = 1.4V f = 10 KHz	T_A = +25°C Only		5	%	9
Frequency Matching	f_{XX}	VKEYA = 2.8V VKEYB = 1.4V f = 10 KHz	T_A = +25°C Only		5	%	9
Frequency Matching	f_{XX}	VKEYA = 2.8V VKEYB = 2.8V f = 20 KHz	T_A = +25°C Only		5	%	9
Frequency Matching	f_{XX}	VKEYA = 1.4V VKEYB = 2.8V f = 20 KHz	T_A = +25°C Only		5	%	9
Upper Frequency	fH	CT = 500pF RT = 2 Kohm	T_A = +25°C -55°C≤T_A≤+125°C	500 500		KHz KHz	9 10, 11
Sweep Linearity	S_{WLIN}	CT = 5000pF RT = 200 Kohm vs FSTD	T_A = +25°C -55°C≤T_A≤+125°C		2 4	% %	9 10, 11
Minimum Timing Resistor	T_{RMIN}	CT = 5000pF RT = 1.5 Kohm	T_A = +25°C -55°C≤T_A≤+125°C	90 85		KHz KHz	9 10, 11
Maximum Timing Resistor	T_{RMAX}	CT = 5000pF RT = 2 Mohm **R_T = 200KΩ**	T_A = +25°C **;55°C≤T_A≤+125°C**	80 **800**	120 **1200**	Hz **Hz**	9 10, 11

Sweep Range	S_{WRNG}	T_{RMIN}/T_{RMAX}	$T_A = +25°C$ **$-55°C \leq T_A \leq +125°C$**	1000 **100**			**9** **10, 11**
Triangle Wave Output Amplitude	$T_{VPP}1$	$V_{CC} = \pm 6V$ CT = 5000pF RT = 20 Kohm	$T_A = +25°C$ $-55°C \leqslant T_A \leqslant +125°C$	4 2		V	**4** **5, 6**
Triangle Wave Output Amplitude	$T_{VPP}2$	$V_{CC} = \pm 13V$ CT = 5000pF RT = 20 Kohm	$T_A = +25°C$ $-55°C \leqslant T_A \leqslant +125°C$	7 7		V	**4** **5, 6**
Triangle Wave	T_{WLIN}	$V_{CC} = \pm 6V$ CT = 5000 pF RT = 20 Kohm	$T_A = +25°C$ **$-55°C \leq T_A \leq +125°C$**		5.0 **5.0**	% **%**	**9** **10, 11**

6

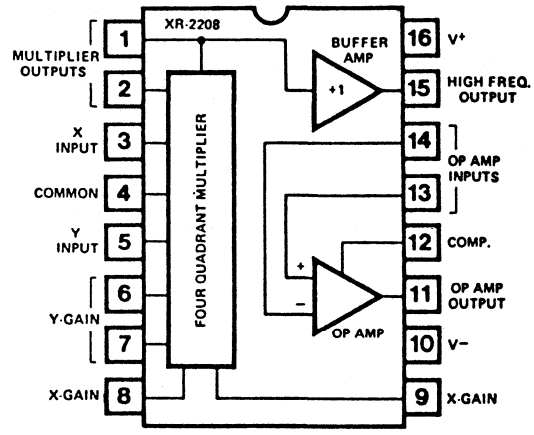
Operational Multiplier

GENERAL DESCRIPTION

The XR-2208 operational multiplier combines a four-quadrant analog multiplier (or modulator), a high frequency buffer amplifier, and an operational amplifier in a monolithic circuit that is ideally suited for both analog computation and communications signal processing application. As shown in the functional block diagram, for maximum versatility the multiplier and operational amplifier sections are not internally connected. They can be interconnected, with a minimum number of external components, to perform arithmetic computation, such as multiplication, division, square-root extraction. The operational amplifier can also function as a pre-amplifier for low-level input signals, or as a post detection amplifier for synchronous demodulator applications. For signal processing, the high frequency buffer amplifier output is available at pin 15. This multiplier/buffer amplifier combination extends the small signal 3-db bandwidth to 8-MHz and the transconductance bandwidth to 100 MHz.

The XR-2208 operates over a wide range of supply voltages, ±4.5V to ±16V. Current and voltage levels are internally regulated to provide excellent power supply rejection and temperature stability.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Maximum Versatility
- Independent Multiplier, Op Amp, and Buffer

Excellent Linearity (0.3% typ.)

Wide Bandwidth
- 3 dB B.W.—8 MHz typ.
- 3° Phase Shift B.W.—1.2 MHz typ.
- Transconductance B.W.—100 MHz typ.

Simplified Offset Adjustments

Wide Supply Voltage Range (±4.5V to ±16V)

APPLICATIONS

Analog Computation
- Multiplication
- Division
- Squaring
- Square-Root

Signal Processing
- AM Generation
- Frequency Doubling
- Frequency Translation
- Synchronous AM Detection
- Triangle-to-Sinewave Converter
- AGC Amplifier
- Phase Detector

Phase-Locked Loop (PLL) Applications
- Motor Speed Control
- Precision PLL
- Carrier Detection
- Phase-Locked AM Demodulation

ABSOLUTE MAXIMUM RATINGS

Power Supply V+	+18 Volts
V−	−18 Volts
Power Dissipation	
Ceramic Package	750mW
Derate above +25°C	6mW/°C
Storage Temperature Range	−65°C to +150°C

SYSTEM DESCRIPTION

The XR-2208 operational multiplier contains a four-quadrant multiplier with a buffer amplifier for one of the differential outputs for applications requiring high frequency applications. The inputs have a dynamic response of 4 MHz (8 MHz for the X input) and a transconductance bandwidth of 100 MHz for phase detector applications. The fully independent operational amplifier features high gain and a large common mode rejection ratio (90 dB). The device can be powered by voltages from ±4.5 VDC to ±16 VDC.

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-2208

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GHOUP A SUBGROUP
Supply Current	I_{CC}	Vs = ±4.5V	T_A = +25°C		7.0	mA	1
			-55°C≤T_A≤+125°C		7.0	mA	2, 3
Supply Current	I_{CC}	Vs = ±16.0V	T_A = +25°C		7.0	mA	1
			-55°C≤T_A≤+125°C		7.0	mA	2, 3
Multiplier Output Voltage	Mvo	Pin 1	T_A = +25°C	12.2	13.7	V	1
			-55°C≤T_A≤+125°C	12.2	13.7	V	2, 3
Multiplier Output Voltage	Mvo	Pin 2	T_A = +25°C	12.2	13.7	V	1
			-55°C≤T_A≤+125°C	12.2	13.7	V	2, 3
Multiplier Output Offset Voltage	Mvos		T_A = +25°C	-80	80	mV	1
			-55°C≤T_A≤+125°C	-80	80	mV	2, 3
Feedthrough	V_{FT}	Vx = -10V, Vy = 0	T_A = +25°C	-150	150	mV	4
			-55°C≤T_A≤+125°C	-150	150	mV	5, 6
Feedthrough	V_{FT}	Vx = 0, Vy = -10V	T_A = +25°C	-150	150	mV	4
			-55°C≤T_A≤+125°C	-150	150	mV	5, 6
Feedthrough	V_{FT}	Vx = 0, Vy **= 10V**	T_A = +25°C	-150	150	mV	4
			-55°C≤T_A≤+125°C	-150	150	mV	5, 6
Feedthrough	V_{FT}	Vx = 0, Vy = 10V	T_A = +25°C	-150	150	mV	4
			-55°C≤T_A≤+125°C	-150	150	mV	5, 6
Nonlinearity	N_{LIN}	Vx = 10V	T_A = +25°C	-0.5	0.5	%	9
		-10V≤Vy≤10V	-55°C≤T_A≤+125°C	**-1.0**	**1.0**	%	10, 11
Nonlinearity	N_{LIN}	Vx = -10V	T_A = +25°C	-0.5	0.5	%	9
		-10V≤Vy≤10V	-55°C≤T_A≤+125°C	**-1.0**	**1.0**	%	10, 11
Nonlinearity	N_{LIN}	Vy = +10V	T_A = +25°C	-0.5	0.5	%	9
		-10V≤Vx≤10V	-55°C≤T_A≤+125°C	**-1.0**	**1.0**	%	10, 11
Nonlinearity	N_{LIN}	Vy **=10V**	T_A = +25°C	-0.5	0.5	%	9
		-10V≤Vx≤10V	-55°C≤T_A≤+125°C	**-1.0**	**1.0**	%	10, 11
Input Bias Current	I_{BX}	X_{INPUT}	T_A = +25°C	-6.0	6.0	µA	1
			-55°C≤T_A≤+125°C	-6.0	6.0	µA	2, 3
Input Bias Current	I_{BY}	Y_{INPUT}	T_A = +25°C	-6.0	6.0	µA	1
			-55°C≤T_A≤+125°C	-6.0	6.0	µA	2, 3
Input Bias Current	I_{BC}	Common Input	T_A = +25°C	-12.0	12.0	µA	1
			-55°C≤T_A≤+125°C	-12.0	12.0	µA	2, 3
Buffer Voltage Gain	BG		T_A = +25°C	0.8	1.1		4
			-55°C≤T_A≤+125°C	0.8	1.1		5, 6
Buffer Output Voltage High	B_{VO}	Vx = 10V, Vy = -10V	T_A = +25°C	10.0	13.0	V	1
			-55°C≤T_A≤+125°C	10.0	13.0	V	2, 3

6

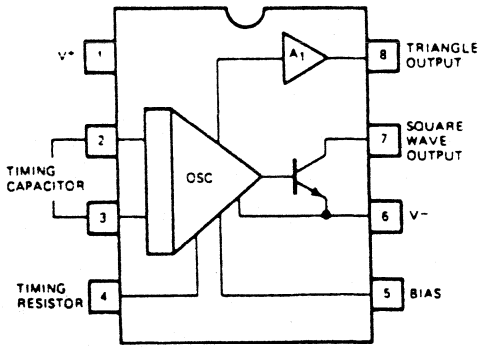
Buffer Output Voltage Difference	B_{VOD}	Vx = -10V, Vy = 10V	T_A = +25°C -55°C≤T_A≤+125°C	-2.1 -2.1	-0.55 -0.55	V V	1 2, 3
Input Offset Voltage	V_{OS}		T_A = +25°C -55°C≤T_A≤+125°C	-3.0 -3.0	3.0 3.0	mV mV	1 2, 3
Input Offset Voltage	I_{OS}		T_A = +25°C -55°C≤T_A≤+125°C	-75.0 -75.0	75.0 75.0	nA nA	1 2, 3
Input Bias Current	I_B		T_A = +25°C -55°C≤T_A≤+125°C	-200 -200	200 200	nA nA	1 2, 3
Common Mode Rejection Ratio	CMRR		T_A = +25°C -55°C≤T_A≤+125°C	70 70		dB dB	1 2, 3
Voltage Gain	A_{VOL}		T_A = +25°C -55°C≤T_A≤+125°C	70 70		dB dB	4 5, 6
Power Supply Rejection	PSRR		T_A = +25°C -55°C≤T_A≤+125°C	70 70		dB dB	1 2, 3
Output Voltage Swing Positive	V_{OSWP}		T_A = +25°C -55°C≤T_A≤+125°C	10.0 10.0		V V	4 5, 6
Output Voltage Swing Negative	V_{OSWN}		T_A = +25°C -55°C≤T_A≤+125°C		-10.0 -10.0	V V	4 5, 6
Short Circuit Current Negative	I_{SCN}		T_A = +25°C -55°C≤T_A≤+125°C	-30.0 -30.0	-5.0 -5.0	mA mA	1 2, 3
Short Circuit Current Positive	I_{SCP}		T_A = +25°C -55°C≤T_A≤+125°C	5.0 5.0	30.0 30.0	mA mA	1 2, 3

Precision Oscillator

GENERAL DESCRIPTION

The XR-2209 is a monolithic variable frequency oscillator circuit featuring excellent temperature stability and a wide linear sweep range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01 Hz to 1 MHz. The frequency is set by an external RC product. It is ideally suited for frequency modulation, voltage to frequency or current to frequency conversion, sweep or tone generation as well as for phase-locked loop applications when used in conjunction with a phase comparator such as the XR-2208.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Excellent Temperature Stability (20 ppm/°C)
Linear Frequency Sweep
Wide Sweep Range (1000:1 Min)
Wide Supply Voltage Range (±4V to ±13V)
Low Supply Sensitivity (0.15%/V)
Wide Frequency Range (0.01 Hz to 1 MHz)
Simultaneous Triangle and Squarewave Outputs

APPLICATIONS

Voltage and Current-to-Frequency Conversion
Stable Phase-Locked Loop
Waveform Generation
FM and Sweep Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Derate above +25°C	8.3 mW/°C
Operating Temperatue Range	
XR-2209M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Rev-B

SYSTEM DESCRIPTION

The XR-2209 precision oscillator is comprised of three functional blocks: a variable frequency oscillator which generates the basic periodic waveforms and two buffer amplifiers for the triangle and the squarewave outputs. The oscillator frequency, set by an external capacitor, C, and the timing resistor, R, operates over 8 frequency decades, from 0.01 Hz to 1 MHz. With no sweep signal applied, the frequency of oscillation is equal to 1/RC.

The XR-2209 has a typical drift specification of 20 ppm/°C. Its frequency can be linearly swept over a 1000:1 range with an external control signal. Output duty cycle is adjustable from less than 1% to over 99%. The device may operate from either single or split supplies from 8 V to 26 V (±4 V to ±13 V).

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-2209

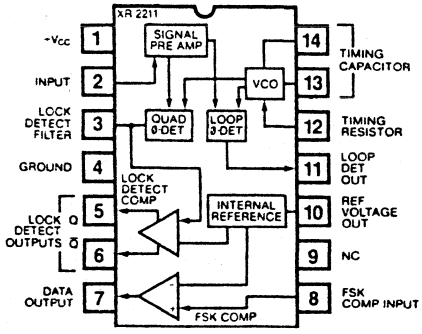
TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current	$I_{CC}1$	Positive V_{CC} = ±6V	T_A = +25°C		8.00	mA	1
			-55°C≤T_A≤+125°C		12.00	mA	2, 3
Supply Current	$I_{EE}1$	Negative V_{CC} = ±6V	T_A = +25°C	-7.00		mA	1
			-55°C≤T_A≤+125°C	-11.0		mA	2, 3
Supply Current	$I_{CC}2$	Positive V_{CC} = ±13V	T_A = +25°C		17.00	mA	1
			-55°C≤T_A≤+125°C		20.00	mA	2, 3
Supply Current	$I_{EE}2$	Negative V_{CC} = ±13V	T_A = +25°C	-17.0		mA	1
			-55°C≤T_A≤+125°C	-20.0		mA	2, 3
Squarewave Output Leakage Current	I_L	V_{CC} = ±13V	T_A = +25°C		100	µA	1
			-55°C≤T_A≤+125°C		200	µA	2, 3
Squarewave Output Low Voltage	V_{OL}	Referenced to V_{EE} V_{CC} = ±6V	T_A = +25°C		0.4	V	1
			-55°C≤T_A≤+125°C		1.00	V	2, 3
Squarewave Output Amplitude	V_O	V_{CC} = ±6V	T_A = +25°C	11.0		V	4
			-55°C≤T_A≤+125°C	11.0		V	5, 6
Frequency Accuracy	f_{STD}	C_T = 5000 pF, V_{CC} = ±6V, R_T = 20KΩ	T_A = +25°C	9.70	10.30	KHz	9
			-55°C≤T_A≤+125°C	9.50	10.50	KHz	10, 11
Power Supply Stability		±6V≤V_{CC}≤±13V	T_A = +25°C		10.0	%	9
			-55°C≤T_A≤+125°C		11.0	%	10, 11
Upper Frequency	f_H	C_T = 500 pF, R_T = 2KΩ, V_{CC} = ±6V	T_A = +25°C	500		KHz	9
			-55°C≤T_A≤+125°C	500		KHz	10, 11
Sweep Linearity	S_{WLIN}	C_T = 5000 pF, R_T = 200KΩ vs. f_{STD}	T_A = +25°C		2.0	%	9
			-55°C≤T_A≤+125°C		4.0	%	10, 11
Minimum Timing Resistor	T_{RMIN}	C_T = 5000 pF R_T = 1.5KΩ	T_A = +25°C	90		KHz	9
			-55°C≤T_A≤+125°C	85		KHz	10, 11
Maximum Timing Resistor	T_{RMAX}	C_T = 5000 pF R_T = 2MΩ	T_A = +25°C Only	80	120	Hz	9 10, 11
		R_T = 200KΩ	**-55°C≤T_A≤+125°C**	**800**	**1400**	**Hz**	
Sweep Range	S_{WRNG}	T_{RMIN}/T_{RMAX}	T_A = +25°C	**90**			9
			-55°C≤T_A≤+125°C				10, 11
Triangle Wave Output Amplitude	T_{VPP1}	V_{CC} = ±6V C_T = 5000 pF R_T = 20KΩ	T_A = +25°C	4		V	4
			-55°C≤T_A≤+125°C	2		V	5, 6
Triangle Wave Output Amplitude	T_{VPP2}	V_{CC} = ±13V C_T = 5000 pF R_T = 20KΩ	T_A = +25°C	7		V	4
			-55°C≤T_A≤+125°C	7		V	5, 6
Triangle Wave Linearity	T_{WLIN}	C_T = 5000 pF R_T = 20KΩ V_{CC} = ±6V	T_A = +25°C Only		5	%	9
			-55°C ≤ T_A ≤ +125°C		**5**	**%**	10, 11

FSK Demodulator/Tone Decoder

GENERAL DESCRIPTION

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications applications. It is particularly suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL, and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power supply provides ratio metric operation for low system performance variations with power supply changes.

FUNCTIONAL BLOCK DIAGRAM



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FEATURES

Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20 V
HCMOS / TTL / Logic Compatibility	
FSK Demodulation, with Carrier Detection	
Wide Dynamic Range	2 mV to 3 V rms
Adjustable Tracking Range (±1% to ±80%)	
Excellent Temp. Stability	20 ppm/°C, typ.

APPLICATIONS

FSK Demodulation
Data Synchronization
Tone Decoding
FM Detection
Carrier Detection

ABSOLUTE MAXIMUM RATINGS

Power Supply	20V
Input Signal Level	3V rms
Power Dissipation	900 mW
Ceramic Package	750 mW
Derate Above T_A = +25°C	8mW°C

Rev-A

SYSTEM DESCRIPTION

The output of the phase detector produces sum and difference frequencies of the input and the VCO (internally connected). When in lock, these frequencies are f_{IN} + f_{VCO} (2 times f_{IN} when in lock) and f_{IN} - f_{VCO} (0HZ when lock). By adding a capacitor to the phase detector output, the 2 times f_{IN} component is reduced, leaving a DC voltage that represents the phase difference between the two frequencies. This closes the loop and allows the VCO to track the input frequency.

The other sections of the XR-2211 act to: determine if the VCO is driven above or below the center frequency (FSK comparator); produce both active high and active low outputs to indicate when the main PLL is in lock (quadrature phase detector and lock detector comparator).

XR-2211 ELECTRICAL PERFORMANCE CHARACTERISTICS

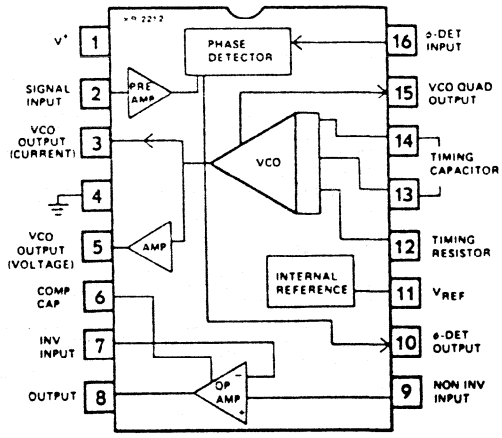
TEST	CONDITIONS		LIMITS		UNIT	GROUP A SUBGROUP
	CONDITIONS	TEMPERATURE	MIN	MAX		
GENERAL CHARACTERISTICS						
Supply Voltage	V_{CC} = 4.5V RT = 30Kohm CT = 0.033UF	TA = 25°C -55°C≤TA≤125°C	900 900	1100 1100	Hz Hz	9 10, 11
	V_{CC} = 20V RT = 30Kohm CT = 0.033UF	TA = 25°C -55°C≤TA≤125°C	900 900	1100 1100	Hz Hz	9 10, 11
Supply Current	V_{CC} = 12V	TA = 25°C -55°C≤TA≤125°C		7 11	mA mA	1 2, 3
	V_{CC} = 20V	TA = 25°C -55°C≤TA≤125°C		14 20	mA mA	1 2, 3
OSCILLATOR SECTION						
Frequency Accuracy	RT = 30Kohm V_{CC} = 12V CT = 0.033UF	TA = 25°C -55°C≤TA≤125°C	970 900	1030 1100	Hz Hz	9 10, 11
Frequency Stability vs Power Supply	V_{CC} = 12V ±1V	TA = 25°C		0.5	%	9
Maximum Frequency	V_{CC} = 12V RT = 8.2Kohm CT = 400pf	TA = 25°C	100		KHz	9
Minimum Timing Resistor	RT = 15Kohm CT = 0.03UF	TA = 25°C	1600	2400	Hz	9
LOOP PHASE DETECTOR SECTION						
Peak Output Current	V_{CC} = 12V Measured at Pin 11	TA = 25°C -55°C≤TA≤125°C	±150 ±100	±300 ±300	µA µA	1 2, 3
Maximum Swing	V_{CC} = 12V Referenced to Pin 10	TA = 25°C -55°C≤TA≤125°C	±4.0 ±2.8		V V	1 2, 3
QUADRATURE PHASE DETECTOR						
Peak Output Current	V_{CC} = 12V Measured at Pin 3	TA = 25°C -55°C≤TA≤125°C	100 50		µA µA	1 2, 3
INPUT PREAMP SECTION						
Input Signal Voltage Required to cause Limiting	V_{CC} = 12V, fo = 1KHz V_{IN} = 10mVrms Measured "Q" output Pin 5	TA = 25°C -55°C≤TA≤125°C		0.6 0.8	V V	7 8
INTERNAL REFERENCE						
Voltage Output	V_{CC} = 12V Measured at Pin 10	TA = 25°C -55°C≤TA≤125°C	4.9 3.8	5.7 6.95	V V	1 2, 3

Precision Phase-Locked Loop

GENERAL DESCRIPTION

The XR-2212 is an ultra-stable monolithic phase-locked loop (PLL) system especially designed for data communications and control system applications. Its on board reference and uncommitted operational amplifier, together with a typical temperature stability of better than 20 ppm/°C, make it ideally suited for frequency synthesis, FM detection, and tracking filter applications. The wide input dynamic range, large operating voltage range, large frequency range, and HCMOS, and TTL compatibility contribute to the usefulness and wide applicability of this device.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Quadrature VCO Outputs	
Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20V
TTL / HCMOS Compatible	
Wide Dynamic Range	2 mV to 3 Vrms
Adjustable Tracking Range (±1% to ±80%)	
Excellent Temp. Stability	20 ppm/°C, Typ.

APPLICATIONS

Frequency Synthesis
Data Synchronization
FM Detection
Tracking Filters
FSK Demodulation

ABSOLUTE MAXIMUM RATINGS

Power Supply	18V
Input Signal Level	3 Vrms
Power Dissipation	
Ceramic Package:	750 mW
Derate Above T_A = +25°C	6 mW/°C

Rev-A

SYSTEM DESCRIPTION

The XR-2212 is a complete PLL system with buffered inputs and outputs, an internal reference, and an uncommited op amp. Two VCO outputs are pinned out; one sources current, the other sources voltage. This enables operation as a frequency synthesizer using an external programmable divider. The op amp section can be used as an audio preamplifier for FM detection or as a high speed sense amplifier (comparator) for FSK demodulation. The center frequency, bandwidth, and tracking range of the PLL are controlled independantly by external components. The PLL output is directly by compatible with CMOS, HCMOS and TTL logic families as well as microprocessor peripheral systems.

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XR-2212 ELECTRICAL PERFORMANCE CHARACTERISTICS

TEST	SYMBOL	CONDITIONS		LIMITS		UNITS	GROUP A SUBGROUP
		CONDITIONS	TEMPERATURE	MIN	MAX		
Supply Current	I_{CC}	V_{CC} = 12V	TA = 25°C -55°C≤TA≤+125°C		10.00 12.00	mA mA	1 2, 3
Supply Current	I_{CC}	V_{CC} = 15V	TA = 25°C		15.00	mA	1
OSCILLATOR SECTION							
Frequency Accuracy	Fo	Ro = 30Kohm Co = 0.033µF	TA = 25°C -55°C≤TA≤+125°C		3.0 5.0	% %	9 10, 11
Frequency Stability vs Power Supply	Fd	V_{CC} = 12 ±1V	TA = 25°C -55°C≤TA≤+125°C		0.5 1.2	%/V %/V	9 10, 11
Upper Frequency Limit	Fmax	Ro = 8.2Kohm Co = 400pF	TA = 25°C -55°C≤TA≤+125°C	100 100		Khz Khz	9 10, 11
OSCILLATOR OUTPUTS							
Voltage Output Positive Swing	VOH	At Pin 5	TA = 25°C -55°C≤TA≤+125°C	9.50 9.50		V V	1 2, 3
Negative Swing	VOL	At Pin 5	TA = 25°C -55°C≤TA≤+125°C		0.4 0.4	V V	1 2, 3
Current Output Peak Current Swing		At Pin 3	TA = 25°C -55°C≤TA≤+125°C	100 100		µA µA	1 2, 3
LOOP PHASE DETECTOR SECTION							
Peak Output			TA = 25°C -55°C≤TA≤+125°C	150 100	300 300	µA µA	1 2, 3
Maximun Swing			TA = 25°C -55°C≤TA≤+125°C	4.00 4.00		V V	1 2, 3
OP AMP SECTION							
Voltage Gain			TA = 25°C -55°C≤TA≤+125°C	55 50		dB dB	4 5, 6
Input Bias Current	IB		TA = 25°C -55°C≤TA≤+125°C		1 1	µA µA	1 2, 3
Offset Voltage	VOS		TA = 25°C -55°C≤TA≤+125°C		20 20	mV mV	1 2, 3
INTERNAL REFERENCE							
Voltage Level	VREF		TA = 25°C -55°C≤TA≤+125°C	4.90 4.75	5.70 5.85	V V	1 2, 3

Programmable Timer/Counter

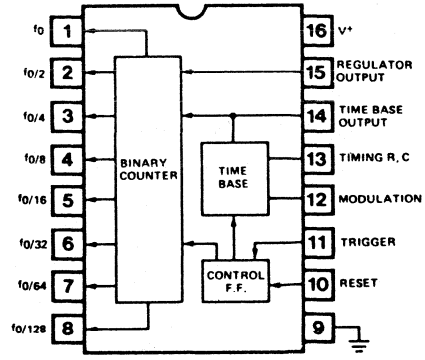
GENERAL DESCRIPTION

The XR-2240 Programmable Timer/Counter is a monolithic controller capable of producing ultra-long time delays without sacrificing accuracy. In most applications, it provides a direct replacement for mechanical or electromechanical timing devices and generates programmable time delays from micro-seconds up to five days. Two timing circuits can be cascaded to generate time delays up to three years.

As shown in Figure 1, the circuit is comprised of an internal time-base oscillator, a programmable 8-bit counter and a control flip-flop. The time delay is set by an external R-C network and can be programmed to any value from 1 RC to 255 RC.

In astable operation, the circuit can generate 256 separate frequencies or pulse-patterns from a single RC setting and can be syncronized with external clock signals. Both the control inputs and the outputs are compatible with TTL and DTL logic levels.

FUNCTIONAL BLOCK DIAGRAM



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FEATURES

Timing from micro-seconds to days
Programmable delays: 1RC to 255 RC
Wide supply range; 4V to 15V
TTL and DTL compatible outputs
High accuracy: 0.5%
External Sync and Modulation Capability
Excellent Supply Rejection: 0.2%/V

APPLICATIONS

Precision Timing	Frequency Synthesis
Long Delay Generation	Pulse Counting/Summing
Sequential Timing	A/D Conversion
Binary Pattern Generation	Digital Sample and Hold

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Power Dissipation	
Ceramic Package	750 mW
Derate above +25°C	6 mw/°C
Operating Temperature	
XR-2240	−55°C to +125°C
Storage Temperature	−65°C to +150°C

SYSTEM DESCRIPTION

The XR-2240 is a combination timer/counter capable of generating accurate timing intervals ranging from microseconds through several days. The time base works as an astable multivibrator with a period equal to RC. The eight bit counter can divide the time base output by any integer value from 1 to 255. The wide supply voltage range of 4.5 to 15 V, TTL and DTL logic compatibility, and 0.5% accuracy allow wide applicability. The counter may operate independently of the time base. Counter outputs are open collector and may be wire-OR connected.

The circuit is triggered or reset with positive going pulses. By connecting the reset pin (Pin 10) to one of the counter outputs, the time base will halt at timeout. If none of the outputs are connected to the reset, the circuit will continue to operate in the astable mode. Activating the trigger terminal (Pin 11) while the timebase is stopped will set all counter outputs to the low state and start the timebase.

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-2240

TEST	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current	V+ = 5V	T_A = +25°C		6	mA	1
		-55°C≤T_A≤+125°C		8	mA	2, 3
Supply Current	V+ = 15V	T_A = +25°C		16	mA	1
		-55°C≤T_A≤+125°C		20	mA	2, 3
Regulator Output	V+ = 5V	T_A = +25°C	4.1		V	1
		-55°C≤T_A≤+125°C	3.7		V	2, 3
Regulator Output	V+ = 15V	T_A = +25°C	6.0	6.6	V	1
		-55°C≤T_A≤+125°C	5.2	7.0	V	2, 3
Timing Accuracy	R = 10KΩ, C = 0.1μF	T_A = +25°C		2.0	%	9
		-55°C≤T_A≤+125°C		6.0	%	10, 11
Supply Drift	8V≤V+≤15V	T_A = +25°C		0.2	%/V	9
		-55°C≤T_A≤+125°C		0.4	%/V	10, 11
Maximum Frequency	R = 1KΩ, C = 0.007μF	T_A = +25°C	100		KHz	9
		-55°C≤T_A≤+125°C	85		KHz	10, 11
Modulation Voltage Level	V+ = 5V	T_A = +25°C	3	4	V	1
		-55°C≤T_A≤+125°C	3	4	V	2, 3
Trigger Threshold		T_A = +25°C		2.0	V	1
		-55°C≤T_A≤+125°C		2.3	V	2, 3
Reset Threshold		T_A = +25°C		2.0	V	1
		-55°C≤T_A≤+125°C		2.3	V	2, 3
Max Toggle Rate		T_A = +25°C	0.5		MHz	9
Input Threshold	V+ = 5V	T_A = +25°C	1.0		V	1
		-55°C≤T_A≤+125°C	0.5		V	2, 3
Output Sink Threshold	V_{OL} ≤0.4V, V_{REG} = V+ = 5V	T_A = +25°C	3		mA	1
		-55°C≤T_A≤+125°C	2		mA	2, 3
Output Leakage Current	V_{OH} = 15V	T_A = +25°C		8	μA	1
		-55°C≤T_A≤+125°C		8	μA	2, 3

Dual Monolithic Tone Decoder

GENERAL DESCRIPTION

The XR-2567 is a dual monolithic tone decoder of the 567-type that is ideally suited for tone or frequency decoding in multiple-tone communication systems. Each decoder of the XR-2567 can be used independently or both sections can be interconnected for dual operation. The matching and temperature tracking characteristics between decoders on this monolithic chip are superior to those available from two separate tone decoder packages.

The XR-2567 operates over a frequency range of 0.01 Hz to 500 kHz. Supply voltages can vary from 4.5V to 12V, with internal voltage regulation provided for supplies between 7V and 12V. Each decoder consists of a phase-locked loop (PLL), a quadrature AM detector, a voltage comparator, and a logic compatible output that can sink more than 100 mA of load current.

The center frequency of each decoder is set by an external resistor and capacitor which determine the free-running frequency of each PLL. When an input tone is present within the passband of the circuit, the PLL "locks" on the input signal. The logic output, which is normally "high", then switches to a "low" state during this "lock" condition.

FEATURES

Replaces two 567-type decoders
Excellent temperature tracking between decoders
Bandwidth adjustable from 0 to 14%
Logic compatible outputs with 100 mA sink capability
Center frequency matching (1% typ.)
Center frequency adjustable from 0.01 Hz to 500 kHz
Inherent immunity to false triggering
Frequency range adjustable over 20:1 range by external resistor.

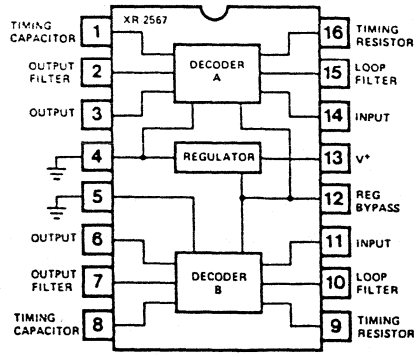
APPLICATIONS

Touch-Tone® Decoding
Sequential Tone Decoding
Dual-Tone Decoding/ Encoding
Communications Paging
Ultrasonic Remote-Control and Monitoring
Full-Duplex Carrier-Tone Transceiver
Wireless Intercom
Dual Precision Oscillator
FSK Generation and Detection

ABSOLUTE MAXIMUM RATINGS

Power Supply	
With Internal Regulator	14V
Without Regulator (Pins 12 and 13 shorted)	10V
Power Dissipation	
Ceramic Package	750 mW
Derate Above +25°C	6 mW/°C
Storage Temperature	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-2567 dual monolithic tone decoder consists of two independent 567-type circuits and an on board voltage regulator. Each decoder has a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. Both devices have normally high open collector outputs capable of sinking 100 mA.

The input signal is applied to Pin 14 (device A) or Pin 11 (device B), both with 20 kΩ nominal input resistance. Free running frequency is controlled by an RC network at Pins 1 and 16 (device A) or Pins 8 and 9 (device B). A capacitor on Pin 2 (A), or Pin 7 (B) serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 15 (A), or Pin 10 (B); bandwidth and skew are also dependent upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 13 is $+V_{CC}$ (4.75 to 12V nominal, 14V maximum); Pin 7 is ground; and Pin 3 (A) or Pin 6 (B) is the open collector output, pulling low when an in-band signal triggers the device.

Voltage supplies below 7V necessitate bypassing the internal regulator. This is accomplished by shorting Pin 12 to V_{CC}; for supplies over 7V, a bypass capacitor of at least 1 μF should AC ground Pin 12.

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-2567

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current Quiescent	Icc	Vcc = +5V	T_A = +25°C		16.0	mA	1
			-55°C≤T_A≤+125°C		16.0	mA	2, 3
Supply Current Quiescent	Icc	Vcc = +12V	T_A = +25°C		40.0	mA	1
			-55°C≤T_A≤+125°C		40.0	mA	2, 3
Supply Current Activated	Icc	Vcc = +5V	T_A = +25°C		26.0	mA	1
			-55°C≤T_A≤+125°C		26.0	mA	2, 3
Highest Center Frequency	Fc	Vcc = +12V	T_A = +25°C	100		KHz	9
			-55°C≤T_A≤+125°C	90		KHz	10, 11
Highest Center Frequency	Fc	Vcc = +5V	T_A = +25°C	100		KHz	9
			-55°C≤T_A≤+125°C	100		KHz	10, 11
Center Frequency Drift with Supply	Fo	4.75V≤Vcc≤6.75V	T_A = +25°C		1.00	%/V	9
			-55°C≤T_A≤+125°C		3.00	%/V	10, 11
Output Saturation Voltage	VSAT	IL = 30 mA Vin = 25 mV	T_A = +25°C		0.4	V	1
			-55°C≤T_A≤+125°C		0.6	V	2, 3
Output Saturation Voltage	VSAT	IL = 100 mA Vin = 25 mV	T_A = +25°C		1.0	V	1
			-55°C≤T_A≤+125°C		1.0	V	2, 3
Output Leakage Current	I_{OL}	**V_{IN} = 7.5mV** Vcc = +5V	T_A = +25°C		25	µA	1
			-55°C≤T_A≤+125°C		35	µA	2, 3
Largest No Output Input Voltage	V_{IL}	Vcc = +5V IL = 100 mA	T_A = +25°C	10		mVrms	4
			-55°C≤T_A≤+125°C	10		mVrms	5, 6
Smallest Detectable Input Voltage	V_{IS}	Vcc = +5V IL = 100 mA	T_A = +25°C		25	mVrms	7
			-55°C≤T_A≤+125°C		50	mVrms	8
Largest Detection Bandwidth	LDBW	Vcc = +5V Vin = 300 mV	T_A = +25°C	12	16	%	4
			-55°C≤T_A≤+125°C	10	27	%	5, 6
Largest Detection Bandwidth Skew	SKEW	Vcc = +5V Vin = 300 mV	T_A = +25°C		2.00	%	4
			-55°C≤T_A≤+125°C		3.00	%	5, 6

Precision Waveform Generator

GENERAL DESCRIPTION

The XR-8038 is a precision waveform generator IC capable of producing sine, square, triangular, sawtooth and pulse waveforms with a minimum number of external components and adjustments. Its operating frequency can be selected over eight decades of frequency, from 0.001 Hz to 200 KHz by the choice of external R-C components. The frequency of oscillation is highly stable over a wide range of temperature and supply voltage changes. Both full frequency sweeping as well as smaller frequency variations (FM) can be accomplished with an external control voltage. Each of the three basic waveforms, i.e., sinewave, triangle and square wave outputs are available simultaneously, from independent output terminals.

The XR-8038 monolithic waveform generator uses advanced processing technology and Schottky-barrier diodes to enhance its frequency performance. It can be readily interfaced with a monolithic phase-detector circuit, such as the XR-2208, to form stable phase-locked loop circuits.

FEATURES

With Improved Sweep Range, Frequency Drift and Max. Operating Frequency
Simultaneous Sine, Triangle and Square-Wave Outputs
Low Sine Wave Distortion—THD
High FM and Triangle Linearity
Wide Frequency Range
Variable Duty-Cycle

APPLICATIONS

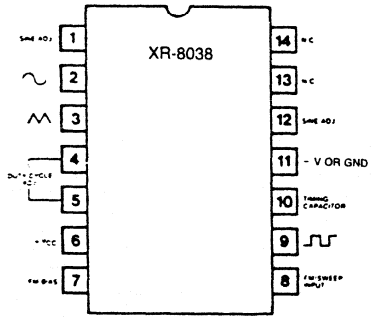
Precision Waveform Generation: Sine, Triangle, Square, Pulse
Sweep and FM Generation
Tone Generation
Instrumentation and Test Equipment Design
Precision PLL Design

ABSOLUTE MAXIMUM RATINGS

Power Supply	36V
Power Dissipation (package limitation)	
Ceramic package	750 mW
Derate above +25°C	6.0 mW/°C
Storage Temperature Range	−65°C to +150°C

REV-A

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-8038 precision waveform generator produces highly stable and sweepable square, triangle, and sine waves across eight frequency decades. The device time base employs resistors and a capacitor for frequency and duty cycle determination. The generator contains dual comparators, a flip-flop driving a switch, current sources, buffers, and a sine wave converter. Three identical frequency waveforms are simultaneously available. Supply voltage can range from 10V to 30V, or ±5V to ±15V with dual supplies.

Unadjusted sine wave distortion is typically less than 0.7%, with Pin 1 open and 82 kΩ from Pin 12 to Pin 11 (− V or ground). Sine wave distortion may be improved by including two 100 kΩ potentiometers between V_{CC} and − V (or ground), with one wiper connected to Pin 1 and the other connected to Pin 12.

Small frequency deviation (FM) is accomplished by applying modulation voltage to Pins 7 and 8; large frequency deviation (sweeping) is accomplished by applying voltage to Pin 8 only. Sweep range is typically 1000:1.

The square wave output is an open collector transistor; output amplitude swing closely approaches the supply voltage. Triangle output amplitude is typically 1/3 of the supply, and sine wave output reaches 0.22 of the supply voltage.

XR-8038 ELECTRICAL PERFORMANCE CHARACTERISTICS

TEST	SYMBOL	CONDITIONS (SEE NOTE 1)		LIMITS		UNIT	GROUP A SUBGROUP
		CONDITIONS	TEMPERATURE	MIN	MAX		
Supply Current	I_{CC} HI	V_{CC} = ±18V Measure Pin 6	TA = 25°C -55°C≤TA≤125°C		60.0 80.0	mA mA	1 2, 3
Supply Current	I_{CC} LO	V_{CC} = ±10V Measure Pin 6	TA = 25°C -55°C≤TA≤125°C	3.0 2.0	15.0 25.0	mA mA	1 2, 3
Timing Capacitor Source Current	I^{+}_{CAP}	V_{CC} = ±15V V_{SWEEP} = +10V $R_A = R_B$ = 10kΩ V_{CAP} = ±5.5V Measure Current at Pin 10	TA = 25°C -55°C≤TA≤125°C	450 400	550 600	µA µA	1 2, 3
Timing Capacitor Sink Current	I^{-}_{CAP}	V_{CC} = ±15V V_{SWEEP} = +10V $R_A = R_B$ = 10kΩ V_{CAP} = -5.5V Measure Current at Pin 10	TA = 25°C -55°C≤TA≤125°C	-550 -600	-450 -400	µA µA	1 2, 3
Timing Capacitor Source Current	I^{+}_{HIGH}	V_{CC} = ±15V V_{SWEEP} = +12V $R_A = R_B$ = 1kΩ V_{CAP} = -5.5V Measure Current at Pin 10	TA = 25°C -55°C≤TA≤125°C	2.50 2.00	3.50 4.00	mA mA	1 2, 3
Timing Capacitor Sink Current	I^{-}_{HIGH}	V_{CC} = ±15V V_{SWEEP} = +12V $R_A = R_B$ = 1kΩ V_{CAP} = +5.5V Measure Current at Pin 10	TA = 25°C -55°C≤TA≤125°C	-3.50 -4.00	-2.50 -2.00	mA mA	1 2, 3
Timing Capacitor Source Current	I^{+}_{LOW}	V_{CC} = ±15V V_{SWEEP} = +10V $R_A = R_B$ = 1MΩ V_{CAP} = +5.5V Measure Current at Pin 10	TA = 25°C -55°C≤TA≤125°C	2.20 -2.00	15.00 50.00	µA µA	1 2, 3
Timing Capacitor Sink Current	I^{-}_{LOW}	V_{CC} = ±15V V_{SWEEP} = +10V $R_A = R_B$ = 1MΩ V_{CAP} =-5.5V Measure Current at Pin 10	TA = 25°C -55°C≤TA≤125°C	-15.00 -50.00	-2.20 2.0	µA µA	1 2, 3
Timing Capacitor Source Current	I^{+}_{IN}	V_{CC} = ±15V V_{SWEEP} = +15V $R_A = R_B = \infty$ V_{CAP} = +5.5V Measure Current at Pin 10	TA = 25°C -55°C≤TA≤125°C	-0.50 -2.00	2.50 10.00	µA µA	1 2, 3

Timing Capacitor Sink Current	I^-_{IN}	V_{CC} = +15V V_{SWEEP} = +10V $R_A = R_B = \infty$ V_{CAP} = +5.5V Measure Current at Pin 10	TA = 25°C -55°C≤TA≤125°C	-8.0 -20.00	1.00 -2.00	µA µA	1 2, 3
Timing Capacitor Source Current	I^+_{LEAK}	V_{CC} = ±15V V_{SWEEP} = +10V $R_A = R_B = \infty$ V_{CAP} = +4.5V Measure Current at Pin 10	TA = 25°C -55°C≤TA≤125°C	-1.00 -10.00	1.00 10.00	µA µA	1 2, 3
Timing Capacitor Sink Current	I^-_{LEAK}	V_{CC} = ±15V V_{SWEEP} = +10V $R_A = R_B = \infty$ V_{CAP} = -4.5V Measure Current at Pin 10	TA = 25°C -55°C≤TA≤125°C	-1.00 -10.00	1.00 10.00	µA µA	1 2, 3
FM Sweep Bias Current	I_{BIAS}	V_{CC} = ±15V No V_{SWEEP} $R_A = R_B$ = 10KΩ V_{CAP} = GND Measure Current at Pin 8	TA = 25°C -55°C≤TA≤+125°C	-1.00 -10.00	1.00 10.00	µA µA	1 2, 3
FM Bias Voltage	V_{BIAS}	V_{CC} = ±15V No V_{SWEEP} $R_A = R_B$ = 10KΩ V_{CAP} = GND Measure Voltage at Pin 7	TA = 25°C -55°C≤TA≤+125°C	8.30 3.00	9.70 10.00	V V	1 2, 3
Square Wave Output Saturation Voltage	SQ_{LOW}	V_{CC} = ±15V V_{SWEEP} = GND $R_A = R_B$ = 10KΩ V_{CAP} =+5.5V I_{PIN9} = 2mA Measure Voltage at Pin 9	TA = 25°C -55°C≤TA≤+125°C	-15.00 -15.00	-14.60 -14.00	V V	1 2, 3
Square Wave Output Leakage Current	SQ_{HIGH}	V_{CC} = ±15V V_{SWEEP} = GND $R_A = R_B$ = 10KΩ V_{CAP} =+5.5V I_{PIN9} = +15V Measure Current at Pin 9	TA = 25°C -55°C≤TA≤+125°C	-2.5 -4.0	20.0 300.0	µA µA	1 2, 3
Triangle Output Offset Voltage	VOS_{TRI}	V_{CC} = ±15V V_{SWEEP} = GND $R_A = R_B$ = 10KΩ V_{CAP} = GND I_{PIN9} = +15V Measure Voltage at Pin 3	TA = 25°C -55°C≤TA≤+125°C	-100 -600	100 600	mV mV	1 2, 3

Sine Output Offset Voltage	VOS_{SIN}	V_{CC} = ±15V V_{SWEEP} = GND $R_A = R_B$ = 10KΩ V_{CAP} = GND Measure Voltage at Pin 2	TA = 25°C -55°C≤TA≤+125°C	-100 -600	100 600	mV mV	1 2, 3
Sine Output Voltage	V_{OUT}^+	V_{CC} = ±15V V_{SWEEP} = GND $R_A = R_B$ = 10KΩ V_{CAP} =+5V Measure Voltage at Pin 2	TA = 25°C -55°C≤TA≤+125°C	2.50 1.70	3.90 4.70	V V	1 2, 3
Sine Output Voltage	V_{OUT}^-	V_{CC} = ±15V V_{SWEEP} = GND $R_A = R_B$ = 10KΩ V_{CAP} =-5V Measure Voltage at Pin 2	TA = 25°C -55°C≤TA≤+125°C	-3.90 -4.70	-2.50 -1.70	V V	1 2, 3
Sine Adjust Voltage	V_{ADJ}^+	V_{CC} = ±15V No V_{SWEEP} $R_A = R_B = \infty$ V_{CAP} =GND Measure Voltage at Pin 1	TA = 25°C -55°C≤TA≤+125°C	2.50 1.70	3.90 4.70	V V	1 2, 3
Sine Adjust Voltage	V_{ADJ}^-	V_{CC} = ±15V No V_{SWEEP} $R_A = R_B = \infty$ V_{CAP} =GND Measure Voltage at Pin 12	TA = 25°C -55°C≤TA≤+125°C	-3.90 -4.70	-2.40 -1.70	V V	1 2, 3

Frequency	F_o	V_{CC} = ±10V CT = 3000pF R_A = R_B = 10KΩ Connect Pin 7 to Pin 8 R_L = 10KΩ Measure Frequency at Pin 9	TA = 25°C -55°C≤TA≤+125°C	8.600 3.400	10.000 10.100	KHz KHz	9 10, 11
Sine Wave Distortion Unadjusted	T_{HD}	V_{CC} = ±10V CT = 3000pF R_A = R_B = 100KΩ R_L = 10KΩ Connect Pin 7 to Pin 8 Measure Distortion at Pin 2	TA = 25°C -55°C≤TA≤+125°C	0.0 0.0	5.5 25.0	% %	9 10, 11
Sine Wave Distortion Adjusted	T_{HD} ADJ	V_{CC} = ±10V CT = 3000pF R_A = R_B = 100KΩ R_L = 10KΩ Connect Pin 7 to Pin 8 Adjust R_A + R_B to get 50% Duty Cycle at Pin 9 Measure Distortion at Pin 2	TA = 25°C -55°C≤TA≤+125°C	0.0 0.0	2.1 20.0	% %	9 10, 11

Note 1 - 82KΩ between Pin 11 and Pin 12

CMOS Dual Channel UART (DUART)

GENERAL DESCRIPTION

The EXAR Dual Univeral Asynchronous Receiver and Transmitter (DUART) is a data communications device that provides two fully independent full duplex asynchronous communications channels in a single package. The DUART is designed for use in micrprocessor based systems and may be used in a polled or interrupt driven environment.

Two basic versions of the DUART are available, each optimized for use with various microprocessor families: XR-88C681 for 8080/85, 8086/88, Z80, Z8000, 68xx and 65xx family based systems, and the XR-68C681 for 68000 family based systems. A programmable mode of the XR-88C681 version provides an interrupt daisy chain capability for use in Z80 and Z8000 based systems. However, the bus interfaces are general enough to allow interfacing with other microprocessors and microcontrollers. The XR--88C681 and XR-68C681 are enhanced versions of the Signetics, Motorola 2681 and 68681 respectively, and are pin and function compatible with those devices.

The DUART is fabricated using advanced two-layer metal high density CMOS process to provide high performance and low power consumption and is packaged in a 40 pin DIP or a 44 pin LCC. The XR-88C861 is also available in a 28 pin DIP.

FEATURES

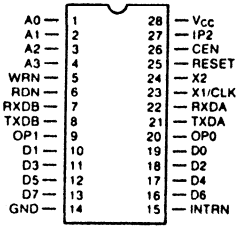
- Full Duplex, Dual Channel, Asynchronous Receiver and Transmitter
- Quadruple-Buffered Receiver, Dual-Buffered Transmitter
- Stop Bits Programmable in 1/16-bit Increments
- Internal Bit Rate Generator with 23 Bit Rates
- Independent Bit Rate Selection for Each Receiver and Transmitter
- Maximum Bit Rate: 1x Clock - 1 Mb/Sec, 16x Clock - 125Kb/Sec
- Normal, Autoecho, Local Loopback, and Remote Loopback Modes
- Multi-Function 16-Bit Counter/Timer
- Interrupt Output with Eight Maskable Interrupting Cond.
- Interrupt Vector Output on Acknowledge
- Programmable Interrupt Daisy Chain
- Up to 15 I/O Pins (Depending on Package and Version)
- Change of State Detectors on Inputs
- Multidrop Mode Compatible with 8051 Nine-Bit Mode
- On-Chip Oscillator for Crystal
- Standby Mode to Reduce Operating Power
- Advanced CMOS Low Power Technology

ABSOLUTE MAXIMUM RATINGS

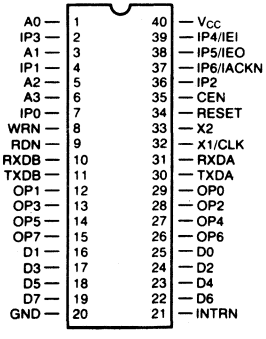
Storage Temperature	−65°C to +150°C
All Voltages with Respect to Ground	−0.5 V to +7.0 V

PACKAGE OUTLINE DIAGRAMS

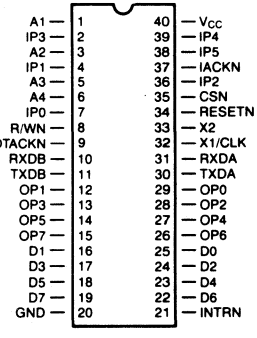
XR-88C681/28

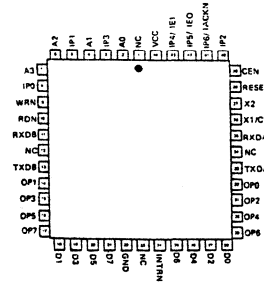


XR-88C681/40

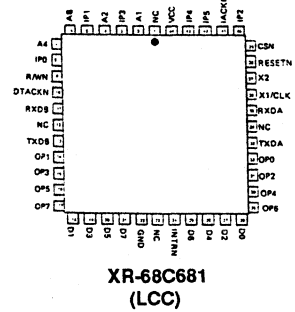


XR-68C681





XR-88C681
(LCC)



XR-68C681
(LCC)

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-68C681

TEST	SYMBOL	CONDITIONS (See Note 1)	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Input Low Voltage	V_{IL}		T_A = +25°C	-0.5	0.8	V	1
			-55°C≤T_A≤+125°C	-0.5	0.8	V	2, 3
Input High Voltage	V_{IH}		T_A = +25°C	2.2		V	1
			-55°C≤T_A≤+125°C	2.2		V	2, 3
Input High Voltage (x1/CLK)	V_{IH1}		T_A = +25°C	4.0	Vcc	V	1
			-55°C≤T_A≤+125°C	4.0	Vcc	V	2, 3
Output Low Voltage	V_{OL}	I_{OL} = 2.4 mA	T_A = +25°C		0.4	V	1
			-55°C≤T_A≤+125°C		0.4	V	2, 3
Output High Voltage (Except Open Drain Outputs)	V_{OH}	I_{OH} = -400 µA	T_A = +25°C	2.4		V	1
			-55°C≤T_A≤+125°C	2.4		V	2, 3
Input Leakage Current (Except x1/CLK,x2)	I_{IL}	V_{IN} = 0 to Vcc	T_A = +25°C	-10	10	µA	1
			-55°C≤T_A≤+125°C	-10	10	µA	2, 3
Data Bus 3 - State Leakage Current	I_{LL}	Vo = 0 to Vcc	T_A = +25°C	-10	10	µA	1
			-55°C≤T_A≤+125°C	-10	10	µA	2, 3
Open Drain Output Leakage Current	Ioc	Vo = 0 to Vcc	T_A = +25°C	-10	10	µA	1
			-55°C≤T_A≤+125°C	-10	10	µA	2, 3
Power Supply Active Current	I_{CCA}		T_A = +25°C		15	mA	1
			-55°C≤T_A≤+125°C		15	mA	2, 3
Power Supply Standby Current	I_{CCS}		T_A = +25°C		10	mA	1
			-55°C≤T_A≤+125°C		10	mA	2, 3
Reset Pulse Width	t_{RES}		T_A = +25°C	1.0		µS	9
			-55°C≤T_A≤+125°C	1.0		µS	10, 11
Port Input Set Up Time To RDN/CSN Low	tPS		T_A = +25°C	0		nS	9
			-55°C≤T_A≤+125°C	0		nS	10, 11
Port Input Hold Time From RDN/CSN High	tPH		T_A = +25°C	0		nS	9
			-55°C≤T_A≤+125°C	0		nS	10, 11
Port Output Valid From WRN/CSN High	tPD		T_A = +25°C		400	nS	9
			-55°C≤T_A≤+125°C		400	nS	10, 11

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ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-68C681

TEST	SYMBOL	CONDITIONS (See Note 1)	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
INTRN or OP3-OP7 When used as Interrupts High from: Clear of Interrupt Status Bit in ISR or IPCR	t_{IR}		T_A = +25°C -55°C≤T_A≤+125°		300 300	nS nS	9 10, 11
Clear of Interrupt Mask Bit in IMR			T_A = +25°C -55°C≤T_A≤+125°C		300 300	nS nS	9 10, 11
X1/CLK (External) High or Low Time	t_{CLK}		T_A = +25°C -55°C≤T_A≤+125°C	100 100		nS nS	9 10, 11
X1/CLK Crystal or External Frequency	f_{CLK}		T_A = +25°C -55°C≤T_A≤+125°C	2.0 2.0	4.0 4.0	MHz MHz	9 10, 11
Counter/Timer External Clock High or Low Time	t_{CTC}		T_A = +25°C -55°C≤T_A≤+125°C	100 100		nS nS	9 10, 11
Counter/Timer External Clock Frequency	f_{CTC}		T_A = +25°C -55°C≤T_A≤+125°C	0.0 0.0	4.0 4.0	MHz MHz	9 10, 11
RXC and TXC (External) High or Low Time	t_{RTX}		T_A = +25°C -55°C≤T_A≤+125°C	220 220		nS nS	9 10, 11
RXC and TXC (External) Frequency 16X	f_{RTX}		T_A = +25°C -55°C≤T_A≤+125°C	0.0 0.0	2.0 2.0	MHz MHz	9 10, 11
RXC and TXC (External) Frequency 1X	f_{RTX}		T_A = +25°C -55°C≤T_A≤+125°C	0.0 0.0	1.0 1.0	MHz MHz	9 10, 11
TXD Output Delay From TXC (External) Low	t_{TXD}		T_A = +25°C -55°C≤T_A≤+125°C		350 350	nS nS	9 10, 11
TXD Output Delay From TXC (Internal) Output Low	t_{TCS}		T_A = +25°C -55°C≤T_A≤+125°C	0 0	150 150	nS nS	9 10, 11
RXD Data Set Up Time to RXC (External) High	t_{RXS}		T_A = +25°C -55°C≤T_A≤+125°C	240 240		nS nS	9 10, 11
RXC Data Hold Time From RXC (External) High	t_{RXH}		T_A = +25°C -55°C≤T_A≤+125°C	200 200		nS nS	9 10, 11
DTACKN High From CSN or IACKN High	t_{DAH}		T_A = +25°C -55°C≤T_A≤+125°C		100 100	nS nS	9 10, 11
DTACKN High Impedance From CSN or IACKN High	t_{DAT}		T_A = +25°C -55°C≤T_A≤+125°C		125 125	nS nS	

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-68C681

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
CSN or IACKN Set Up Time to CLK High	t_{CSC}		T_A = +25°C	90		nS	9
			-55°C≤T_A≤+125°C	90		nS	10, 11
A1-A4 Set Up Time Time to CSN Low	t_{AS}		T_A = +25°C	10		nS	9
			-55°C≤T_A≤+125°C	10		nS	10, 11
A1-A4 Hold Time From CSN High	t_{AH}		T_A = +25°C	0		nS	9
			-55°C≤T_A≤+125°C	0		nS	10, 11
RWN Set Up Time To CSN Low	t_{RWS}		T_A = +25°C	0		nS	9
			-55°C≤T_A≤+125°C	0		nS	10, 11
RWN Hold Time To CSN High	t_{RWH}		T_A = +25°C	0		nS	9
			-55°C≤T_A≤+125°C	0		nS	10, 11
CSN High Pulse Width	t_{CSW}		T_A = +25°C	90		nS	9
			-55°C≤T_A≤+125°C	90		nS	10, 11
CSN or IACKN High From DTACKN Low	t_{CSD}		T_A = +25°C	20		nS	9
			-55°C≤T_A≤+125°C	20		nS	10, 11
Data Valid From CSN or IACKN Low	t_{DD}		T_A = +25°C		175	nS	9
			-55°C≤T_A≤+125°C		175	nS	10, 11
Data Bus Floating From CSN or IACKN High	t_{DF}		T_A = +25°C	10	100	nS	9
			-55°C≤T_A≤+125°C	10	100	nS	10, 11
Data Set Up Time To CLK High	t_{DS}		T_A = +25°C	100		nS	9
			-55°C≤T_A≤+125°C	100		nS	10, 11
Data Hold Time From CSN High	t_{DH}		T_A = +25°C	0		nS	9
			-55°C≤T_A≤+125°C	0		nS	10, 11
DTACKN Low From Read Data Valid	t_{DAL}		T_A = +25°C	0		nS	9
			-55°C≤T_A≤+125°C	0		nS	10, 11
DTACKN Low (Read Cycle) From CLK High	t_{DCR}		T_A = +25°C		125	nS	9
			-55°C≤T_A≤+125°C		125	nS	10, 11
DTACKN Low (Write Cycle) From CLK High	t_{DCW}		T_A = +25°C		125	nS	9
			-55°C≤T_A≤+125°C		125	nS	10, 11

Notes:

1. Vcc = 5.0 V ± 10%

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-88C681

TEST	SYMBOL	CONDITIONS (See Note 1)	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
INTRN or OP3-OP7 When used as Interrupts High from: Clear of Interrupt Status Bit in ISR or IPCR	t_{IR}		$T_A = +25°C$ $-55°C \leq T_A \leq +125°$		300 300	nS nS	9 10, 11
Clear of Interrupt Mask Bit in IMR	t_{IR}		$T_A = +25°C$ $-55°C \leq T_A \leq +125°C$		300 300	nS nS	9 10, 11
X1/CLK (External) High or Low Time	t_{CLK}		$T_A = +25°C$ $-55°C \leq T_A \leq +125°C$	100 100		nS nS	9 10, 11
X1/CLK Crystal or External Frequency	f_{CLK}		$T_A = +25°C$ $-55°C \leq T_A \leq +125°C$	2.0 2.0	4.0 4.0	MHz MHz	9 10, 11
Counter/Timer External Clock High or Low Time	t_{CTC}		$T_A = +25°C$ $-55°C \leq T_A \leq +125°C$	100 100		nS nS	9 10, 11
Counter/Timer External Clock Frequency	f_{CTC}		$T_A = +25°C$ $-55°C \leq T_A \leq +125°C$	0.0 0.0	4.0 4.0	MHz MHz	9 10, 11
RXC and TXC (External) High or Low Time	t_{RTX}		$T_A = +25°C$ $-55°C \leq T_A \leq +125°C$	220 220		nS nS	9 10, 11
RXC and TXC (External) Frequency 16X	f_{RTX}		$T_A = +25°C$ $-55°C \leq T_A \leq +125°C$	0.0 0.0	2.0 2.0	MHz MHz	9 10, 11
RXC and TXC (External) Frequency 1X	f_{RTX}		$T_A = +25°C$ $-55°C \leq T_A \leq +125°C$	0.0 0.0	1.0 1.0	MHz MHz	9 10, 11
TXD Output Delay From TXC (External) Low	t_{TXD}		$T_A = +25°C$ $-55°C \leq T_A \leq +125°C$		350 350	nS nS	9 10, 11
TXD Output Delay From TXC (Internal) Output Low	t_{TCS}		$T_A = +25°C$ $-55°C \leq T_A \leq +125°C$	0 0	150 150	nS nS	9 10, 11
RXD Data Set Up Time to RXC (External) High	t_{RXS}		$T_A = +25°C$ $-55°C \leq T_A \leq +125°C$	240 240		nS nS	9 10, 11
RXC Data Hold Time From RXC (External) High	t_{RXH}		$T_A = +25°C$ $-55°C \leq T_A \leq +125°C$	200 200		nS nS	9 10, 11

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-88C681

TEST	SYMBOL	CONDITIONS (See Note 1)	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Input Low Voltage	V_{IL}		T_A = +25°C	-0.5	0.8	V	1
			-55°C≤T_A≤+125°C	-0.5	0.8	V	2, 3
Input High Voltage	V_{IH}		T_A = +25°C	2.2		V	1
			-55°C≤T_A≤+125°C	2.2		V	2, 3
Input High Voltage (x1/CLK)	$V_{IH}1$		T_A = +25°C	4.0	Vcc	V	1
			-55°C≤T_A≤+125°C	4.0	Vcc	V	2, 3
Output Low Voltage	V_{OL}	I_{OL} = 2.4 mA	T_A = +25°C		0.4	V	1
			-55°C≤T_A≤+125°C		0.4	V	2, 3
Output High Voltage (Except Open Drain Outputs)	V_{OH}	I_{OH} = -400 µA	T_A = +25°C	2.4		V	1
			-55°C≤T_A≤+125°C	2.4		V	2, 3
Input Leakage Current (Except x1/CLK,x2)	I_{IL}	V_{IN} = 0 to Vcc	T_A = +25°C	-10	10	µA	1
			-55°C≤T_A≤+125°C	-10	10	µA	2, 3
Data Bus 3 - State Leakage Current	I_{LL}	Vo = 0 to Vcc	T_A = +25°C	-10	10	µA	1
			-55°C≤T_A≤+125°C	-10	10	µA	2, 3
Open Drain Output Leakage Current	Ioc	Vo = 0 to Vcc	T_A = +25°C	-10	10	µA	1
			-55°C≤T_A≤+125°C	-10	10	µA	2, 3
Power Supply Active Current	I_{CCA}		T_A = +25°C		15	mA	1
			-55°C≤T_A≤+125°C		15	mA	2, 3
Power Supply Standby Current	I_{CCS}		T_A = +25°C		10	mA	1
			-55°C≤T_A≤+125°C		10	mA	2, 3
Reset Pulse Width	t_{RES}		T_A = +25°C	1.0		µS	9
			-55°C≤T_A≤+125°C	1.0		µS	10, 11
Port Input Set Up Time To RDN/CSN Low	tPS		T_A = +25°C	0		nS	9
			-55°C≤T_A≤+125°C	0		nS	10, 11
Port Input Hold Time From RDN/CSN High	tPH		T_A = +25°C	0		nS	9
			-55°C≤T_A≤+125°C	0		nS	10, 11
Port Output Valid From WRN/CSN High	tPD		T_A = +25°C		400	nS	9
			-55°C≤T_A≤+125°C		400	nS	10, 11

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ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-88C681

TEST	SYMBOL	CONDITIONS (See Note 1)	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
IEI Set Up Time to RDN Low	T_{EIS}		T_A = +25°C	50		nS	9
			-55°C≤T_A≤+125°C	50		nS	10, 11
IEO Delay Time from INTRN Low	T_{EOD}		T_A = +25°C		100	nS	9
			-55°C≤T_A≤+125°C		100	nS	10, 11
A0-A3 Set Up Time to RDN, WRN Low	t_{AS}		T_A = +25°C	10		nS	9
			-55°C≤T_A≤+125°C	10		nS	10, 11
A0-A3 Hold Time from RDN, WRN High	t_{AH}		T_A = +25°C	0		nS	9
			-55°C≤T_A≤+125°C	0		nS	10, 11
CEN Set Up Time from RDN, WRN High	t_{CS}		T_A = +25°C	0		nS	9
			-55°C≤T_A≤+125°C	0		nS	10, 11
CEN Hold Time to RDN, WRN Low	t_{CH}		T_A = +25°C	0		nS	9
			-55°C≤T_A≤+125°C	0		nS	10, 11
RDN, WRN Pulse Width	t_{RW}		T_A = +25°C	225		nS	9
			-55°C≤T_A≤+125°C	225		nS	10, 11
Data Valid from RDN Low	t_{DD}		T_A = +25°C		175	nS	9
			-55°C≤T_A≤+125°C		175	nS	10, 11
Data Bus Floating RDN High	t_{DF}		T_A = +25°C	10	100	nS	9
			-55°C≤T_A≤+125°C	10	100	nS	10, 11
Data Set Up Time To WRN High	t_{DS}		T_A = +25°C	100		nS	9
			-55°C≤T_A≤+125°C	100		nS	10, 11
Data Hold Time From WRN High	t_{DH}		T_A = +25°C	5		nS	9
			-55°C≤T_A≤+125°C	5		nS	10, 11
High Time Between Reads and/or Writes	t_{RWD}		T_A = +25°C	200		nS	9
			-55°C≤T_A≤+125°C	200		nS	10, 11
IEO Delay Time From IEI	t_{DIO}		T_A = +25°C		100	nS	9
			-55°C≤T_A≤+125°C		100	nS	10, 11
IACKN Hold Time From RDN High	t_{IAH}		T_A = +25°C	0		nS	9
			-55°C≤T_A≤+125°C	0		nS	10, 11

Notes:

1. V_{CC} = 5.0 V ± 10%

CMOS Quad Channel UART (QUART)

PRELIMINARY

GENERAL DESCRIPTION

The EXAR Quad Universal ASynchronous Receiver and Transmitter (QUART) is a data communications device that provides four fully independent full duplex asynchronous communications channels in a single package. The QUART is designed for use in microprocessor based systems and may be used in a polled or interrupt driven environment.

The XR-82C684 offers a single IC solution for various microprocessor families. The 88 and 68 modes can be selected by tying SEL pin to VDD or VSS.

The QUART is fabricated using advanced two layer metal, with a high density EPI/CMOS process to provide high performance and low power consumption.

FEATURES

Four Full Duplex, Independent Channels, Asynchronous Receiver and Transmitter
Quadruple Receive and Transmit Buffer
Programmable Stop Bits in 1/16 Bit Increments
Pin Selectable 88 and 68 mode
Four Independent Internal Bit Rate Generator with more than 33 Bit Rates
Independent Bit Rate Selection for each Transmitter and Receiver
External Clock Capability
Normal, Autoecho, Local Loop Back and Remote Loopback Modes
Two Multifunction 16-Bit Counter/Timer
Interrupt Output with Sixteen Maskable Interrupt Conditions
Prioritized Interrupt Vector Output on Acknowledge
Programmable Interrupt Daisy Chain
16 General Purpose Outputs
16 General Purpose Inputs with Eight Change of State Detectors on Inputs
Multidrop Mode Compatible with 8051 Nine-Bit Mode
On Chip Oscillator for Crystal
Stand-by Mode to Reduce Operating Power

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to 150°C
All Voltages with respect to ground	-0.5V to +7 V

Consult Factory for Package Information.

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XR-82C684 ELECTRICAL PERFORMANCE CHARACTERISTICS

TEST	SYMBOL	CONDITIONS		LIMITS		UNIT	GROUP A SUBGROUP
		SEE NOTE 1	TEMPERATURE	MIN	MAX		
Input Low Voltage	V_{IL}		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C	-0.5 -0.5	0.8 0.8	V V	1 2,3
Input High Voltage	V_{IH}		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C	2.0 2.2		V V	1 2,3
Input High Voltage (x1 / CLK)	$V_{IH}1$		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C	4.0 4.0	V_{CC} V_{CC}	V V	1 2,3
Output Low Voltage	V_{OL}	I_{OL} = 2.4mA	T_A = +25 °C -55°C ≤ T_A ≤ + 125°C		0.4 0.4	V V	1 2,3
Output High Voltage (Except open Drain Outputs)	V_{OH}	IOH = -400µA	T_A = +25 °C -55°C ≤ T_A ≤ + 125°C	2.4 2.4		V V	1 2,3
Input Leakage Current	I_{IL}	V_{IN} = 0 to Vcc	T_A = +25 °C -55°C ≤ T_A ≤ + 125°C	-15 -25	15 25	µA µA	1 2,3
Data Bus 3-State Leakage Current	I_{IL}	V_O = 0 to Vcc	T_A = +25 °C -55°C ≤ T_A ≤ + 125°C	-10 -10	10 10	µA µA	1 2,3
Open Drain Output Leakage Current	I_{OC}	V_O = 0 to Vcc	T_A = +25 °C -55°C ≤ T_A ≤ + 125°C	-10 -10	10 10	µA µA	1 2,3
Power Supply Active Current	I_{CCA}		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C		15 15	mA mA	1 2,3
Power Supply Standby Current	I_{CCS}		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C		10 10	mA mA	1 2,3
Reset Pulse Width	t_{RES}		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C	1.0 1.0		µS µS	9 10,11

XR-82C684 ELECTRICAL PERFORMANCE CHARACTERISTICS

TEST	SYMBOL	CONDITIONS		LIMITS		UNIT	GROUP A SUBGROUP
		SEE NOTE 1	TEMPERATURE	MIN	MAX		
Port Input Set Up Time To RD/CS Low	t_{PS}		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C	0 0		nS nS	9 10,11
Port Input Hold Time From RD/CS High	t_{PH}		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C	0 0		nS nS	9 10,11
Port Output Valid From WR/CS High	t_{PD}		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C		400 400	nS nS	9 10,11
Intr or OP3-OP7 / OP10-OP15 When Used as Interrupt High From: Clear of Interrupt Status Bit in ISR or IPCR	t_{IR}		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C		300 300	nS nS	9 10,11
Clear of Interrupt Mask In IMR	t_{IR}		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C		300 300	nS nS	9 10,11
X1/CLK (external) High or Low Time	t_{CLK}		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C	100 100		nS nS	9 10,11
X1/CLK Crystal or External Frequency	f_{CLK}		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C	2.0 2.0	7.372 7.372	MHz MHz	9 10,11
Counter / Timer External Clock High or Low Time (1P2/1P10)	t_{CTC}		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C	100 100		nS nS	9 10,11
Counter / Time External Clock Frequency	f_{CTC}		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C	0.0 0.0	7.372 7.372	MHz MHz	9 10,11
RXC and TXC (External) High or Low Time	t_{RTX}		T_A = +25 °C -55°C ≤ T_A ≤ + 125°C	220 220		nS nS	9 10,11

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XR-82C684 ELECTRICAL PERFORMANCE CHARACTERISTICS

R_{XC} and T_{XC} (External) Frequency 16X	f_{RTX}		TA = +25°C -55°C ≤ T_A ≤ + 125°C	0.0 0.0	16.0 16.0	MHz MHz	9 10,11
R_{XC} and T_{XC} (External) Frequency 1X	f_{RTX}		TA = +25°C -55°C ≤ T_A ≤ + 125°C	0.0 0.0	1.0 1.0	MHz MHz	9 10, 11
T_{XD} Output Delay from T_{XC} (External) Low	t_{TXD}		TA = +25°C -55°C ≤ T_A ≤ + 125°C		350 350	nS nS	9 10, 11
T_{XD} Output Delay from T_{XC} (Internal) Output Low	t_{TCS}		TA = +25°C -55°C ≤ T_A ≤ + 125°C	0 0	150 150	nS nS	9 10, 11
R_{XD} Data Setup Time to R_{XC} External High	t_{RXS}		TA = +25°C -55°C ≤ T_A ≤ + 125°C	240 240		nS nS	9 10, 11
R_{XD} Data Hold Time from R_{XC} External High	t_{RXH}		TA = +25°C -55°C ≤ T_A ≤ + 125°C	200 200		nS nS	9 10, 11
IEI Setup Time to RD Low	T_{EIS}		TA = +25°C -55°C ≤ T_A ≤ + 125°C	50 50		nS nS	9 10, 11
IEO Delay Time from Internal Low	T_{EOD}		TA = +25°C -55°C ≤ T_A ≤ + 125°C		100 100	nS nS	9 10, 11
A0-A4 Setup Time to RD, WR Low	t_{AS}		TA = +25°C -55°C ≤ T_A ≤ + 125°C	10 10		nS nS	9 10, 11
A0-A4 Hold Time from RD, WR Low	t_{AH}		TA = +25°C -55°C ≤ T_A ≤ + 125°C	0 0		nS nS	9 10, 11
CS Setup Time to RD, WR Low	t_{CS}		TA = +25°C -55°C ≤ T_A ≤ + 125°C	0 0		nS nS	9 10, 11

XR-82C684 ELECTRICAL PERFORMANCE CHARACTERISTICS

CS Hold Time from RD, WR High	tC_H		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
RD, WR Pulse Width	t_{RW}		TA = +25°C -55°C≤TA≤+125°C	225 225		nS nS	9 10, 11
Data Valid from RD Low	t_{DD}		TA = +25°C -55°C≤TA≤+125°C		175 175	nS nS	9 10, 11
Data Bus Floating from RD High	t_{DF}		TA = +25°C -55°C≤TA≤+125°C	10 10	100 100	nS nS	9 10, 11
Data Setup Time to WR High	t_{DS}		TA = +25°C -55°C≤TA≤+125°C	100 100		nS nS	9 10, 11
Data Hold Time from WR High	t_{DH}		TA = +25°C -55°C≤TA≤+125°C	5 5		nS nS	9 10, 11
High Time Between Reads and/or Writes	t_{RWD}		TA = +25°C -55°C≤TA≤+125°C	100 100		nS nS	9 10, 11
IEO Delay Time from IEI	t_{DIO}		TA = +25°C -55°C≤TA≤+125°C		100 100	nS nS	9 10, 11
IACK Hold Time from RD High	t_{IAH}		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11

XR-82C684 ELECTRICAL PERFORMANCE CHARACTERISTICS

DTACK High from CS or IACK High	t_{DAH}		TA = +25°C -55°C≤TA≤+125°C		100 100	nS nS	9 10, 11
DTACK High Impedasnce from CS or IACK High	t_{DAT}		TA = +25°C -55°C≤TA≤+125°C		125 125	nS nS	9 10, 11
CS or IACK Setup Time to Clock High	t_{CGC}		TA = +25°C -55°C≤TA≤+125°C	90 90		nS nS	9 10, 11
A1-A5 Setup Time to CS Low	t_{AS}		TA = +25°C -55°C≤TA≤+125°C	10 10		nS nS	9 10, 11
A1-A5 Hold Time from CS High	t_{AH}		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
RW Setup Time to CS Low	tR_{WS}		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
RW Setup Time to CS High	t_{RWH}		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
CS High Pulse Width	tC_{SW}		TA = +25°C -55°C≤TA≤+125°C	90 90		nS nS	9 10, 11
CS or IACK High from DTACK Low	t_{CSD}		TA = +25°C -55°C≤TA≤+125°C	20 20		nS nS	9 10, 11
Data Valid from CS or IACK Low	t_{DD}		TA = +25°C -55°C≤TA≤+125°C		175 175	nS nS	9 10, 11
Data Bus Floating from CS or IACK High	t_{DF}		TA = +25°C -55°C≤TA≤+125°C	10 10	100 100	nS nS	9 10, 11
Data Setup Time to Clock High	t_{DS}		TA = +25°C -55°C≤TA≤+125°C	100 100		nS nS	9 10, 11
Data Hold Time from CS High	t_{DH}		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
DTACK Low from Read Data Valid	t_{DAL}		TA = +25°C -55°C≤TA≤+125°C	100 100		nS nS	9 10, 11
DTACK Low (Read Cycle) from Clock High	tD_{CR}		TA = +25°C -55°C≤TA≤+125°C		125 125	nS nS	9 10, 11
DTACK Low (Write Cycle) from Clock High	t_{DCW}		TA = +25°C -55°C≤TA≤+125°C		125 125	nS nS	9 10, 11

Notes: 1) V_{CC} = 5.0V±10%

EXAR ...the analog plus™ company

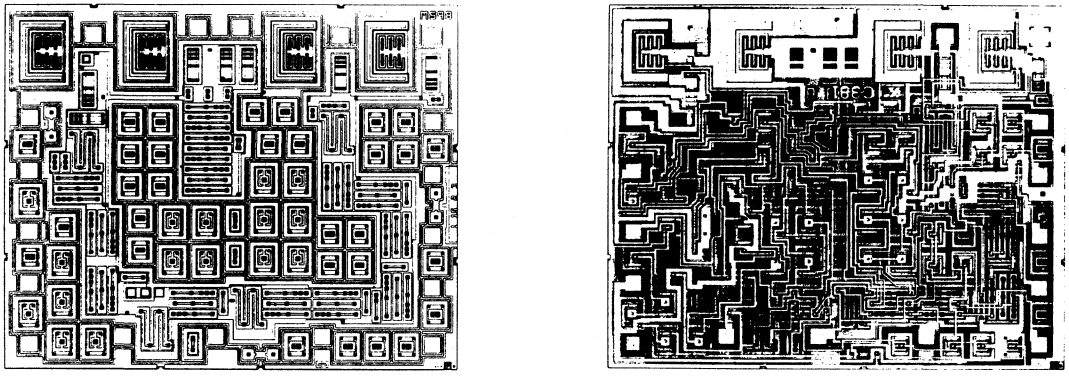
BIPOLAR SEMI-CUSTOM DESIGN CONCEPT

Traditionally, the development of custom IC's has been a long and costly undertaking. The development time would normally run in excess of one year, design changes are slow and costly, and it may take a long time to get from the prototype stage to full production. Because of these difficulties, the use of custom IC's could be economically justified only when a very large quantity of circuits, i.e., several hundred-thousand units, were required during the life of the end product. In the past, these drawbacks have severely limited the use of custom monolithic IC's.

The bipolar semi-custom design concept, pioneered by Exar, now overcomes this traditional problem. Exar makes this possible by stocking wafers that are completely fabricated except for the final process step of device interconnection which metalizes all selected components together in the required circuit configuration This enables an engineer to design a metal mask based on his circuit which will interconnect the uncommitted components on the prefabricated wafers, and thus convert them into customized chips corresponding to the customer's design. This allows one to develop an almost unlimited variety of custom linear or digital integrated circuits at very substantial cost savings.

The semi-custom program is intended for those customers seeking cost effective methods of reducing component count and board size in order to compete more effectively in a changing marketplace. The program allows a customized monolithic IC to be developed with a turnaround time of several weeks, at approximately 10% to 20% of the development costs for tooling associated with the conventional full custom designs. The semi-custom design concept is an interactive or cooperative development effort between Exar and the customer. In most cases, the cost and development time for the program can be reduced even further, if the customer does the design and breadboarding of his own semi-custom IC, using Exar Design Kits, instruction manuals and layout sheets.

The semi-custom design approach is based on a number of standardized IC chips with fixed component locations. These standardized IC chips, called Master-Chips, contain a large number of undedicated active and passive components (i.e., transistors, resistors, logic gates, etc.). These integrated components can be interconnected in thousands of different ways with a customizing interconnection pattern. Each different metal interconnection pattern creates a new custom IC. The figures below show the magnified photograph of a Master-Chip, both in its prefabricated form and after its customization with a special interconnection pattern. This method is called semi-custom rather than full custom, since only the last layer of tooling is changed to customize an IC chip, and rest of the layers are standard. As a result, the development phase is very short, far less expensive and risk free, compared to conventional full or dedicated custom IC's. Similarly, if a design change or iteration is necessary, it can be readily accommodated within a matter of weeks by simply generating a new or modified interconnection pattern.



Magnified Photograph of a Linear Master-Chip Before and After Customizing

YOUR FIRST STEP

Your very first step, at the start of a semi-custom program, should be to contact Exar for a preliminary analysis and discussion of your needs. This can be done even while the program is still at the thought stage. This initial review by Exar is performed at no cost to the customer and is essential to the success of the program. It avoids any possible design pitfalls or misunderstandings. This early interaction also allows you to find out some of the options or variations available in Exar's semi-custom programs and choose the one which is best suited to your needs.

The following is required by Exar's technical staff to provide you with an accurate feasibility study of your project. and a budgetary estimate of the development costs, timetables and production pricing.

- A block diagram of circuit function and input/output interface requirements.
- A circuit schematic or logic diagram of your circuit.
- Preliminary or objective performance specifications and limits on critical circuit parameters (also possible tradeoffs which may be allowed).
- Test specifications
- Packaging requirements.
- Production quantity requirements.
- Desired development and production timetables.
- An indication of how much of the breadboarding, layout, etc., can be done by you, the customer, using Exar's Kit Parts or Soft Macros

Once the above data package is submitted to Exar, we would review it and respond to you within a few days.

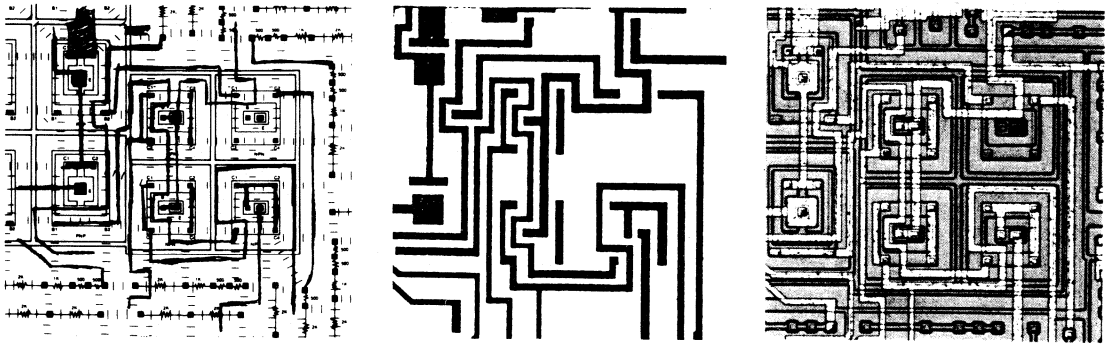
Normally, the test system development effort is initiated in parallel with chip development. Exar has a complete computer controlled IC test facility and offers complete IC testing capability for production units.

FREQUENTLY ASKED QUESTIONS AND THEIR ANSWERS

Based on our long experience with Exar's semi-custom Master-Chips, we have compiled a comprehensive glossary of the most often asked questions concerning the program. The following is a list of these questions and their answers.

WHAT IS THE COST OF THE BASIC PROGRAM?

The cost of the semi-custom development program depends on how much of the design and layout is done by the customer. In general, the basic semi-custom program is where the customer does the design, breadboard evaluation and layout on the Master-Chip worksheet; and Exar does only the IC tooling and prototype fabrication. This is the most economical and cost effective approach.



Steps of Semi-Custom Design

For bipolar semi-custom designs, the development cost of the basic program is in the range of $2,000 to $10,000, starting with an accurate layout supplied by the customer. The above prices also include the cost of 25 monolithic prototypes delivered at the completion of the program. Additional prototypes are available at a nominal cost.

WHAT IS THE DEVELOPMENT TIME?

Typical development time for the basic bipolar semi-custom program is four weeks, starting with the customer's layout and ending with the monolithic prototypes. If Exar is required to do the IC layout or breadboarding evaluation, several additional weeks may be required to complete the development program.

WHAT IF ADDITIONAL DESIGN CYCLES ARE NEEDED?

If the customer desires to modify the design or layout after evaluation of the initial prototypes, a new design iteration cycle can be completed within 4-6 weeks. Cost for this iteration is dependent on the complexity of modification.

WHAT ABOUT PRODUCTION PRICING?

The production pricing of monolithic IC's depends upon a number of important factors such as:

a) Master-Chip type.

b) Circuit complexity (i.e., yield).

c) Device performance and test requirements.

d) Special environmental screening requirements (burn-in, hermeticity tests, etc.).

e) Package type required.

In the case of a custom IC, it is impossible to anticipate the impact of these factors without detailed knowledge about the circuit and its application. Each custom IC, by definition, has some unique requirement or feature associated with it. After reviewing your specific needs, particularly with regard to the circuit performance and quality requirements, Exar can provide you with a detailed proposal outlining the development costs and production pricing for your particular circuit.

WHAT ABOUT THE TESTING OF SEMI-CUSTOM IC's?

Exar will develop test software and fixtures to provide fully tested production IC's. All production devices receive 100% electrical test and screening to a mutually agreed upon device specification. In addition to the complete electrical testing, all of the production devices are screened by Exar's Quality Assurance department to assure compliance with the agreed upon Acceptable Quality Level (AQL) standards.

ECONOMICS OF SEMI-CUSTOM DESIGN

In developing either linear or digital custom circuits, one is always confronted with the following key question: for a given product type and production requirement, is it cheaper to develop a semi-custom or full custom IC? Since the functional requirements of each custom IC program vary greatly, there is no general answer to the above question. However, based on Exar's long experience in both full and semi-custom IC design and depending on the overall production requirements, it is possible to establish some sound economic guidelines for choosing the most cost effective approach.

COST FACTORS INVOLVED

Any custom IC development, whether full or semi-custom, involves similar types of cost factors. These are:

1. Non recurring engineering (NRE) or development costs.

2. Cost or unit price of the product in production quantities.

In the case of monolithic IC's, particularly those which have relatively limited production volume, the development costs may be a significant factor in the cost of the end product. Therefore, when discussing the economics of custom IC's for medium to low production quantities, it is best to consider the cost tradeoffs in terms of the amortized unit price of the IC at a given production volume. This amortized unit price is defined as the actual cost of each unit including its share of the development cost. As an example, a full custom IC may cost $50,000 to develop and may be priced at $2.90 each at a 50,000 piece total production level. Then, its true amortized unit price including development costs will be $2.90 plus $1.00, or $3.90. Similarly, an equivalent semi-custom IC may cost $5,000 to develop and be priced at $3.20 each, at the same 50,000 production level. Then, its amortized per unit price will be $3.30, or approximately 20% cheaper than a full custom.

The figure below gives a comparative graph of the amortized unit price for a typical full custom design, along with the equivalent in semi-custom form for various production quantities. For comparison purposes, the relative ratio of the amortized unit price is plotted along the vertical axis. If this ratio is greater than 1.0 then the semi-custom method is the more cost effective solution.

NO TWO IC's ARE THE SAME

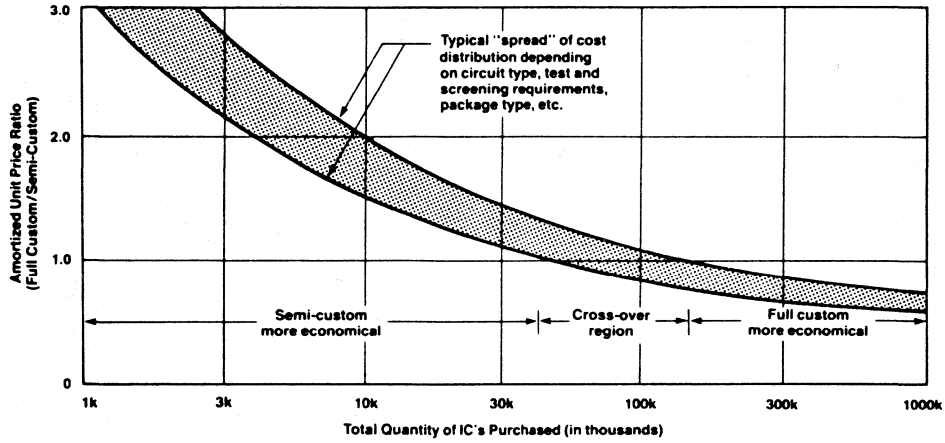
By definition, each custom IC type is unique. Therefore, the cost comparison curve given below is shown as a spread rather than a single line. This is because, in addition to the production quantity, the cost of monolithic IC's also depends on the circuit complexity, special test requirements and the IC package type.

The key information contained in the relative cost vs. quantity figure can be summarized as follows:

1. For a total production requirement of 50,000 pieces or less, the semi-custom approach is definitely the most economical.

2. For a production requirement of 200,000 pieces or more, the full custom design is more cost effective.

3. For production quantity requirements in the 50,000 to 200,000 piece range, the crossover point for the most economical approach will depend strongly on the specifics of a particular IC function; i.e., its special test, environmental screening, and package requirements.



TYPICAL COST VS QUANTITY COMPARISON OF FULL CUSTOM AND SEMI-CUSTOM DESIGNS

CONVERTING SEMI-CUSTOM TO FULL CUSTOM

Exar can offer you the combined advantages of semi-custom and full custom design programs. This is because Exar has a complete semiconductor manufacturing facilities. This unique capability allows Exar to state a custom development program using a combination of semi-custom Master-Chips during the initial phases of a customer's product, taking full advantage of the low tooling cost and short development cycle. As the product matures and its market expands (resulting in higher volume production run rates) Exar can convert the multiple semi-custom chip approach into a single custom IC, thus achieving a cost reduction and in many cases a performance improvement. The significant advantage of this type of program is that the risk associated with a custom development is greatly reduced. The IC design approach has been proven, production "bugs" are out of the product and your production line continues to flow during the full custom chip development. Once the custom chip is completely characterized and found acceptable, the semi-custom IC system in your product can be phased out while the full custom IC is being phased in.

SEMI- AND FULL CUSTOM COMBINATION: THE TWO-STEP DEVELOPMENT

In many custom development programs one is faced with very short development times and a rapid transfer into high volume production. Such a requirement does not leave room for lengthy development and design change or iteration cycles associated with conventional full custom IC design.

Exar combines full and semi-custom design capabilities, and a complete wafer fabrication facility under one roof, therefore, providing a unique solution to this problem; initially developing the prototypes in a semi-custom form, and then converting them to full custom.

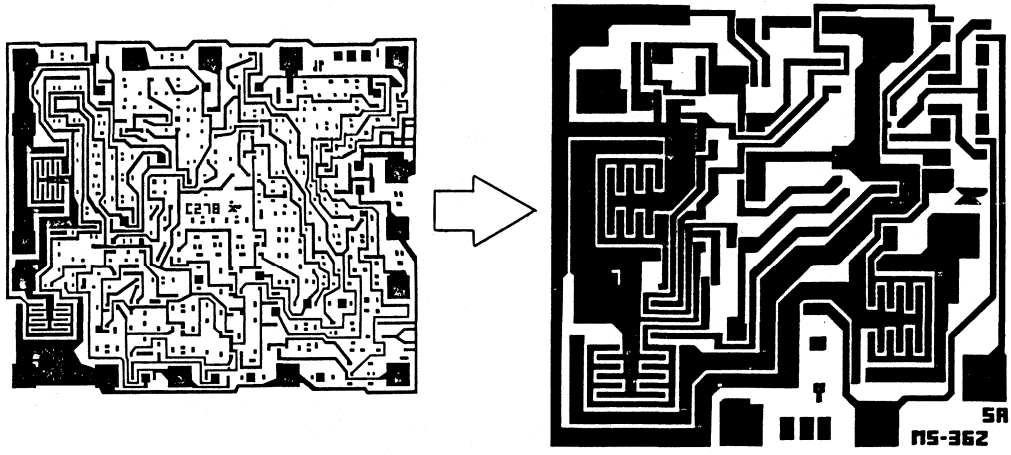
In this manner, the customer has the best of both worlds with the combination of these two technologies. The quick turnaround advantage of semi-custom Master-Chips provide prototypes and initial production units, while the subsequent full custom design provides cost savings at high volume production. During this transition, the customer is assured of a continuous flow of product through its production line.

In such a two-step development, the semi-custom prototypes often serve as a monolithic breadboard to optimize and debug the final design. This allows design iterations or changes to be made quickly and inexpensively. In fact, the only difference between the semi-custom and full custom chip is the actual size of the silicon chip.

Once the design is satisfactory, conversion of a semi-custom to a full custom chip is very straight forward and relatively risk free. We simply remove the unused electrical components from the chip to reduce the chip size and pass the resulting cost savings on to you in the form of a reduced unit price.

The two-step development capability; i.e., start as semi-custom and finish as full custom, is a very powerful design technique. It avoids the risks associated with a conventional black box type of custom design where one does not know until the very last day of development whether the circuit works or if it can be manufactured.

The two-step program is faster and less expensive than the conventional full custom development, since it avoids costly and lengthy design iteration or modification cycles for a full custom IC. In addition, it gives the customer a very high degree of assurance that the final full custom unit will work the first time.



SEMI-CUSTOM DESIGN AND ITS FULL CUSTOM EQUIVALENT

ADVANTAGES OF SEMICUSTOM DESIGN

Significant lower costs	Hybrids and discretes are quite expensive as compared to semicustom ICs. Less inventory cost also.
Higher reliability	Than hybrids and discretes. Because one semicustom IC replaces many components.
Quick turnaround	Semicustom protos are delivered in less than seven (7) weeks.
Lower development cost	Less than half the full custom cost.
Iterations	Are quick and less expensive than full custom because only one mask needs to be changed.
Reduced real estate & power	Because one IC is replacing many components. Therefore, your PC board may shrink 60-80%. Consequently, less power too.
Quick production ramp up	Need 200,000 units in less than 12 weeks? Exar can deliver using its semicustom **Master-Chip®** approach.
Product security	Semicustom IC is specifically designed for you; it is not available to your competitors as an off-the-shelf ITEM.
Reduced power, inventory cost, and production cost	Because one custom IC replaces many discrete components.

FULL CUSTOM DEVELOPMENT

Exar offers a complete design and production capability for full custom IC development. This provides an excellent complement to Exar's unique semi-custom capability. Exar's full custom IC development and production capabilities offer complete flexibility to meet changing customer needs or design problems. We can develop a complete custom IC starting from your black box specifications, or reduce your working breadboard prototype to a monolithic chip. Alternately, if you have the facilities and resources to do the IC design and layout, Exar will provide you with the device characteristics and IC layout rules for the particular process suitable to your design and review your IC layout for you. Then, Exar can generate the IC tooling and fabricate your IC prototypes.

YOUR FIRST STEP FOR FULL CUSTOM DESIGN

The following technical data package is required in order for Exar to provide you with a quotation for your full custom development program:

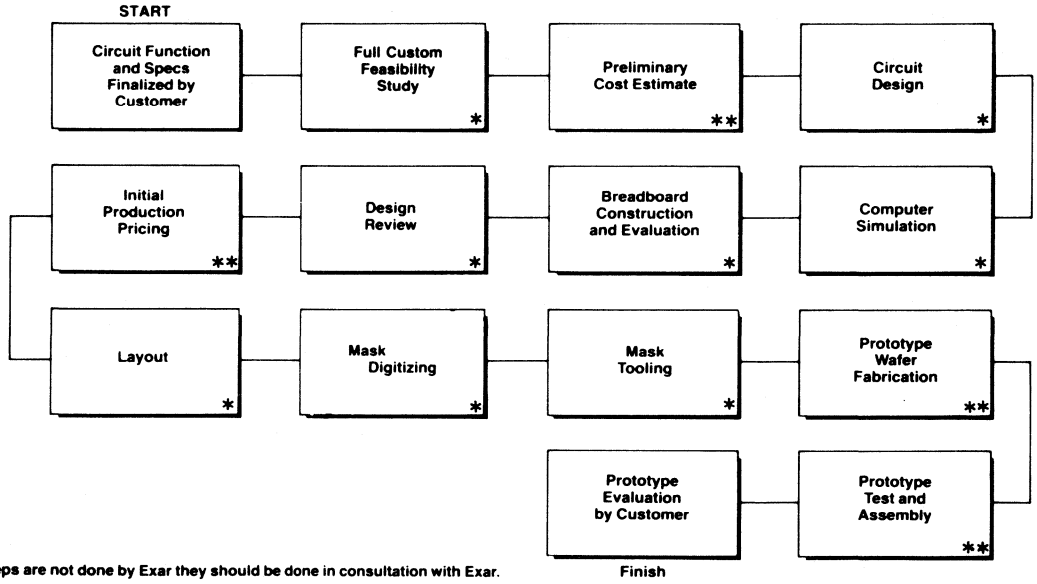
1. Circuit block diagram with subblocks.
2. Circuit schematic or logic diagram.
3. Description of circuit operation and pertinent application information.
4. Preliminary or objective device specification indicating min/max conditions and limits for the critical parameters; i.e., input/output voltage and current levels, operating frequency, timing diagrams, input/output impedances, power dissipation, etc.
5. Production requirements and the desired development timetable.
6. Packaging requirements.
7. Level of screening required.

IC FABRICATION FROM CUSTOMER'S TOOLING

Exar has a complete in-house silicon wafer fabrication and processing line at its main manufacturing plant in Sunnyvale, California. This facility currently runs 4-inch silicon wafers and is also available for manufacturing custom IC's directly from a set of customer supplied IC tooling, in coordination with Exar's Mask Design department.

If you have a set of IC tooling (masks and composite overlays) or are contemplating having one designed for you, Exar's technical staff will be glad to review it for you to assure compatibility with Exar's technology and layout tolerances. Our wafer processing technology and capabilities are compatible with the industry standards, and with the technologies of other leading IC manufacturers.

For additional information on Exar's wafer fabrication services, contact Exar directly. We pride ourselves in our flexibility and quick response to your needs.



*If these steps are not done by Exar they should be done in consultation with Exar.

**These steps must be done by Exar.

FLOW CHART OF TYPICAL FULL CUSTOM DEVELOPMENT

TESTING OF SEMI-CUSTOM IC's

All production units of semi-custom IC's are 100% electrically tested and screened to test specifications which have been mutually agreed upon between Exar and the customer, using one of Exar's several computerized test systems. In addition, Exar's Quality Assurance department performs an independent set of electrical tests on randomly selected samples of production units, prior to shipment, to assure conformity with Exar's Acceptable Quality Level (AQL) standards.

Exar provides 100% electrical testing of IC chips in wafer form, using automated wafer probe stations, and in packaged form, using automatic handlers. Exar's test facility currently has fifteen independent computer controlled test systems, with more being added as we grow. Exar's automated test system compliment is comprised of:

- Teradyne A311
- Teradyne A312
- Teradyne A360
- Sentry

Testing is one of the most critical steps in IC production. Therefore, to insure efficient and cost effective testing of production IC's, it is essential that a preliminary test plan be prepared jointly between the customer and Exar at an early stage of the custom development. This preliminary test plan will lead to the final detailed test specifications, once the development prototypes are fully evaluated and characterized and the circuit is ready to release to production.

TEST INTERFACE DEVELOPMENT

The performance and characterization data derived from careful prototype evaluation is the basis upon which test hardware and software is developed. Exar and the customer will jointly determine the performance expectations to be placed on this new IC, and once these specifications are agreed upon, Exar will proceed with test development.

Test development involves the design and construction of a test interface circuit, probe card and automatic handler hardware as well as writing the software which allows Exar's test system to perform the desired electrical tests. All these elements are then brought together under actual production conditions for evaluation and system debugging. This process can take from four to six weeks to complete, depending on the sophistication and complexity of the test plan under development. Test development begins concurrently with the start of production wafers

SPECIFICATION AGREEMENT LETTER

With each new custom IC Design Exar issues a Specification Agreement Letter. This specification states precisely the test conditions, performance levels and environmental requirements which each production IC must meet before it can leave our factory, and is the document upon which acceptability of the IC is judged. It is issued in duplicate and signed by responsible representatives form both companies prior to beginning production. One copy is retained by the customer, the other is returned to Exar.

If, for some reason, changes in the IC's specification are required, a new Specification Agreement Letter will be issued by Exar reflecting these changes. No change, however, will be put into effect until both companies have signed the new agreement. This document will then supercede all prior agreements and remain in effect until both firms, again agree, a change is required.

LINEAR SEMI-CUSTOM DESIGN CYCLE: SIX SIMPLE STEPS

The basic linear semi-custom design program involves only *6 single steps*, from the beginning of circuit design to the completion of monolithic prototypes. The first four of these steps can be done by either the customer in consultation with Exar or by Exar. The last two are performed by Exar.

	Step 1
Circuit design and breadboard using Linear Design Kit.	Customer purchases Exar's Linear IC Design Kit, made up of a comprehensive Design Manual and monolithic kit parts. The circuit is designed, breadboarded and its performance evaluated using these kit parts. The electrical characteristics of the kit parts Are virtually identical to the component which will be on the finished IC chip. Thus, this step provides a true simulation of the final IC performance.
	Step 2
Circuit layout is prepared	After the completion of breadboard evaluation, a layout of the circuit on the selected Master Chip by following the basic layout rules given in the Design Manual. The layout is done simply by interconnecting appropriate device terminals with pen or pencil lines on oversize drawings of the Master Chips supplied with the kit.
	Step 3
Layout review	Exar reviews the circuit layout and schematic to check the following: a) That basic circuit function is feasible b) No layout rules are violated c) Circuit layout accurately represents the circuit schematic. *NOTE: Exar offers consulting service and design advice during these first three steps.*
	Step 4
Exar generates custom interconnection pattern.	Using the completed Master-Chip layout sheet, Exar generates a custom interconnection pattern, or metal mask to be applied to pre-fabricated Master-Chip wafers.
	Step 5
Exar fabricates customized IC wafers.	Exar applies the custom interconnection patterns to pre-fabricated Master-Chip wafers. During this customization process, the hardware and software necessary to test the prototypes is made ready. After the wafers are customized, each die is tested by an automatic tester.
	Step 6
Exar assembles and delivers monolithic prototypes.	The customized IC wafers are scribed or cut into individual IC chips. After a visual inspection, several die that tested "good" are assembled in cerdip packages. These packaged devices are then tested again before shipment. Twenty-five assembled IC's are sent to the customer.

FULL CUSTOM DESIGNS

EXAR offers direct full custom designs to its customers. However, recognizing the risks, costs, and longer turnaround times involved in full custom development, EXAR also provides full custom conversions.

Full custom conversion is a two-step approach that provides the best of both worlds; quick turnaround time with minimum risk of semi-custom arrays, and the efficient use of silicon with full custom which invariably means reduced unit costs.

The first step is to implement customer's design on one of EXAR's **Master-Chips** to take advantage of the fast integration times as well as very easy, fast and low risk design iteration cycle in comparison to full custom. This enables customers to design and penetrate their product into the market in a short time frame and qualify the product for production rapidly. In addition, any application or production problems that may require design iterations can be implemented at a low cost and with a fast turn-around time. This way, all production oriented problems are fully debugged and the device is production proven in semi-custom form.

The second step, then, would consist of a straightforward full custom conversion to minimize the chip size and hence the unit cost when the device is in full production. This ensures a risk free and a very smooth transition to shipping cost effective, high volume products.

THREE STEPS TO SUCCESS

Get EXAR To Work For You

Step 1: Discuss Your Needs With EXAR

We are proud of our quick and flexible response to your needs. During the conception stage of your project, our highly talented Design Engineers can go through the technical options and variations available to you through EXAR. This is done at absolutely no cost to you.

Step 2: Get a Quotation From EXAR

To help us get an accurate and complete quotation to you faster, your request for quotation (RFQ) should contain:

- ☐ A block diagram of your application
- ☐ A schematic at discrete or transistor level
- ☐ The circuit specifications
- ☐ Your volume requirements

The more information you supply us, the sooner we can respond. EXAR can also assist you in compiling this information.

Step 3: Relax and Enjoy The Services Offered by EXAR

Depending on your requirements, a project may be started with EXAR at YOUR desired level of involvement. EXAR engineering having successfully completed over 1000 user specific projects (automotive, industrial control, telecom, modems, computer peripherals, medical and switch capacitor filter applications), has the necessary expertise to be involved in system design, IC design, layout or integration level. YOUR CHOICE. In either case, throughout the development process, a close contact is maintained between EXAR and your staff. NO SURPRISES.

In addition to our extensive engineering expertise in various user specific applications, as a standard IC manufacturer, EXAR brings years of accumulated engineering know-how and expertise in telecommunications, computer peripherals, data communications, including switch capacitor filters and modems, industrial control, and instrumentation to our customers. All this design expertise is available to you. Make use of our easily acessible wealth of valuable engineering resources now.

SERVICES OFFERED

Depending on the annual volume requirements of the customer and the selectivity criteria, EXAR offers a wide variety of Engineering services. These services are briefly outlined below:

1. System Design: This type of design service evolves from the conceptual system description and specification. It requires EXAR to come up with the system design using a block diagram approach. It requires definition of the functional blocks and system implementation with discrete IC blocks to verify the performance, as per the objective specs. Discrete IC implementation of each functional block and determination of the product or circuit specifications required to meet the system performance concludes the System Design.

2. Circuit Design: In this type of service, the system is well-defined by the customer in block diagrams and at the discrete IC level. EXAR determines the partitioning of the system and the definition of the product and objective specs. Then the transistor level design of the circuit is implemented to meet the IC specs. For circuit simulation, EXAR's **Master-Chip** models with SPICE programs are also available.

The circuit is breadboarded using the kit parts of the appropriate **Master-Chip**. A fully evaluated and finalized breadboard is submitted to the customer together with the evaluation results and performance characteristics for approval.

3. Design Assistance: This service is intended as a joint effort between EXAR and the customer's engineering staff. EXAR's Engineering Staff will work very closely with the customer to define the system and the objective IC specs to achieve the desired performance. EXAR's Engineering Staff will then provide the customer with a conceptual transistor level paper design of the circuit. It will be the customer's responsibility to breadboard and troubleshoot the circuit. EXAR will provide "handholding" during this stage, and assist the customer in determining the test specs and layout of the circuit (optional).

4. Layout: After the transistor level circuit schematic of the breadboard is finalized, the 200X **Master-Chip** layout sheets or Electronic Layout Sheets are used to do the interconnect. Since the interconnections of the circuit on the Master-Chip is an integral part of the design and can have a significant effect on the performance of the circuit, all critical paths and matched circuit components must be identified and taken into consideration in achieving an optimum layout. This layout sheet along with the test specification of the circuit, provided by the customer, and the pin-out (bonding diagram) form the integration package.

5. Integration: This service involves generating silicon from the layout sheet. After the Integration Package is ready, EXAR will take the layout sheet and digitize it. At this stage, EXAR will check the digitized plots versus transistor level circuit schematic. After digitization, Design Rule Check (DRC) is performed to eliminate any violations. The final digitized plots are then used to generate masks (working plates) using automated techniques.

Finally, metallization and passivation (glass or nitride) masking steps are performed on EXAR's premises to finish fabrication of the **Master-Chip** wafers. After the wafer fabrication is completed, prototypes are built at EXAR's in-house Hi-Rel assembly facility.
The prototypes are then fully evaluated and sent to the customer along with a prototype binder which includes all pertinent information. These prototypes are for electrical evaluation purposes only.

6. Wafer Foundry: In addition to all the services mentioned above, EXAR offers wafer foundry services utilizing its in-house state-of-the-art wafer fabrication line which includes all diffusion processes, epi, ion implantation, and a wide variety of deposition processes. Technologies offered cover all bipolar processes, including I^2L and high voltage.
Services are also available for partial or full processing of wafers using customer owned emulsion or chrome tooling.

MODELS AVAILABLE

For running simulations, SPICE model parameters (AC/DC) are available on bipolar (20V, 36V and 75V) and Bi-FET (36V, ion implant) processes. Contact EXAR for further information.

EXAR LINEAR MASTER-CHIPS

The following section profiles the available Exar linear Master-Chips.

INDUSTRY STANDARD (20V) ARRAYS

	A-100	B-100	C-100A	D-100	E-100	F-100	G-100	H-100	J-100	L-100	M-100
Transistors											
NPN, small	58	69	23	50	48	93	58	73	36	76	137
NPN, 100mA								2	2	2	4
NPN, 200mA	2					4	2			2	4
NPN, low noise											4
PNP, single collector	18	12	8								
PNP, dual collector				16	15	36	18	22	12	22	44
PNP, quad collector										4	8
PNP, vertical											4
Schottky Diodes	15	16	6								
15 N+ Resistors								4		8	15
Base Resistors											
200Ω	16	28	8	15	6	18	19	33	8	27	60
450Ω	43	44	18	30	41	88	68	87	34	106	188
900Ω	43	46	20	28	34	68	65	81	30	78	140
1.8KΩ	29	39	13	29	27	61	44	60	24	53	104
3.6KΩ	28	36	12	24	30	61	27	36	20	36	84
Total Base Resistance	214K	266K	94K	178K	206K	433K	266K	356K	159K	348K	712K
Pinch Resistors											
30KΩ	4	6	2		5	9					
100KΩ	4										
60KΩ				2			8	8	4	10	16
90KΩ		6									
Pads	16	16	14	16	18	24	18	18	18	24	28
Die Size (mils)	73x83	85x85	56x62	80x81	82x82	98x115	90x90	95x80	80x75	102x85	176x121

HIGH VOLTAGE (75V) ARRAY

	X-100
Transistors	
NPN, small	30
NPN, 100mA	
NPN, 200mA	4
PNP, dual collector	16
20Ω XU	1
Base Resistors	
500Ω	64
1KΩ	27
2KΩ	58
5KΩ	12
Total Base Resistance	234K
N+ Resistors	
5Ω	14
10Ω	7
20Ω	7
Pinch Resistors	
100K Ω Pinched	3
30K Ω Pinched	3
Pads	18
Die Size (mils)	115x95

BI-FET ARRAYS (36V)

	U-100	V-100	W-100
Transistors			
NPN, small	94	140	192
Supermatched small NPN's			16
NPN, 100mA	2		
NPN, 200mA		4	4
J-FET (P-channel)	4	4	8
PNP, dual collector	40	56	60
PNP, (med. vertical)	2	4	4
PNP, vertical	8	4	10
Base Resistors			
280Ω	40	40	24
450Ω	158	112	100
900Ω	56	72	100
1.8KΩ	32	64	88
3.6KΩ	32	56	72
Total Base Resistance	305K	443K	559K
Implant Resistors			
1KΩ			32
5KΩ	16	32	32
10KΩ	16	32	32
20KΩ	16	32	32
50KΩ	16	32	28
Total Implant Resistance	1.36M	2.72M	2.55M
Cross Unders			
15Ω XU	9	4	
5Ω XU		8	
30Ω LVXU (5V max)		8	
15Ω LVXU	4	4	
Capacitors			
MOS capacitors (10pF max)	4	4	8
Pads	28	28	40
Die Size (mils)	110x110	146x113	163x133

NOTE: LV—low voltage (5V max. to substrate). XU—N+ cross under

KIT PARTS

Please Note: Large NPN ≡ 200 ma
Medium NPN ≡ 100 ma
Small NPN ≡ 10 ma
* Absolute maximum ratings

Item	Kit Part No.	Description	Max Voltage	Applicable for Master-Chip
1.	XR-A103	Two 200 ma, & 3 Schottky transistors	20V	A-100, B-100, C-100
2.	XR-B101	5 small NPNs	20V	A-100, B-100, C-100
3.	XR-B202	5 lateral PNPs single collector	20V	A-100, B-100, C-100
4.	XR-F101	5 small NPNs	20V	
5.	XR-F108	Four 200 ma NPNs	20V	
6.	XR-F206	4 lateral PNPs dual collector	20V	All of these kit parts are useable for breadboarding the following Chips: E-100, F-100, G-100, H-100, J-100, L-100, and M-100.
7.	XR-J114	7 small NPNs – common base	20V	
8.	XR-J117	3 Wilson current sources NPNs	20V	
9.	XR-J215	7 PNPs common base	20V	
10.	XR-J216	3 Wilson current source PNPs	20V	
11.	XR-M111	4 small NPNs	20V	
12.	XR-M112	2 medium NPNs, 2 large vertical PNPs, 1 small NPN	20V	
13.	XR-M210	2 quad collector PNPs	20V	
14.	XR-D101	5 small NPNs	36V	D-100
15.	XR-D206	4 lateral PNPs dual collector	36V	D-100
16.	XR-W101	5 small NPNs	36V	U-100, V-100, W-100
17.	XR-W108	Four 200 ma NPNs	36V	U-100, V-100, W-100
18.	XR-W111	4 small NPNs	36V	U-100, V-100, W-100
19.	XR-W206	4 lateral PNPs dual collector	36V	U-100, V-100, W-100
20.	XR-W213	5 small, 2 large vertical PNPs	36V	U-100, V-100, W-100
21.	XR-W421	4 P channel, JFets	36V	U-100, V-100, W-100
22.	XR-CA111	4 small NPNs	20V	CA-100
23.	XR-CA118	2 large NPNs 2 large PNPs	20V	CA-100
24.	XR-CA206	4 dual collector PNPs	20V	CA-100
25.	XR-CA101	5 small NPNs	20V	CA-100
26.	XR-RN1	Resistor network		Applicable to all Master-Chips except U, V, and W100
27.	XR-RN2	Resistor network		Applicable to all Master-Chips except U, V, and W100
28.	XR-X101	5 small NPNs	75V	X-100
29.	XR-X108	Four 200 ma NPNs	75V	X-100
30.	XR-X206	4 lateral PNPs dual collector	75V	X-100

FLEXAR™
Programmable Linear Bipolar Arrays

The BETA Series

FLEXAR™

THE FLEXIBLE LINEAR BIPOLAR ARRAYS

EXAR adds a new dimension to its wide variety of linear arrays, NEVER BEFORE AVAILABLE in semi-custom design. EXAR introduces "FLEXAR,™" the Programmable Linear Array. For the first time a designer can select either a NPN or PNP transistor from a specific location by using only a single layer of metal. This means that a circuit can be laid out for the total number of transistors without regard to polarity. For example, if the chip has space for 100 transistors, the designer could use 100 PNP's or 100 NPN's or any combination of NPN's and PNP's. In addition, unused bonding pads may be converted to active or passive components giving greater than 100 percent utilization and a chip size and cost approaching full custom.

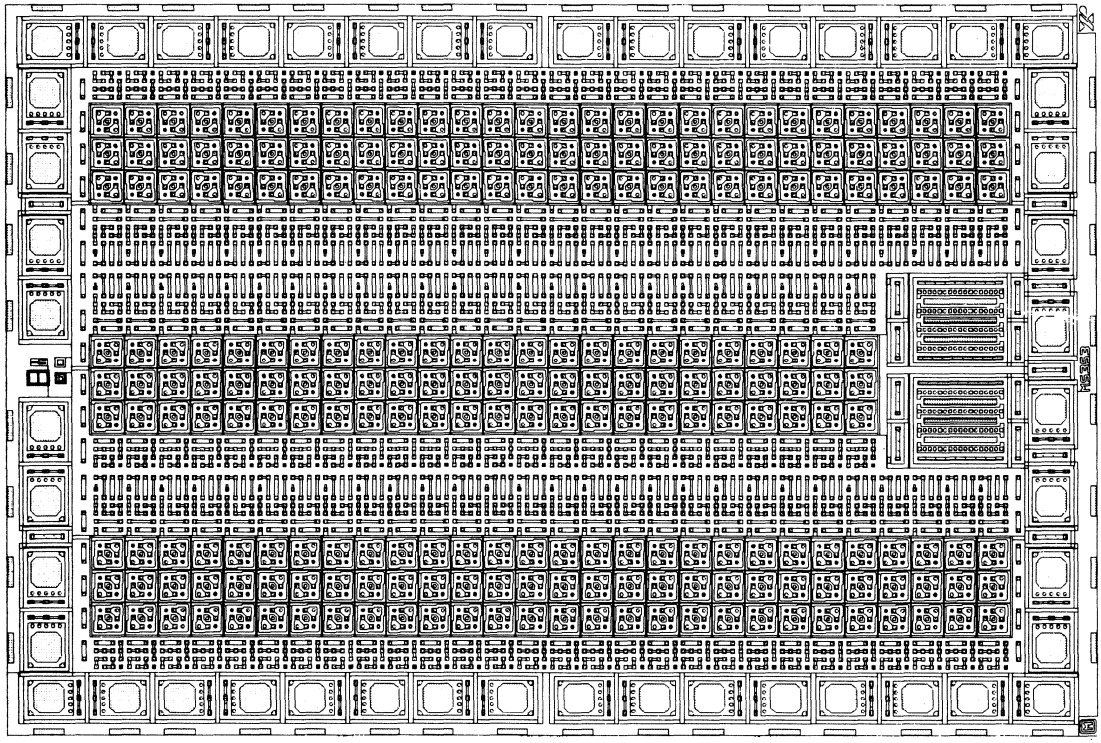


Figure 1. The BETA 240 Array, Topography and Component Count

The FLEXAR™ topology is perfectly suitable for mixed technology designs. Now you can truly design both linear and digital circuitry on the same chip—another first in the industry.

EXAR is developing an extensive "SOFT MACRO Library of already proven circuits. Designing form this library will greatly simplify the schematic capture tasks and minimize the time required to get from working schematic to the final IC.

Any user designed function can also be made into a circuit building block and, like EXAR soft macro library, can be transferred to various locations on the chip or to other chips in the FLEXAR family.

The new FLEXAR™ family is designed with the same layout architecture. All applications are covered with only three different arrays.

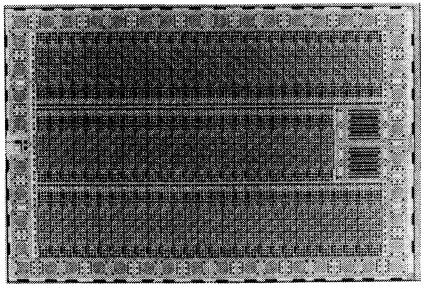
Four types of "Kit Parts" are required to breadboard your circuit. These are the TWINSTOR (NPN, PNP), PADSTOR, and TWINBOOSTOR (patent applied for).

FLEXAR™ BETA ARRAY TOPOLOGY

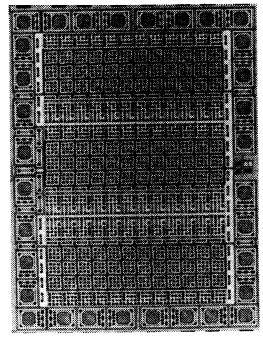
The V+ metal is preassigned to run perpendicular to the 1.5K ohm resistors. A wide substrate metal (most negative supply) around the perimeter of the die is easily accessible to every CELL regardless of location. Within each CELL, a low current direct V+ tap is provided in resistor Array A and a low current V− tap in resistor Array B.

In case of multiple supplies, the designer should pay careful attention to biasing of the four independent resistor tubs. To avoid latch-up during power on of the power supplies, it is recommended to keep resistors to each supply in a separate tub or bias all the tubs to the highest V_{CC} you are using.

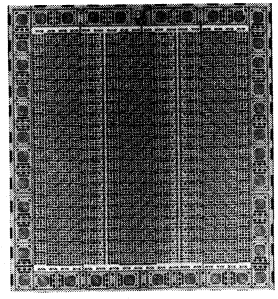
Every bonding pad, being a multifunction PADSTOR, is located at the perimeter of the die. The grid format is set at a constant pitch, designed especially for compatibility of EXAR's routing software. This reduces the digitizing time and shortens the overall mask design time.



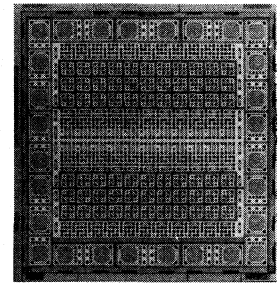
Beta 240 Array



Beta 100 Array



Beta 180 Array



Beta 66 Array

Figure 2

FLEXAR™ BETA ARRAY CELL ARCHITECTURE

The architecture of the FLEXAR™ Beta array is built around a flexible CELL which is repeated throughout the array and on the other arrays of the family (see figure 6). /this enables a circuit to be duplicated anywhere within an array or transferred from one array to another with unchanged characteristics. The designer's tack becomes greatly simplified for the same layout may be placed in any location and on any array in the family, giving a major reduction in design cycle. This is far superior to the typical semi-custom IC which does not have this cell structure. Before the introduction of FLEXAR™, a new layout would have been required if the same circuit was to be transferred from one array to another or even to a different location on the same array.

Each cell contains three TWINSTORS flanked by two resistor arrays as shown in figure 3. The resistor arrays are part of the four independent resistor islands (see figure 1) Resistor Array A, in figure 3 on the left, contains 3K ohms base resistance, 10K ohms implant resistance, a 40 ohms P-type crossunder and a low current bias contact to V+ (the most positive supply) Resistor Array B, in figure 3 on the right, contains 5.5K ohms base resistance, 35K ohms implant resistance, two P-type crossunders (40 and 45 ohm), an independent bias contact, a low current substrate and a wide preassigned V+ track running perpendicular to the 1.5K ohm resistors. Interconnections between CELLS become simple and make the layout compact and efficient.

When the TWINSTORS are not used as active elements, each TWINSTOR may be used either as a 90 ohm crossunder or as a 500 ohm matched resistance pair conveniently close to the active elements.

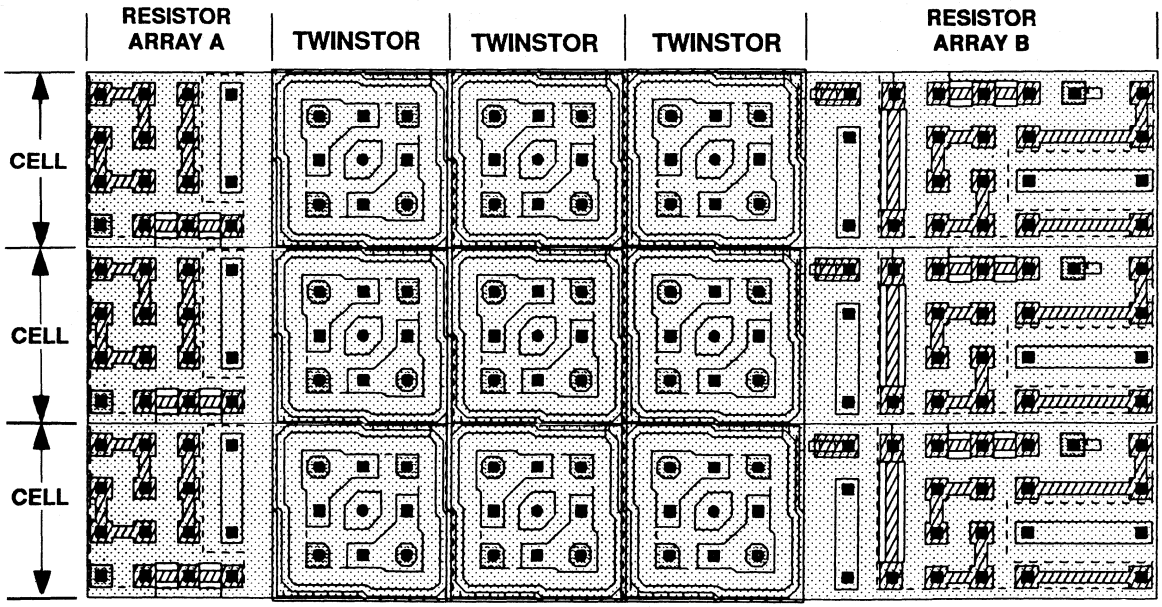


Figure 3.

FLEXAR™BETA ARRAYS

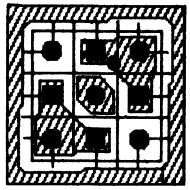
	COMPONENT COUNT			
	BETA-240	BETA-180	BETA-100	BETA-66
CELLS	80	60	33	22
TWINSTOR NPR OR PNP	240	180	99	66
PADSTOR OR PADSTOR AS				
NPN	48	42	34	28
PNP	48	42	34	28
Resistor	48	42	34	28
Capacitor	48	42	34	28
Bonding Pad	48	42	34	28
Twinbooster NPN PR PNP	2	0	0	0
Base Resistors				
500 ohm	880	660	363	242
1.5K ohm	160	120	66	44
Total Base Resistance	680KΩ	510KΩ	280KΩ	190KΩ
Ion Implant Resistors				
5K ohm	320	240	132	88
25K ohm	80	60	33	22
Total Implant Resistance	3.6MΩ	2.7MΩ	1.5MΩ	1MΩ
P+ Crossunder Resistors				
(XU1) 500 ohm	480	360	216	132
(XU4) 45 ohm	86	66	39	26
(XU3) 40 ohm	184	150	96	64
(XU5) 20 ohm (PADSTOR)	48	42	34	28
N+ Crossunder Resistors				
(XU7) 90 ohm	240	180	99	66
(XU2) 20 ohm (PADSTOR)	96	84	68	44
(XU6) 15 ohm	15	4	0	0
DIE DIMENSION	110x160 mils	110x121 mils	110x78 mils	78x82 mils

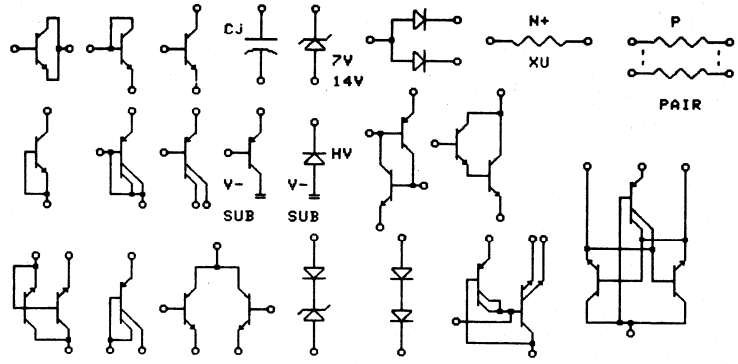
FLEXAR™BETA ARRAY COMPONENTS

Three multifunction components (TWINSTOR, PADSTOR, and TWINBOOSTER) in FLEXAR™ Beta array family of linear/digital arrays and the continuity of the topology of the FLEXAR™ series are unique to the industry. For the first time, each component can be programmed to serve as one of many active or passive functions. The designer defines the desired function by proper connections with the single metal layer.

TWINSTOR - MULTIFUNCTION AND MULTIPURPOSE

The TWINSTOR is the star of the family. Its versatility comes from its composite structure: a dual collector PNP (common base) merged with a two common collector NPN. With the 9 available contacts, you have a choice of over 20 active or passive functions from a single TWINSTOR.

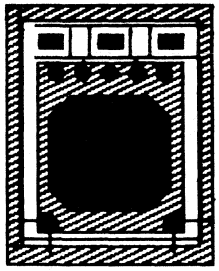


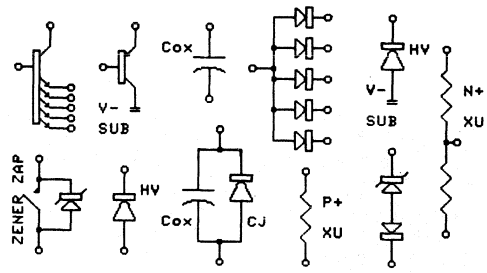


TWINSTOR AS NPN (2X)	Min	Typical	Max	Units
Breakdown voltage BVCEO, I_C = 1 mA	26	35		Volts
Current gain, I_C = 1 mA, 5V	80	180	360	
Current gain, I_C = 15 mA, 5V	30	60		
Saturation resistance (two collectors)		50	100	Ohms
Collector Current			15	mA
f_T NPN at I_C = 3 mA, 5V		500MHz		
TWINSTOR AS PNP				
Breakdown voltage, I_C = 0.1 mA	26	45		Volts
Current gain, I_C = 10 µA, 5V	50	140	300	
Current gain, I_C = 1 mA, 5V	10	20		
Saturation resistance		200	300	Ohms
Collector Current			3	mA
f_T PNP at I_C = 100 µA, 5V		5 MHz		
TWINSTOR AS RESISTOR				
Resistance	400	500	650	Ohms

PADSTOR - A BUSY BONDING PAD

With the bonding pad merged with a five emitter NPN and a large vertical substrate PNP, the PADSTOR complements the TWINSTOR. Not only can it drive loads as NPN or PNP, but it can stabilize your design by acting as a large compensation capacitor (both MOS and junction). It can also trim design parameters as a zener zap, provide pad protection as a high voltage and a high current clamping diode and even serve as a dual series resistor network for sink/source output stages.

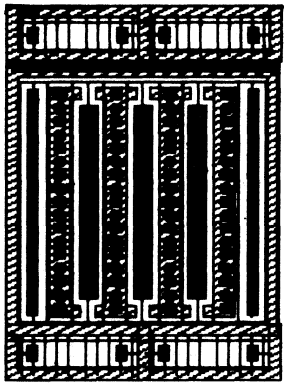


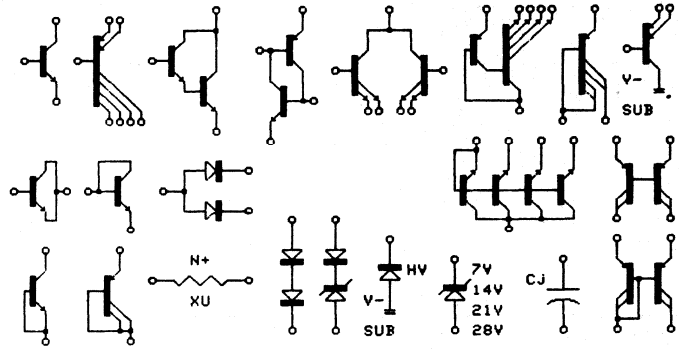


PADSTOR AS NPN	Min	Typical	Max	Units
Breakdown voltage BVCEO, I_C = 1 mA	26	40		Volts
Current gain, I_C = 5 mA, 5V	80	250		
Current gain, I_C = 50 mA, 5V	30	60		
Saturation resistance at 50 mA		20		Ohms
Collector Current			50	mA
PADSTOR AS PNP				
Breakdown voltage BVCEO, I_C = 1 mA	26	70		Volts
Current gain, I_C = 1 mA, 3V	200	400	550	
Collector Current			25	mA
PADSTOR AS CAPACITOR				
Junction capacitor, Vj = ov		3.8		pF
Oxide/Nitride capacitor, tox. = 0.22 μ		2.5		pF
PADSTOR AS N+ RESISTOR (2 in series)				
Resistor value (each)		20		Ohms
PADSTOR AS P+ RESISTOR				
Resistance		20		Ohms
PADSTOR AS BONDING PAD	—	—		

THE TWINBOOSTER - "THE SLEDGEHAMMER"

The TWINBOOSTOR has a 32 emitter NPN merged with a four collector and a three large emitter lateral PNP. It can handle up to 500 mA loads as a NPN and 25 mA loads as a PNP.

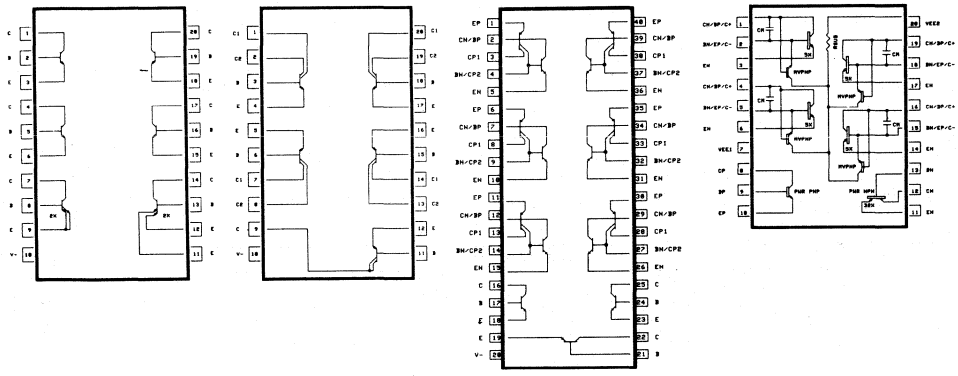




TWINBOOSTOR AS NPN	Min	Typical	Max	Units
Breakdown voltage BVCEO, I_C = 10 mA	26	35		Volts
Current gain, I_C = 20 mA, 3V	80	250	430	
Current gain, I_C = 30 mA, 5V	80	200		
Saturation resistance		4		Ohms
Collector Current			500	mA
TWINBOOSTOR AS PNP				
Breakdown voltage BVCEO, I_C = 1 mA	26	55		Volts
Current gain, I_C = 500 µA, 3V	35	45		
Current gain, I_C = 10 mA, 5V	5	15		
Saturation resistance		25		Ohms
Collector Current			25	mA

FLEXAR™ BETA ARRAY KIT PARTS

The simplicity and ease of designing with FLEXAR™ BETA-arrays is demonstrated by the fact that only four different types of KIT PARTS are required to breadboard and check your design.



FLA-101
6 TWINSTORS Programmed as NPNs

FLA-102
5 TWINSTORS Programmed as PNPs

FLA-103
6 TWINSTORS—Programmable
3 TWINSTORS—Programmed as NPNs

FLA-104A
4 PADSTORS—Programmable
1 TWINBOOSTOR—Programmed as Power PNP
1 TWINBOOSTOR—Programmed as Power NPN

7

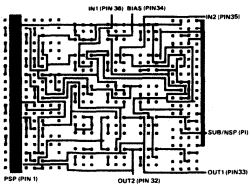
DESIGNING WITH SOFT MACROS

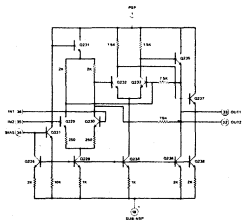
A Softmacro is a predesigned, fully characterized circuit that is ready to be implemented on any of the FLEXAR™ BETA-arrays. The Softmacro approach makes IC design simple. An engineer who is unfamiliar with IC design can, for the first time, reduce a working circuit to an IC just by following these simple steps:

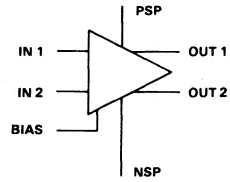
1. Draw a block diagram of the system.
2. Choose the appropriate Softmacro(s) for each block, using the extensive library of Softmacros provided by EXAR.
3. Connect the Softmacro(s), forming the desired circuit.
4. Simulate the circuit, on your computer or on EXAR's.
5. Lay out the circuit, or let EXAR do the layout for you.
6. EXAR—always ready to support you—will pick up the project at any stage, including at your building block concept.
7. EXAR will provide functionally tested prototypes ⟶ ***FAST!***

TYPICAL SOFT MACRO

BTA-AMP-01 is a wideband, differential input-output amplifier. It is similar to the industry standard 733 except that the gain is fixed. The optional circuit bias permits additional versatility. This circuit is capable of operating from either a single or a split power supply.







BTA—AMP—01

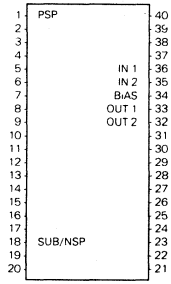
FEATURES		MAXIMUM RATINGS	
GAIN	20dB	PSP-NSP	26V
BANDWIDTH	UP TO 30MHz	V IN (DIFF)	7V
SLEW RATE	160V/μS	I OUT	10mA

Partial list of Soft Macro Library.

Low Level Full-wave Rectifier
Full-wave Rectifier with Ground Reference
Inductive Coupled Rectifier
Precision Full-wave Rectifier
Single-ended Full-wave Rectifier
Simple Rectifier
Transconductance Amplifier
Low Voltage Output Amplifier

Current Source With Low TC
Voltage to Current Converter
Voltage to Current Pump
Current Source With Multiple Outputs
Ground Sensing V-I Converter
High Accuracy Current Source
Differential-voltage Controlled Current Generator
Low Voltage Bandgap Referenced Current Source

Frequency Divider
D Latch
AND Gate
Exclusive OR Gate
NOR Gate
Phase Detector
Peak Detector
Zero Crossing Detector
Sample-and-Hold



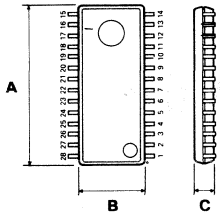
FLEXAR™ BETA ARRAY SUPPORT

User-support for FLEXAR™ BETA-arrays is available on IBM PC/AT personal computers. With the FLEXAR Integrated Development System (FIDS) your PC/AT can be equipped with a schematic entry system, circuit simulation and layout software. This allows you to design a circuit, capture the schematic, check the circuit simulation, make modifications if necessary, and resimulate as often as desired. When the circuit has been sufficiently verified, a net list can be printed out. EXAR will pick up the development at any stage, and fabricate your design into an integrated circuit. You can maintain full control of your system—and complete privacy—when you perform the entire design at your facility. Of course, EXAR engineering and applications personnel are always available for technical support.

By special arrangement schematic capture may be performed at EXAR. Our VAX-8600 computer may be accessed using your video display terminal and modem. Remote controlled SPICE runs could then be used to confirm your initial design data. EXAR will do the rest.

PACKAGING

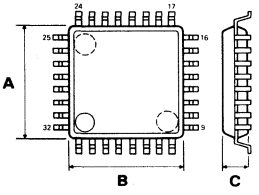
EXAR provides all standard dual-in-line packages in plastic, cerdip, and side braze. The list below describes some of the surface mount packages available. Contact EXAR for a complete discussion of your package requirements.



SMALL OUTLINE (SO) PACKAGES (50 mil spacings) (plastic)

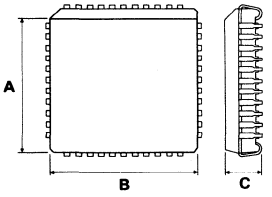
No of Pins	.Size (inches) A/B/C	Theta- Free Air C/W	Theta-* Substrate C/W	Availability B66	B100	B180	B240
16	.394/.173/.059	200	100	*	*		
18	.441/.212/.070	180	100	*	*		
20	.492/212/.070	180	100	*	*		
22	.539/.212/.070	180	100	*	*	*	*
24	.590/.212/.070	180	100	*	*	*	*
28	.728/.295/.086	165	90	*	*	*	*
40	1.039/.370/.102	140	80		*	*	*

*Considering their size, the SO packages exhibit excellent power dissipation. In addition to being measured in free air, the power dissipation is measured when mounted on a ceramic substrate. These figures are for comparison only to demonstrate the greater power dissipation when properly mounted to your printed circuit board.



QUAD FLAT PACKAGES (plastic)

No of Pins	Size (inches) A/B/C	Theta - C/W	Availability B100	B180	B240
32	.275/.275/.057	250	*	*	*
44	.394/.394/.085	250	*	*	*



CHIP CARRIER (PLCC) (plastic)

No of Pins	Size (inches) A/B/C	Theta- C/W	Availability B66	B100	B180	B240
28	.420/.420/.145	100	*	*	*	*
44	.850/.620/.170	80		*	*	*

7

FLEXAR ™
Programmable Linear Bipolar Arrays
The DELTA Series

- High Speed Process
- Programable Components
- Programmable DIE-SIZE

DELTA ARRAYS: The DELTA series has two arrays, for different component counts. The DELTA 2000 has two cells per row, the DELTA 4000, four per row. BV_{CEO} is greater than 18V.

TYPICAL COMPONENT COUNTS:
(For 12 and 22 horizontal rows)

	DELTA 2000-12	DELTA 4000-122
Twinstors	80	320
NPN	44	168
NPN Common Collector	88	336
NPN 50 mA	44	84
Padstor, (Bond. Pad/PNP/NPN/Cap.	22	42
Total Transistors	228	1010
Schottky diode	24	44
Resistor 1kOhm	528	2016
Resistor 2kOhm	66	126
Resistor 5kOhm	176	672
Resistor 30k Ohm	22	42
Total Resistors	1144	4200
Cross-under	44	84
Total Components	1500	5338
DIE DIMENSION	66 x 102 mils	107 x 187 mils

Given a maximum length of three times the height, and a minimum dimension of 25 mils, maximum transistor counts would be as follows:

	DELTA 2000	DELTA 4000
Rows	3 to 21	6 to 36
Transistors	45 to 531	226 to 1696
DIE DIMENSION	26 X 66 to 66 x 179 mils	51 x 107 to 107 x 306 mils

The size of the IC is user programmable. The horizontal dimension is defined by the number of cells used in the core of the layout. The chip is completed by placing the vertical pads and scribe line. (see the example below)

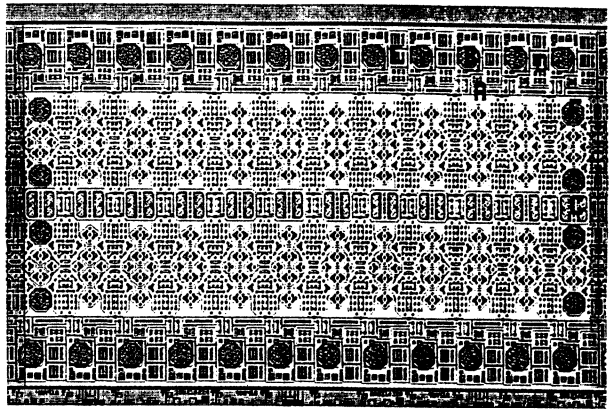
Silicon efficiency is nearly three times greater than previous arrays. That translates to a unit cost that approaches that of full custom.

The NPN configured TWINSTOR has an Ft of 1 Ghz and a current handling capacilty of 10 mA. With the TWINSTOR configured as a lateral PNP, the Ft is greater than 10 Mhz. Each PADSTOR contains a 100 mA NPN as well high current vertical PNP and low noise NPN capability. A sinker diffusion is used to improve V_{SAT} of the NPN of each twinstor and padstor.

Well matched diffused and implant resistors are available throughout the array in addition to programmable capacitors up to 6pF, small signal surface barrier diodes, and pad capacitors.

The TWINSTOR groupings called "cells" are symmetrical and identical to all other cells. This permits the creation and use of a true library of function blocks and maximizes device flexibility.

Only one metal mask and passivation step are required to complete the IC. This means that prototype samples may be produced in weeks as opposed to months.



DELTA 2000-12 ARRAY

FLEXAR DELTA ARRAY

A. Twinstor
B. Padstor, Fixed Pad
C. Thin Film Resistors/ Programmable Capacitors
D. Schottky Diodes
E. Power NPNs
F. User Programmable Pad

Note: This Delta 2000 Array is stacked two cells high.

DELTA STRATEGY:

EXAR's aim is to replace the full custom methodology with the use of DELTA. For large volume applications DELTA is an ideal solution and the unit cost is within 5 to 10 percent of an IC developed using a full custom approach. Development of circuits using DELTA will be completed months earlier than full custom development programs and typical NRE charges will be significantly less.

As DELTA is the modern alrernative to full custom development, it will be used primarily to focus onlarge volume applications such as automotive, computer peripheral, and consumer devices. Availability to the general market will be announced and support at that time will include PC/AT based design tools similar to those in use with the FLEXAR BETA sereis. Thses will include schematic capture, circuit simulation, and IC layout software.

DESIGN CENTERS:

EXAR Customer Design Center:

EXAR's newly established Customer Design Center in San Jose is staffed and equipped to help you familiarize yourself with the PC based tools for FLEXAR IC design. Customers and independent design consultants can opt to purchase this system, and training on the use of the system is provided here at no additional charge. Many have come with actual design projects in-hand, thus making the training session a time efficient design session as well. The Custom Design Center is also available to provide design and software applicaiton assistance for the FLEXAR arrays. By special arrangement, large circuits may be analyzed by linking the design to EXAR's VAX main-frame computer.

With completed designs and layouts, the Customer Design Center can provide a hardware interface to the integration phase of your project. Your layout is converted to GDSII standard data which is subsequently used to make the metal mask for your IC.

Independent Design Centers:

In addition to the EXAR Customer Design Center, we have a host of qualified independent Design Centers throughout the world. For additional information on the Design Centers. Please contact factory directly.

Full Custom Designs:

EXAR offers direct, full custom design service to irs customers. However, recongizing the risks, costs, and turnaround times involved, EXAR also provides full custom CONVERSIONS.

Full custom conversion is a two-step approach that provides the best of both worlds: the quick turnaround time and minimum risk of semicustom, and the efficient silicon utilization of full custom (which, invariably, means reduced unit cost).

The first step is to implemnt the design on a FLEXAR™ BETA-array, to take advantage of the fast integration time, as well as the very fast, easy and low-risk design iteration cycle. This enables you to complete your design and achieve market penetration in a short-time frame, and to qualify your products for volume production rapidly. In addition, any application or production problems, which may require design iterations, can be implemented at low cost and with fast turnaround. All production-related problems are fully debugged and the device is production-proven in semicustom form.

For high volume production, the unused portion of the chip can be removed and the pads relocated. This requires only a few hours in mask design and can result in a chip size only 20 to 25 percent larger than a full hand crafted design. You retain the benefits of semicustom because of the minimum change to your original circuit. Since the package remains the same, the final cost approaches that of full custom.

EXAR also provides full custom conversion, wicll give you the smallest size and lowest cost possible. These two high volume choices offer the ultimate in smooth and risk free transition to cost effective, high volume products.

FLEXAR INTEGRATED DESIGN SYSTEM

Get Acquainted with FIDS

The FLEXAR Integrated Design System (FIDS) is the industry-first, fully-integrated CAD/CAE tool. FIDS converts 386-based personal computers into complete analog IC workstations for FLEXAR Beta-arrays.

- User-friendly FIDS Executive Shell interfaces with all resources
- Schematic entry (OrCAD/SDT III™ V3.2, OrCAD Systems Corporation)
- Simulation(PSpice™V4.0, MicroSim Corporation)
- Graphic layout editing (EXAR-proprietary SW)
- Design-Rule-Check (DRC)
- Electrical-Rule-Check (ERC)
- Layout-Versus-Schematic checking (LVS)
- Pattern Generation (PG) output in David Mann 3000 format

Get a Growing Library of Softmacros

Schematics and layouts for 65 building block circuits: industry standards, special designs, are being developed. Layouts are easily ported across all four Beta-arrays.

Use a Popular Low Cost PC Design Platform

Minimum hardware requirements:

- PC/386 with DOS 3.0
- 387 Match co-processor
- 4Mbyte RAM
- EGA color capability
- 1.2Mbyte 5.25" floppy drive
- 20Mbyte hard drive
- 1 serial port (COM1)
- 1 parallel port
- Mouse Systems™ Mouse (MSC Technologies Inc.)

Optional additions:

- 2nd serial port (COM2)
- HPGL plotter
- dot matrix printer

Documentation and Training

FIDS comes with a comprehensive users manual and free registration for two participants in our 3-day training class. Classes are offered quarterly. Additional registrations are available at a cost of $1000.

Dedicated Follow Up

Exar issues software upgrades and additions to the Softmacro library, quarterly, as they are developed. Nominal cost per release.

Hotline Support

A 24-hour answering service has been established for FIDS users. Call our west coast headquarters at 408-434-6400, ext. 3650. Inquires acknowledged promptly in your timezone, anywhere in the world.

Packaging Options

Choose one of four packages, according to whether the site has OrCAD, PSpice, both or neither. Manuals can be ordered separately.

EXAR ...the analog plus™ company

XR-N2000 Standard Cells

The N2000 series of standard cells from EXAR Corporation is manufactured using an advanced 1.5 micron, double poly, double metal, CMOS process. This is process is unmatched in its versatility and perfromance, providing the user with fast digital switching, precise analog functions, and dense memory, including EEPROM. This access to highly integrated, digital and analog solutions assures the associated system advantages that VLSI provides. The N2000 standard cell library offers high noise immunity and very low power consumption typical of CMOS technology. All inputs and outputs may be selected to be compatible with either TTL or BICMOS logic levels or any analog signal from 0 to 50 Volts. The small geometries allow over 150 I/O signals and integration complexities up to 10,000 equivalent gates.

The digital portion of the Standard Cell library consists of cell primitives, Macro-cells and Mega-cells, implementing functions ranging from simple NAND gates to high speed multipliers. The 1.5 micron drawn feature size permits very fast clock rates and very high levels of integration.

XR-N2000 analog cells reflect EXAR's extensive experience in linear semi-custom design. These cells allow the merging of digital processing with the analog world of motors, sensors and communications. Basic analog functions available include op-amps, comparators, voltage references, and oscillators. In addition, the library includes high level analog functions, such as A/D and D/A converters, phase-locked loops, and switched capacitor filters. Of course, all these cells take full advantage of the capabilities offered by EXAR's advanced analog BICMOS process.

FEATURES	
1.5 micron BICMOS	
3 to 17 Volt supply voltages	
Over 150 input/output pads	
Fast generation of user specific cells	• Digital silicon compilation • Analog custom product experience • Memory standard products up to 256K
Extensive 125 cell digital library	• Toggle frequencies to 75 MHz • Clock frequencies to 50 MHz
Expanding 20 cell EEPROM	• 1.0 nS typical 2 input NAND delay • Output drivers to 48 mA • Up to 10,000 equivalent gates
Comprehensive 50 cell analog library	• Op amps, comparators, oscillators • A/D, D/A switched capacitor filters, phase lock loops, voltage references
Reconfigurable memory macros	• EEPROM, RAM, ROM

MAXIMUM RATINGS	
Storage Temperature	-65 to+ 150°C
Operating Temperature	-55 to +125°C
Supply Voltage, VDD	+3.0V to +17V
Voltage on any pin	VSS -.3V to VDD +.3V
ESD	3000V at 100pF thru 1.5k Ohms

DC OPERATING CHARACTERISTICS

VDD = 5.0V ±10%, Temperature = −55 to +125°C

Parameter	Condition	Limit	Value	Unit
IOH, Output High Current	VOH = 2.4V	MIN	4.0	mA
IOL, Output Low Current	VOL = 0.40	MIN	4.0	mA
VIH, Input High Voltage	TTL Input	MIN	2.0	V
	Digital Input	MIN	3.5	V
VIL, Input Low Voltage	TTL Input	MAX	0.8	V
	Digital Input	MAX	1.5	V
IIN, Input Current	Digital	MAX	±0.1	µA
IDD, Supply Current	Active/Cell/MHz	TYP	1.5	µA
	Quiescent/Chip	TYP	±1.0	µA
Capacitance				
Chip input	DIP Package	TYP	4.0	pF
Chip output	DIP Package	TYP	6.0	pF
Cell input		TYP	0.1	pF

AC OPERATING CHARACTERISTICS DIGITAL CELLS

VDD = 5.0V, Temperature = 25°C, 2µ Transistor Lengths

Parameter	Condition	Limit	Value	Unit
Propagation Time				
Inverter	0.5 pF Load	MAX	0.8	ns
2-input NAND	0.5 pF Load	MAX	1.0	ns
2-input NOR	0.5 pF Load	MAX	1.3	ns
Output Buffer	15 pF Load	MAX	3.7	ns
Frequency				
Flip Flop Toggle		MIN	100	MHz
Oscillator		MIN	50	MHz

AC OPERATING CHARACTERISTICS MEMORY CELLS

VDD = 5.0V, Temperature = 25°C

Parameter	Condition	Limit	Value	Unit
Access Time				
256 x 8 EEPROM		MAX	100	nS
256 x 8 RAM		MAX	80	nS
256 x 8 ROM		MAX	60	nS

AC OPERATING CHARACTERISTICS ANALOG CELLS

VDD = 10.0V, Temperature = 25°C

Parameter	Condition	Limit	Value	Unit
Opamp				
Gain Bandwidth		MIN	3.5	MHz
PSRR	1 KHz	MIN	80	dB
A/D Converter	8 Bits			
Resolution		MAX	½	LSB
Conversion Time		MAX	100	µS
D/A Converter	8 Bits			
Resolution		MAX	½	LSB
Settling Time		MAX	10	µS

Cell Name	Cell Description
Analog:	
DAC7A	7-bit bipolar DAC
VREFHALF	Volt generate VDD/2
INPAW	Wide pad only (no IP)
VOLTSEL	Voltage regulator macro w/ power down
OP3	Low power op amp
BGP1V2LV	1.2V band gap VREF, LV
BIAS2LV	Med current bias, LV
CMP2LV	Near Vss CMR comparator, LV
IREFW	Current ref bias gen wide pad
CMP1	High resolution comparator
OPC	Low offset op amp
BIAS	Bias circuit for CMP1 and OPC
CGEN	Clock generator of CMP1
CMP3	50 mV dual hysteresis comparator (high vltg)
CMP3	A10 mV dual hysteresis comparator (high vltg)
CMP4	100 mV single hysteresis comp. (high vltg)
COMPHV	1 mV high voltage comparator
BGPHV	2.46V bandgap voltage reference
OP4	15V supply internal op amp
BIAS3HV	15V supply bias generator
OPB4	15V supply, high gain op amp buffer
VCO	10-50 MHzmid frequency, +40% tune
ZEROP	Zero phase VCO restart
ATOD8SLV	8 bit A to D, mask programmable bias/speed
OPBDU1HV	Less than 5mV offset buffered op amp
BIASDU1H	Dual bias
CMP13PHV	Less than 1mV offset comparator
ASW100X	General Purpose analog switch
BGP1V2X	Generates 1.23 Volt reference voltage
BGPD1V2X	Generates 1.25 Volt reference voltage
BGPD2V5X	Generates 2.50 Volt reference voltage
BIAS2X	Bias network providing medium bias current
BIAS3X	Bias newwork providing high bias current
CMP1X	General purpose voltage comparator
CMP2X	General purpose voltage comparator
DAC7	Eight bit D-to-A converter
OP1X	General purpose operational amplifier
OP2X	High frequency operational amplifier
OPB2X	General purpose Op Amp 10KΩ minimum load
OPB3X	Op Amp, common mode includes VSS]
RNW100K	Resistor network w/ resistance value of 100 KΩ
RNW10K	Resistor network w/ resistance value of 10 KΩ
RNW200K	Resistor network w/ resistance value of 200 KΩ
RNW20K	Resistor network w/ resistance value of 20 KΩ
RNW400K	Resistor network w/ resistance value of 400 KΩ
RNW40K	Resistor network w/ resistance value of 40 KΩ
RNW60K	Resistor network w/ resistance value of 60 KΩ
RNW80K	Resistor network w/ resistance value of 80 KΩ

Digital:

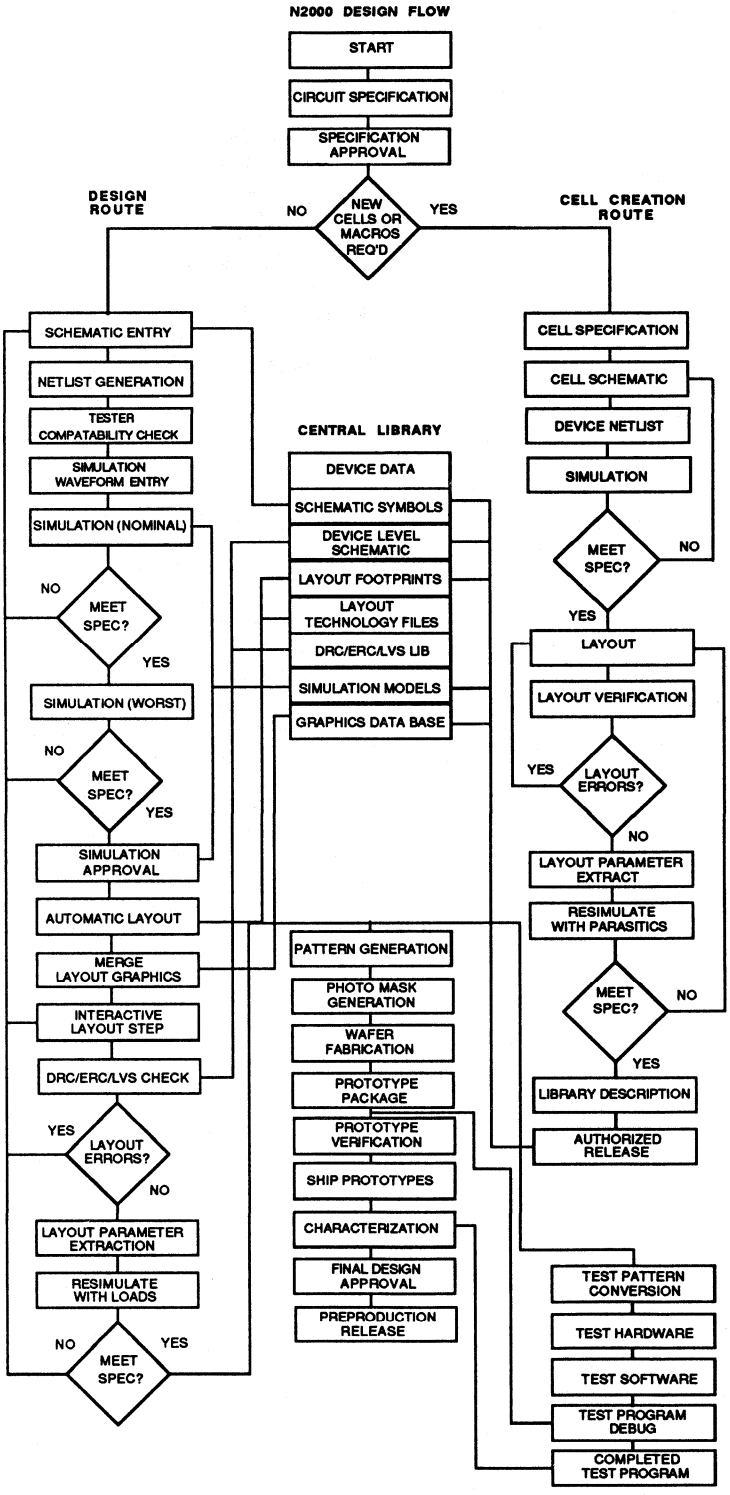
A2202	2 Wide, 2 Input AND-OR
AND2	Two input AND gate
AND3	Three input AND cell
AND4	Four input AND cell
AND5	Five input AND cell
BUF2	Medium drive buffer
BUF4	High drive strength buffer
BUFT2	Non-inverting Hi-Z state buffer, medium drive
BUFT4	Non-inverting Hi-Z state buffer, high drive
CIN2	Pad cell and buffer
CIS2	Schmidtt trigger with .8V typical hysteresis
DF	Fully static D-type flip-flop
DFR	DF cell w/ asynchronous reset
DFS	DF cell w/ asynchronous preset
DFSR	DF cell w/ asynchronous reset and preset
EXN2	Two input exclusive NOR cell
EXO2	Two input exclusive OR cell
INP	Unbuffered pad cell
INV2	Inverting buffer cell, medium drive
INV4	Inverting buffer cell, high drive
INVT2	Inverting Hi-Z state buffer cell, medium drive
INVT4	Inverting Hi-Z state buffer cell, high drive
LD	Fully static D-type transparent latch
LDR	LD cell w/ asynchronous reset
LDS	LD cell w/ asynchronous preset
LDSR	LD cell w/ asynchronous reset and preset
LNAND	Active low set/reset latch, medium drive
LNOR	Active high set/reset latch, medium drive
MUX21	Two channel data selector
NAND2	Two input NAND, medium drive
NAND3	Three input NAND, medium drive
NAND4	Four input NAND, medium drive
NAND5	Five input NAND, medium drive
LVSH	Internal CMOS level shifter
NOR2	Two input NOR, medium drive
NOR3	Three input NOR, medium drive
NOR4	Four input NOR, medium drive
O22A2	2-wide, 2 input OR-AND, inverted output
OB4	Output buffer
OBBCI4	4 mA bidirectional Hi-Z input/output buffer
OBN4	Open drain output buffer
OBP4	Open source output buffer
OBT4	Hi-Z state output buffer
OR2	Two input OR, medium drive
OR3	Three input OR, medium drive
OR4	Four input OR, medium drive
OSC4	Low frequency, single pad oscillator
OSRC4	Low frequency, dual pad RC oscillator
OSX16	Medium frequency crystal oscillator, 10 kHz-1 MHz
OSX32	High frequency crystal oscillator, 1-40 MHz
OSX4	Low power crystal oscillator, 1-100 kHz
POR	Logical low output at power up
TIN2	Pad cell and buffer, senses TTL logic
TIS2	TIN2 w/ a Schmidtt trigger
MUX21U	2 to 1 MUX unbuffered
CISD	2WCIS2 w/ 2µs delay wide pad

SD2U	2μs delay cell
POR4HV	POR 4±1V trip, HV
OBN30WQ	OBN30W low noise (quiet)
DFRU	DFR unbuffered
CINBUF2	Core CMOS level shift
CRIP3	3 bit ripple count
CRIP4	4 bit ripple count
CRIPT4	4 bit ripple count w/ Hi-Z state
RDF4	4 bit DF reg
RDF8	8 bit DF reg
RDFR4	4 BIT DFR reg
RDFR8	8 bit DFR reg
RDFRT4	4 bit DFR reg w/ Hi-z state
RDFRT8	8 bit DFR reg w/ Hi-Z state
RDFT4	4 bit DF reg w/ Hi-Z state
RDFT8	8 bit DF reg w/ Hi-Z state
OBT8	8 mA Hi-Z state output pad
TRI4	4 bit Hi-Z state
TRI8	8 bit Hi-Z state
OBP8W	8 mA open drain output wide pad
MUX81	8 to 1 multiplexer
DFRM	DFR with master Q and slave QB
RSHF4	4 bit DF shift reg
RSHF8	8 bit DF shift reg
RSHF12	12 bit DF shift reg
RSHF16	16 bit DF shift reg
RSHFR4	4 bit DFR shift reg
RSHFR8	8 bit DFR shift reg
RDF4S	4 bit DF reg with synch shift
RDF8S	8 bit DF reg with synch shift
RDFR4S	4 bit DFR reg with synch shift
RDFR8S	8 bit DFR reg with synch shift
OB7W	7 mA output buff wide pad
CIS2W	CMOS Schmidtt trigger wide pad
OSC4W	Single pin oscillator wide pad
INPW	Wide pad with input prot only
POR4L	POR with 6μA standby current
MDFR	D-tpye flip flop with reset and 2 to 1 mux
MDFR1B	MDFR w/ 3 to 1 mux & buffered outputs
BUFT1	Internal Hi-Z state, lower drive/output capacitor
RSHFR6	Shift register macros serial-in ser/par out
SD500N	500 nS delay cell
D20N5V	20 nS delay cell at 5V
D20N12V	20 ns delay cell at 12V
LDRU	Unbuffered data latch with reset
LDSU	Unbuffered data latch with set
OSX4B	OSX4 w/ bias control wide pad
OBN12A	12 mA open drain output buffer (5V Vdd)
OBN4A	4 mA open drain output buffer
OB4A	4 mA output buffer
OB12A	12 mA output buffer
OBN12P4	12 mA sink, 4 mA source output buffer
OBP12N4	4 mA sink, 12 mA source output buffer
CIS2APU	Schmidtt trigger with 10K pull-up
IS2BPU	Schmidtt trigger input buffer w/ 10K pull-up
OSXA	3.6864 MHz crystal oscillator(-5V substrate)
LVSHA	Level translator (5V to +5V)
OBN12PU	12 mA open drain w/ 10K pull-up output buf
DCLKG	Non-overlapping clock generator
ECLCON1	ECL to CMOS level converter

DSX50LV	50 MHz oscillator
TTLIN	TTL to ECL converter
TTLINP	TTL to ECL converter, pad
PLLCP	PLL charge pump
CGEN3PHV	3 phase clock generator
OSXUW	32 KHz oscillator - wide cell
TIN2W	TTL input - wide cell
OBN15	Open drain 15 mA
CIN2W	CMOS input - wide cell
TIS2W	TTL Schmidtt trigger input cell

EEPROM:

EEHVPAD	External EE high voltage
EEHVPADW	External EE high voltage wide cell
EEDF	Nonvolatile D-type flip-flop
EEDFR	EEDF w/ asynchronous reset
EEDFS	EEDF w/ asynchronous preset
EEDFSR	EEDF w/ asynchronous preset and reset
EELAT	Single bit non-volatile memory
EERAMPLV	EE VPP ramp control, LV
EERAMPHV	EE VPP ramp control, HV
EENON	Programming cell for nonoverlapping clock
EEOSC	Programming cell for oscillator
EEPOR	Power on reset pulse
EEPSFLV	Pass and/or inhibit VPP pulse LV
EEPSFHV	Pass and/or inhibit VPP pulse HV
EEPUM	High voltage generator
EEREF	Reference voltage generator
EEWRTL	Control signal generator
EE64B16	EE array configured as 64 words by 16 bits
EE64B8	EE array configured as 16 words by 8 bits


N2000 DESIGN FLOW
START
CIRCUIT SPECIFICATION
SPECIFICATION APPROVAL
NEW CELLS OR MACROS REQ'D
NO
YES
DESIGN ROUTE
CELL CREATION ROUTE
SCHEMATIC ENTRY
NETLIST GENERATION
TESTER COMPATABILITY CHECK
SIMULATION WAVEFORM ENTRY
SIMULATION (NOMINAL)
MEET SPEC?
SIMULATION (WORST)
MEET SPEC?
SIMULATION APPROVAL
AUTOMATIC LAYOUT
MERGE LAYOUT GRAPHICS
INTERACTIVE LAYOUT STEP
DRC/ERC/LVS CHECK
LAYOUT ERRORS?
LAYOUT PARAMETER EXTRACTION
RESIMULATE WITH LOADS
MEET SPEC?
CENTRAL LIBRARY
DEVICE DATA
SCHEMATIC SYMBOLS
DEVICE LEVEL SCHEMATIC
LAYOUT FOOTPRINTS
LAYOUT TECHNOLOGY FILES
DRC/ERC/LVS LIB
SIMULATION MODELS
GRAPHICS DATA BASE
PATTERN GENERATION
PHOTO MASK GENERATION
WAFER FABRICATION
PROTOTYPE PACKAGE
PROTOTYPE VERIFICATION
SHIP PROTOTYPES
CHARACTERIZATION
FINAL DESIGN APPROVAL
PREPRODUCTION RELEASE
CELL SPECIFICATION
CELL SCHEMATIC
DEVICE NETLIST
SIMULATION
MEET SPEC?
LAYOUT
LAYOUT VERIFICATION
LAYOUT ERRORS?
LAYOUT PARAMETER EXTRACT
RESIMULATE WITH PARASITICS
MEET SPEC?
LIBRARY DESCRIPTION
AUTHORIZED RELEASE
TEST PATTERN CONVERSION
TEST HARDWARE
TEST SOFTWARE
TEST PROGRAM DEBUG
COMPLETED TEST PROGRAM

WORKSTATION SUPPORT

EXAR supports customer design by providing true mixed mode simulation libraries for the Viewlogic™and Mentor™ CAE environments. This includes schematic entry symbols, intelligent simulation models, environmental configuration files, and design database translation programs to EXAR's internal format. Hardware and software requirements are as follows:

Viewlogic Designs

Hardware Requirements: Any hardware presently supported by Viewlogic. Currently this includes 80386 PC AT compatible and Sun™ workstations. A multitasking system is required for simultaneous mixed mode simulation but separate analog and digital simulations can be done on any system.

Software Requirements: The Workview™ environment software with the Viewdraw, Viewsim, and Viewwave options. Also required for simultaneous analog and digital simulation is either PSPICE or HSPICE combined with either Viewsim A/D PSPICE or Viewsim A/D HSPICE respectively plus the XR VIEWLOGIC/AD N2000 cell library. Additional software required for separate analog and digital simulation is either PSPICE or HSPICE combined with either the XR PSPICE model file or the XR HSPICE model file respectively, plus the XR VIEWLOGIC/SPICE N2000 cell library.

Mentor Designs

Hardware requirements: Any hardware presently supported by Mentor. Currently this includes Apollo™ and Sun workstations.

Software requirements: The Mentor environment software with the Neted, Symed, and Quicksim option. Also required for concurrent analog and digital simulation is Swiftlogic MIXIM™ and the XR MENTOR/MIXIM N2000 cell library. Additional requirements for separate analog and digital simulations is MSPICE and the XR MSPICE model files, plus the XR MENTOR/SPICE N2000 cell library.

CUSTOM SWITCHED CAPACITOR CIRCUITS

Exar has developed a broad line of custom switched capacitor circuits that are used to perform all of the classical signal processing functions in datacommunications, telecommunications, spectrum analysis, sonar, and general purpose applications.

Exar process technology includes a 2 micron double poly, double metal CMOS process capable of implementing analog, digital and EEPROM. With this technology, Exar can implement switched capacitor circuits with bandwidths of 50 KHz. Also available is a 1.5 micron BiCMOS process with an Ft of 3-5 GHz. This process enables Exar to go beyond the usual audio frequencies developing circuits with bandwidths of well over 100 KHz.

The basic element of a switched capacitor filter is a switched capacitor integrator that utilizes a capacitor and a pair of transistors (forming a switch) to act as a resistor. The value of this "resistor" is dependent on the frequency of the clock controlling the switch and the value of capacitor. The transfer function ultimately depends on the ratio of that capacitor to the feedback capacitor connected across an opamp. In MOS technology, this ratio can be very accurately controlled. Overall, switched capacitor technology brings with it savings in silicon area, less complexity in design, and stability over time and temperature.

Switched capacitor technology is used to implement the basic filter types of lowpass, bandpass, highpass, allpass and notch (band reject). Mathematical approximations are used to make filter functions in real life. There are four basic approximations:

Butterworth: Maximally flat with good overshoot response and medium roll off.

Chebyshev: Equiripple in passband with steep roll off.

Elliptical: Equiripple in both the passband and the reject band with monotonically decreasing characteristics after cutoff.

Bessel: Droopy amplitude response in passband, but with linear phase and good overshoot response.

APPLICATIONS OF SWITCHED CAPACITOR TECHNOLOGY

Exar has successfully developed many custom programs utilizing switched capacitor technology. Major application areas that utilize switched capacitor circuits are as follows:

- Modems
- Videophones
- Disk drive/VCR servomechanisms
- Cellular telephones
- Sensors
- Speech Processing
- Audio/Video filters
- DSP front ends
- Cordless telephones
- Data converters

All of the above applications make use of Exar's switched capacitor expertise to develop mixed-mode integrated circuits.

EXAR ...the analog plus™ company

QUALITY ASSURANCE

Introduction

The practice of Quality Assurance (QA) at Exar revolves around the use of active controls in the purchase of materials, the fabrication of wafers, the assembly of die, test and shipment of finished parts. This requires that all materials and processes be properly documented and that audits and inspections be used to insure that the written specifications are available and being followed. Adherence to written specifications is the foundation of consistent and repeatable processes. This provides the "basis" upon which more elegant statistical control procedures may be used.

The Exar QA program also contains those key elements necessary to comply to MIL-STD-883 and MIL-M-38510, Appendix A. These elements include control of equipment maintenance and calibration, control of cleanliness and atmosphere in the wafer fab area, personnel training and certification, and corrective action programs.

Vendor Control

All critical purchased materials are documented so that Exar vendors know exactly what is expected. critical material vendors are qualified prior to accepting material. Qualified vendors are periodically audited and those consistently meeting these requirements are preferred by placing them on the approved vendor list (AVL). Use of vendors who are not on the AVL requires the prior approval of Exar QA (there may be new vendors who are being qualified prior to placing on the AVL, for example). Incoming QA (IQA) inspection is performed either on a sample or 100% basis. IQA results are monitored by statistical process control (SPC) charts to monitor the ability of the vendor to control critical processes. Vendors who consistently utilize statistical control receive less frequent audits and IQA inspections making them more cost effective for Exar operations. Exar vendors are rated accordingly with orders being placed with the best ones.

Wafer Fabrication Process Control

All critical wafer fabrication processes are documented and those specifications are followed by Exar processing personnel. For this reason, Exar QA signs off on the approval of all process specifications and audits all wafer fabrication processes on a periodic basis. The audits enforce the adherence to those specifications and indicate when updating is required. All major process changes require that a process qualification be run prior to acceptance of material from the changed process. Any deviations from specifications for production wafer lots requires the approval of Exar QA. Critical process steps are monitored by use of in-process inspections and SPC charting which enables process adjustment by statistical criteria only. Each wafer must pass thorough in-process inspections including EPI thickness, EPI resistivity, oxide thickness to name a few. This enables the ability to control state of the art processes within very tight tolerances. Critical process steps which consistently exhibit control are candidates for less frequent collection of data for SPC purposes. The emphasis is upon the capability of given processes to exhibit statistical control (uniformity).

Assembly Process Control

Assembly vendors are selected on the basis of their ability to control the packaging process. Each vendor is placed on the AVL after successful completion of a vendor qualification. This includes the use of vendor internal written specifications and audits by Exar of those processes. Exar QA audits each assembly house a minimum of once per year. Additionally, Exar QA pulls lot samples for destructive incoming inspections of assembled product. The sample inspection results are monitored by SPC charts to assess the vendors ability to control the processes. Vendors who consistently utilize statistical control receive less frequent audits making them more cost effective for Exar operations.

Exar also maintains an onshore assembly facility with well documented processes. Again, the area is audited once every ninety (90) days for adherence and monitored with SPC charts to assess the control over the process. Material processed in the onshore facility receives the same lot destructive sample inspection as material from the offshore facilities.

Test and Shipping Process Control

All handling of finished product through final test and shipping is per written specification. These areas are periodically audited to assure adherence to specification. The handling specifications include ESD protection for all Exar products.

After final test, every lot goes through a sample test with an AQL less than or equal to 0.1% at room temperature by Final QA to assure that all final tests and handling of the material has been performed to specification. Any lot which fails the sample criteria is re-screened to make sure that no defective product gets shipped. Plant clearance inspection is performed by Exar QA to assure that all customer specifications have been met prior to shipment. This insures that the test traveller is correct and that all steps have been accomplished according to customer requirements.

SPC Program

In order for Exar to maintain a competitive edge in the manufacturing of integrated circuit products, we need to minimize the production of defective material in fabrication, assembly and test. In this effort, Exar is implementing Statistical Process Control (SPC).

The traditional approach to ensuring quality is for the production group to manufacture material and the quality group to inspect and/or test the product to sort out any defects prior to shipment. The definition of what is acceptable is provided either by the customer or by the design and manufacturing specifications. However, the use of after-the-fact inspection is not a very effective

strategy because the damage (of producing defective material) has already been done. In order to improve Exar products overall, systematic ally eliminating the causes of defective production is crucial; it is clearly necessary to maximize the production of good material and minimize the production of unusable material.

The major indication of production of defective unusable material is excessive variation in manufacturing. SPC is an effective method to continuously monitor the variation in key process steps, and to provide the criteria for making adjustments to the process, when necessary, to maintain control. As the product is sampled repeatedly, the mark of a process under (statistical) control is that over time, each critical process parameter is proven to follow one statistical distribution with one mean (average) and one standard deviation. When a process is not under control, the distributions of key process parameters will tend to wander (having more than one mean and/or standard deviation).

When all critical processes are in control, neverending quality improvement can take place. customers will benefit by improved levels of quality and reliability of products received from Exar.

The implementation of such a program is not a simple task, given the vast number of process steps (and the inherent complexity of those steps) required by Exar's semiconductor products. An SPC plan has been written and implementation is in progress.

If you or any of your customers are interested in our progress in implementation of SPC, please contact Exar Quality Assurance.

OUTGOING QUALITY MONITOR

Introduction

One task of Exar Quality Assurance is to monitor outgoing quality, or estimate that rate of defective that a customer is likely to observe in the inspection or application of parts produced by Exar.

Outgoing electrical quality estimates are given in parts per million (PPM) defective. Outgoing lots are sampled an inspected/tested by the Quality Control (QC) group in Quality Assurance using the QC test program and visual criteria to estimate outgoing electrical quality. The QC program tests all critical parameters and functions to the data sheet or specification. All Exar parts are 100% functionally and parametrically tested prior to the QC sample electrical test, with the QC sample, the final guarantee that something catastrophic has not occurred in the process. The QC electrical sample, in most cases, is run at room temperature (approximately 25°C). The visual criteria are provided in Exar's external visual inspection specification.

It is important to note that Exar guarantees an acceptable quality level (AQL) of less than 0.1% (1000 PPM) for electrical parameters and visual criteria. With current Exar QC electrical sample plan (of 116 devices tested per lot, accept with no defectives, reject on one or more defectives), the sample AQL is actually 0.04% (400 PPM defective) for large lots. AQL implies nothing about the average outgoing quality (AOQ) that we currently ship. We track AOQ values on a monthly basis.

DEFINITIONS

Before getting into further details, some definitions are called for as follows:

p : Process average PPM defective, the PPM defective observed in the QC electrical test and visual samples or simply the number defective divided by the number sampled.

Pa(p) : Probability of acceptance for a given lot sample based on the lot sample plan which includes sample acceptance/rejection criteria. For instance, a popular plan is to pull a sample of 116 parts from a lot and run the QC electrical test and visual inspection. If one or more parts fail, the lot from which the sample came is rejected and goes back for a complete screen to sort out all defectives. Pa(p) is simply the probability that a lot with a given process average PPM defective, p, will pass the 116 piece sample test with no defectives.

AQL : Acceptable quality level, that value of p for which we have Pa(p) = 0.95, or that PPM defective for which we have a 95% chance of passing the QC sample test/inspection for a given lot.

LTPD : Lot tolerance percent defective, that value of p for which we have Pa(p) = 0.10, or that PPM defective for which we have a 10% chance of passing the QC sample test/inspection for a given lot.

Rectifying Sample Inspection Plan: A sample plan for which a lot failing to pass the sample acceptance criteria is re-screened thereby sorting out all defectives.

AOQ : Average outgoing quality, the average PPM defective which we are shipping when we use rectifying sample inspection. It is important to know that there is some very low rate of defectives that exists in lots which pass the acceptance criteria when rectifying sample inspection is used. We use a method to estimate AOQ which uses results from a series of lots. This estimator is calculated as follows:

$$AOQ\ (estimate) = A/B$$

Where A = the sum of lot sizes in the series with one defective in the QC sample test/inspection divided by the lot sample size and B = the sum of lot sizes in the series with no defectives in the QC electrical sample test.

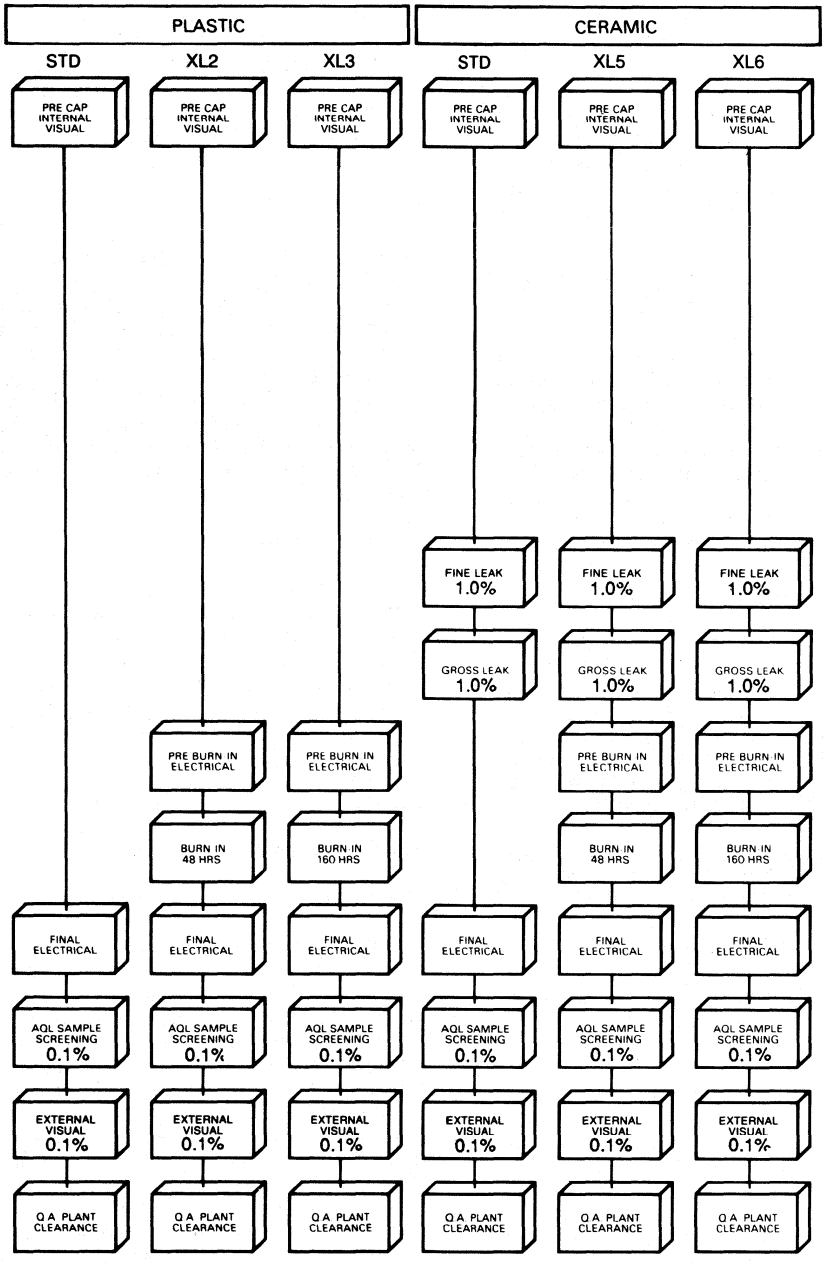
AOQL : Average outgoing quality limit, the absolute maximum level of PPM defective that can be shipped based on use of rectifying sample inspection plan. This recognizes that as we produce lots, the PPM defective varies. For p values that are high, we tend to reject the lot samples and screen lots so that shipments of the screened lots are defect free. For p values that are low,

we tend to pass lots which have very few defectives. AOQL tells us what the worst PPM defective is under that sample plan regardless of how much p varies from lot to lot.

We use a rectifying sample inspection scheme in which lots failing the sample acceptance criteria are re-screened 100% prior to lot acceptance. This implies that lots which fail the sample acceptance criteria are considered defect free after screening and lots which pass the sample criteria have a very low defective rate. Therefore, we know that even after we run the QC electrical sample that some (very few) defectives may exist in the lot. It is necessary to estimate what the rate of defective is for lots shipped. This requires that we collect QC electrical sample results for a series of lots in order to estimate the average PPM defective value AOQ (average outgoing quality). We can assemble the results in a way that we can sum the lot sizes for lot samples in the series that were defect free, and the sum of lot sizes for samples containing one defective. For example, suppose we have a series of 100 lots for which we ran a QC sample test/inspection of 116 pieces per lot. Further suppose that 94 samples were defect free with a sum of lot sizes of 250,000 pieces, 3 samples had one defective and sum of lot sizes of 2000 pieces, 2 samples had two defectives and 1 sample had three defectives, we would compute AOQ as follows:

$$AOQ = \frac{2000/116}{250{,}000} = 69 \text{ PPM}$$

Any questions regarding Exar PPM defective levels or the methods of AOQ estimation should be addressed to the Quality Assurance Department.



NOTE: ALL OPERATION ARE 100% UNLESS OTHERWISE SPECIFIED

9

RELIABILITY ASSURANCE

EXAR Reliability Assurance begins with product design and continues throughout the life of the product.

During the design phase of a new product Reliability Engineering reviews the design rules, and the processes and material to be used. The review insures that at least the minimum requirements of MIL-M38510 paragraph 3.5 are satisfied.

A reliability evaluation or qualification is performed on all new design rules, processes and materials.

When the design is frozen, but before the product is released to production, Reliability Engineering performs an extensive physical analysis and stress tests to verify the reliability of the design. The physical analysis includes internal and external visual, bonding and die attach evaluation, passivation integrity and SEM. Stress tests includes mechanical, environmental and electrical stresses. The results of the stress tests are used to predict the life of the product and to identify the prevalent failure mechanisms.

Once the product is released to production Reliability Engineering performs qualification in accordance with MIL-STD-883 method 5005, establishes a reliability data base for the product tests. The reliability data base includes data from qualification and extended lifetime tests. The data base is reviewed periodically to identify reliability trends and to establish reliability statistics.

Reliability Engineering analyzes all qualification and field failures and provides feedback into the system to enhance the rellability of EXAR product.

FAILURE ANALYSIS CAPABILITY

After EXAR has performed all of the environmental stress testing on the product any failures that have occurred during the stress need to be analyzed to determine the cause of failure. EXAR has a full complement of tools available to perform extensive failure determination. The results of the analysis are then relayed to the appropriate groups to determine any corrective action for improving the product. Also any customer requested failure analysis can be handled by EXAR's failure analysis group. Reports are generated and the information is provided to the customer for his analysis. The following is a short description of EXAR's failure analysis capability.

Procedure

Exar can analyze a failure starting with an initial electrical examination all the way through to a detailed structural and internal visual examination pinpointing the exact physical element on the die that has failed. The failure analysis group uses a variety of analysis equipment to perform this determination.

Curve Tracer

The curve tracer is a simple but essential tool to perform the first level of analysis on a failing device. The current-voltage characterisitics are taken on every pin of the device to determine electrical opens, shorts or anomalous behavior at the dc level. At this point it may be possible to limit the analysis to particular pin. Some of the types of failures isolated at this stage may be electrical overstress, ESD (Electostatic discharge) failures, bonding problems or other assembly related issues.

Package Decapsulation

Almost all failures require decapsulating the device to perform an internal visual examination of the die. Ceramic and cerdip packages are decapsulated mechanically while plastic packages may require chemical methods. A plastic package is usually decapsulated using either sulphuric acid of fuming nitric acid. In some cases plastic packages can also be mechanically decapsulated. In the normal situation a "Jet Etcher" is used to quickly but carefully remove the plastic over the die surface. The die is then exposed and a visual examination can be performed.

High Power Optical Microscope

A high power optical microscope is used to examine the die surface and the bonding and assembly quality of the device. The microscope is equipped to perform phase contrast and dark field analysis to enhance any topographical features during visual examination. At this point in the analysis failure mechanisms which exhibit any visual change may be observed. A multitude of failure mechanisms may show up now due to physical changes caused by the failure process. The exact location of the failure may now be determined and correlated to previous electrical data. Process induced failures are also evident at this point. Some failure mechanisms that are observed may be electromigration, electrostatic discharge damage, junction or oxide failure, metal corrosion among many others.

Electrical Microprobing

When the visual examination via the optical microscope shows no anomalies then it may be necessary to do electrical microprobing to determine the location of the failing element on the die. This is done by physically measuring electrical characteristics on the individual elements of the die itself. Probing may entail a sequential cutting and electrical measuring on the metal interconnects between transistors until the failure location is determined.

Liquid Crystal Analysis

This technique can be used in lieu of or in conjunction with microprobing. It uses temperature sensitive liquid crystal that changes color when a spot on the die draws excessive power. This may be a way to determine areas which are damaged but show no visual evidence during the optical microscope analysis. Oxide shorts and junction damage are quite often apparent during use of this procedure.

Selective Deprocessing

When there is a need to look at different layers of the die surface then various selective deprocessing techniques are used. Plasma enhanced etching along with wet chemical etching removes layer after layer of the die surface with visual examination being performed after each removal. This allows the failure site to be examined in more detail and to pin point the precise layer at which failure has occurred. Gate oxide ruptures and pin holes in the interlayer oxides can be usually found during this procedure. Deprocessing allows previously hidden fail sites to to become apparent.

Scanning Electron Microscope

One of the final methods to obtain a detailed look at a failure site is to use a Scanning Electron Microscope. This method allows extremely high (300,000x) magnification of the fail site. Very fine detail can be obtained which is possible in no other way. The failure mechanisms can be studied and a cause can be assigned based on the morphology of the fail site. Metallurgical problems can be studied at this level of magnification and process issues become very evident. An additional feature that is possible with the help of the SEM is the use of Voltage Contrast and Electron Beam Induced Current techniques. Voltage contrast allows one to electrically exercise the device and observe voltage levels as they propogate along the internal conducting lines. When an unexpected break in the voltage level occurs a fail site has been identified. Electron Beam Induced Current (EBIC) analysis allows one to find degraded or damaged junctions which would otherwise not be visible optically.

Cross-Sectioning Analysis

Cross-Sectioning is performed on both die failures and assembly failures. This technique allows one to see the entire profile of the process and to delineate areas which are at or below the silicon surface. Assembly failures, in particular, are brought out very clearly with this technique. In addition, staining can show the depth of and damage to diffused junction below the silicon surface. Electrical shorts between multiple level conductors can be seen using crossectioning and interlevel oxide quality can be determined.

Electron Dispersive X-Ray Analysis

This technique (EDX) is used in conjunction with the SEM and determines the elemental (Periodic Table) composition of the material being observed. It allows one to find the identity of contaminants that may cause specific failures. These contaminants may have been introduced during the fabrication of the die or possibly during the assembly operation. Corrective action may then be taken at the appropriate manufacturing site based on the EDX finding.

FAILURE RATE CALCULATIONS

Failure rate prediction calculations are based on what is known as the Arrhenius Model. This model assumes that most failures are due to component degradation that follow the laws of Reaction-rate kinetics. This model has been shown to work quite well for most types of failure mechanisms.

Each failure mechanism is observed to have its own characteristic Acceleration Factor when doing Temperature accelerated environmental stress testing. By performing environmental testing at elevated temperatures one can then use this factor to predict failure rates at actual application temperatures. In practice the acceleration factor is obtained from an Activation Energy of the failure mechanism. The Activation Energy (in Electron Volts) is an average value that is determined from experimental data taken over an extended period of time. Activation Energy is a rough measure of the thermal energy that is required for an electrochemical reaction (failure mechanism) to occur.

The formula for the Acceleration Factor is given as:

$$\text{ACCELERATION FACTOR} = e^{\left(\frac{Ea}{K}\frac{1}{T2} - \frac{1}{T1}\right)}$$

where:

R1 = Failure rate at junction temperature T1
R2 = Failure rate at junction temperature T1
e = Base for Natural Logarithms - 2.71818....
Ea = Activation Energy (units of Electron Volts)
T1 and T2 = Junction temperatures in degrees Kelvin

K = Boltsmann's Constant (8.63×10^{-5})

T1 is taken as the Accelerated test temperature
T2 is taken as the Operating temperature

Also Mean Time Between Failure (MTTF) is defined as:

$$\text{MTTF} = \frac{1}{R}$$

For Bipolar Devices Experience has shown that an Activation Energy of .9 electron volts is appropriate and that for MOS devices .7 electron volts gives the best results.

To calculate the failure rate the total Device Hours (No. of devices on test times the total hours on test) is multiplied by the Acceleration Factor to give the Total Equivalent Device hours at the operating temperature. Then the following formula gives the failure rate (at a particular Confidence Level).

$$\text{Failure Rate at } 1-\alpha \text{ upper Confidence Level} = \frac{CHI^2}{2t}$$

where $DF = 2(f + 1)$
and CHI^2 evaluated at $1-\alpha$

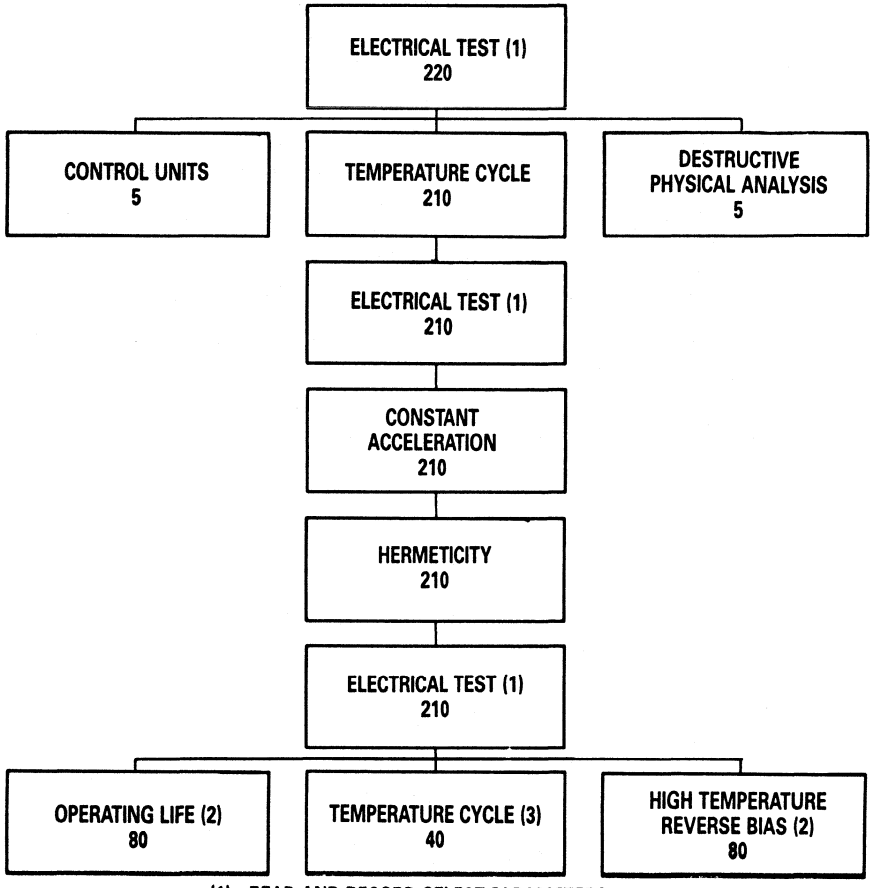
where:

CHI^2 = CHI Square distribution (available from mathematics handbooks)
DF = Degrees of freedom (defined with the CHI Square distribution
t = Total Equivalent Device Hours
f = Total Number of Failures
α = Statistical error expected in the failure rate

$1-\alpha$ = is the confidence level we have (i.e. 90 percent or 60 percent sure) that the ACTUAL failure rate is no worse than the above CALCULATED failure rate.

The failure rates are generally expressed in either percent fails per 1000 hours or in FITS (1 fail in 1 billion hours of operation).

EXAR
RELIABILITY FLOW CHART



(1) READ AND RECORD SELECT PARAMETERS
(2) TEST, R&R @ 160, 500, 1000, 2000 AND 4000 HOURS
(3) TEST, R&R @ 100, 200, 500 CYCLES

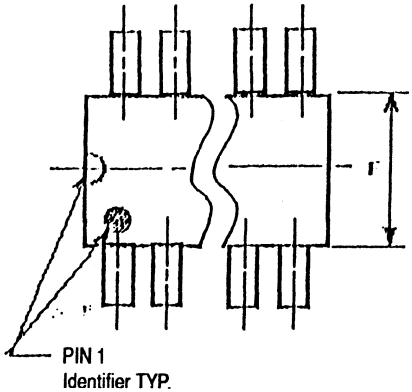
TYPICAL MONITOR PROGRAM CERAMIC PACKAGE

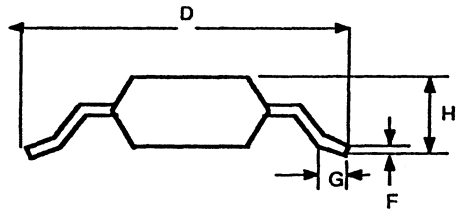
APPENDIX A

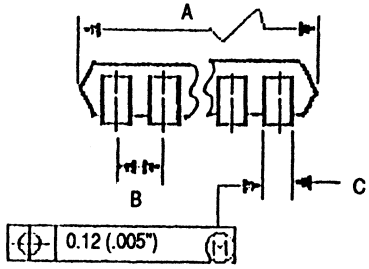
D = SOIC JEDEC DIMENSION

LD	A	B	C	D	E	F	G	H
	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX
8LD	.189/196	0.05	.013/.019	.228/.244	.149/.157	.007/.009	0.016/.05	.053/.068
14LD	.336/.344	0.05	.013/.019	.228/.244	.149/.157	.007/.009	0.016/.05	.053/.068
16LD(.150)	.385/.393	0.05	.013/.019	.228/.244	.149/.157	.007/.009	0.016/.05	.053/.068
16LD(.300)	.397/.413	0.05	.013/.019	.394/.419	.291/.299	.009/.012	0.016/.05	.092/.104
18LD	.446/.462	0.05	.013/.019	.394/.419	.291/.299	.009/.012	0.016/.05	.092/.104
20LD	.496/.511	0.05	.013/.019	.394/.419	.291/.299	.009/.012	0.016/.05	.092/.104
24LD	.598/.614	0.05	.013/.019	.394/.419	.291/.299	.009/.012	0.016/.05	.092/.104
28LD	.696/.712	0.05	.013/.019	.394/.419	.291/.299	.009/.012	0.016/.05	.092/.104
32LD	.800/.815	0.05	.013/.019	.493/.519	.390/.398	.009/.012	.016/.050	.092/.104

ALL DIMENSIONS ARE IN INCHES





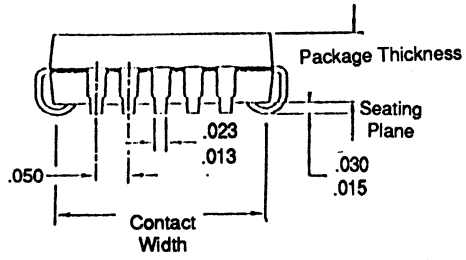


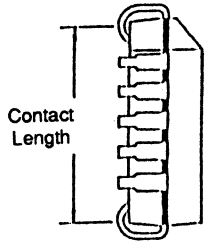
APPENDIX B

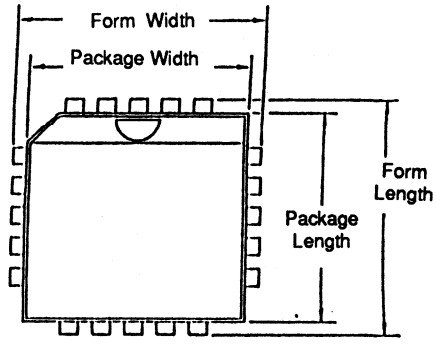
J = PLASTIC LEADED CHIP CARRIER (PLCC)

PKG LD COUNT	PKG.LENGTH (MIN/MAX)	PKG.WIDTH (MIN/MAX)	PKG.THICK (MIN/MAX)	FORM WIDTH (MIN/MAX)	FORM LENGTH (MIN/MAX)	CONTACT WI (MIN/MAX)	CONTACT LEN (MIN/MAX)
20LD	.350/.356	.350/.356	.140/.160	.385/.395	.385/.395	.290/.330	.290/.330
28LD	.450/.456	.450/.456	.140/.160	.485/.495	.485/.495	.390/.430	.390/.430
32LD	.547/.553	.547/.553	.140/.160	.585/.595	.585/.595	.490/.530	.490/.530
44LD	.650/.656	.650/.656	.140/.160	.685/.695	.685/.695	.590/.630	.590/.630
52LD	.750/.756	.750/.756	.140/.160	.785/.795	.785/.795	.690/.730	.690/.730
68LD	.950/.958	.950/.958	.140/.160	.985/.995	.985/.995	.890/.930	.890/.930
84LD	1.150/1.158	1.150/1.158	.140/.160	1.185/1.195	1.185/1.195	1.090/1.130	1.090/1.130

ALL DIMENSIONS ARE IN INCHES







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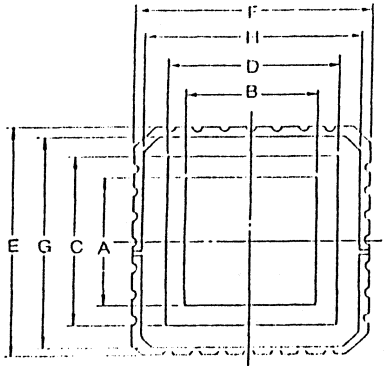
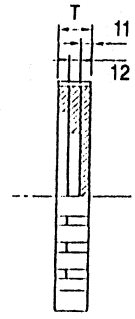
APPENDIX C

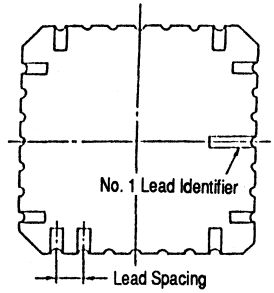
L = LEADED CHIP CARRIER (LCC)

LD	A X B	C X D	E X F	G X H	t1/t2/T	Lead
	Die Pad	Post Sq.	Overall	S/R O.D.	Thickness	Spacing
20 LD	.130 X .130	.230 X .230	.350 X .350	.314 X .314	.020/.020/.060	0.05
24 LD	.185 X .185	.235 X .235	.400 X .400	.335 X .335	.020/.020/.060	0.05
28 LD	.250 X .250	.330 X .330	.450 X .450	.404 X .404	.020/.020/.060	0.05
32 LD	.280 X .360		.550 X .450		.020/.020/.060	0.05
44 LD	.300 X .300	.390 X .390	.650 X .650	.500 X .500	.020/.020/.060	0.05
68 LD	.350 X .350	.440 X .440	.950 X .950	.545 X .545	.040/.020/.080	0.05
84 LD	.390 X .390	.560 X .560	1.150 X 1.150	.734 X .734	.040/.020/.080	0.05

ALL DIMENSIONS ARE IN INCHES





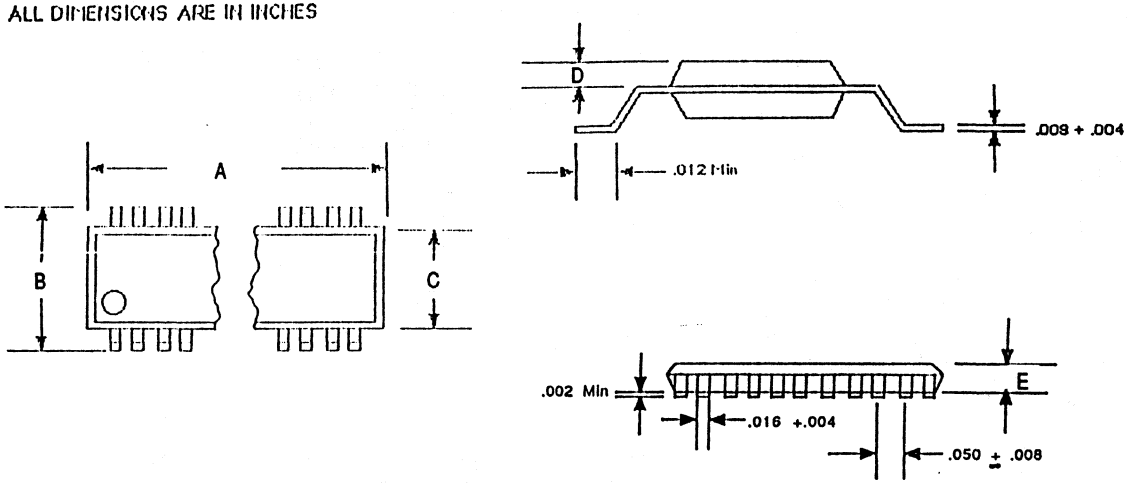


APPENDIX E

MD = JAPANESE SMALL OUTLINE PACKAGE

LD	A	B	C	D	E
	(Max./Min.)	(Max./Min.)	(Max./Min.)	(Max./Min.)	(Max./Min.)
8 LD	.209/.185	.256/.232	.181/.165	0.025	.055/.063
14 LD	.354/.330	.253/.232	.181/.165	0.025	.055/.063
16 LD	.406/.382	.256/.232	.181/.165	0.026	.055/0.63
18 LD	.452/.432	.319/.295	.221/.205	0.031	.076/.066
20 LD	.504/.480	.319/.295	.221/.205	0.031	.074/.066
22 LD	.551/.527	.319/.295	.221/.205	0.031	.074/.066
24 LD	.602/.578	.319/.295	.221/.205	0.031	.074/.066
28 LD	.740/.716	.401/.377	.303/.287	0.039	.090/.082
40 LD	1.051/1.027	.478/.452	.378/.362	0.047	.106/.098

ALL DIMENSIONS ARE IN INCHES



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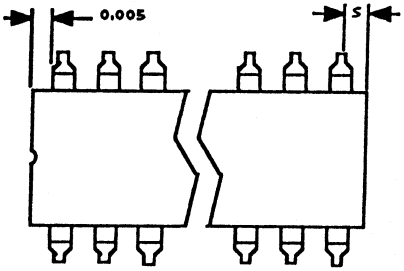
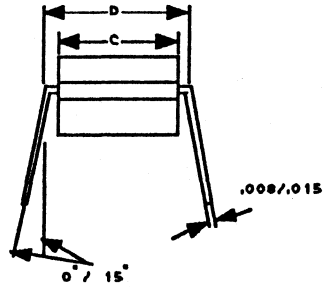
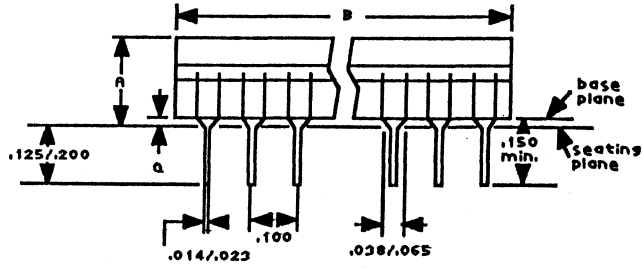
APPENDIX F

N = CDIP CERAMIC DUAL INLINE PACKAGE

	A	B	C
8 LD	.404/.376	.289/.245	.316/.300
14 LD	.766/.754	.291/.245	.316/.300
16 LD	.766/.754	.291/.245	.316/.300
18 LD	.898/.882	.291/.245	.320/.300
20 LD	.958/.942	.291/.245	.320/.300
22 LD	1.078/1.062	.291/.245	.420/.400
24 LD	1.260/1.240	.384/.356	.600/.560
28 LD	1.460/1.440	.583/.514	.600/.560
40 LD	2.060/2.040	.583/.514	.600/.560



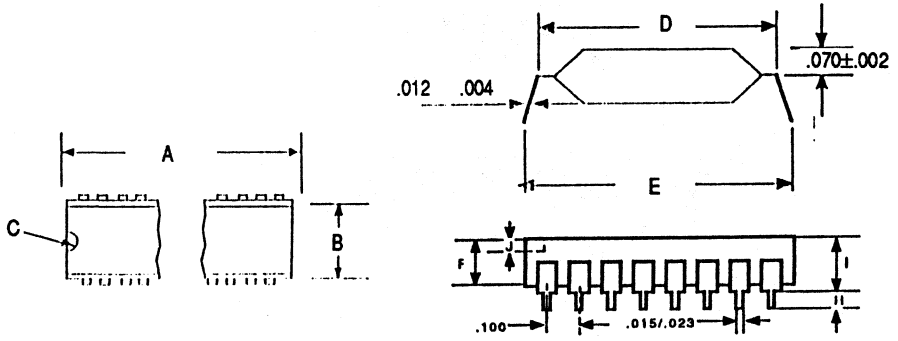




P = PLASTIC DUAL INLINE PACKAGE (PDIP)

LD	A	B	C	D	E	F	G	H	I	J
	(Max./Min.)	(Max./Min.)		(Max./Min.)	(Max./Min.)	(Max./Min.)	(Max./Min.)	(Max./Min.)	(Max./Min.)	
8 LD	.386/.362	.260/.236	.039R	.312/.288	.370/.322	.134/.118	.312/.288	.134/.118	.177/.153	0.31
14 LD	.775/.748	.268/.244	.047R	.312/.288	.370/.322	.142/.126	.612/.522	.134/.118	.177/.153	0.31
16 LD	.775/.748	.268/.244	.047R	.312/.288	.370/.322	.142/.126	.712/.588	.134/.118	.177/.153	0.31
18 LD	.912/.888	.268/.244	.047R	.312/.288	.370/.322	.142/.126	.812/.788	.134/.118	.177/.153	0.31
20 LD	1.047/1.023	.268/.244	.047R	.312/.288	.370/.322	.152/.126	.912/.888	.134/.118	.177/.153	0.31
22 LD (300MIL)	1.12/1.180	.352/.345		.410/.390	.475/.425	.132/.128		.130/.110	.165/.155	0.31
24 LD (600MIL)	1.200/1.240	.551/.538		.620/.600	.660/.640	.152/.148		.138/.114	.177/.153	0.023
24 LD (300MIL)	1.255/1.235	.254/.538	0.60R	.330/.250	.668/.630	.152/.148	1.319/1.281	1.138/.114	.177/.153	0.023
28 LD	1.468/1.448	.551/.538	.060R	.625/.600	.668/.630	.152/.148	1.919/1.881	1.138/.114	.117/.153	0.023
40 LD	2.067/2.050	.551/.538	.060R	.625/.600	.668/.630	.152/.148	1.919/1.881	1.138/.114	.117/.153	0.023
48 LD	2.423/2.393	.556/.536	.060R	.625/.600	.668/.630	.152/.148		.138/.144	.117/.152	0.023

ALL DIMENSIONS ARE IN INCHES

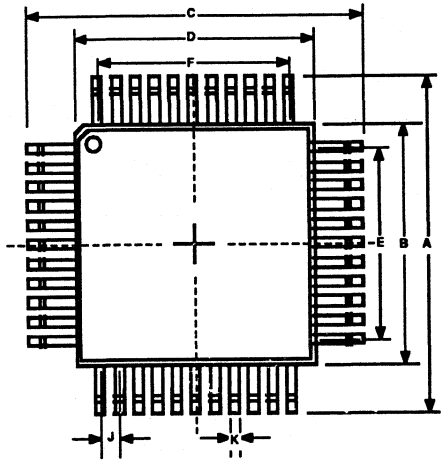


APPENDIX H

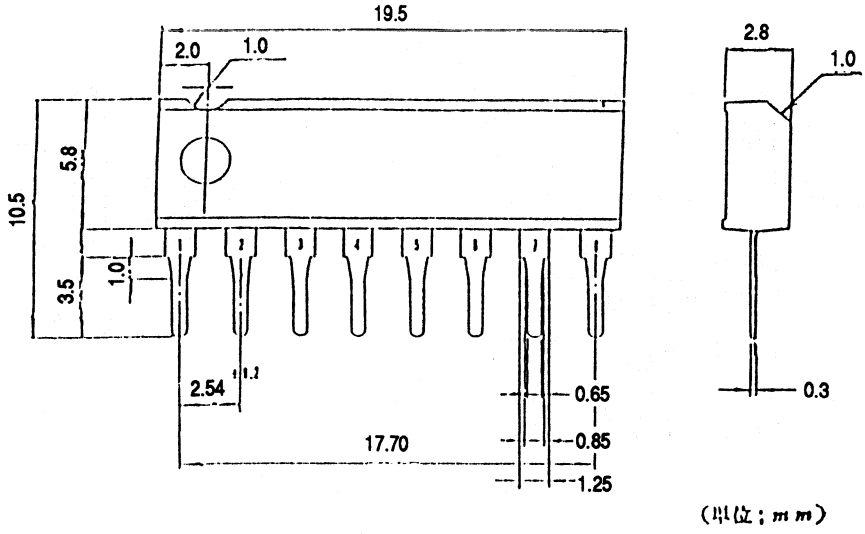
Q = PLASTIC QUAD FLAT PACKAGE (PQFP)

LEAD COUNT	A max/min	B max/min	C max/min	D max/min	E max/min	F max/min	G max/min	H max/min	I max/min	J max/min	K max/min	
*32LD	.366/.342	.287/.263	.366/.342	.287/.263	.232/.208	.232/.208	.057/.056	0.025	0.015	0.031	0.016	ROHM STD.
*44LD	.405/.382	.563/.539	.405/.382	.563/.539	.327/.303	.327/.303	.085/.084	0.039	0.047	0.031	0.016	ROHM STD.
44LD	.557/.537	.398/.390	.557/.537	.398/.390	.315(REF)	.315(REF)	.094/.083		.037/.026	0.0315	.018/.012	EIAJ STD.
52LD	.557/.537	.398/.390	.557/.537	.398/.390	.307(REF)	.307(REF)	.094/.083		.037/.026	0.0256	.014/.010	EIAJ STD.
*68LD	.957/.933	.799/.776	.957/.933	.799/.776	.721/.697	.721/.697	.085/.084	0.039	0.047	0.039	0.016	ROHM STD.

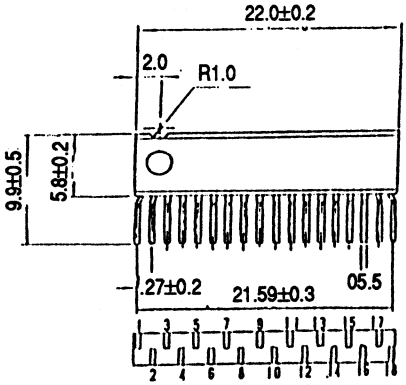
ALL DIMENSIONS ARE IN INCHES

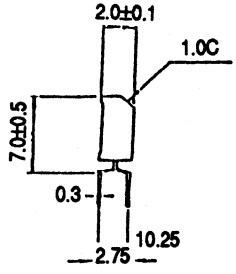


SIP = SINGLE INLINE PACKAGE



ZIP = STAGGERED INLINE PACKAGE





Marking Limitations for each package & pin count

Package	PDIP	CDIP	D&K	J	L	Q
Pin Count	*A/*B	*A/*B	*A/*B	*A/*B		
08LD	7/3	7/3	4/2			
14LD	15/3	15/3	8/2			
16LD	15/3	15/3	12/3			
18LD	15/3	15/3	12/3			
20LD	22/3	22/3	14/3			
22LD	24/4	24/4				
24LD	26/6	26/6	18/3			
28LD	32/6	32/6	24/3	8/4		
32LD						
40LD	44/6	44/6				
44LD				13/6		
48LD	446	446				
64LD						
68LD					11/6	
84LD						

*A = # of characters/line

*B = # of lines

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